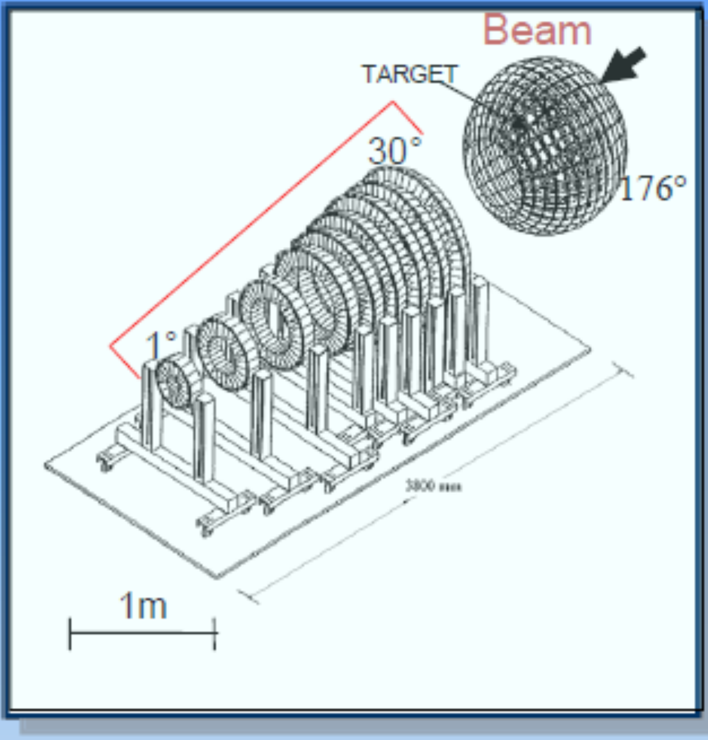
Chapt.8 Data Acquisition Systems

The CHIMERA Detector

1192 Si-CsI(Tl) Telescopes



18 rings in the range 1° ≤ θ ≤ 30°

17 rings in the range 30° ≤ θ ≤ 176° (sphere)

High granularity and efficiency up to 94% 4π

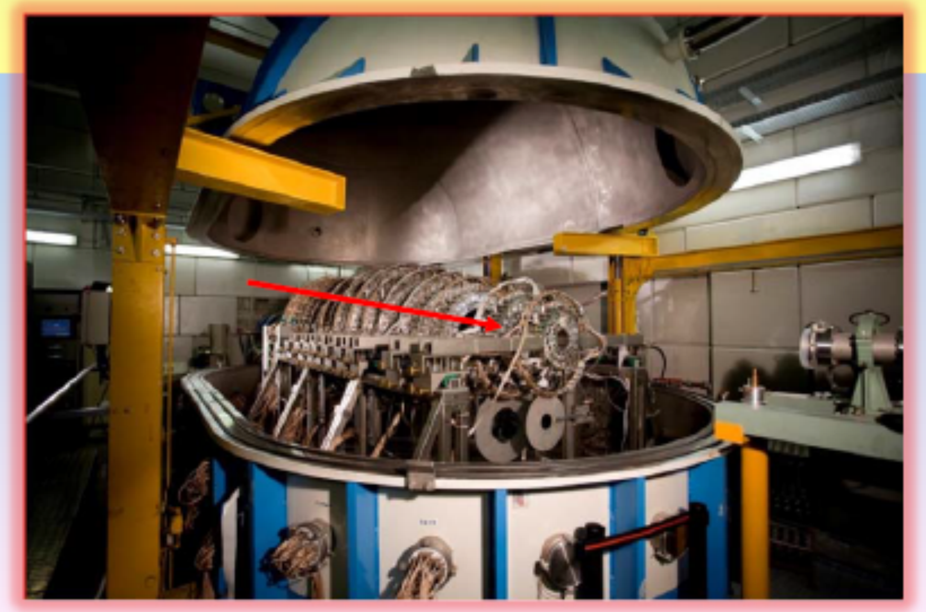
Z identification up to beam charge (ΔE-E)

Z and A identification by ΔE-E up to Z ≤ 9

Z and A identification in CsI up to Z ≤ 4

Mass identification with low energy threshold (<0.3 A.MeV) by Time-of-flight

Zeta identification for particles stopping in Si (pulse shape)



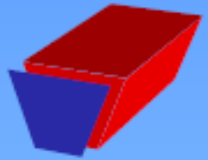
Experimental Methods:

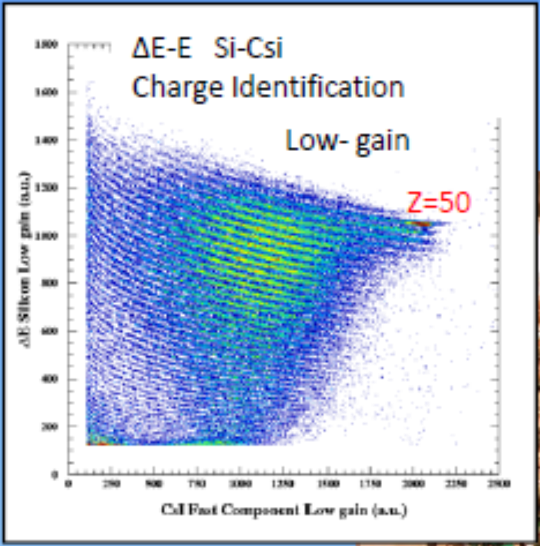
ΔE(Si)-E(CsI(tl)): CHARGE, ISOTOPES

E(Si) –TOF(Si) VELOCITY - MASS

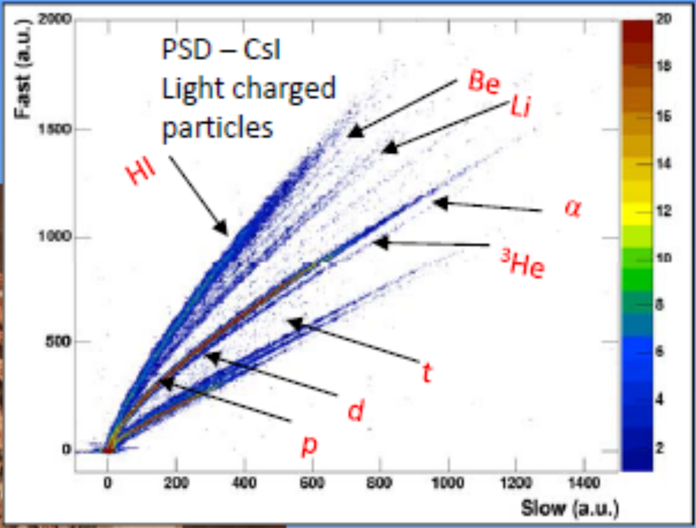
PULSE SHAPE in CsI(Tl)
p,d,t,^{3}He,^{4}He,.$^{6,7,..}$Li,… Z_{light}<5
Pulse shape for particle stopping in Si (CHARGE)

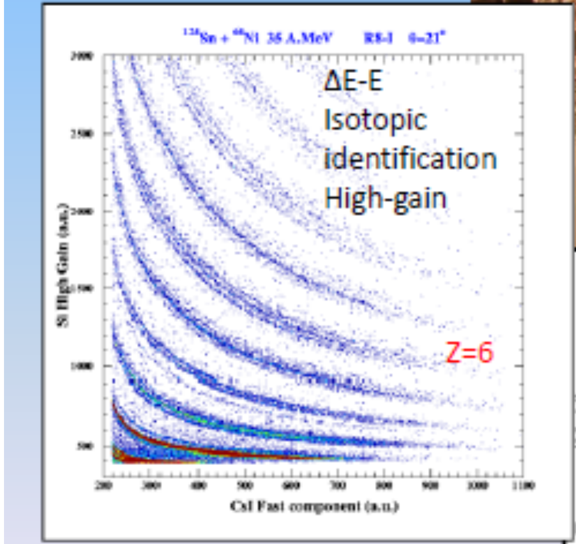
Chimera signals



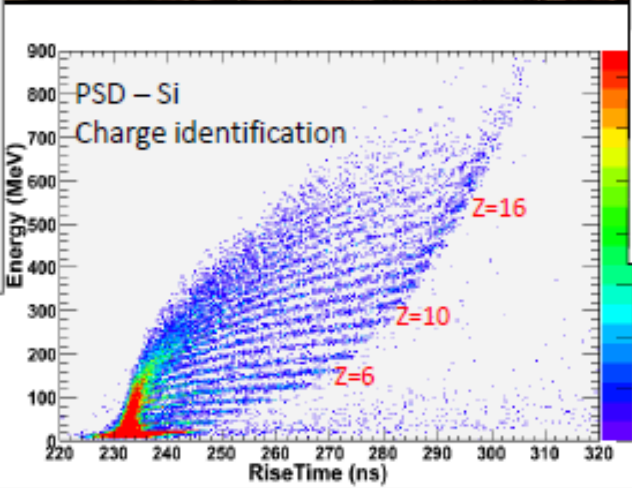

ΔE-E Si-CsI Charge Identification

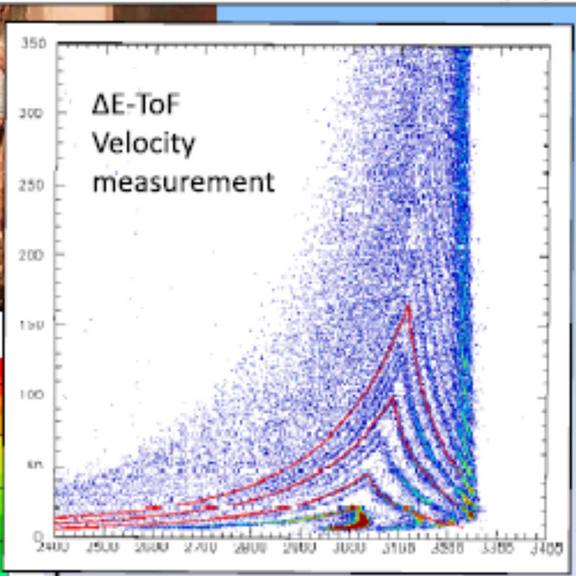
Low- gain


PSD – CsI Light charged particles


^{124}Sn + ^{64}Ni 35 A.MeV R8-1 θ=21°

ΔE-E Isotopic identification High-gain


PSD – Si Charge identification


ΔE-ToF Velocity measurement

Why do we need a Data Acquisition System ?

- Primary objective is to have the most comprehensive information about the physical process under study.

- For complex processes, many outgoing channels would require a large number of sensors and the simultaneous collection of data from all the channels.

Typical present generation experiments would have:

- >200 parameters per event
- 10,000 events per second
- $> 10^{12}$ bytes of data / experiment.

Needs high throughput and massive storage requirement.

- Detectors are large and distributed -containing many thousands of individual channels.

- The complete set of signals which describe a single nuclear interaction is called an Event. there can be thousands to millions of events occurring per second.

- Events occur at random.

Event1

Si1E, Si1T, CsI1E, CsI1Slow, CsI1Fast, CsI1T -Det1
Si2E, Si2T, CsI2E, CsI2Slow, CsI2Fast, CsI2T -Det2
… …
SinE, SinT, CsInE, CsInSlow, CsInFast, CsInT -Detn
Timestamp

Event2
Event3
…
EventN

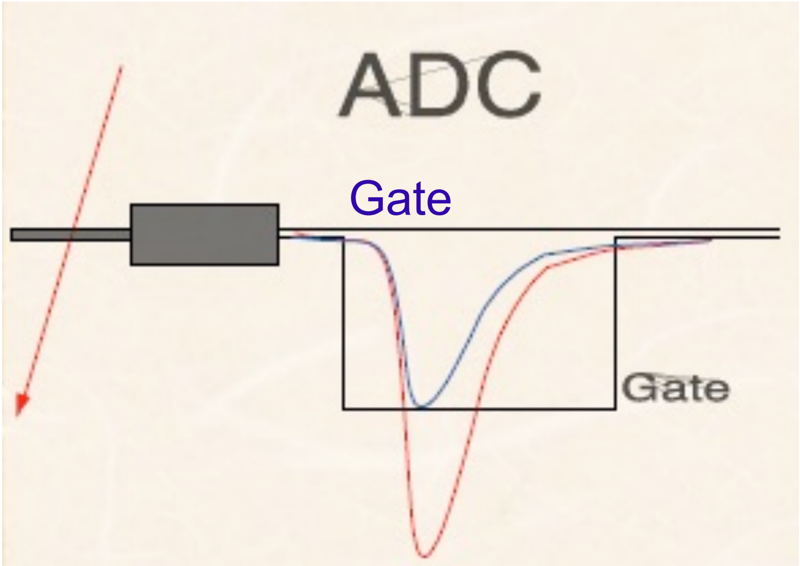
- Only a few events are interesting.

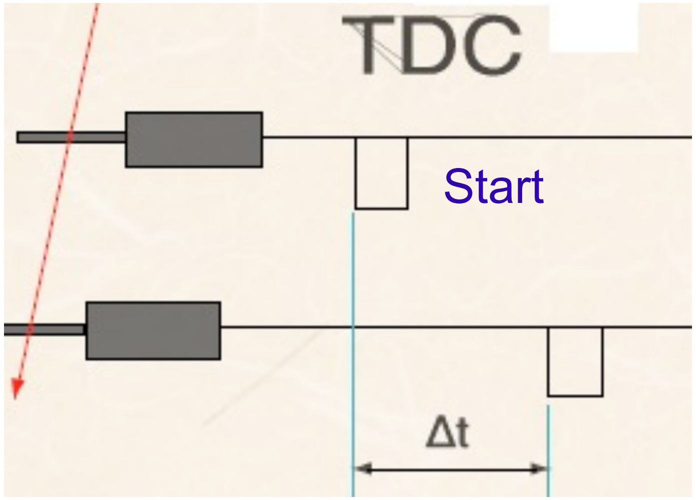
- The data acquisition system digitizes, formats and stores these information in a way which can be retrieved for later analysis.

Trigger/Gate & Busy

- Digital Camera is a “simple” physics DAQ system.
- 3-6 million channels
- Dead-time(BUSY) is important! -How long before I can take another picture??

ADC/TDC Modules need a Trigger to start conversion



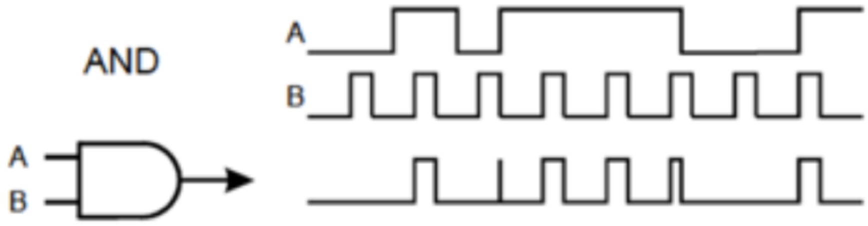


Trigger

- The data acquisition system needs to know when an interaction “Event” has occurred in the detector.
- Some detectors are faster than others.
- Signals from fast detectors are combined to make a decision on when an interesting event has occurred. This is called a ***trigger***.

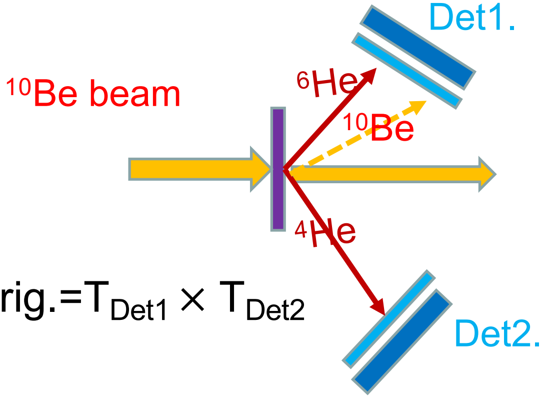
the trigger make a selection starting from the signals coming from the front-end electronics (hardware trigger) thus deciding if the event have to be readout or rejected.

Basic trigger logic

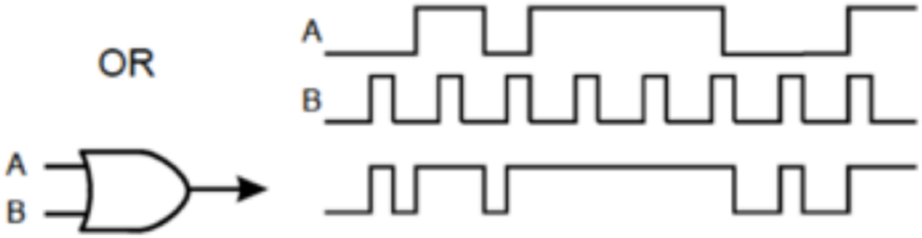


→ AND: Output high, when both inputs are high.

Reaction: (^{10}Be,^{6}He+^{4}He)

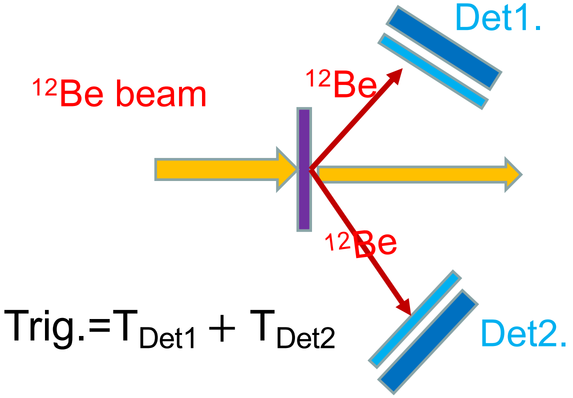


Trig.=$T_{Det1} \times T_{Det2}$

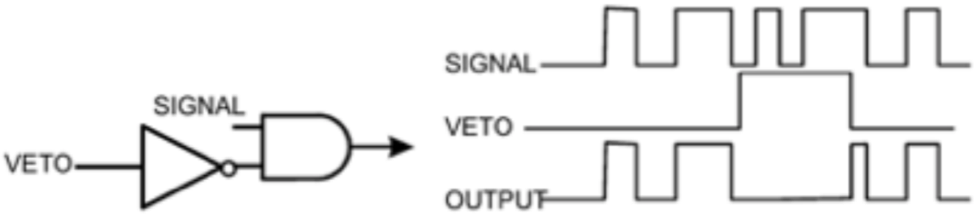


→ OR: Output high, when any input is high.

Reaction: (^{12}Be,^{12}Be')

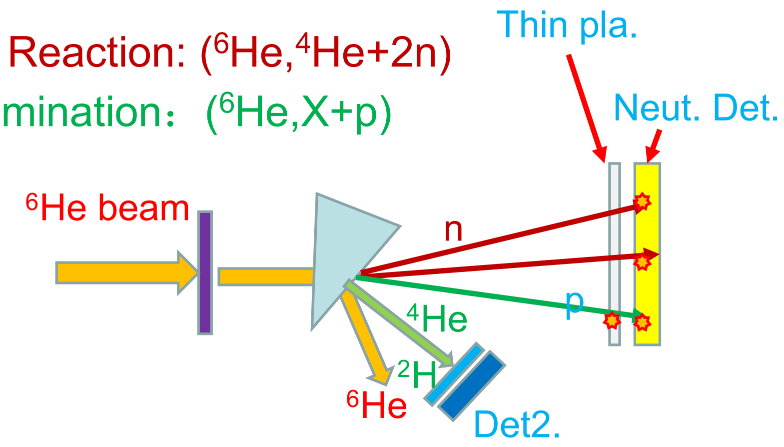


Trig.=$T_{Det1} + T_{Det2}$



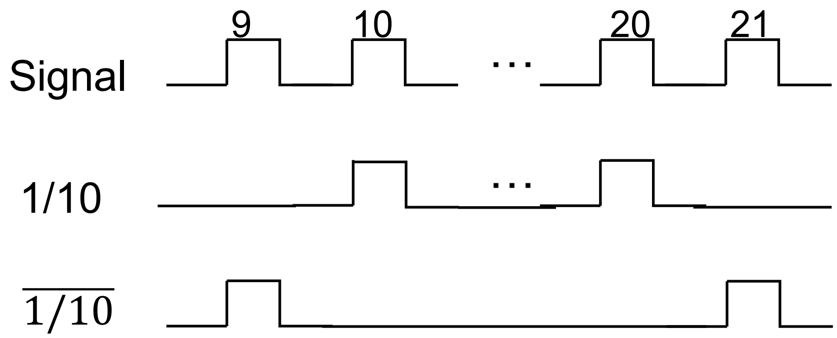
Reaction: (^{6}He,^{4}He+2n)

Contamination：(^{6}He,X+p)



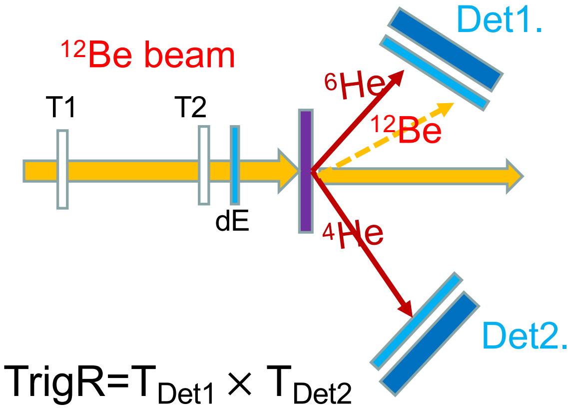
$\text{Trig.}=T_{\text{Det2}}\times T_{\text{Neut}}\times \overline{T}_{\text{pla}}$

Sampling(Rate Divider)



sampling rate:1/n

Reaction: (^{12}Be,^{6}He+^{4}He)



$\text{TrigR}=T_{\text{Det1}}\times T_{\text{Det2}}$

$\text{TrigDB}=(T_{\text{det1}}+T_{\text{det2}})/n$

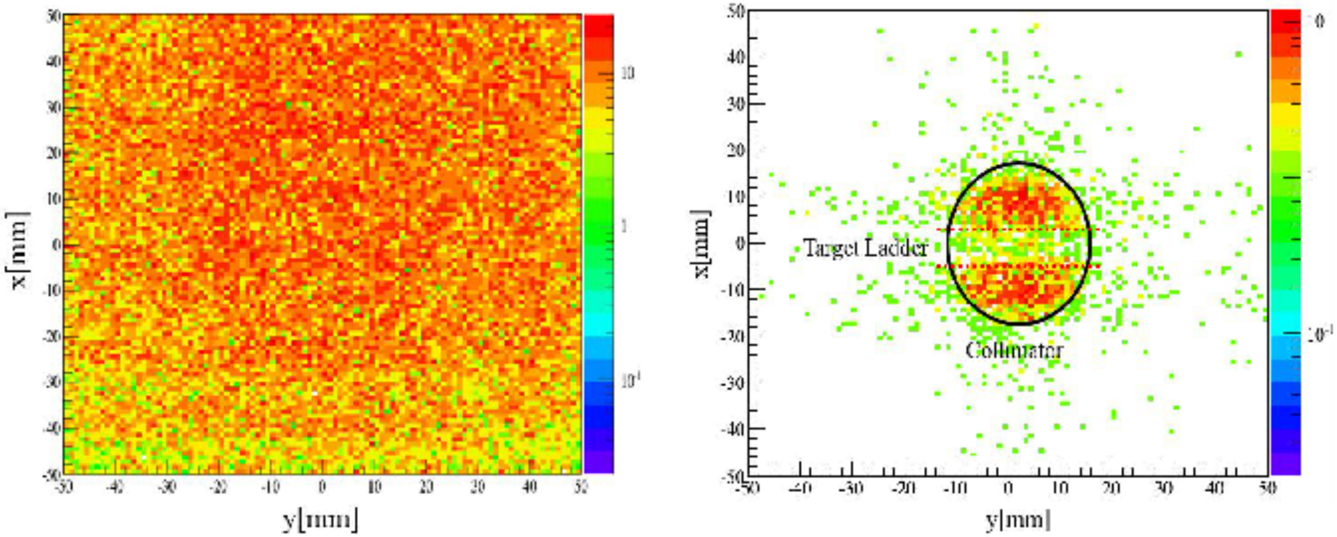


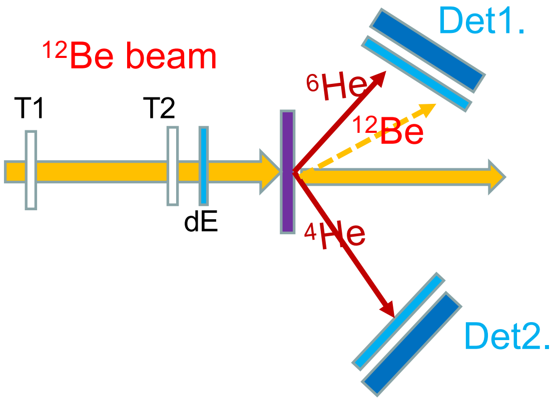
图 3.3-9　靶上束流的位置分布，左图束流子触发的结果，右图选择束流和 HODOSCOPE 符合的结果

$TrigR = T_{Det1} \times T_{Det2}$ — Main Physics

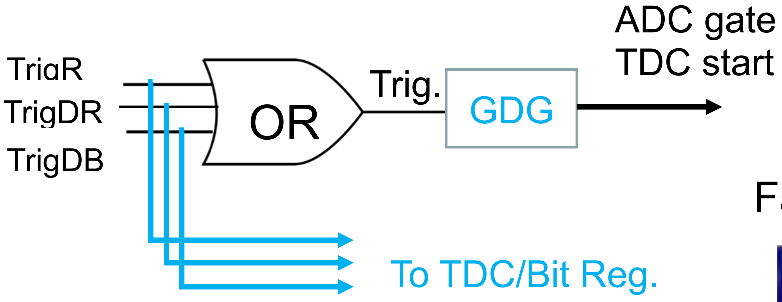
$TrigDR = (T_{Det1} + T_{Det2})/n_1$ — By products
- elastic scattering etc.

$TrigDB = T_1 \times T_2/n_2$ — Upstream events. monitoring

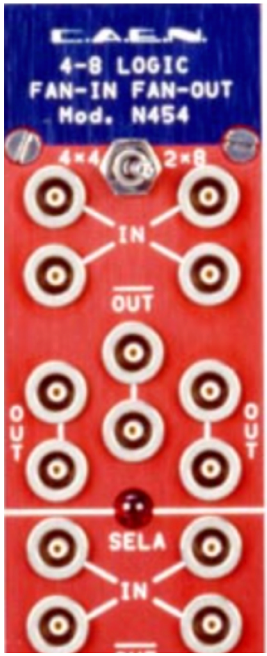
Reaction: (^{12}Be,^{6}He+^{4}He)



Trig.=TrigR+TrigDR+TrigDB



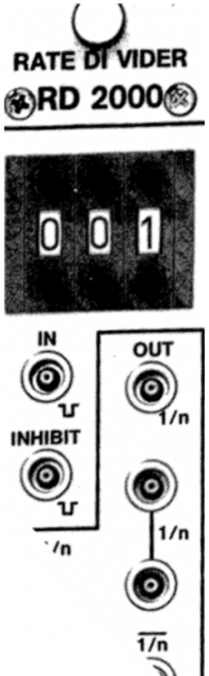
Fan In/Fan out



GDG

Logic unit

Rate Divider



Trigger and DAQ

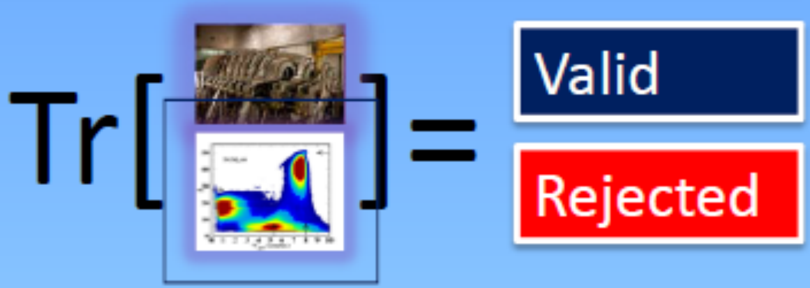
TRIGGER: the trigger make a selection starting from the signals coming from the front-end electronics (hardware trigger) thus deciding if the event have to be **readout** or **rejected**.

First level trigger **L1:** is based generally on hardware (discriminators, charged particle multiplicity, etc). It is generally fast (100ns-1µs).

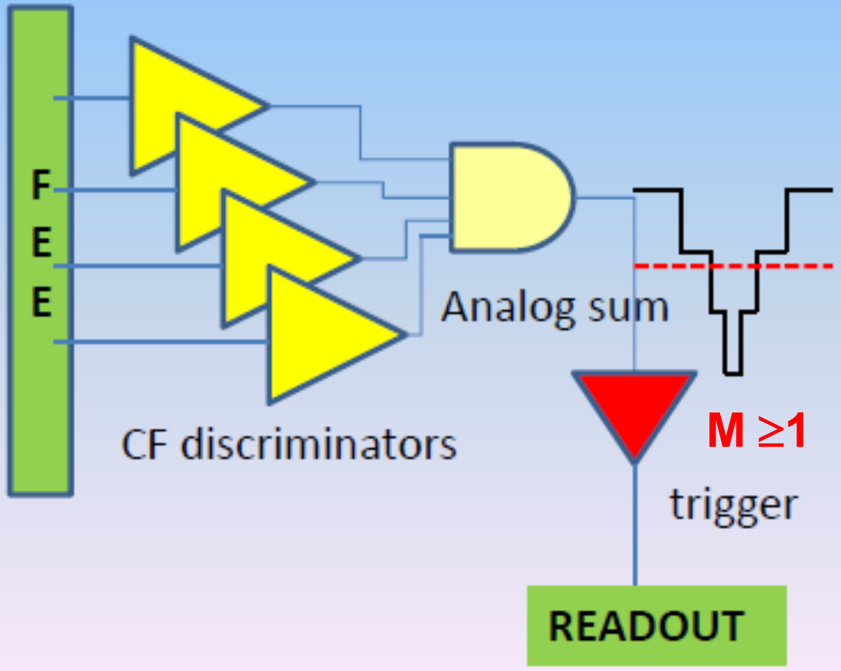
Second level trigger **L2:** for example particle identification, energy calibration, etc. (CPUs, FPGA, etc). (milliseconds)

Third level trigger **L3-Ln:** in high energy physics, event reconstruction, physics processes (computer's farms). (10^{-2}- 10^{0} sec).

Simplified L1 trigger in CHIMERA based on particles Multiplicity

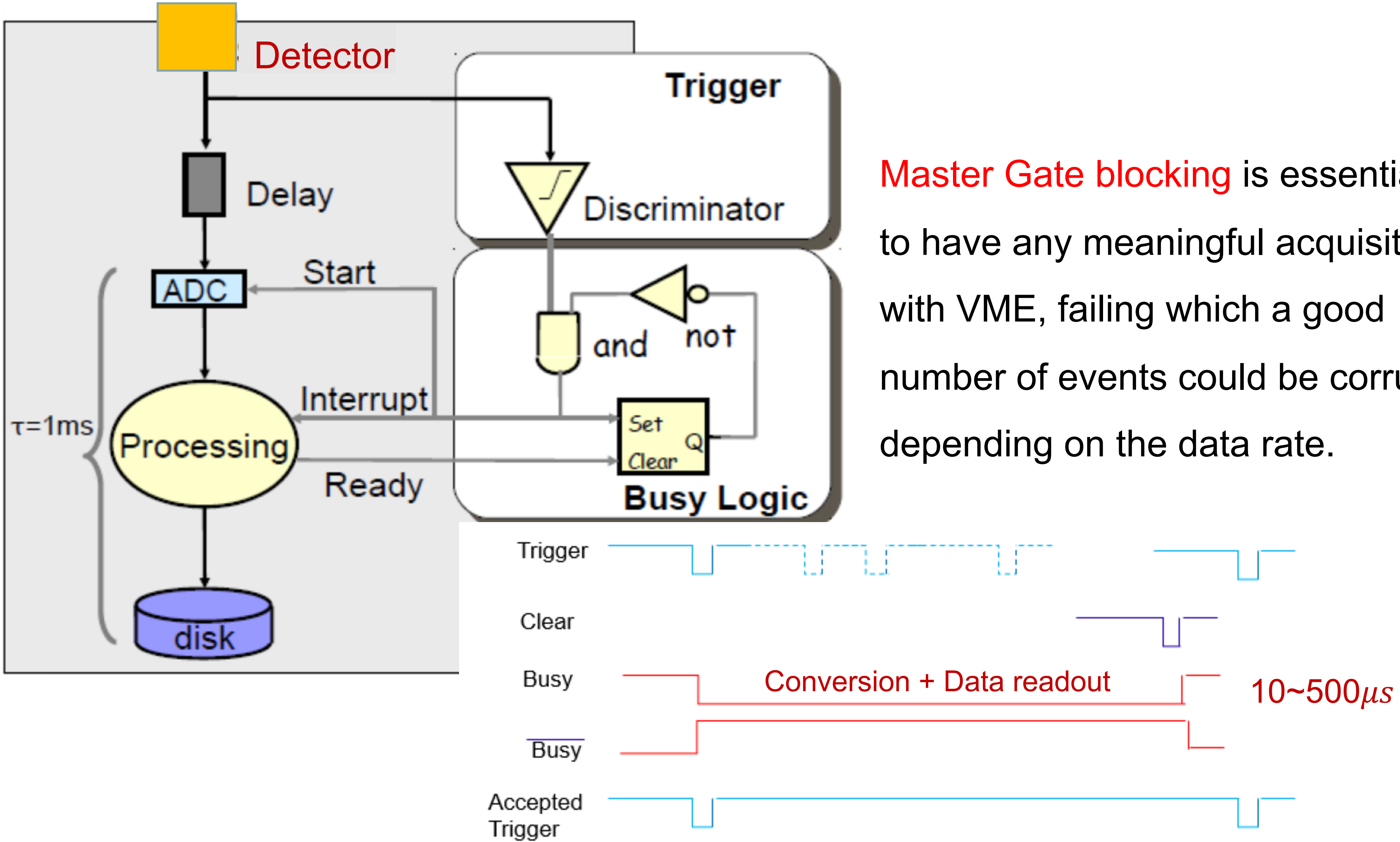


Trigger choice depends on **detector and physics**



real trigger & busy logic

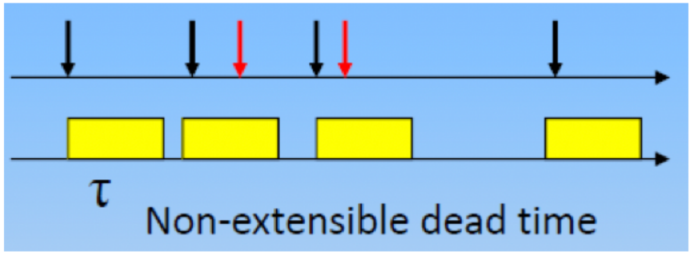
- No master gate should reach the modules until the current event has been completely digitized and read out. (especially for VME)



Master Gate blocking is essential to have any meaningful acquisition with VME, failing which a good number of events could be corrupt depending on the data rate.

Deadtime and Efficiency

Deadtime (%): ratio between the time the DAQ is busy and the total time .



f=true interaction rate
v=recorded count rate
τ=system dead time

$$v = n/(1+n\tau)$$

Efficiency: $N_{record}/N_{tot} = 1/(1 + f\cdot\tau)$

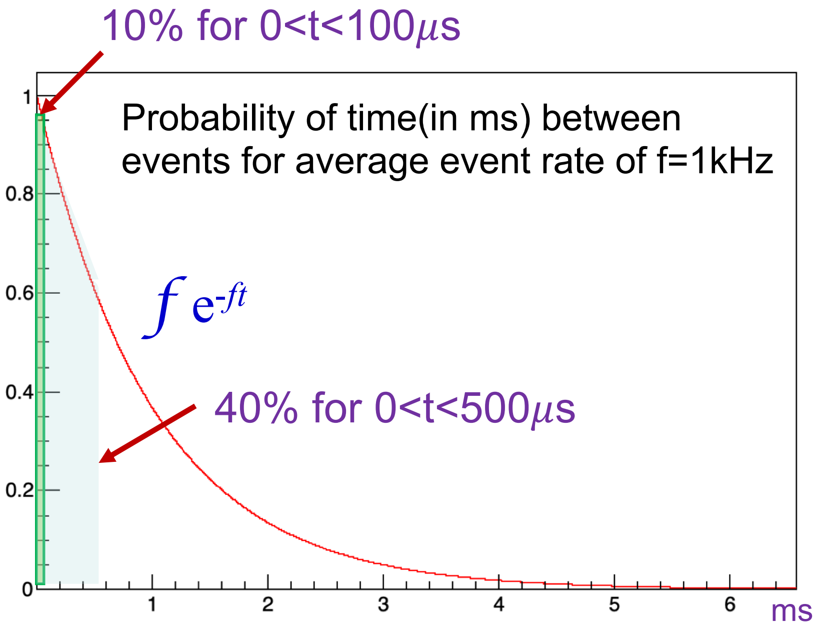
Due to the fluctuations introduced by the stochastic process the efficiency will always be less 100%

To have higher efficiency → $f\tau \ll 1$

e.g. f =1kHz, ε >90%

→ $\tau = 1/f\,(1/\varepsilon - 1) = 100\mu s$

→ $1/\tau$ >10kHz



In order to cope with the input signal fluctuations, we would need to overdesign our DAQ system by a factor 10.

Single cycle data readout: event by event readout

System BUSY = Conversion + Data readout

$\sim 10\mu s$ $\sim a\ few\ 100\mu s$

- Software cycle time to process an instruction
- Data transfer (only a event)
- Store to hard disk

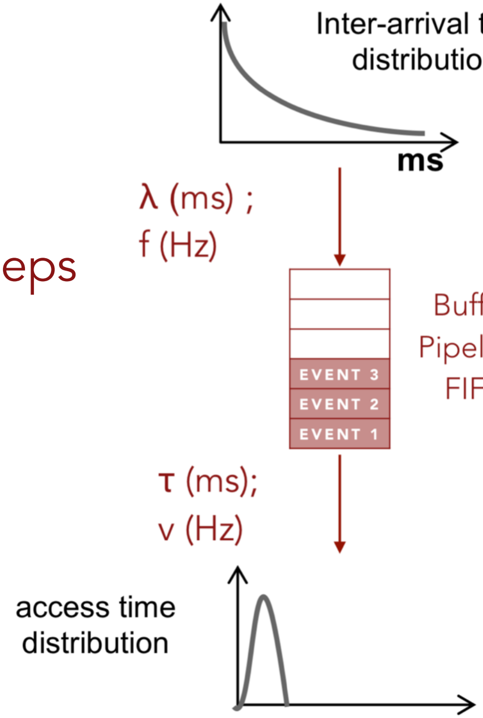
Buffers(FIFO) are introduced which hold temporarily the data.
The FIFO absorbs and smooths the input fluctuation, providing a steady (De-randomized) output rate.

ex. Multi-Event Buffer: for CAEN v785 (VME ADC)

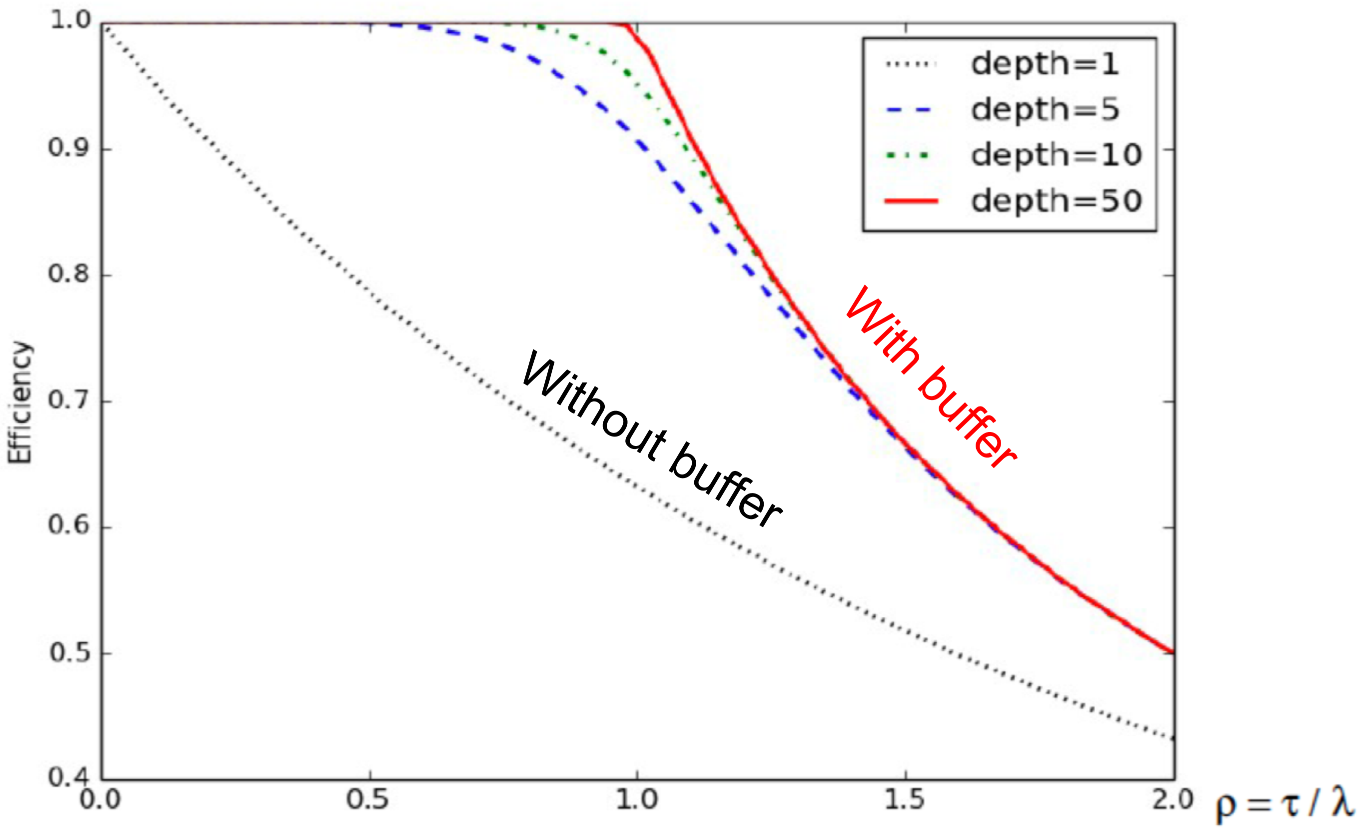
•Busy is now defined by if the buffer is full or not.
•Processor pulls data from the buffer at fixed rate, separating the event receiving and data processing steps

Data readout

- Software cycle
- Block Data transfer (multi-events)
- Store to hard disk

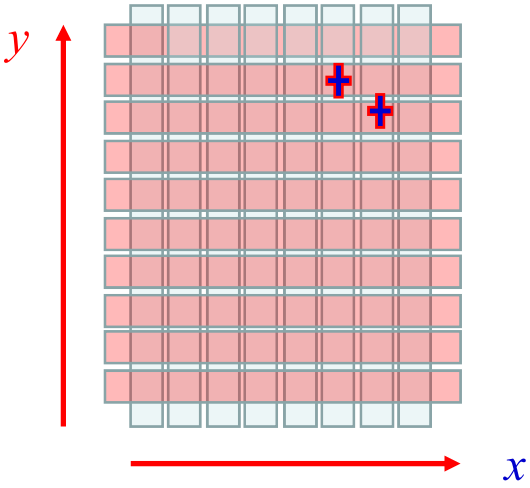


- Efficiency as a function of the ratio of the event processing time (τ) to average event arrival time (λ)



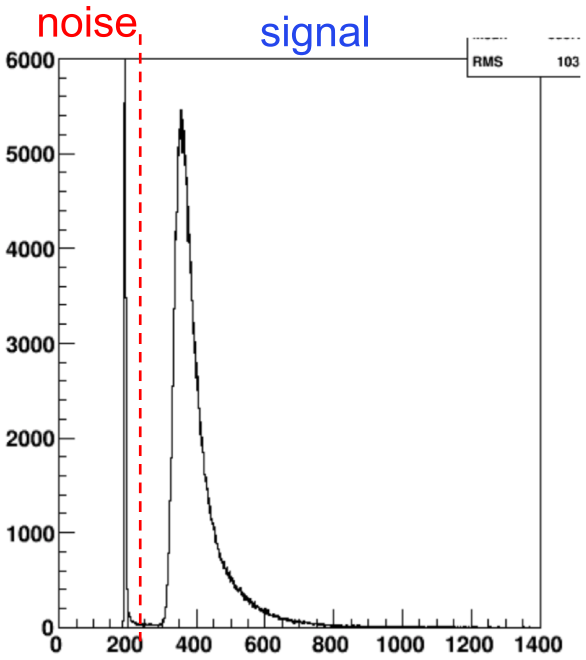
Zero-suppression

DSSD Hit pattern



Raw data

	X		Y
0	203	0	195
1	216	1	1191
2	209	2	4090
3	215	3	216
4	220	4	209
5	199	5	200
6	3100	6	207
7	2300	7	197
	198		203



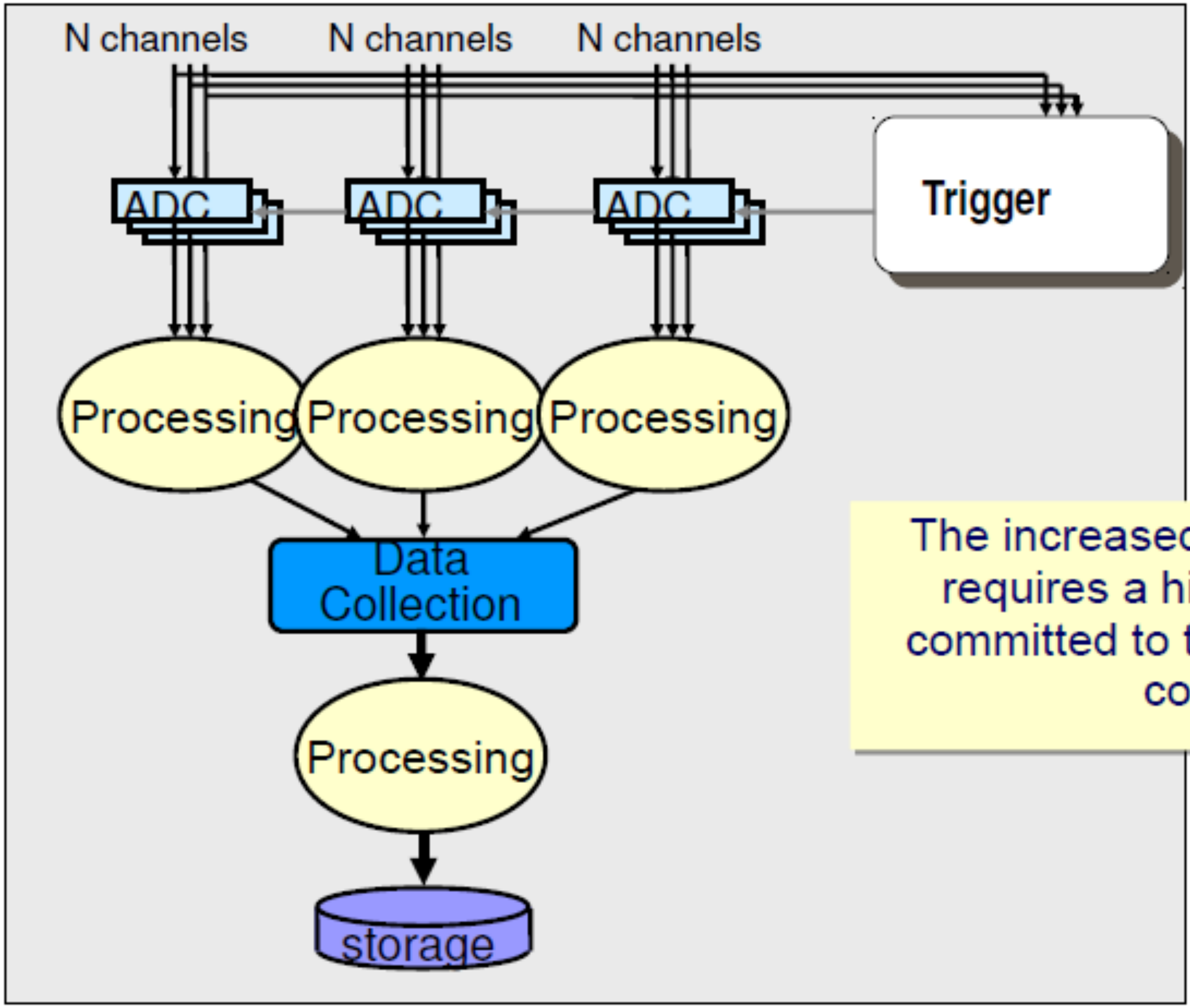
Before event data is passed to the DAQ system it must be properly zero-suppressed to limit the loading of the data links and the DAQ system. Data must also be properly organized in self-describing data structures.

After Zero-suppression

	X		Y
5	3100	1	1191
6	2300	2	4090

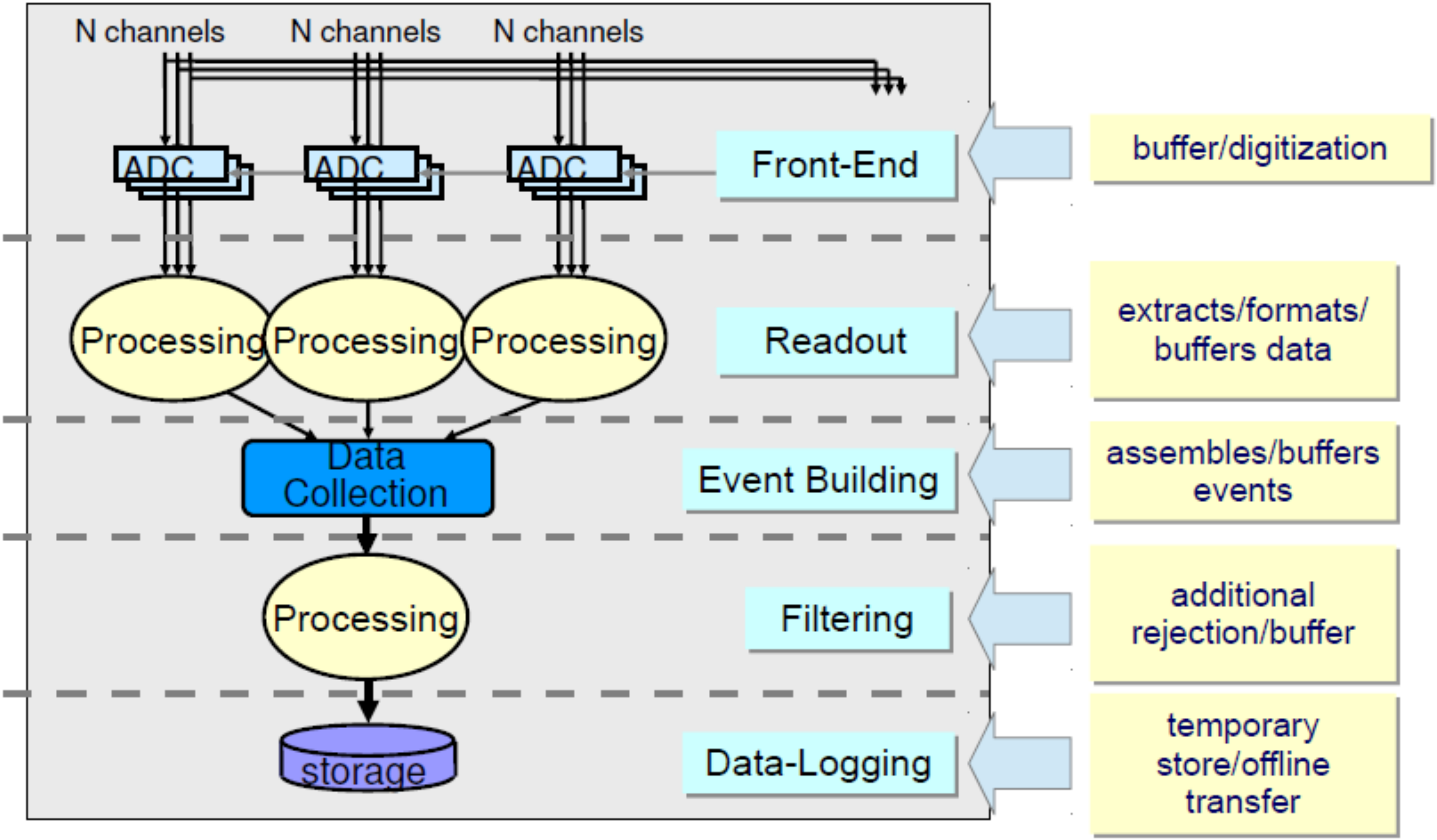
Zero-suppression(ADC) <-> Overflow-suppression(TDC)

Basic DAQ: more channels



The increased number of channels requires a hierarchical structure committed to the data handling and conveyance

Large DAQ: Constituents



Front-End — buffer/digitization

Readout — extracts/formats/ buffers data

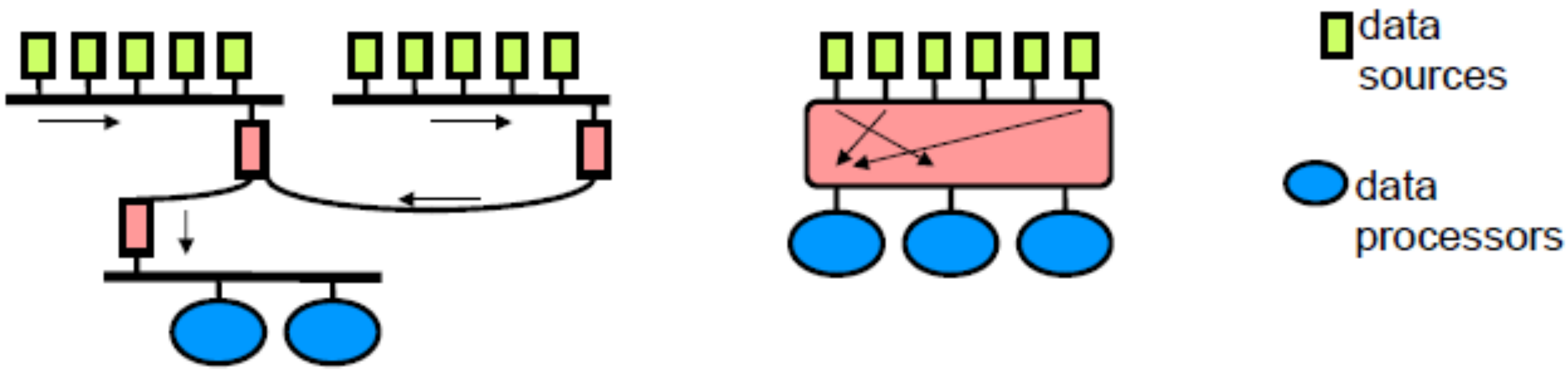
Event Building — assembles/buffers events

Filtering — additional rejection/buffer

Data-Logging — temporary store/offline transfer

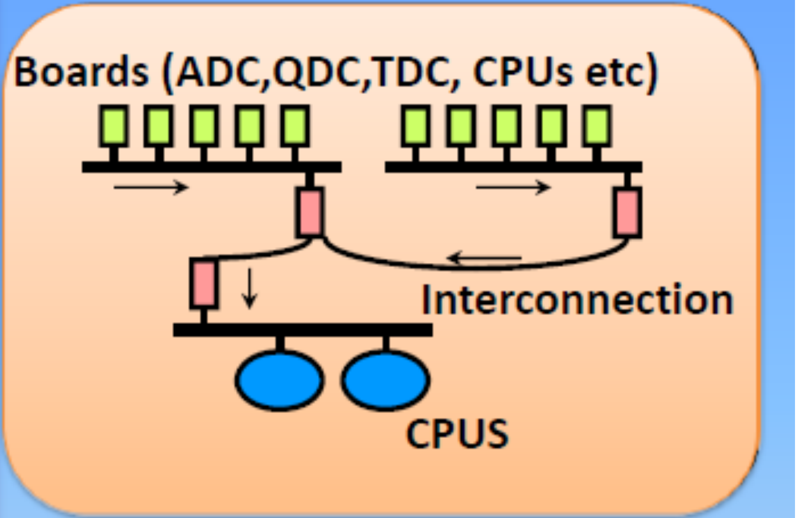
If there are many channels, DAQ can be divided in blocks (for example all boards of a crate, all crates, a farm of computers to process data). All theses blocks have to be **interconnected**. Synchronization: to form full events from partial ones. **INTERCONNECTION** **Bus, Networks**

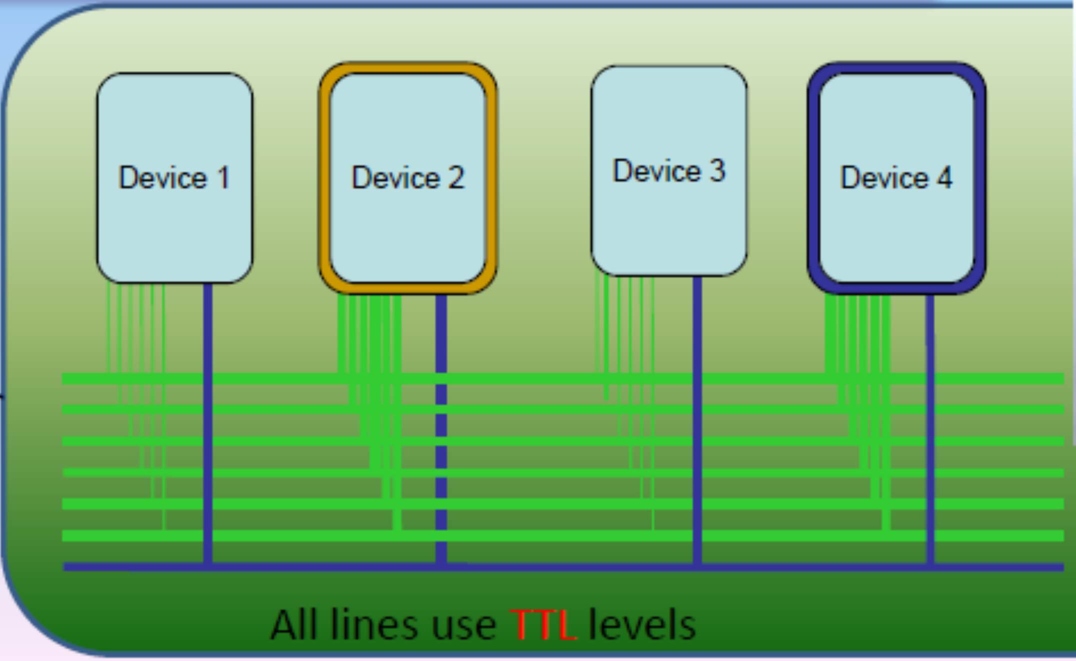
→ Two main classes: bus or network



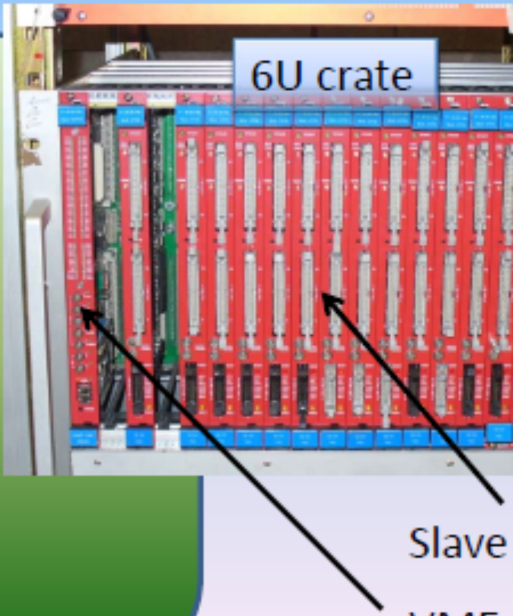
Buses

- → Esemples: VME, VXI, CAMAC, PCI, PCIe …
- → Devices are connected by a “shared” bus
- → Devices can be “master” or “slave”
- → Devices can be addressed in a unique way in the bus.
- → Because the bus is shared among different board a bus “arbitrer” is generally necessary (VME)





Courtesy W. Vandelli



Bus adapter/ controller:

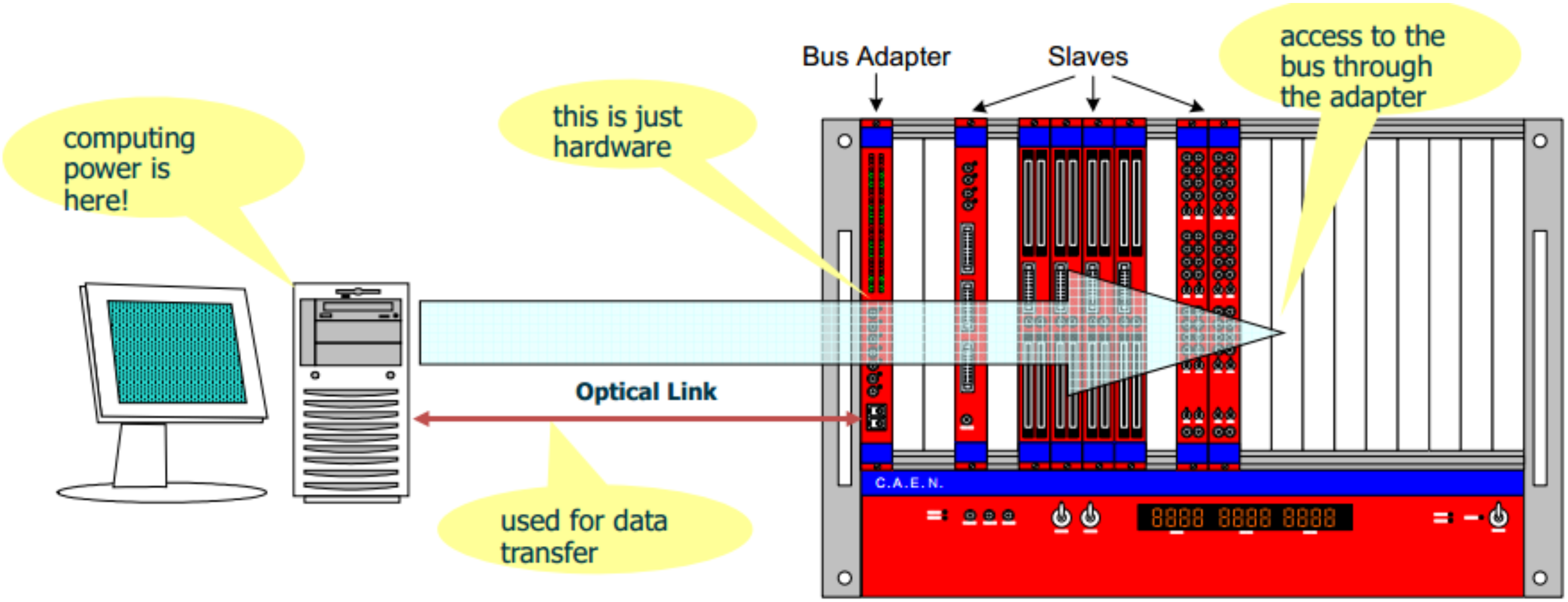
- It makes possible to control the bus remotely from a standard PC through a high speed link
- The acquisition program (DAQ) runs on the remote PC
- Computing power (processors, memories, disks) is on the PC

Addressing:

All modules have a unique address in the bus.

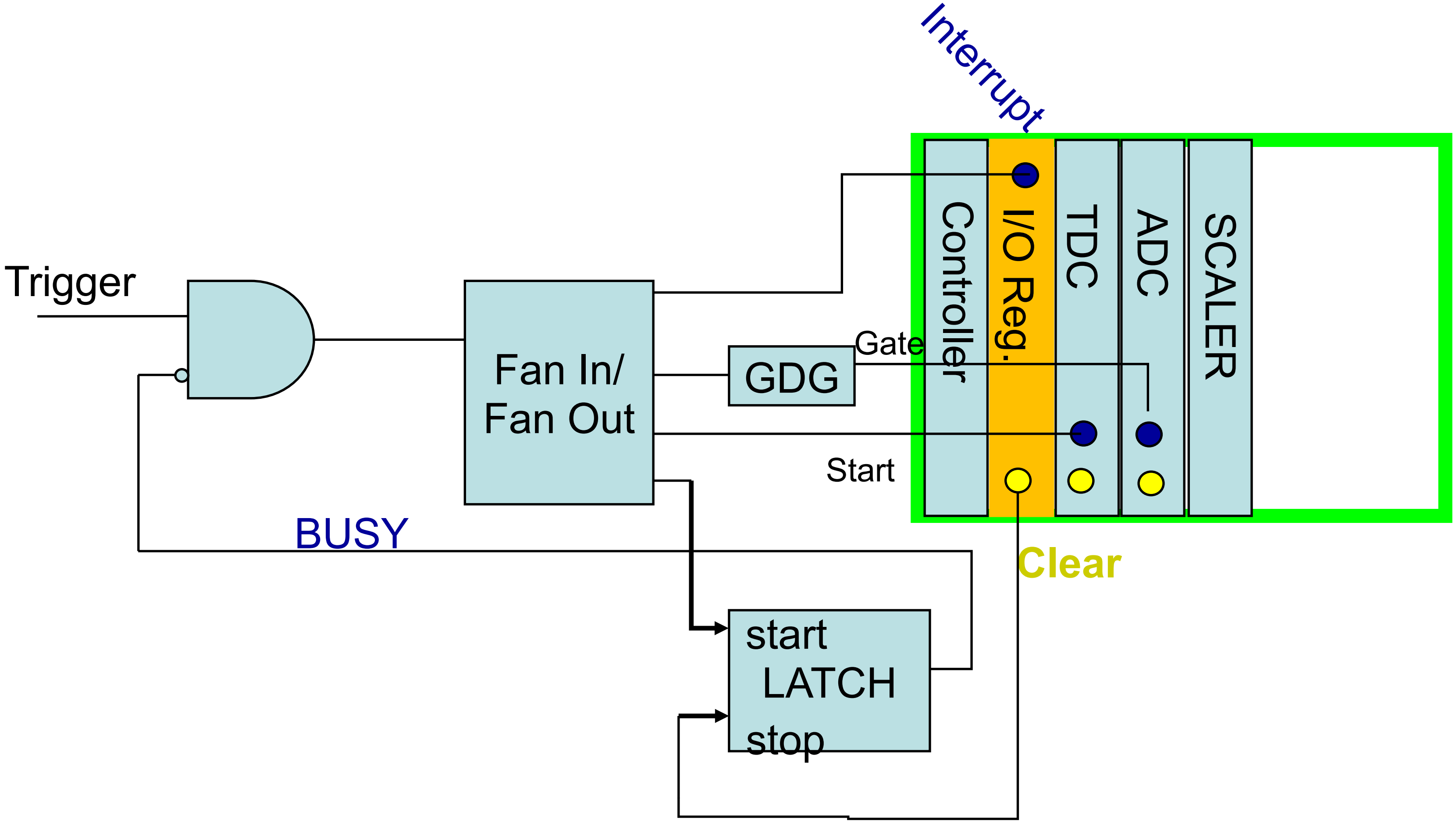
Registers/buffers in a modules have a unique address.

Access and control modules through their addresses.



Interrupt:

All modules included into the measurement are operated in the "master trigger“ mode, i.e. a simultaneous data collection of all parameters is triggered by the interrupt given by one in particular defined module. The interrupt of the other modules are usually disabled.



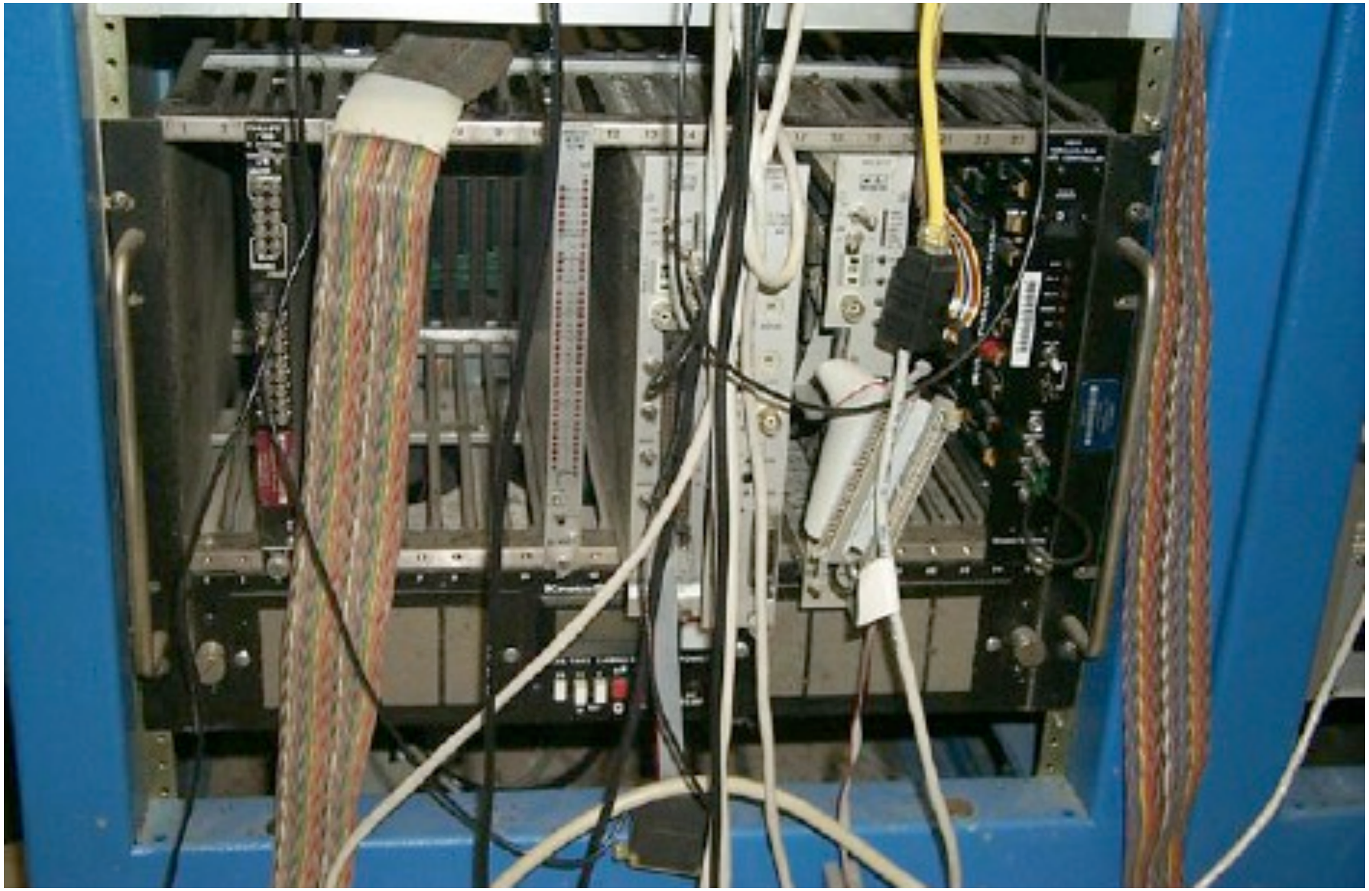
CAMAC(Computer Automated Monitoring And Control)

Old IEEE Standard 24 bit bus.

Relatively slow(3 MB/sec).

Small boards.

A lot still around.

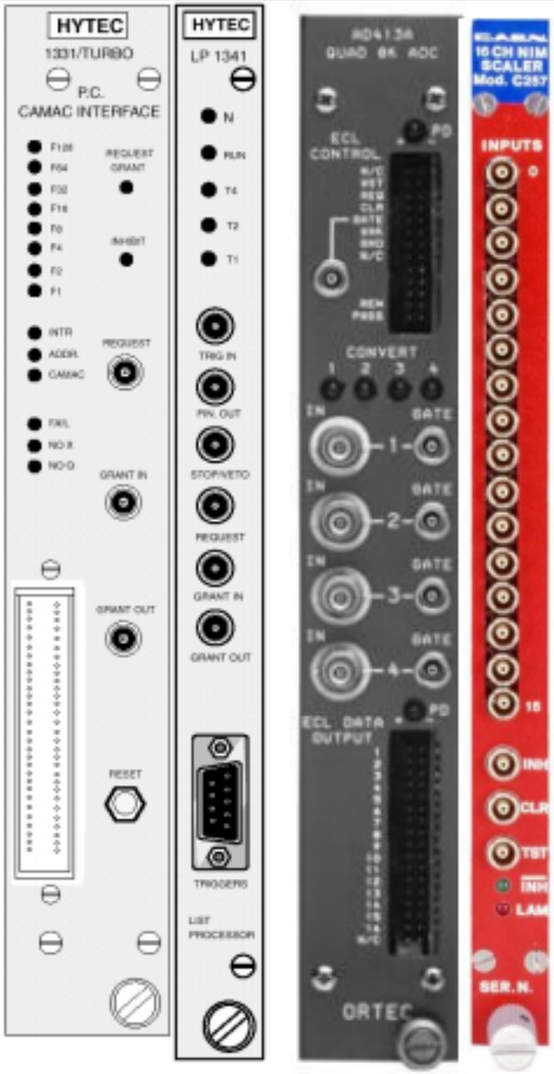


CAMAC

- CAMAC: Computer Automated Measurement And Control
- Standardized by ESONE, IEEE/ANSI, IEC around 1972

Specification

- 19” Crate, modular hardware form factor, 25 slots to attach modules.
- Crate contains power supply, backplane & FAN unit.
- Slot 25 is for CAMAC Crate controller module. The slot 1-24 may be occupied by CAMAC modules.
- The CAMAC backplane provides +6V, -6V, +24V & -24V, 0V (return) DC power; optionally +12V, -12V,



CAMAC backplane signals

- CAMAC Data & Address lines:
  - 24bit *READ* & 24bit *WRITE* bus.
  - N – Slot number: each slot is directly addressed by controller with this signal
  - A – sub-address : Each CAMAC module can host 16 sub-unit
  - F – Function: Each sub-unit can perform 32 functions
- Control signals
  - S1, S2: Timing signal for dataway operations
  - Z: Initialize
  - C: Clear
  - B: Busy
  - I: Inhibit
- Module responds with signals:
  - L: Look At Me (LAM) signal. L line individually connects each slot to the controller, works as a interrupt to controller.
  - Q: asserts the operation status
  - X: asserts the command has been accepted

CAMAC dataway operations

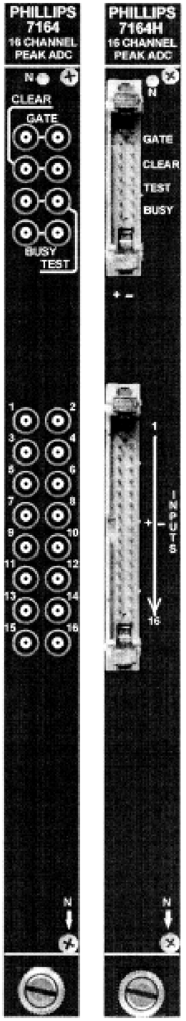
Phillips Scientific | **16 Channel Peak ADC** | **CAMAC MODEL 7164 7164H**

DATA WORD FORMAT

16 ... 13	12 ... 1
Channel ID	Channel Data

CONTROL REGISTER FORMAT

16 ... 9	8 ... 4	3	2	1
Conversion Delay (Read Only)	0	UT Enable	LT Enable	PED Enable



CAMAC DATAWAY OPERATIONS

F(0) •A(X) : Read event data memory for Channel (X+1). Data word as described above.

F(1) •A(X) : Read the parameter memory pointed to by the most recent F17 operation for channel (X+1).

F(4) •A(0) : Read Sparse Data. Only those channels with data that falls between the upper and lower thresholds are read, starting with the highest numbered channel. Reading an empty buffer returns Q false. Data word as described above.

F(6) •A(0) : Read the Control Register. Format described above.

F(6) •A(1) : Read the Hit Register. Shows which channels' pedestal corrected data falls within their upper and lower thresholds.

F(8) : Test LAM. A Q=1 response is generated if LAM is present and enabled. The address lines have no effect on this command.

F(9) : Clear the Module. Resets front end, clears and disables LAM, disables pedestals and thresholds. The address lines have no effect on this command.

F(10) : Clear LAM. Occurs on S2 strobe. The address lines have no effect on this command.

F(11) •A(0) : Reset the Control Register. Occurs on S2 strobe.

F(11) •A(1) : Reset the Hit Register and LAM. No effect on data memory. Occurs on S2 strobe.

F(11) •A(2) : Reset the Test Register. Occurs on S2 strobe.

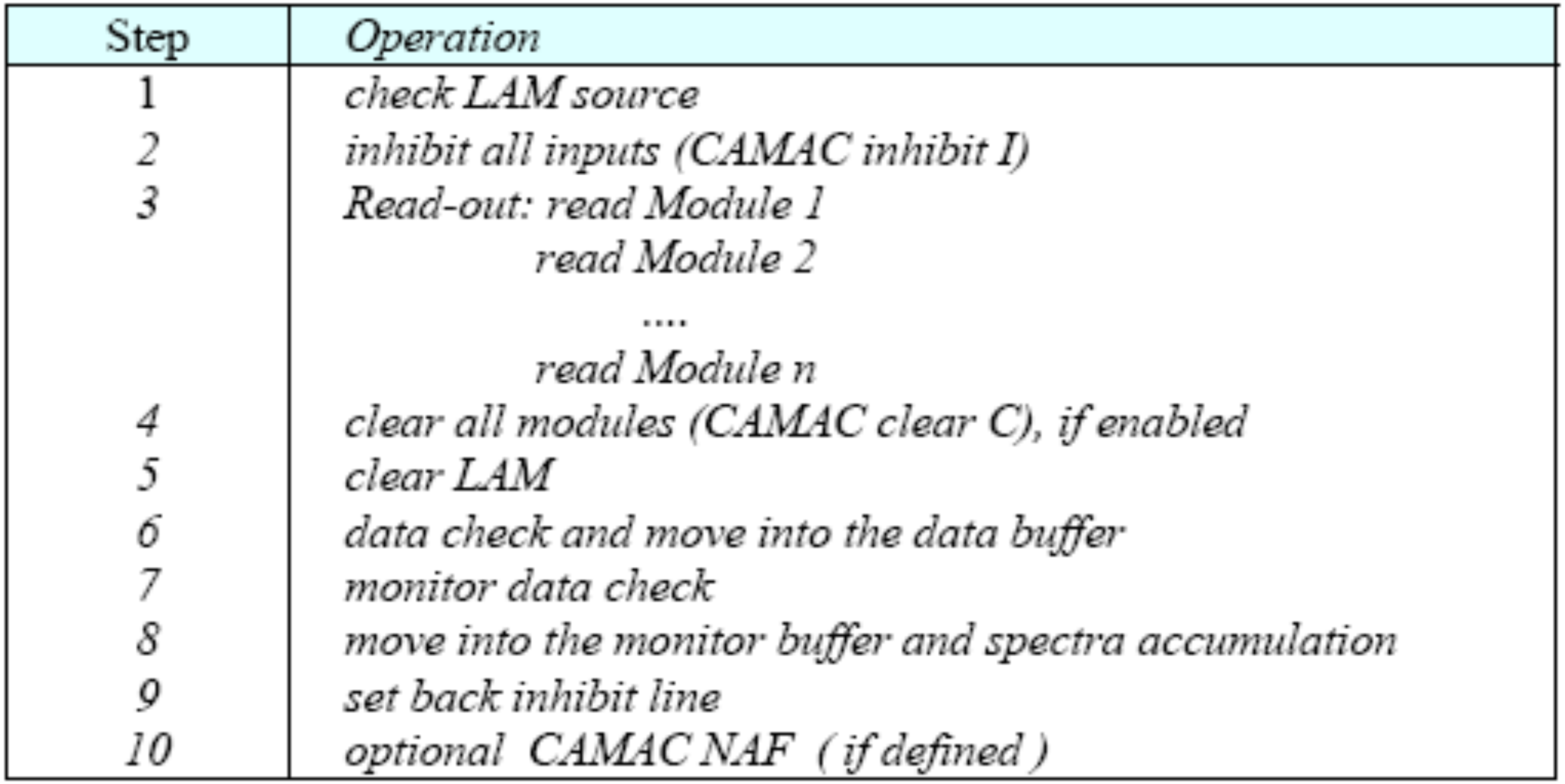
F(11) •A(3) : Reset the Hit Register, LAM and data memory. Occurs on S2 strobe.

F(16) •A(X) : Write to data memory for channel (X+1).

CAMAC based DAQ

All modules Triggered by the LAM (CAMAC Look-At-Me) given by one in particular defined module. This module is characterized by an enabled LAM line in contrast to the other modules where the LAM lines are automatically disabled

- After getting the LAM the following data collection cycle is started



Step	Operation
1	*check LAM source*
2	*inhibit all inputs (CAMAC inhibit I)*
3	*Read-out: read Module 1* *read Module 2* .... *read Module n*
4	*clear all modules (CAMAC clear C), if enabled*
5	*clear LAM*
6	*data check and move into the data buffer*
7	*monitor data check*
8	*move into the monitor buffer and spectra accumulation*
9	*set back inhibit line*
10	*optional CAMAC NAF (if defined)*

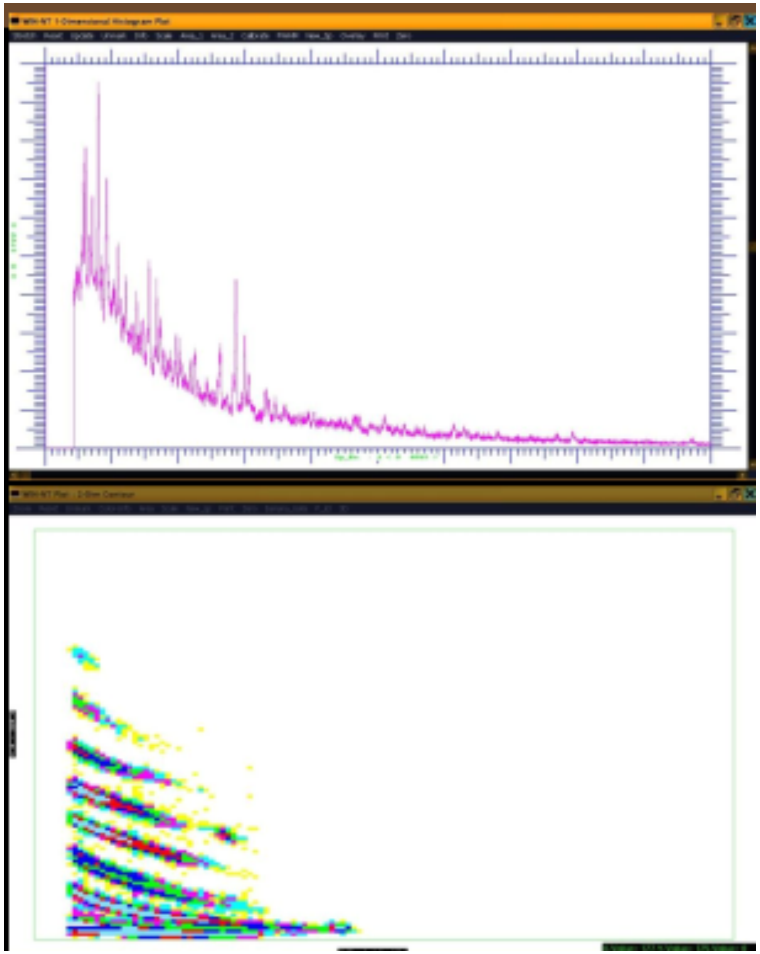
A CAMAC Data Acquisition system with CC7700 and PC-Linux

http://rarfaxp.riken.go.jp/~iwasa/cc7700.html

```
static int camacNAF(int N, int A, int F, long *data, int *stat)  /* long word data NAF operation */
```

```
static int dc_int(unsigned short buffer[])
{
  static long j;
    j=inl(BASE_ADDRESS+4);
    pos=3;
   for(j=0;j<16;j++){
     camacNAF(ADC1,j,0,&i,&k);
     buffer[pos++]=i;
  }

  for(j=17;j<32;j++){
     camacNAF(TDC1,j,0,&i,&k);
     buffer[pos++]=i;
  }
…
}
```



VME (Versa Module Europa)

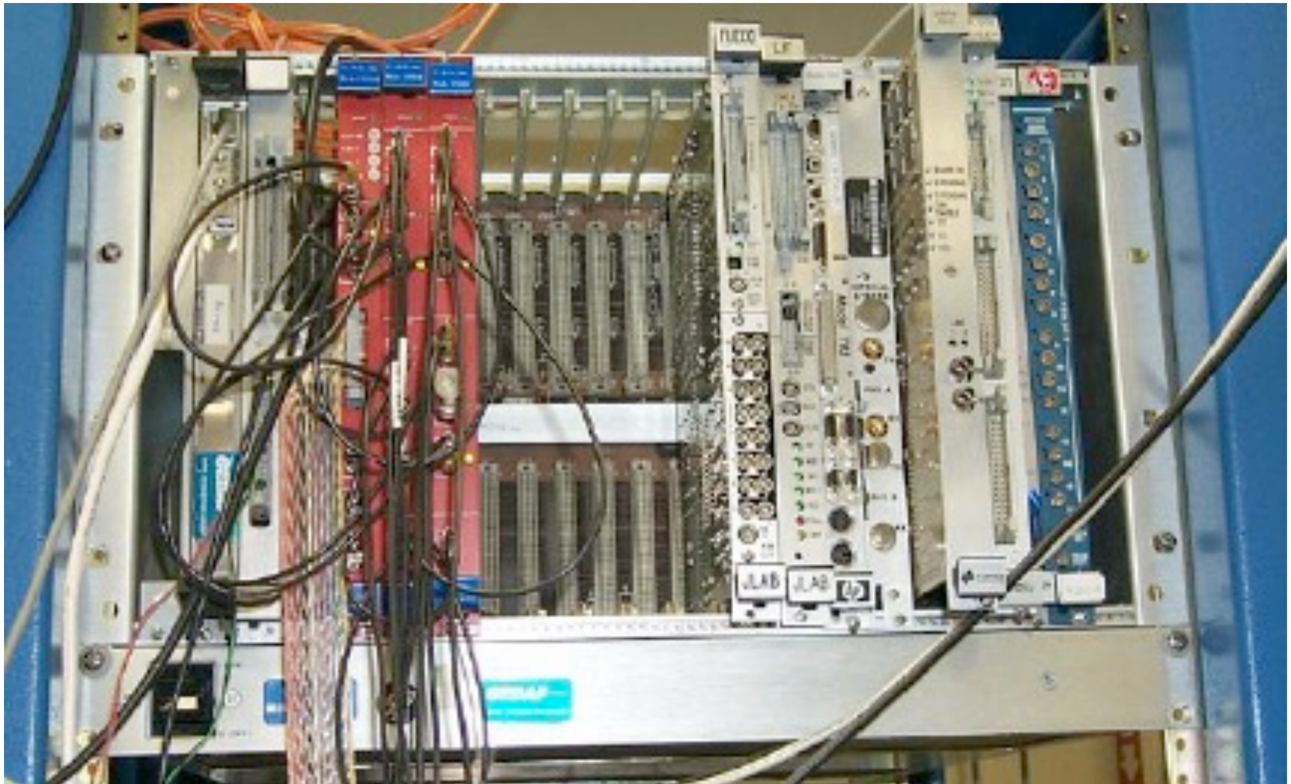
International standard for interconnecting modules.

32/64 bit bus (80MB/s)

Large number of commercial products (used heavily in the military).

VME64X provide bandwidth options (160-320 MB/s).

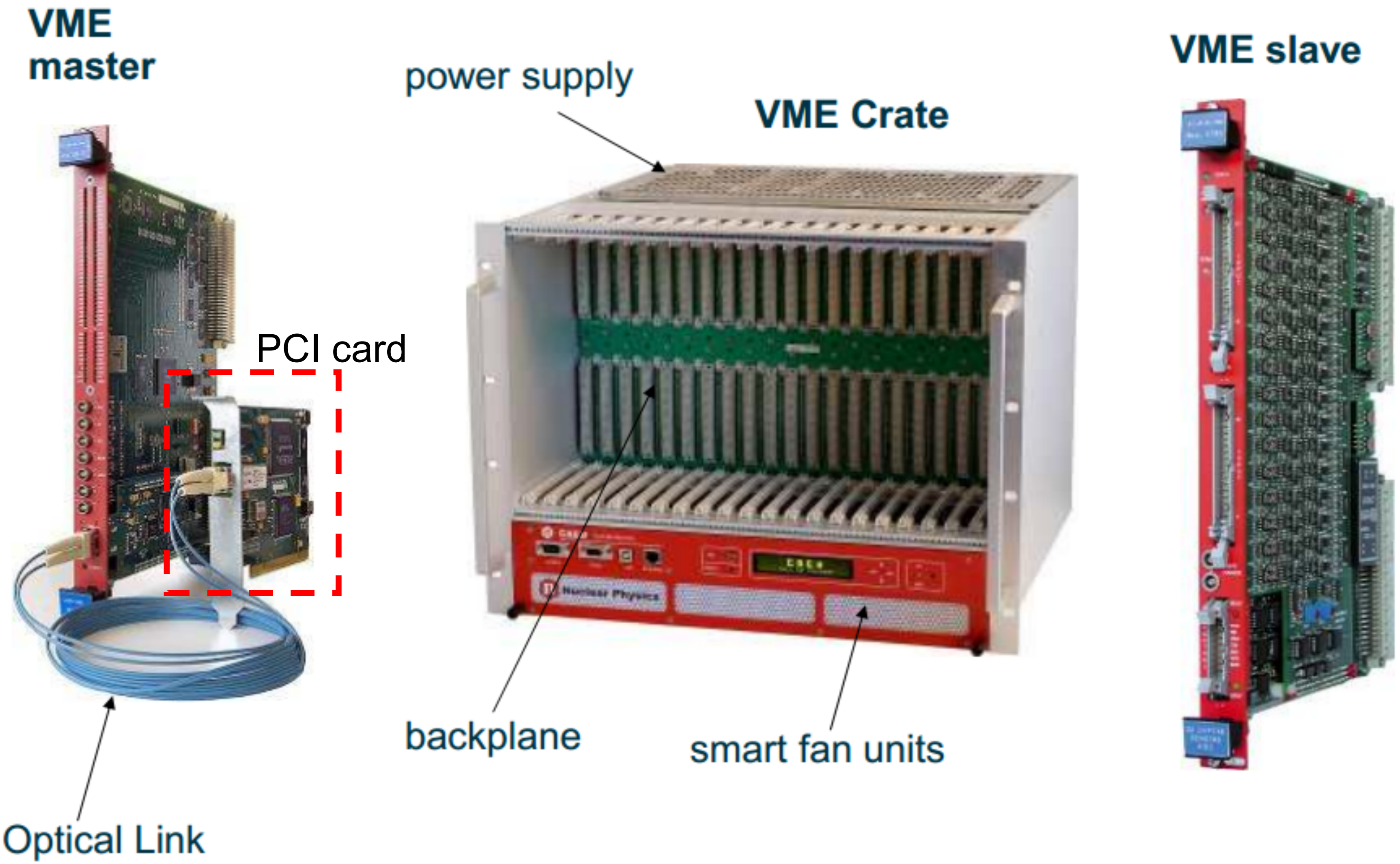
Currently transitioning from FASTBUS



VME

- VME: Versa Module Eurocard

- 19" crate with power supply unit & FAN unit
- Crate's height and depth depend on form-factor. 3U, 6U and 9U crates (1U=1.75") are available
- 6U VME64x crate has 21 slots and common backplane for all the signal and power lines
- p1 & p2 160pin and p0 is 95pin connector for each module
- +5V, +12V, -12V, +3.3V DC power are available in VME64X crate
- Hot-swappable, User IO



VME master

power supply

VME Crate

VME slave

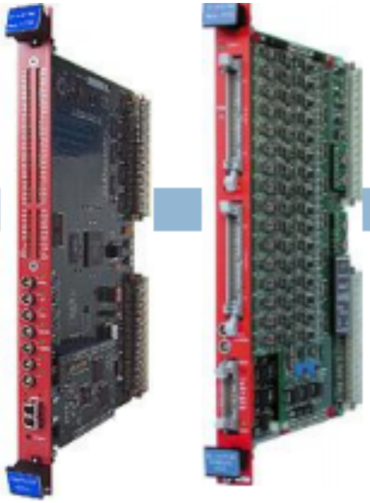
PCI card

backplane

smart fan units

Optical Link

VME modules

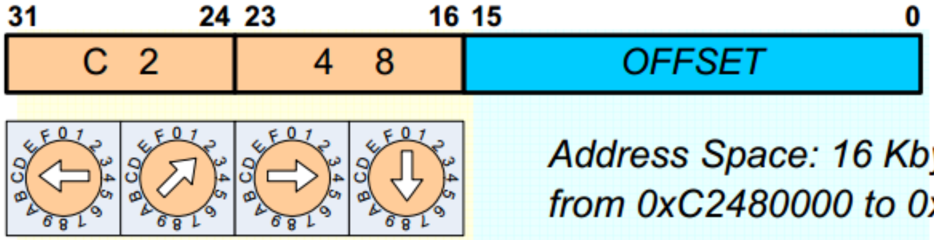


- CAEN VME785, 792 & 775
  - 32 channel 12bit resolution
  - 5.7us ADC conversion time for all 32channels
  - 32event FIFO memory
  - External ECL bus for control and synchronization
  - BLT32, CBLT and MBLT capable
- MDI2, MADC32 from mesytec

Zero suppression
Overflow suppression
 - to speedup data transfer, i.e. reduce dead time of DAQ

VME Base Address (Hardware Setting)

A32 mode

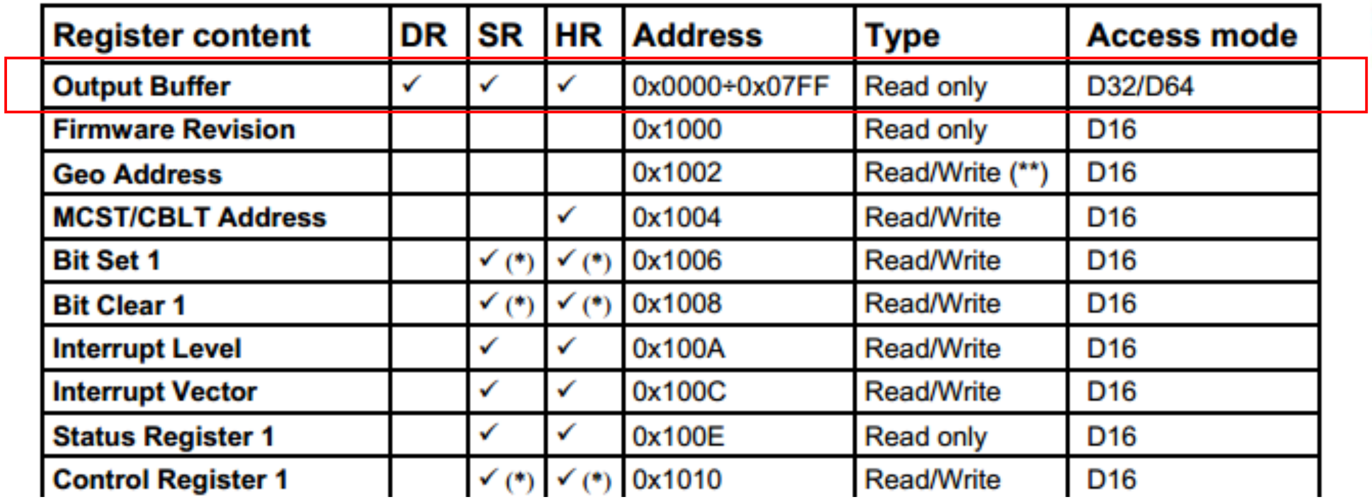


Address Space: 16 Kbytes
from 0xC2480000 to 0xC248FFFF

BASE ADDRESS:
which board inside
the crate

OFFSET:
which register inside
the board

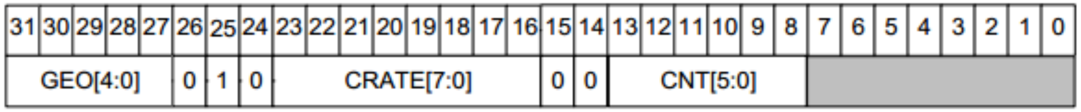
Table 4.2: Address Map for the Model V785



Register content	DR	SR	HR	Address	Type	Access mode
Output Buffer	✓	✓	✓	0x0000÷0x07FF	Read only	D32/D64
Firmware Revision				0x1000	Read only	D16
Geo Address				0x1002	Read/Write (**)	D16
MCST/CBLT Address			✓	0x1004	Read/Write	D16
Bit Set 1		✓ (*)	✓ (*)	0x1006	Read/Write	D16
Bit Clear 1		✓ (*)	✓ (*)	0x1008	Read/Write	D16
Interrupt Level		✓	✓	0x100A	Read/Write	D16
Interrupt Vector		✓	✓	0x100C	Read/Write	D16
Status Register 1		✓	✓	0x100E	Read only	D16
Control Register 1		✓ (*)	✓ (*)	0x1010	Read/Write	D16

```
cmdvme -wr addr                    : word read
cmdvme –wr 0xC2480000        : read a word from the first channel of the module
```

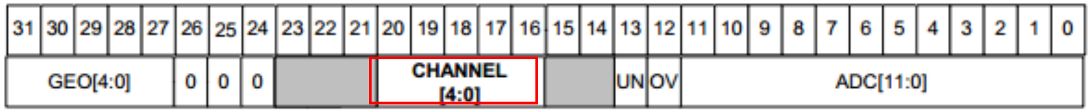
Data Output Buffer



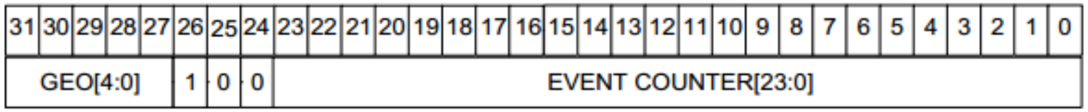
<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">GEO[4:0]</td><td>0</td><td>1</td><td>0</td><td colspan="8">CRATE[7:0]</td><td>0</td><td>0</td><td colspan="6">CNT[5:0]</td><td colspan="8">▨</td></tr>
</table>

Fig. 4.5: Output buffer: the Header

V785:

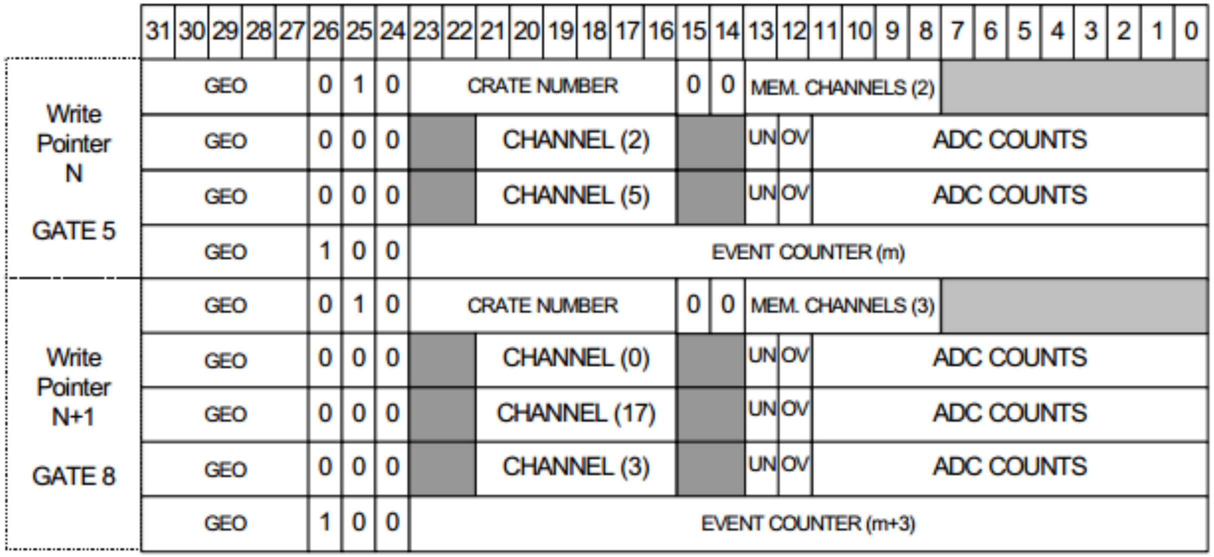


<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">GEO[4:0]</td><td>0</td><td>0</td><td>0</td><td colspan="3">▨</td><td colspan="5">CHANNEL [4:0]</td><td colspan="2">▨</td><td>UN</td><td>OV</td><td colspan="12">ADC[11:0]</td></tr>
</table>



<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">GEO[4:0]</td><td>1</td><td>0</td><td>0</td><td colspan="24">EVENT COUNTER[23:0]</td></tr>
</table>

Fig. 4.7: Output buffer: the End Of Block



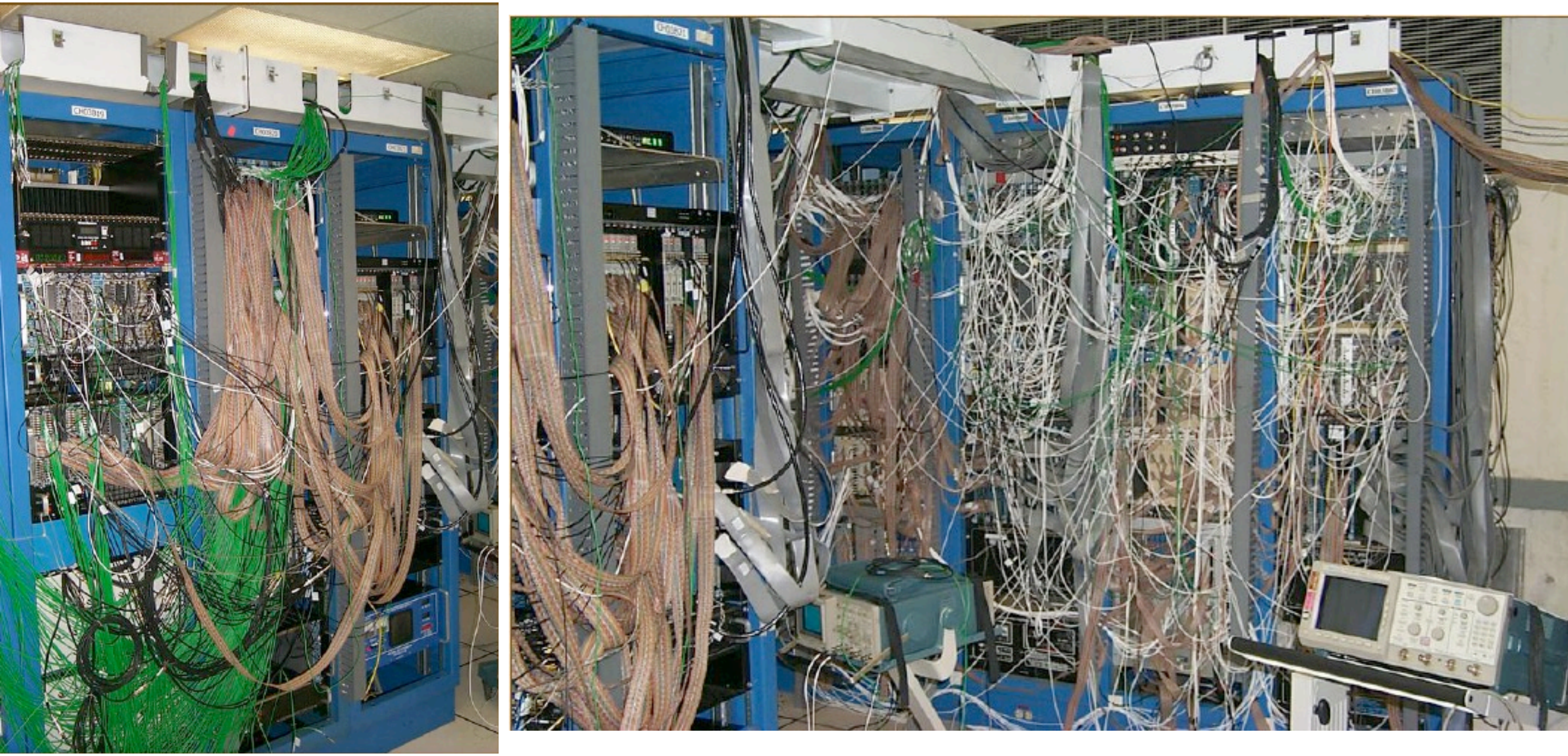
<table>
<tr><td></td><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td rowspan="4">Write Pointer N
GATE 5</td><td colspan="5">GEO</td><td>0</td><td>1</td><td>0</td><td colspan="8">CRATE NUMBER</td><td>0</td><td>0</td><td colspan="6">MEM. CHANNELS (2)</td><td colspan="8">▨</td></tr>
<tr><td colspan="5">GEO</td><td>0</td><td>0</td><td>0</td><td colspan="2">▨</td><td colspan="6">CHANNEL (2)</td><td colspan="2">▨</td><td>UN</td><td>OV</td><td colspan="12">ADC COUNTS</td></tr>
<tr><td colspan="5">GEO</td><td>0</td><td>0</td><td>0</td><td colspan="2">▨</td><td colspan="6">CHANNEL (5)</td><td colspan="2">▨</td><td>UN</td><td>OV</td><td colspan="12">ADC COUNTS</td></tr>
<tr><td colspan="5">GEO</td><td>1</td><td>0</td><td>0</td><td colspan="24">EVENT COUNTER (m)</td></tr>
<tr><td rowspan="5">Write Pointer N+1
GATE 8</td><td colspan="5">GEO</td><td>0</td><td>1</td><td>0</td><td colspan="8">CRATE NUMBER</td><td>0</td><td>0</td><td colspan="6">MEM. CHANNELS (3)</td><td colspan="8">▨</td></tr>
<tr><td colspan="5">GEO</td><td>0</td><td>0</td><td>0</td><td colspan="2">▨</td><td colspan="6">CHANNEL (0)</td><td colspan="2">▨</td><td>UN</td><td>OV</td><td colspan="12">ADC COUNTS</td></tr>
<tr><td colspan="5">GEO</td><td>0</td><td>0</td><td>0</td><td colspan="2">▨</td><td colspan="6">CHANNEL (17)</td><td colspan="2">▨</td><td>UN</td><td>OV</td><td colspan="12">ADC COUNTS</td></tr>
<tr><td colspan="5">GEO</td><td>0</td><td>0</td><td>0</td><td colspan="2">▨</td><td colspan="6">CHANNEL (3)</td><td colspan="2">▨</td><td>UN</td><td>OV</td><td colspan="12">ADC COUNTS</td></tr>
<tr><td colspan="5">GEO</td><td>1</td><td>0</td><td>0</td><td colspan="24">EVENT COUNTER (m+3)</td></tr>
</table>

Fig. 4.9: Multi-Event Buffer: data structure example

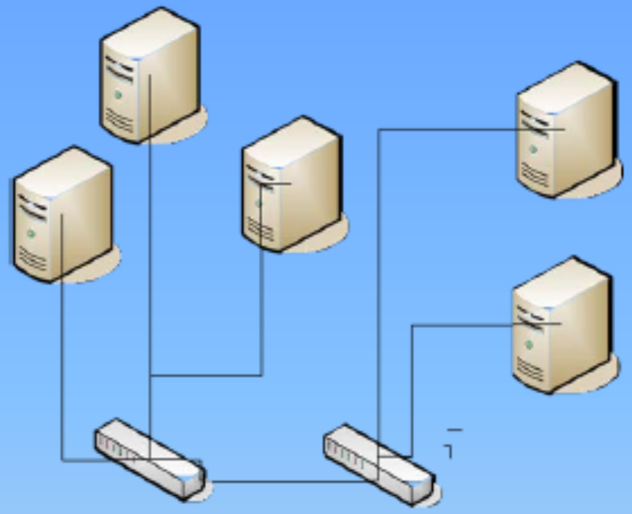
VME Data Readout

Data readout is possible in following modes -

- Single cycle
  - Reads a word from the slave FIFO
- BLT/MBLT (Block Transfer/Multiplexed Block Transfer)
  - Reads a number of events limited to 256 words from any slave module
  - In MBLT two 32 bit words are multiplexed to read as a single 64-bit word in VME64 standard
- CBLT (Chained Block Transfer)
  - Most pertinent mode for nuclear physics applications allowing for event-by-event data acquisition.
  - Reads the data belonging to the same physical event from several contiguous boards in a crate limited to 256 words per CBLT cycle



READOUT NETWORKS IN A DAQ



INTERCONNECTION IS OBTAINED BY **SWITCHES (it switchs frames to destination using MAC)**

It is possible to connect and exchange data between different "crates" or devices in a network making in parallel the readout of different parts of a multidetector

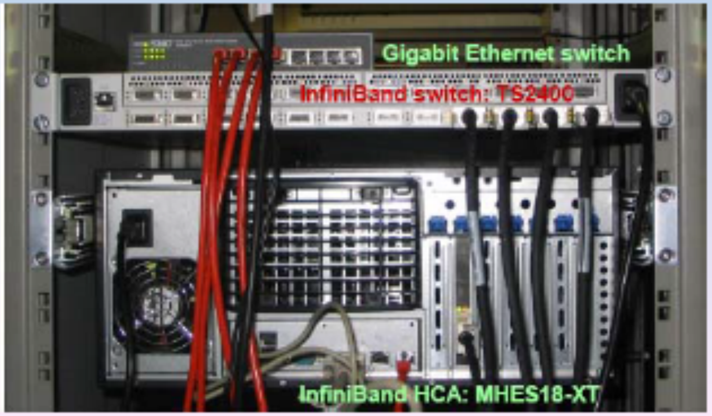
A network can link also different devices (for example permitting the coupling of different data acquisitions (in a network the connected devices are called "nodes" or "peers" **(no master or slaves)**. In a network devices communicates directly (or through a switch) exchanging data and messages.

ETHERNET is the most used protocol

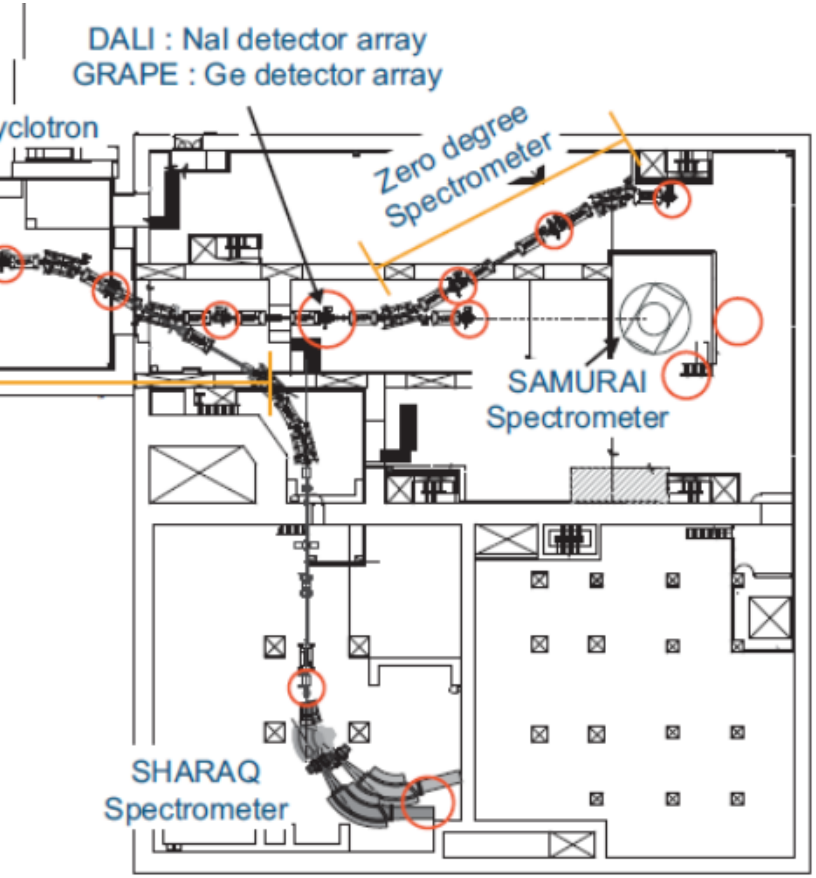
Others high bandwidth (data-transfer/second) , low latency protocols , low distances:
INFINIBAND
MYRINET

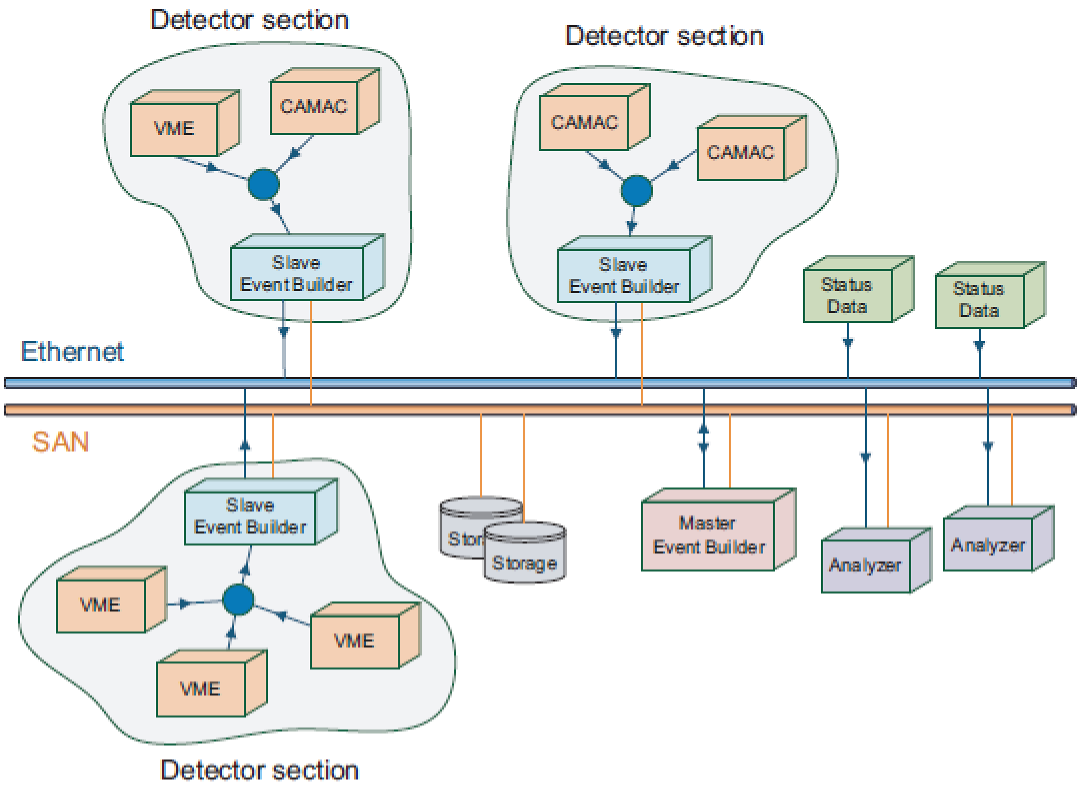
. . . .

Foto: GSI



Network distributed DAQ system

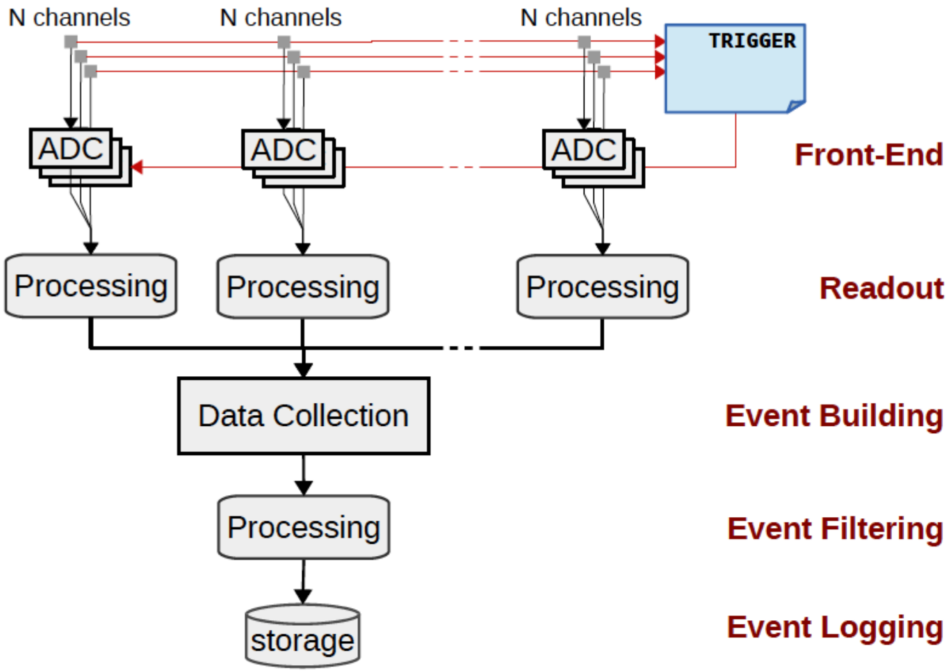




Event Building

- The detectors are spread over a physical volume of space.
- Bits and pieces of events arrive at different times from different places.
- All the parts of the event need to be collected together and packaged with other information needed by the analysis.

The Event builder is a very fast collating machine.



Run Control

- Need to start and stop the DAQ
- Place to input parameters which change from run to run.
- Place to read parameters from.
- Automatic monitor of the health of the DAQ system.
- Something nice for the operator to look at.

Run Control

Static parameters

Database: clasrun

Session: clasprod

Configuration: BONUS

Run Status

Run number: 49799

Run state: Active

Start time: Nov 10 13:35:47 EST 2005

End time:

Limits

Events:

KBytes:

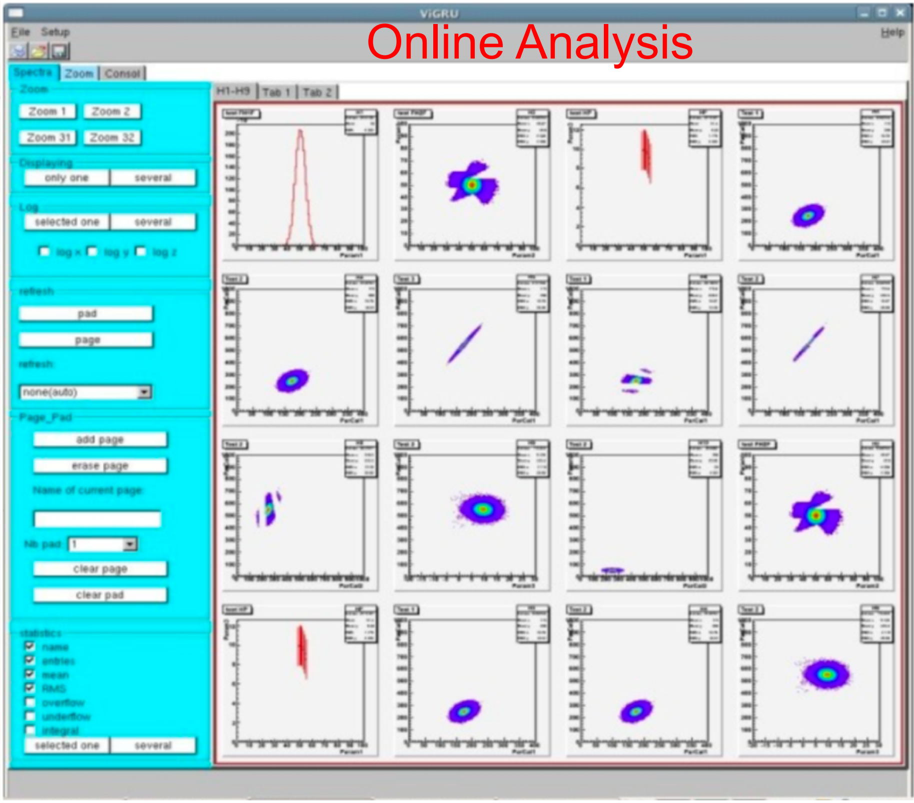
Run progress

Events this run: 274675

Event rate: 399

Data rate: 52073.67

```
prego succeeded.
Initiating go
5 sec. waiting scaler2 to go
Go
go succeeded.
Initiating postgo
Postgo
postgo succeeded.
```

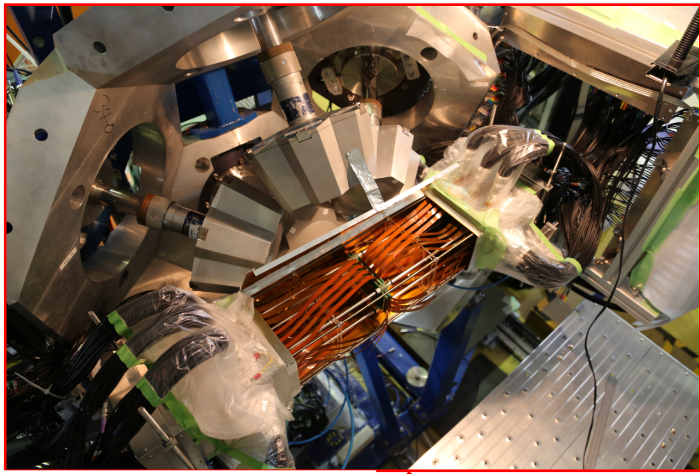


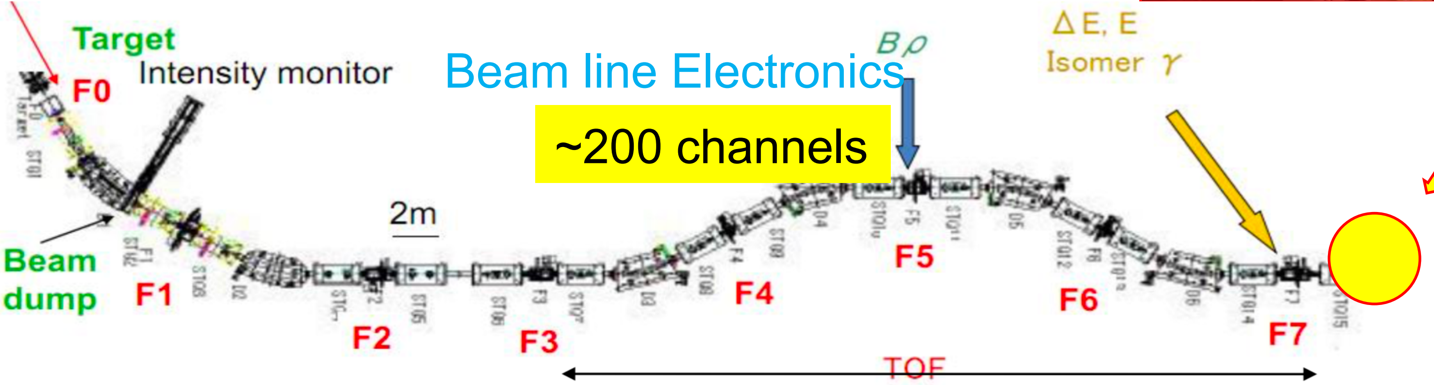
Online Analysis

☑ name
☑ entries
☑ mean
☑ RMS
☐ overflow
☐ underflow
☐ integral

Timestamp-based DAQ

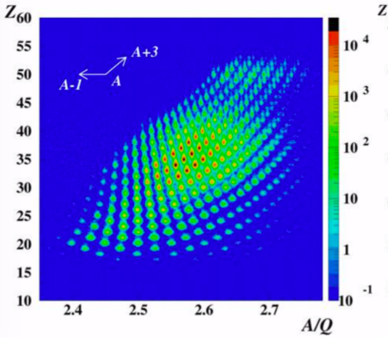
- Independent DAQ for each sub-system
  - own trigger and timestamp
- Synchronize sub-systems with timestamp
  - fixed time difference and offset

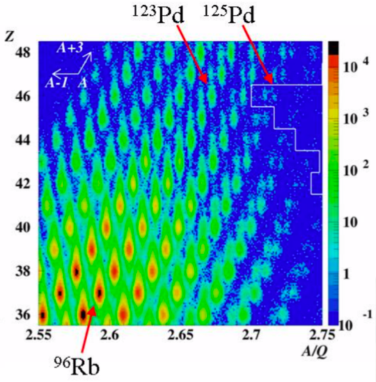


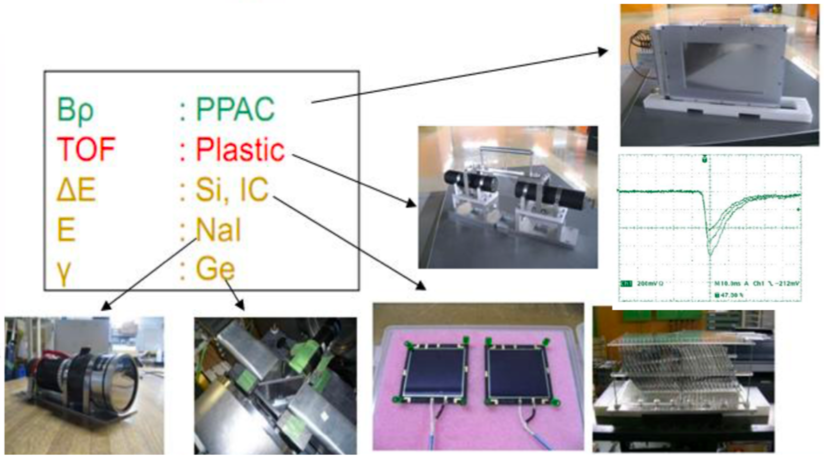


Beam line Electronics

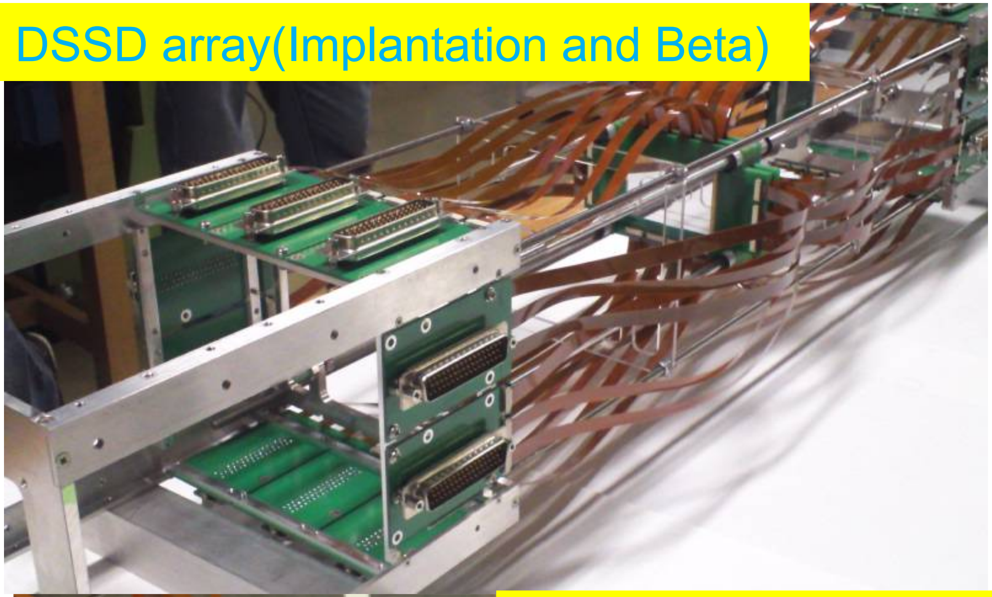
~200 channels

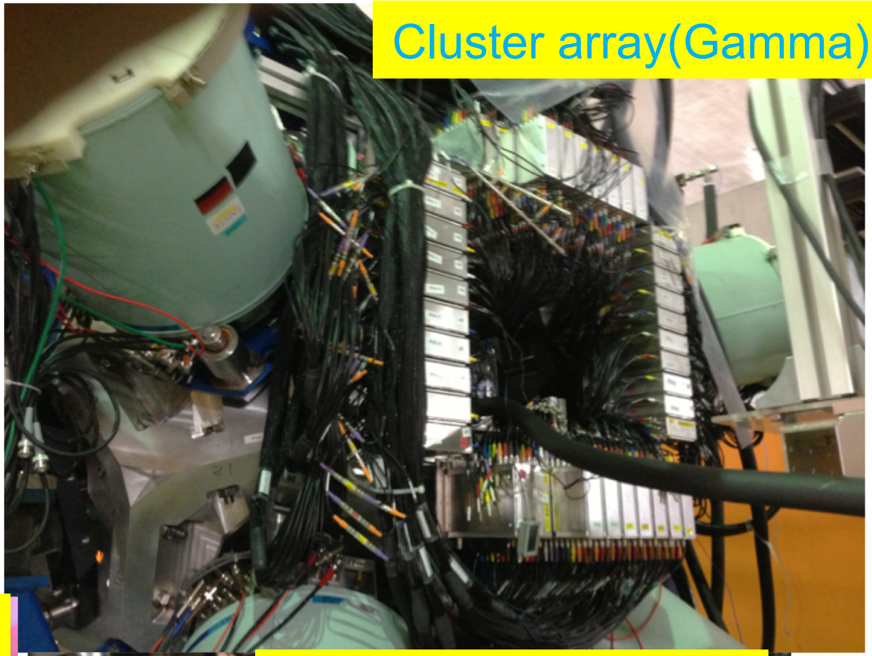






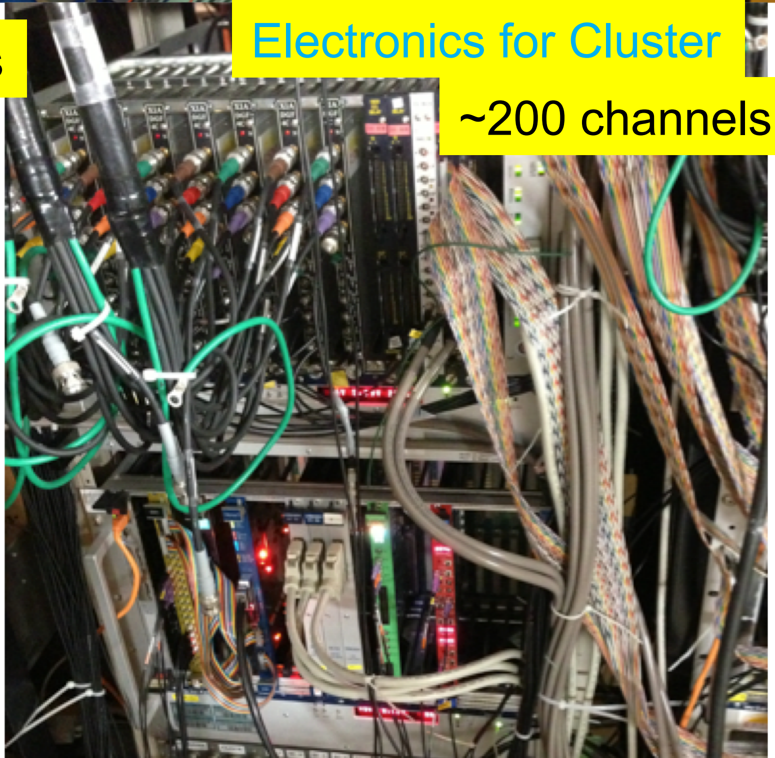
Bρ : PPAC
TOF : Plastic
ΔE : Si, IC
E : NaI
γ : Ge


DSSD array(Implantation and Beta)


Cluster array(Gamma)

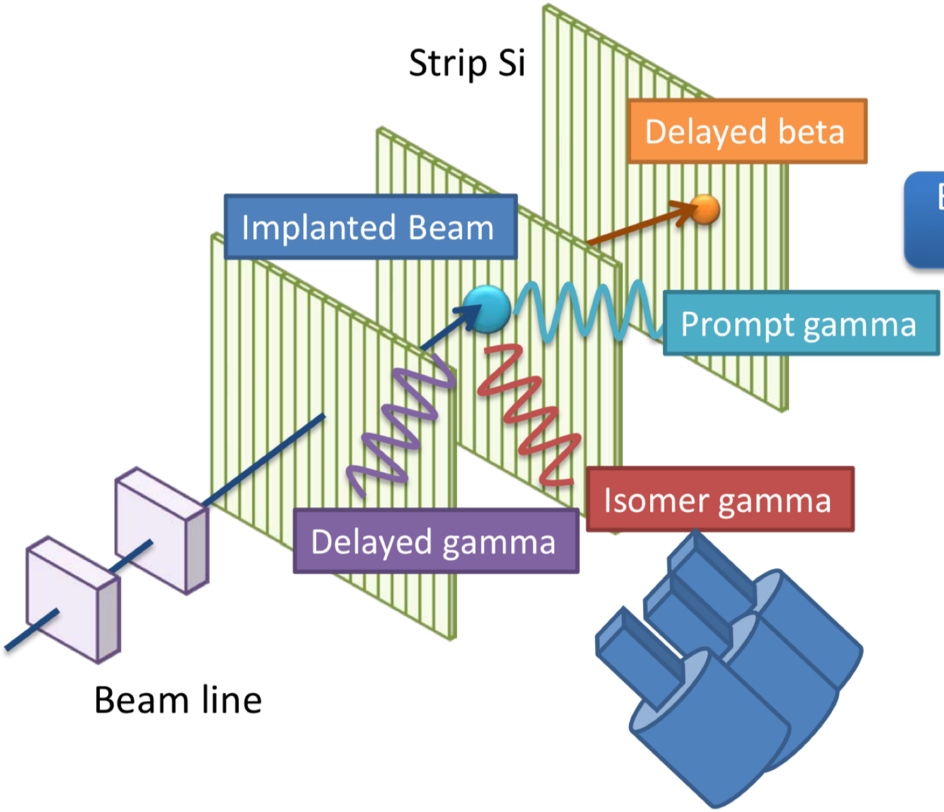

Electronics for DSSD

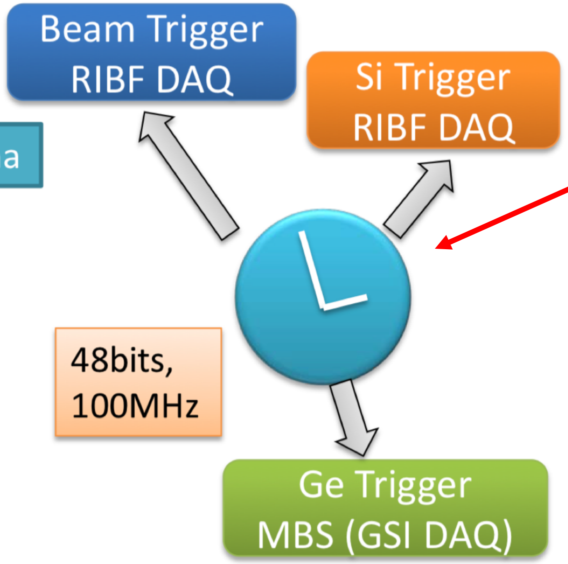
~2000 channels


Electronics for Cluster

~200 channels

Beta decay experiments with EURICA



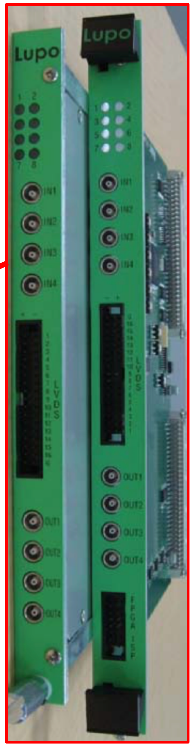

Beam Trigger
RIBF DAQ

Si Trigger
RIBF DAQ

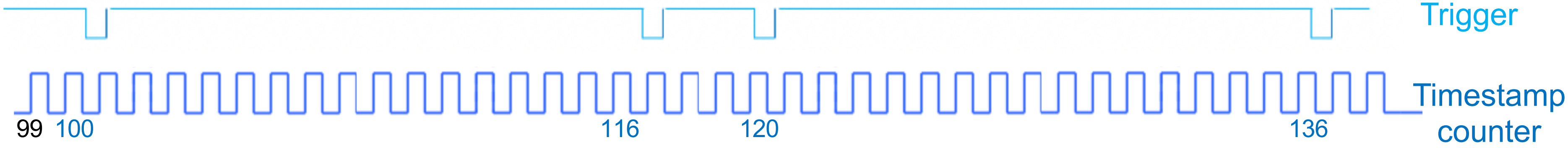
48bits,
100MHz

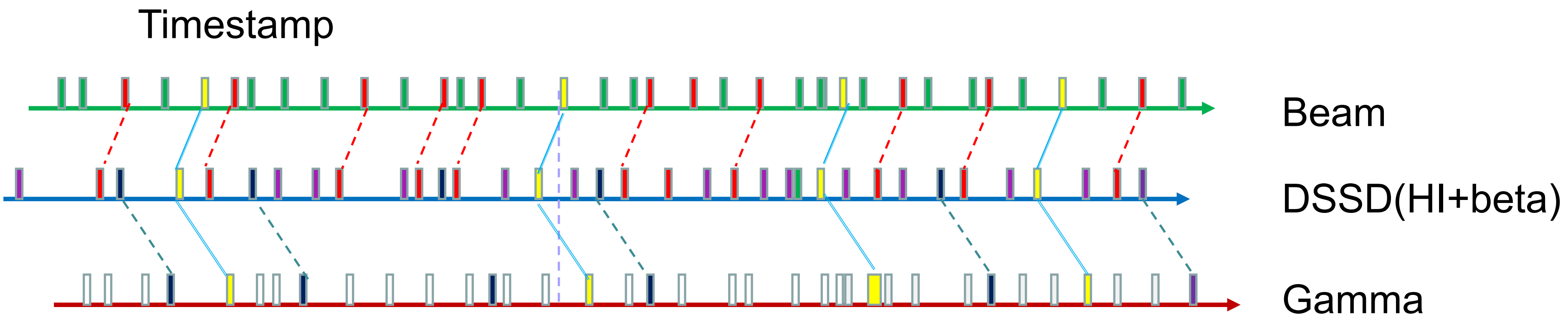
Ge Trigger
MBS (GSI DAQ)

Timestamp
module



100MHz,
48bit counter



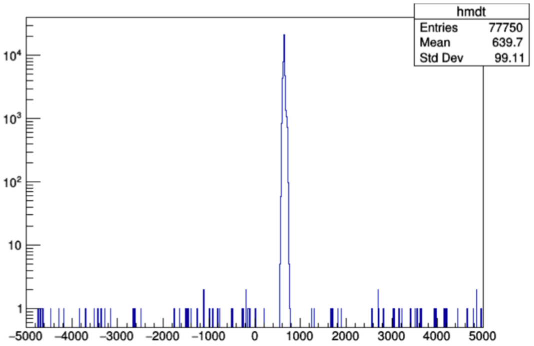


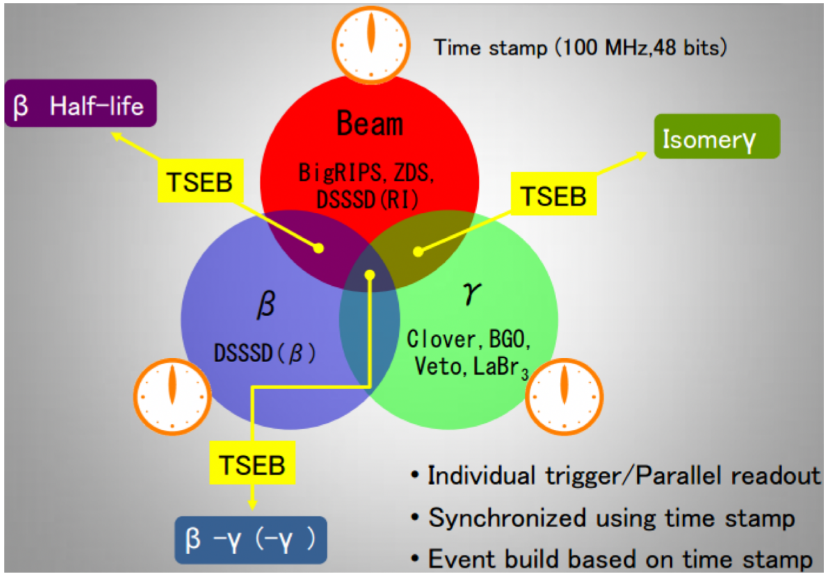
heavy ion : beam x DSSD(HI)

heavy ion-gamma : beam x DSSD(HI) x Gamma (isomer)

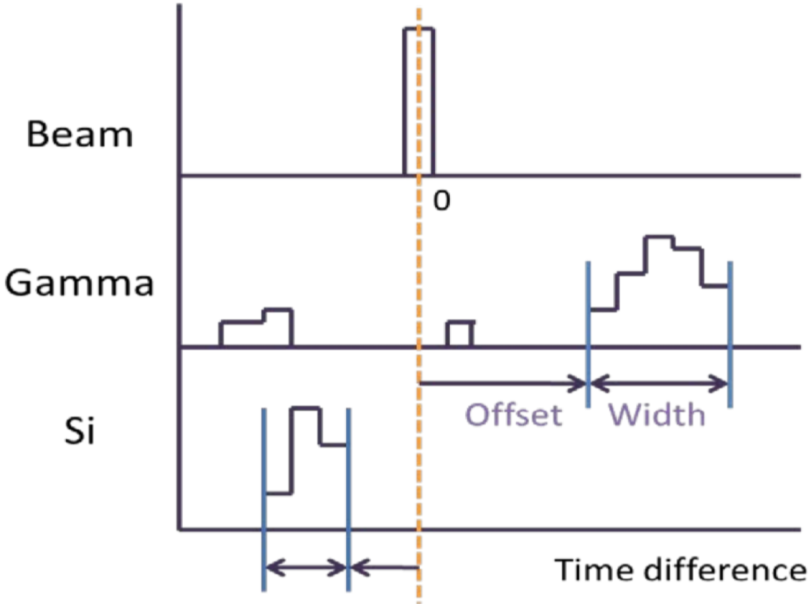
Beta : $\overline{\text{beam}}$ x DSSD(beta)

Beta-gamma : $\overline{\text{beam}}$ x DSSD(beta) x Gamma





- Individual trigger/Parallel readout
- Synchronized using time stamp
- Event build based on time stamp

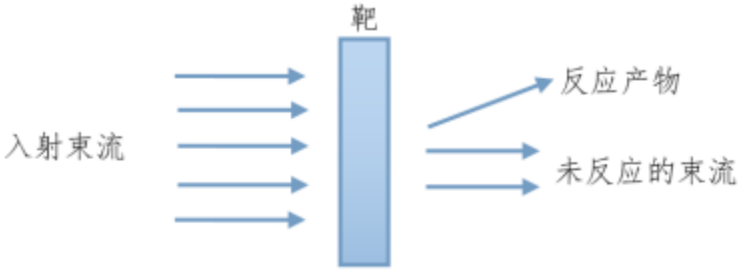


Application:

Study of Knockout Reaction Mechanism from ^{14}O at 60MeV/u

Phys. Rev. C 93, 044607 (2016)

Physics goal: the breakup reaction cross section of ^{14}O to ^{11}C



$$\sigma = \frac{N_{11C}}{N_{14O} N_s}$$

N_s为单位面积的靶原子数目

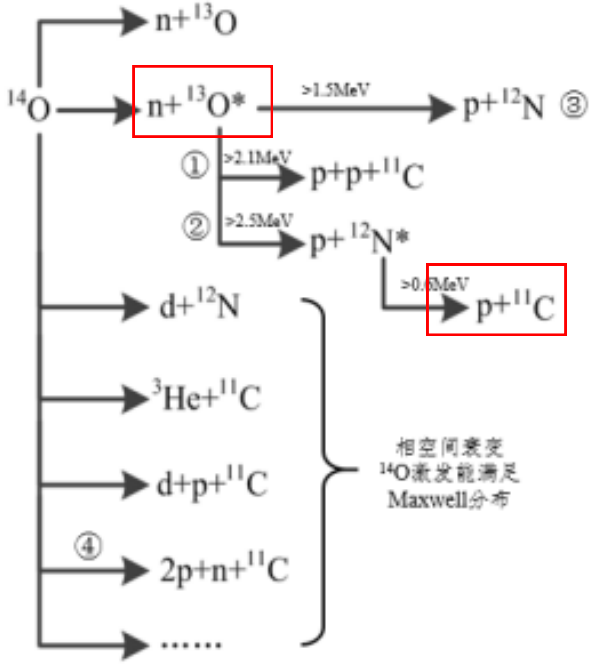
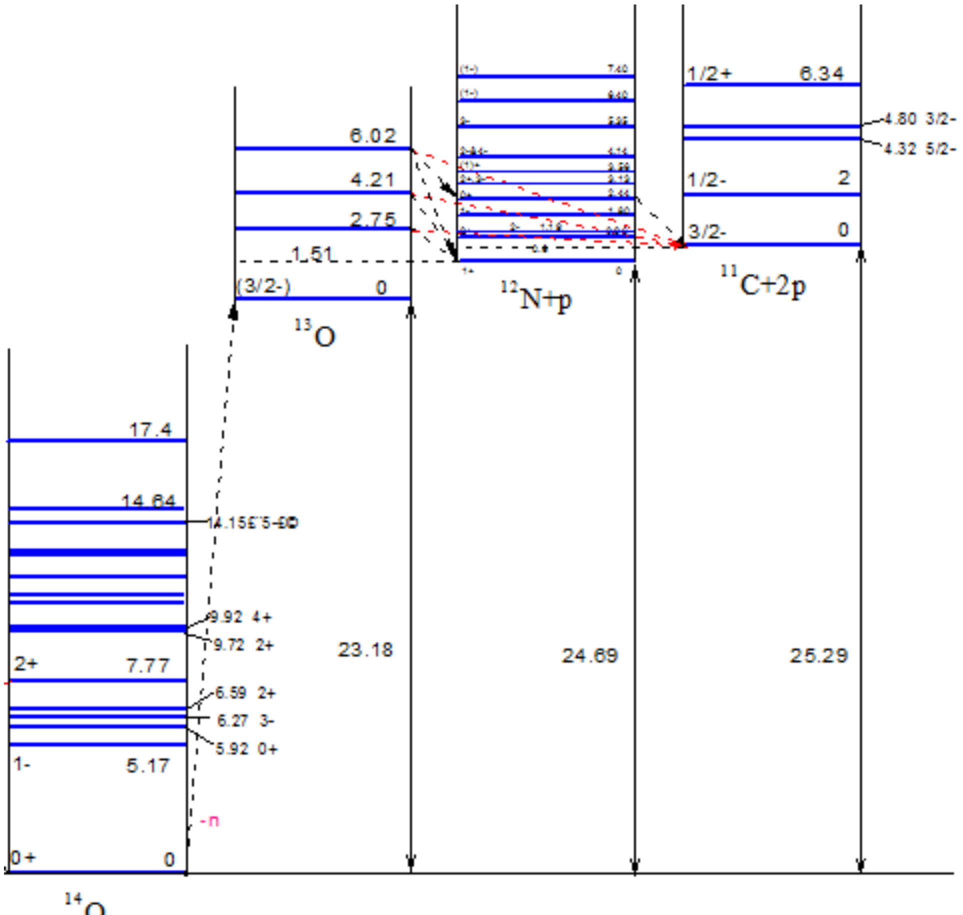
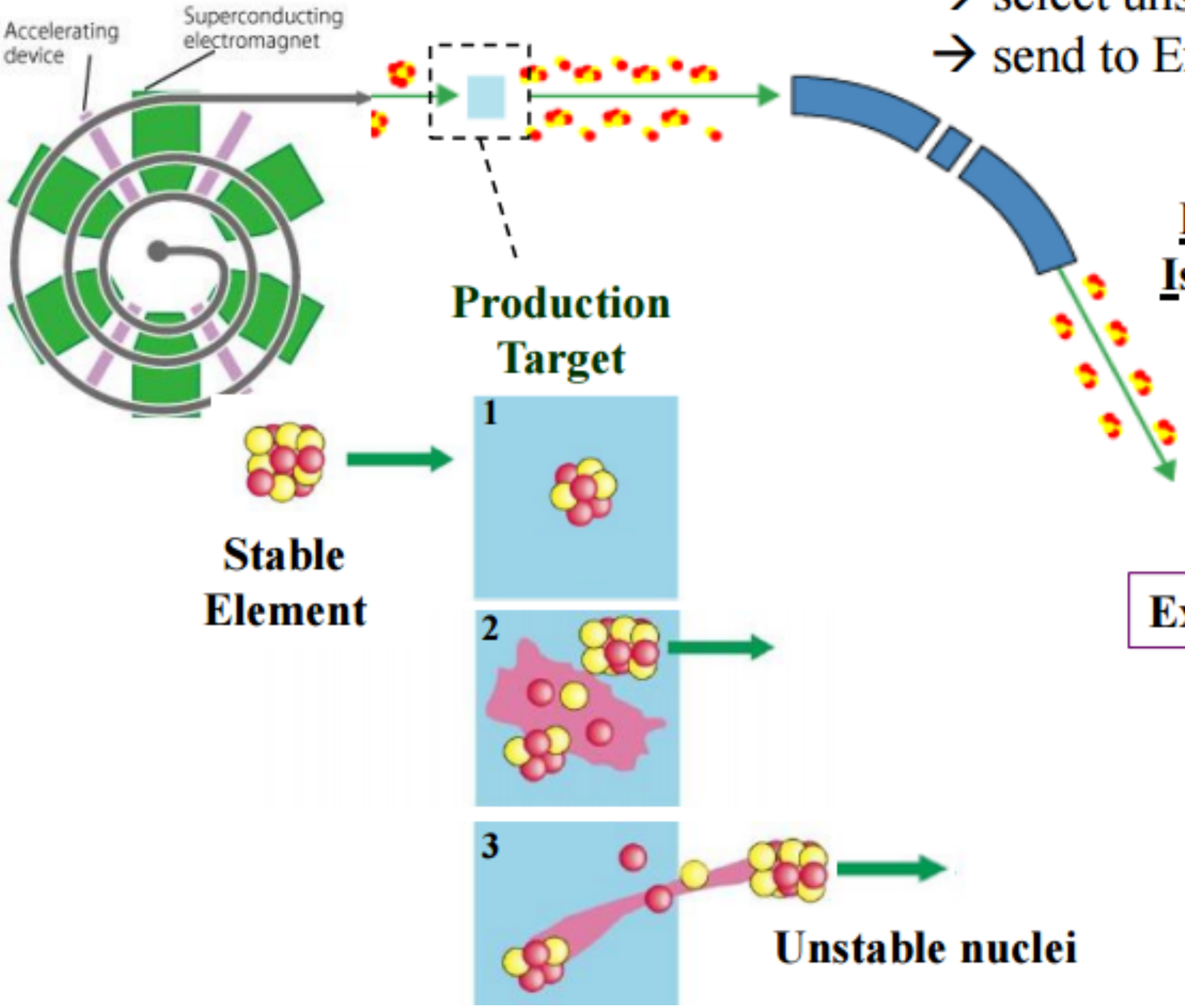


图 3.6-14 相关的反应道



Radioactive Isotope Beam Production



Cyclotron: Acceleration of Stable Elements

Fragment separator (Magnets)
→ select unstable nuclei of interest
→ send to Experiment Hall

Radioactive-Isotope Beams

Production Target

Stable Element

Experimental Area

Unstable nuclei

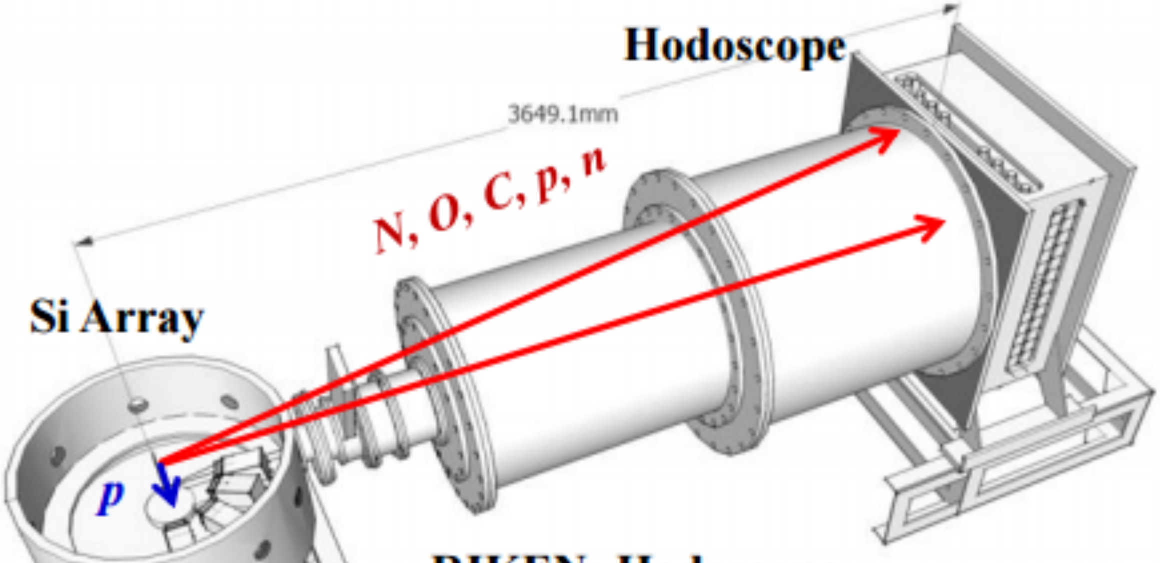
Study of Reaction Mechanism

Fully Exclusive Measurements of reaction products

大阪大学·核物理研究中心
Osaka University *Research Center for Nuclear Physics*

$$^{14}O + {}^{12}C \rightarrow {}^{13}N + p$$
$$\rightarrow {}^{12}N + p$$
$$\rightarrow {}^{11}C + 2p$$

EN-Course Beam line



RIKEN: Hodoscope

Peking University: Si Arrayc

Beam production

$$\sigma = \frac{N_{11C}}{\boxed{N_{14O}} N_s}$$

^{14}O 次级束流通过 78.2MeV/u 的 ^{16}O 在 2.1mm 的 ^{9}Be 靶上产生。

Secondary Beam line @RCNP

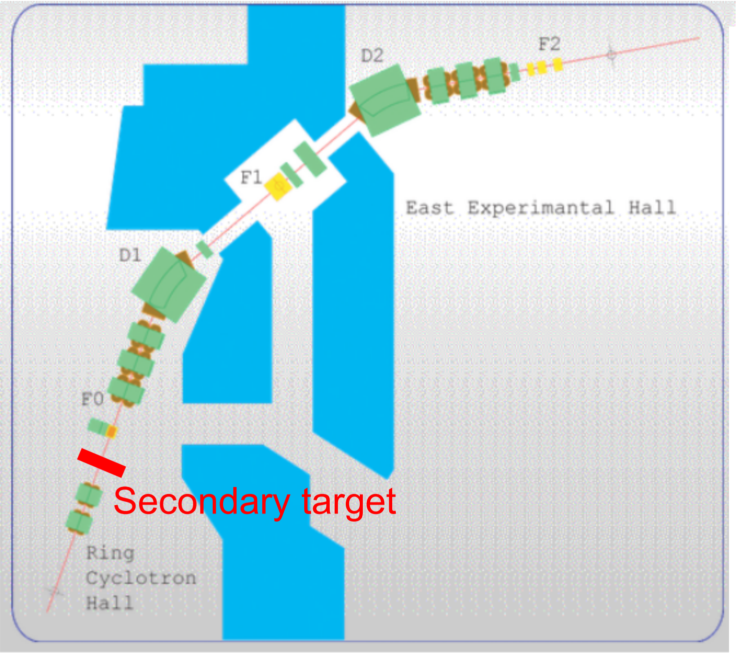


图 2.2-2 RCNP EN Course 束流线设置

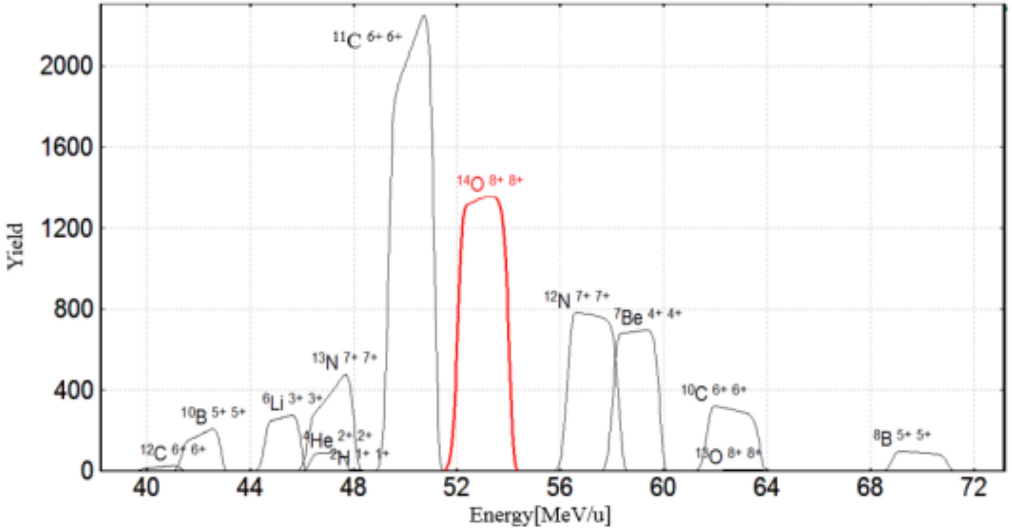


图 2.2-3 实验设置条件下 LISE++次级束计算结果

Particle identification

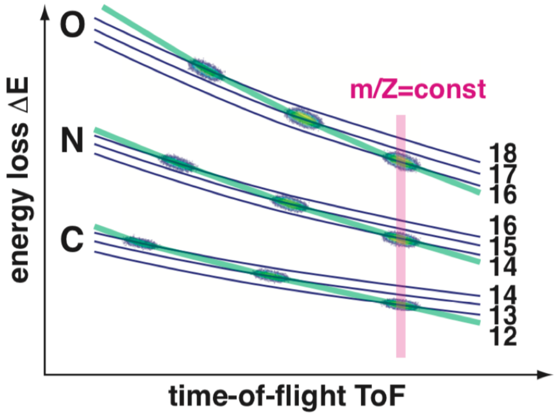
$$dE/dx \propto z^2/v^2 \quad (1)$$

$$TOF \propto 1/v \quad (2)$$

$$B\rho = mv/z = c \quad (3)$$

$$dE \propto z^2 TOF^2 \quad (1)-(2)$$

$$TOF \propto \frac{1}{c}\frac{m}{z} \quad (2)-(3)$$



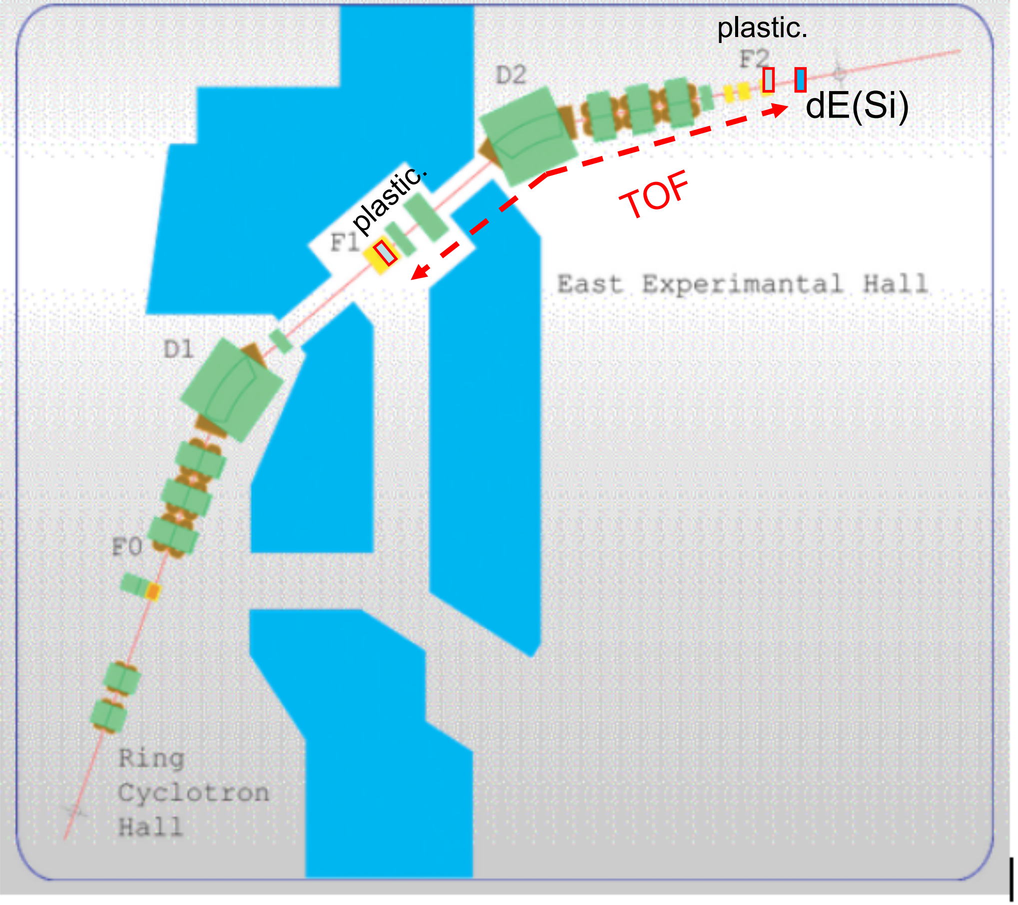
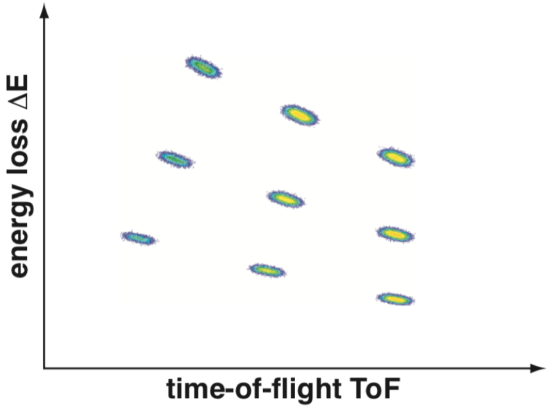
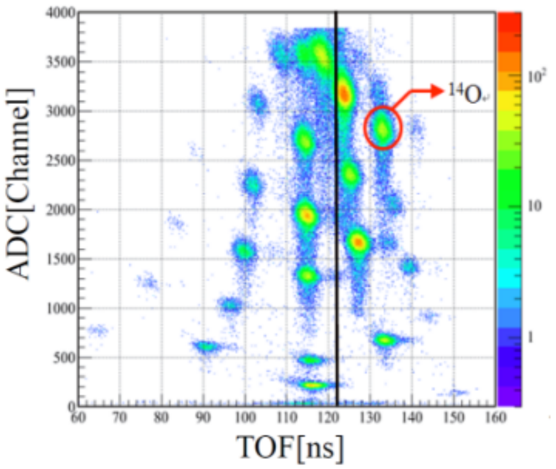


图 2.2-2 RCNP EN Course 束流线设置





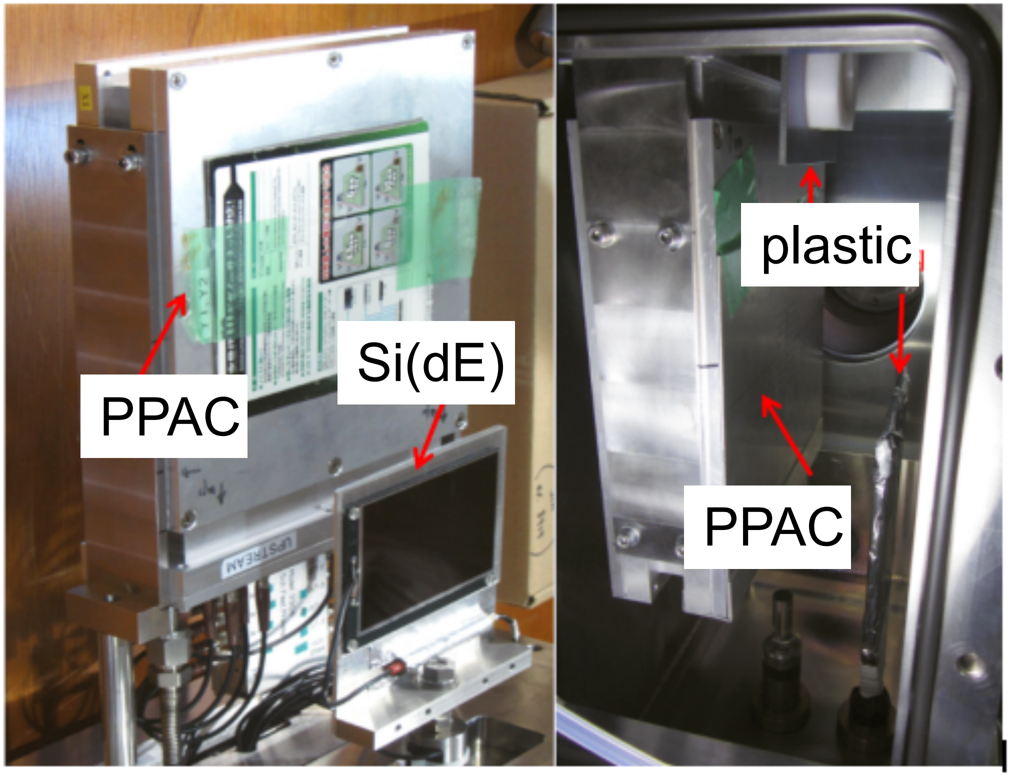


图 2.2-4 F2 PPAC 方硅和塑闪实物照片

PPAC - xy, tracking
Si- dE
RF- TOF start
plastic- TOF stop

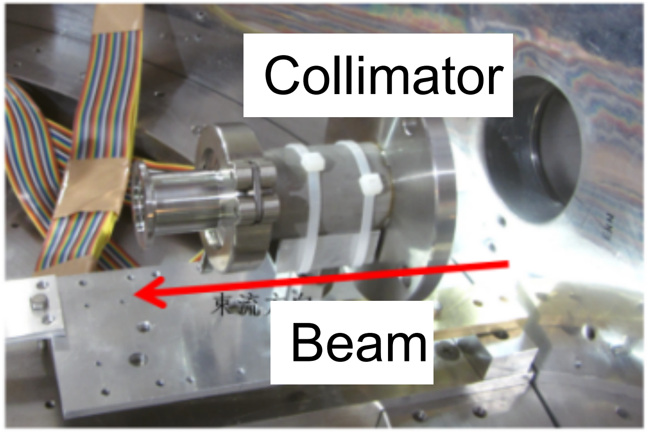
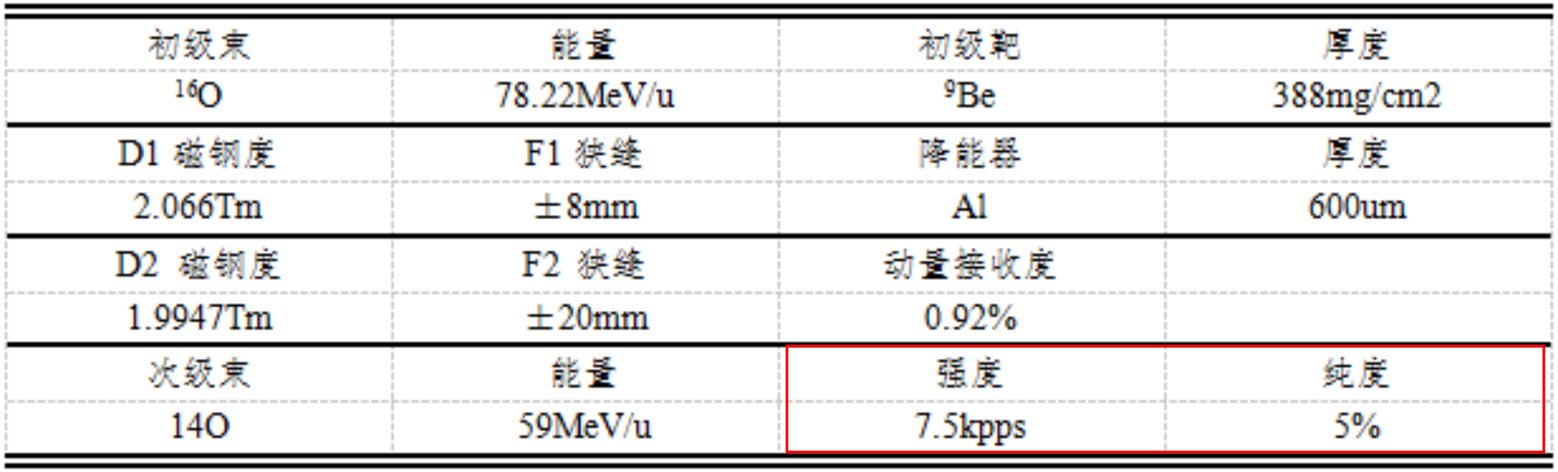


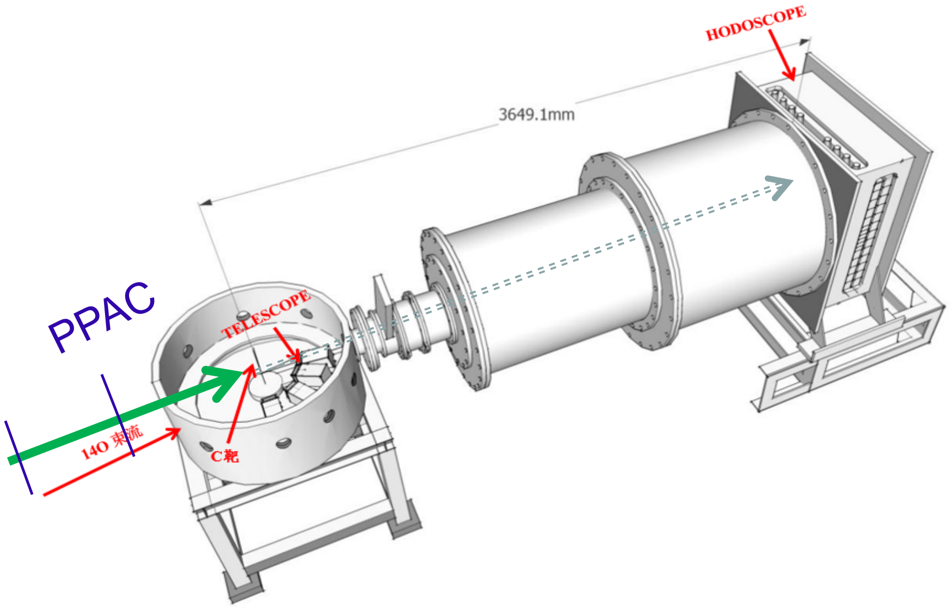
图 2.2-5 靶前准直器以及靶架

Target

表 2.2-1 EN-Course ^{14}O 次级束调束参数



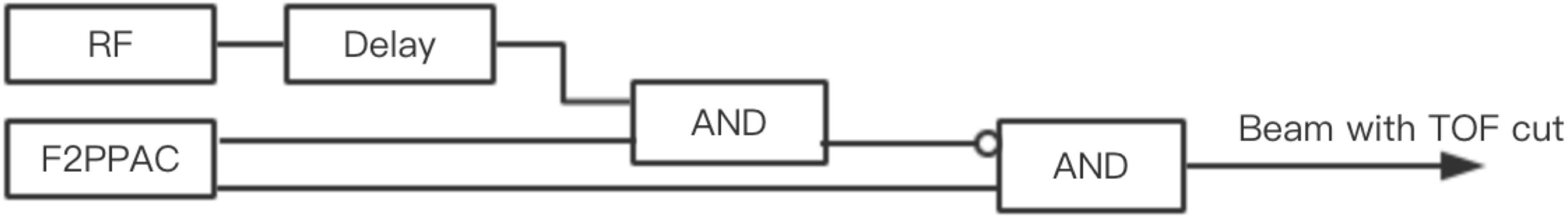
初级束	能量	初级靶	厚度
^{16}O	78.22MeV/u	^{9}Be	388mg/cm2
D1 磁钢度	F1 狭缝	降能器	厚度
2.066Tm	±8mm	Al	600um
D2 磁钢度	F2 狭缝	动量接收度	
1.9947Tm	±20mm	0.92%	
次级束	能量	强度	纯度
14O	59MeV/u	7.5kpps	5%



DAQ：~ 600 channels
dead time 20% @ 2kHz ！

trigger rate ~ beam rate 150kcps

need to suppress beam contaminants



RF

Delay

F2PPAC

AND

AND

Beam with TOF cut

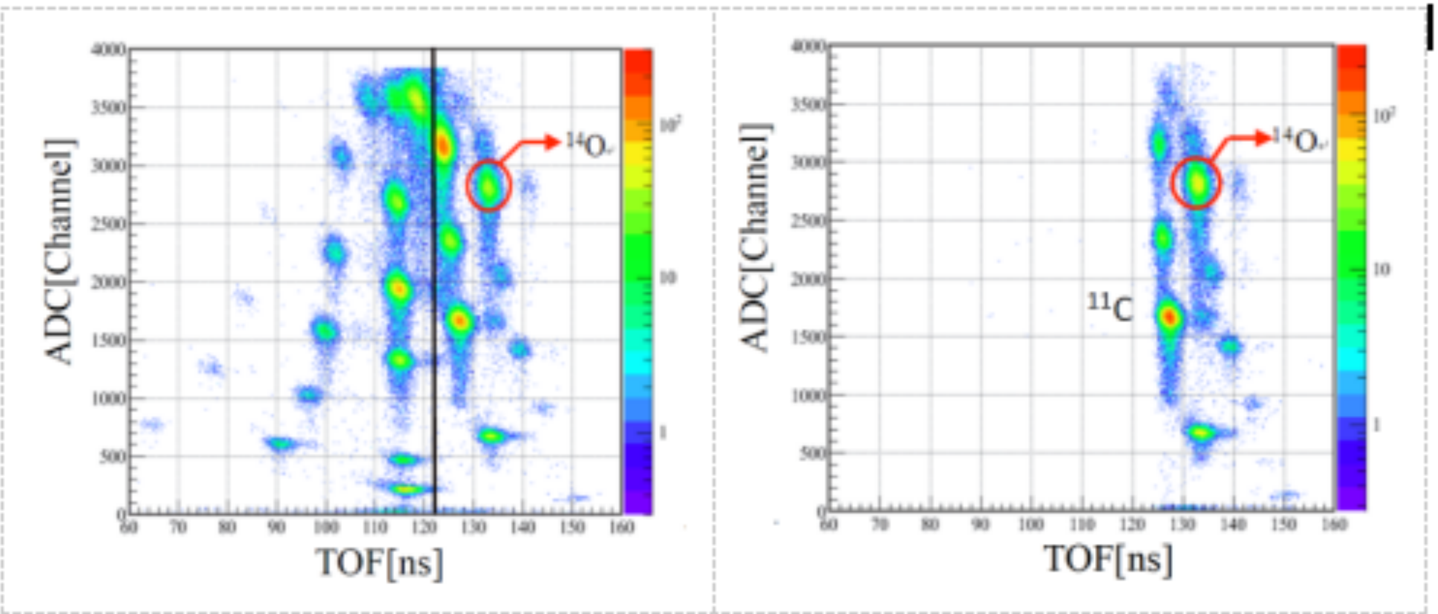


图 3.3-1　靶前 PID:ΔE-TOF，TOF 硬件选择之前(左)和之后(右)，左图黑线表示 TOF 选择的位置

Beam intensity: 150kcps ->30kcps

Need more strict trigger from downstream detectors(Physics)

Detector array

$$\sigma = \frac{\boxed{N_{11C}}}{N_{14O}N_s}$$

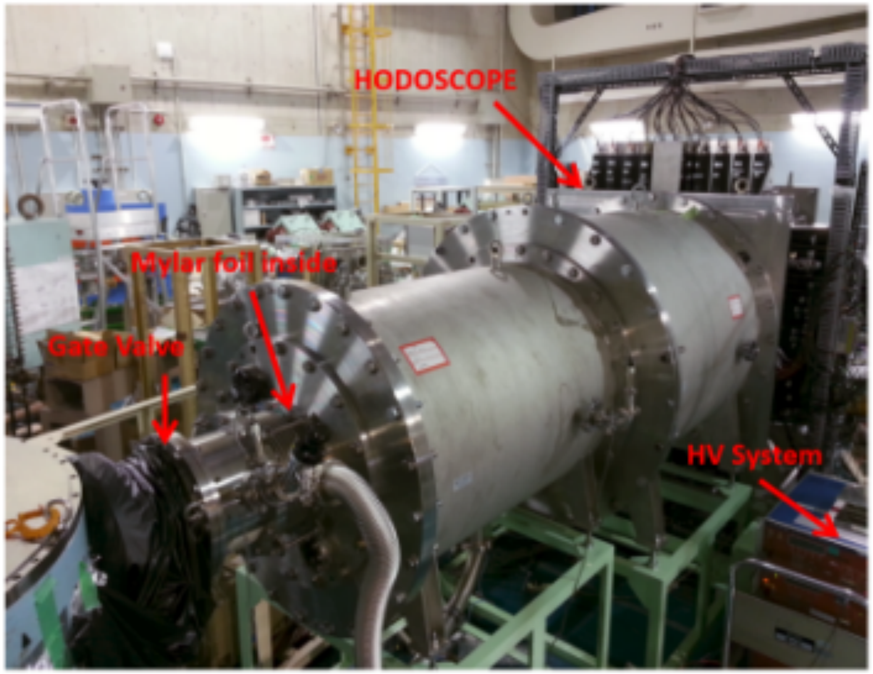


图 2.2-6 HODOSCOPE 的实验设置

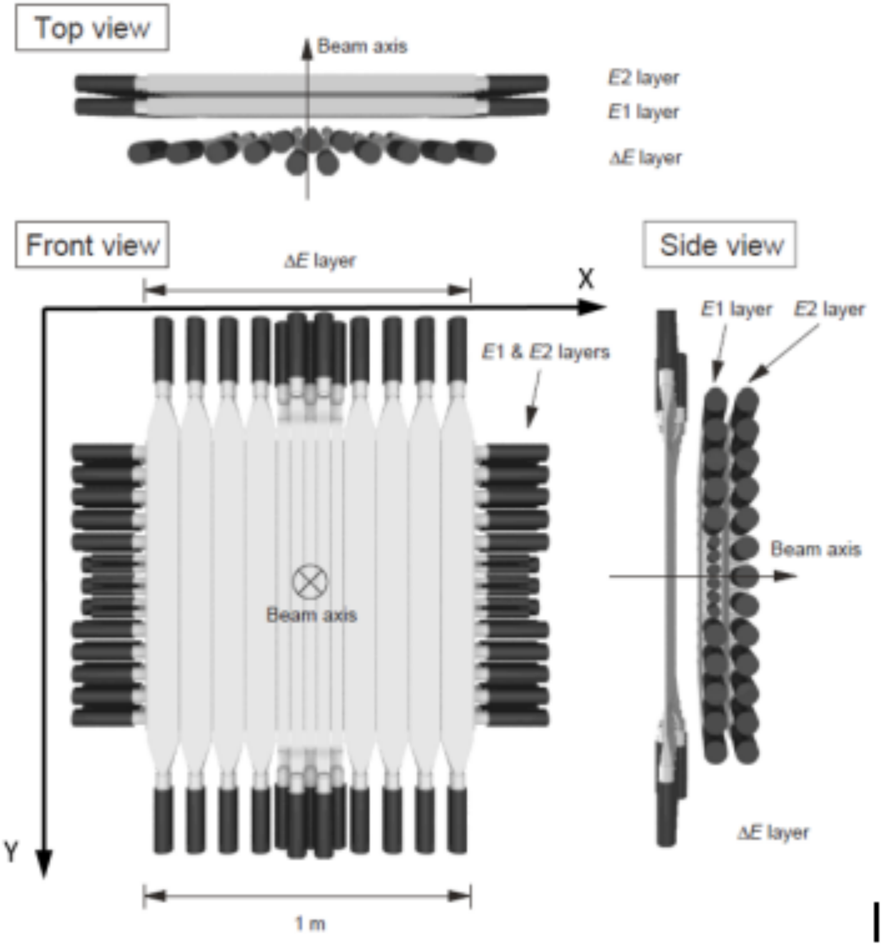


图 2.2-7 HODOSCOPE 塑料闪烁体阵列的组成[104]

如图所示，HODOSCOPE由42条BC408塑料闪烁体构成，每条闪烁体耦合光电倍增管(Photomultiplier，PMT)双端读出。整个阵列共三层，第一层(ΔE)厚度5mm，沿水平方向(X)分成13条；第二层(E1)厚度60mm，沿垂直方向(Y)分成16条；第三层(E2)厚度也是60mm，沿垂直方向分成13条。

particle identification using hodoscope

$$\sigma = \frac{\boxed{N_{11C}}}{N_{14O} N_s}$$

$$dE \propto z^2 / v^2$$

$$E \propto Av^2$$

$$TOF \propto 1 / v$$

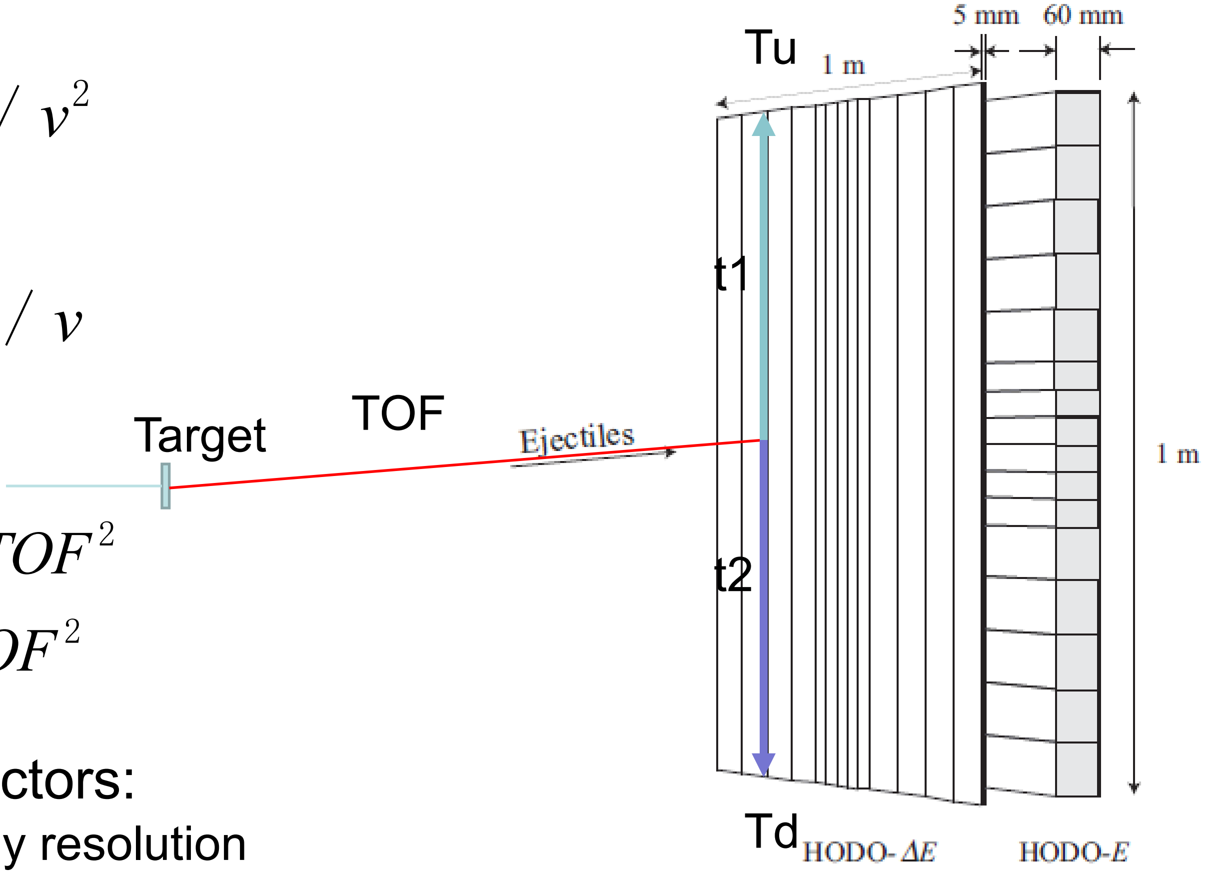


Figure 3.9: A schematic layout of the plastic scintillator hodoscope for detection of the ejectiles.

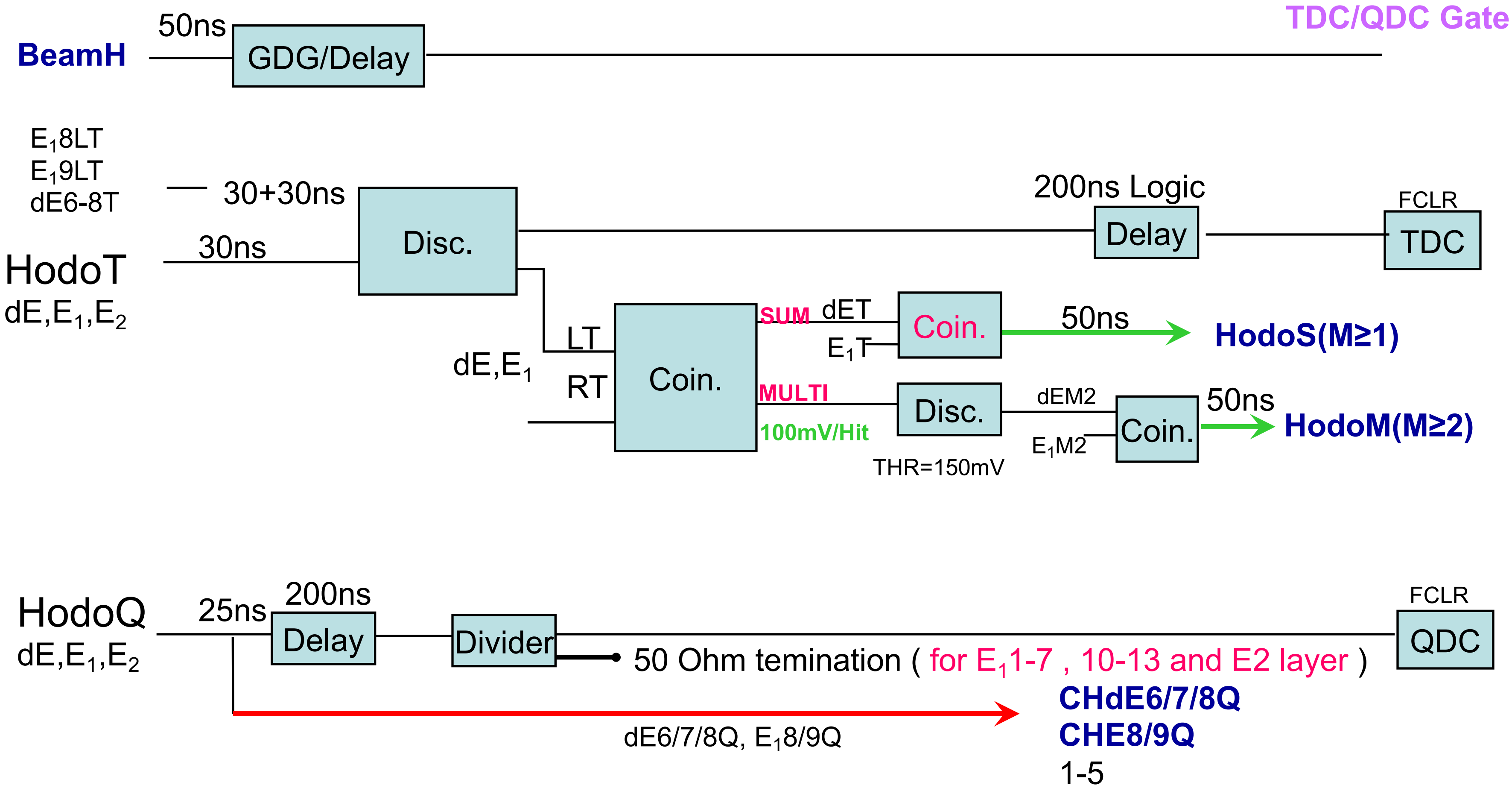
$$dE \propto z^2 \cdot TOF^2$$

$$E \propto A / TOF^2$$

Plastic detectors:

- ✓ Poor energy resolution
- ✓ Good timing
- ✓ Large acceptance

Hodoscope Area



TDC/QDC Gate

BeamH

50ns

GDG/Delay

E_18LT
E_19LT
dE6-8T

30+30ns

HodoT
dE,E_1,E_2

30ns

Disc.

200ns Logic

Delay

FCLR

TDC

SUM

dET

E_1T

Coin.

50ns

HodoS(M≥1)

LT

dE,E_1

RT

Coin.

MULTI

100mV/Hit

Disc.

THR=150mV

dEM2

E_1M2

Coin.

50ns

HodoM(M≥2)

HodoQ
dE,E_1,E_2

25ns

200ns

Delay

Divider

50 Ohm temination (for $E_1$1-7 , 10-13 and E2 layer)

FCLR

QDC

dE6/7/8Q, $E_1$8/9Q

CHdE6/7/8Q
CHE8/9Q
1-5

Trigger from Hodo Osilloscope:

HodoM: 11C+p : dE & E multiplicity ≥2

counting rate: 30kcps-> 1.5kcps

Main trigger: Beam x HodoM

Hodoscope Veto Trigger

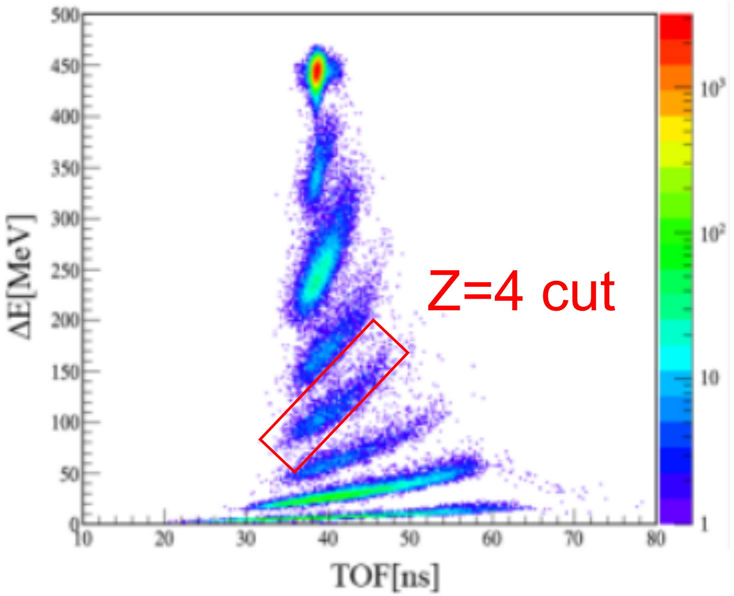
Condition: $\overline{(DE6 + DE7 + DE8) \text{ AND } (E1\text{-}8 + E1\text{-}9)}$

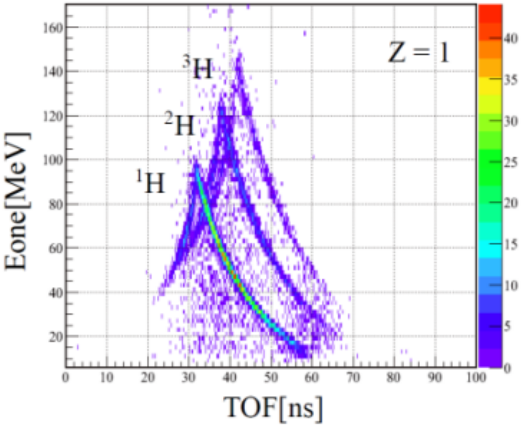
Beam with intensity > 10^4 → Huge Dead Time !
→ Exclude central area in data-taking

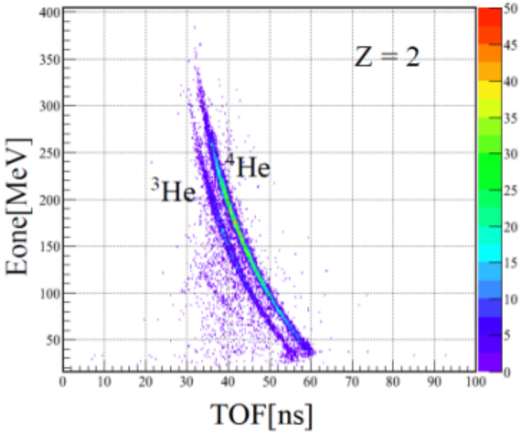
Rate Meter

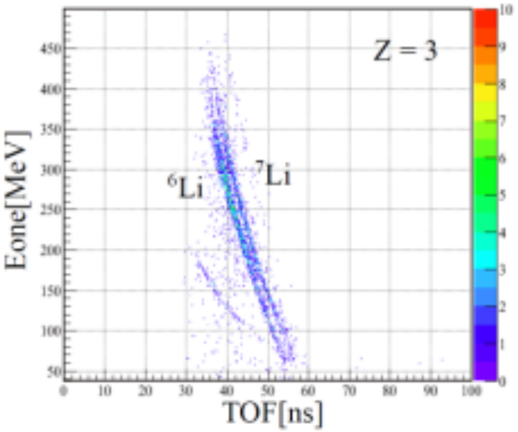
$$dE \propto z^2 \cdot TOF^2$$

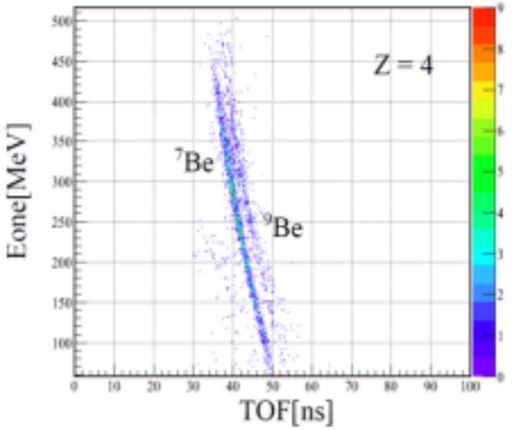
$$E \propto A / TOF^2$$

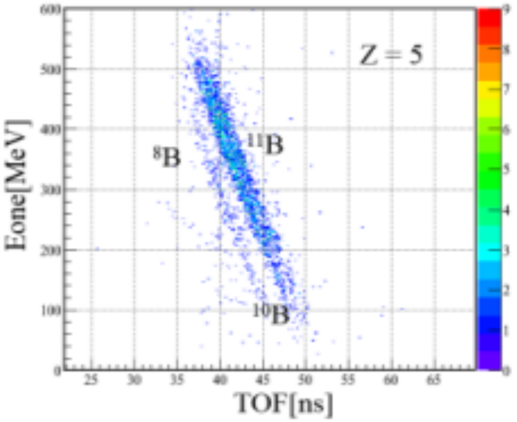


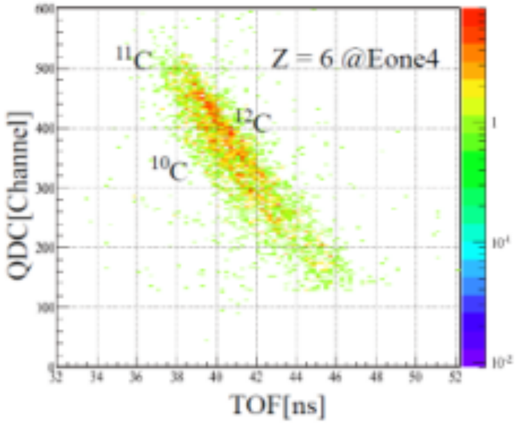


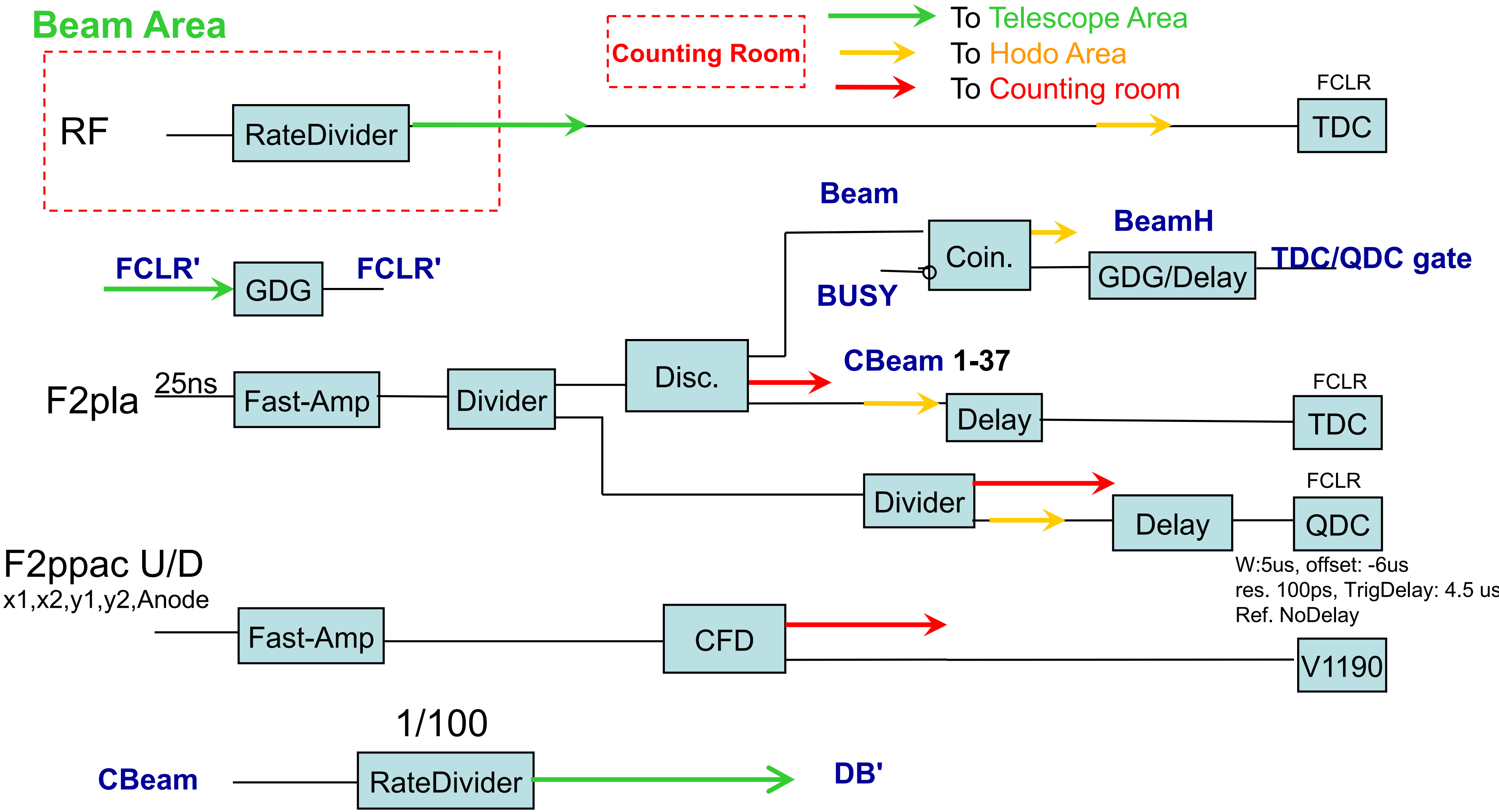












Trigger from Beam line detector:

DB: Beam/100~ 300cps - sampling

Monitor beam condition during beam time.

Telescope array at upstream(back angle)

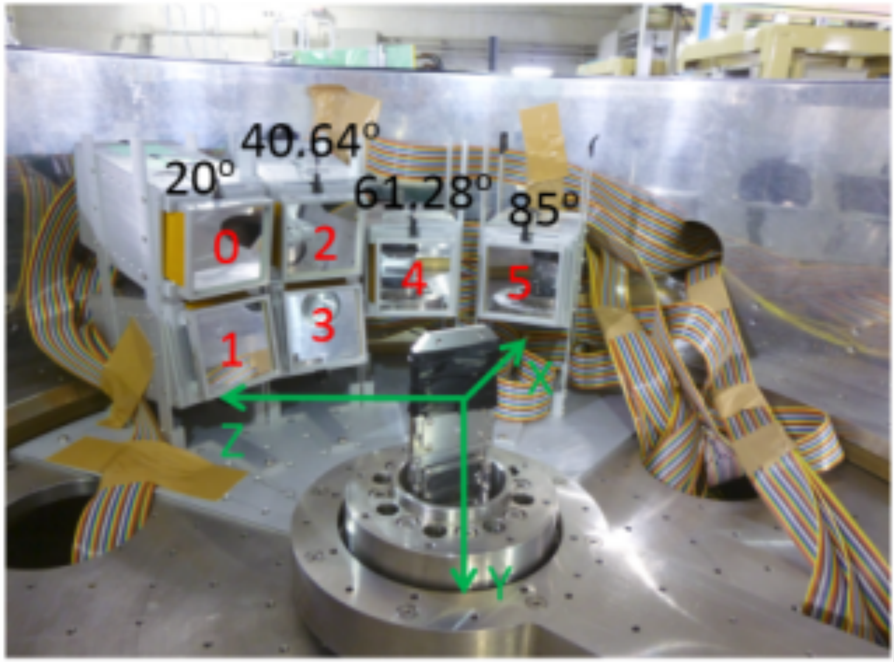
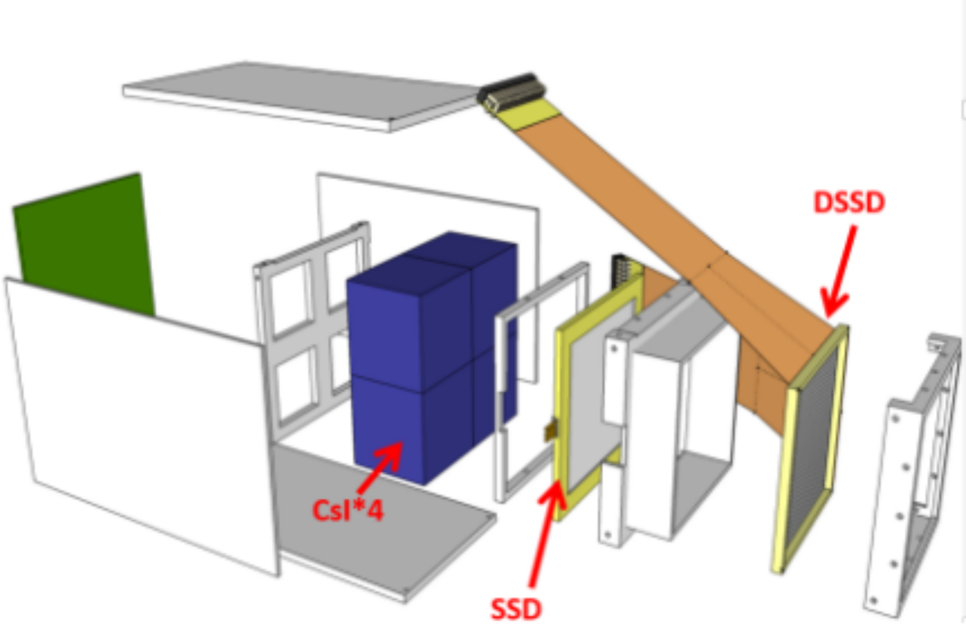
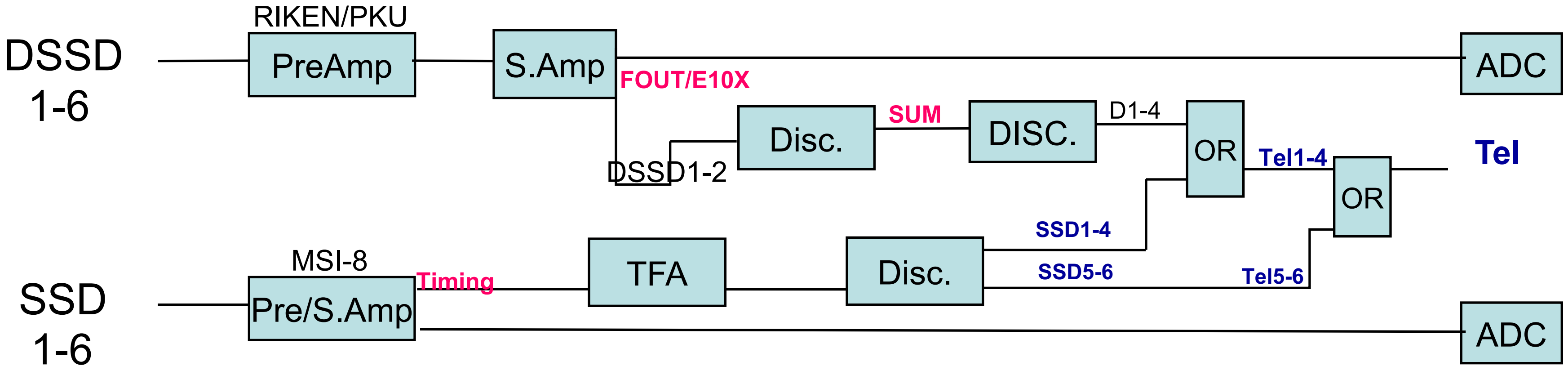


图 2.2-9　靶室内望远镜阵列设置

图中数字为望远镜编号(红色)以及中心和 Z 束流线的夹角(黑色)

图中的绿线标示了坐标系的定义




DSSD 1-6
RIKEN/PKU
PreAmp
S.Amp
FOUT/E10X
ADC
Disc.
SUM
DISC.
D1-4
OR
Tel1-4
OR
Tel
DSSD1-2
SSD1-4
SSD 1-6
MSI-8
Pre/S.Amp
Timing
TFA
Disc.
SSD5-6
Tel5-6
ADC

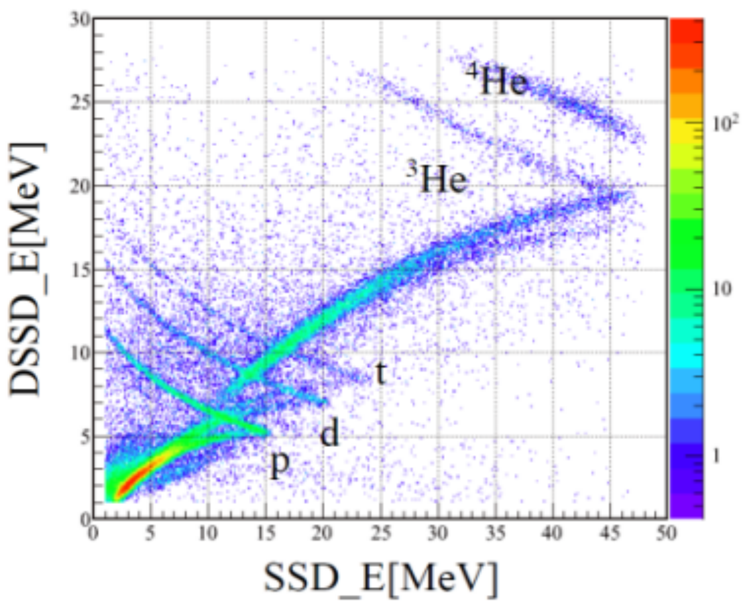


图 3.5-3 TELESCOPE 的粒子鉴别，DSSD_E vs SSD_E

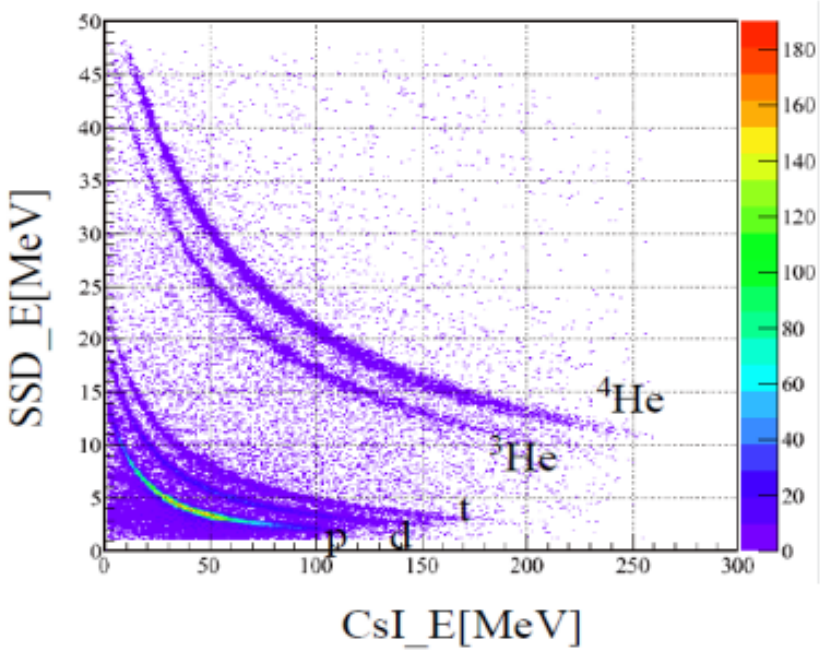
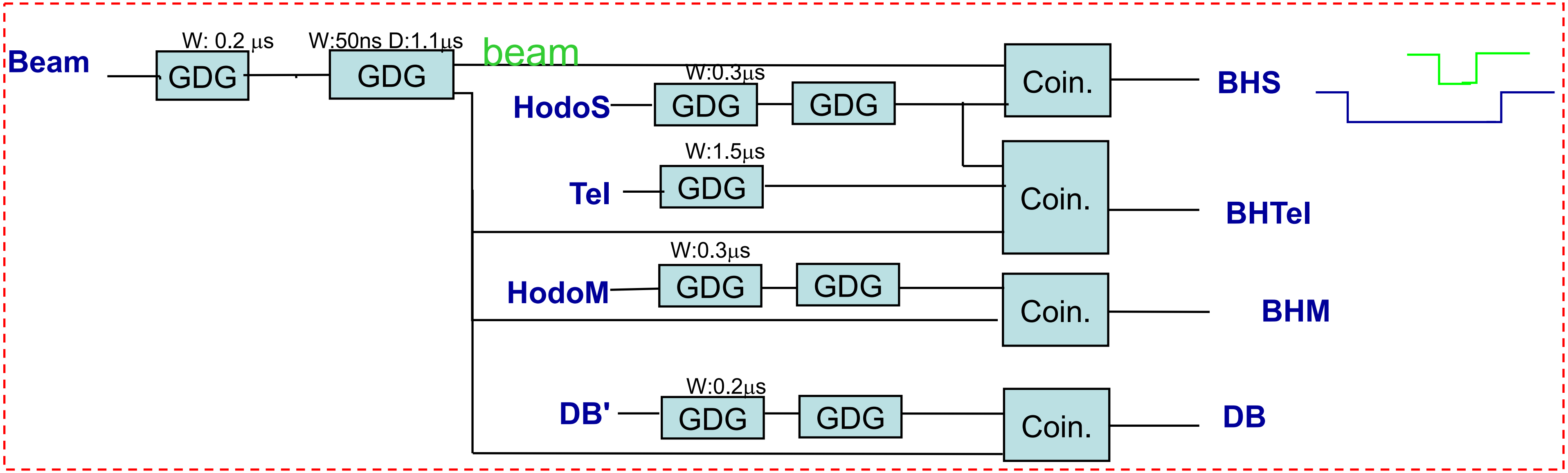


图 3.5-4 TELESCOPE 的粒子鉴别，SSD_E vs CsI_E

Trigger from telescope:
HodoS x Tele



Beam

W: 0.2 μs

GDG

W:50ns D:1.1μs

GDG

beam

HodoS

W:0.3μs

GDG

GDG

Coin.

BHS

Tel

W:1.5μs

GDG

Coin.

BHTel

HodoM

W:0.3μs

GDG

GDG

Coin.

BHM

DB'

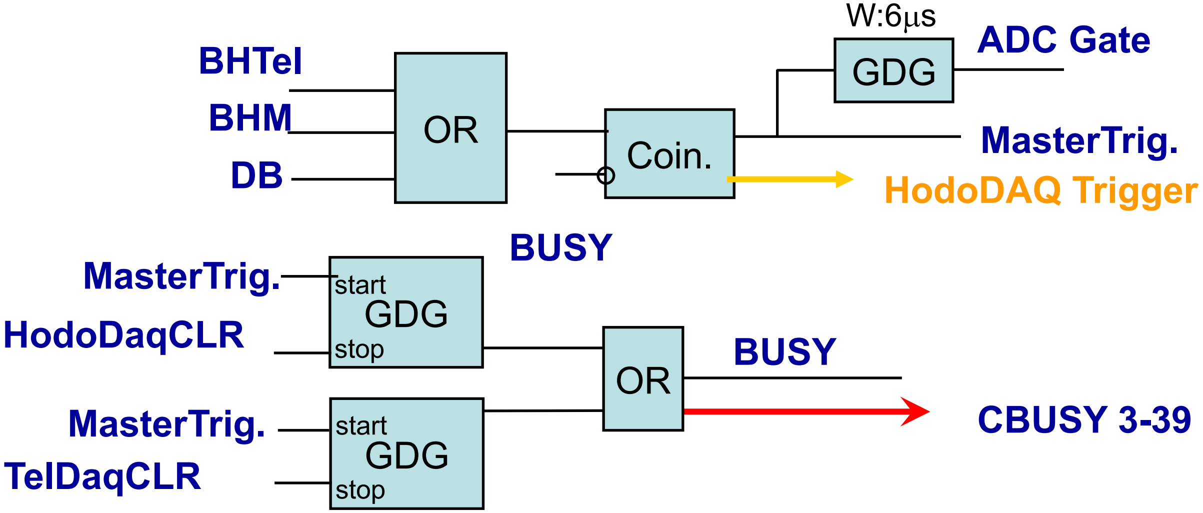
W:0.2μs

GDG

GDG

Coin.

DB



BHTel

BHM

DB

OR

Coin.

W:6μs

GDG

ADC Gate

MasterTrig.

HodoDAQ Trigger

BUSY

MasterTrig.

HodoDaqCLR

start

GDG

stop

MasterTrig.

TelDaqCLR

start

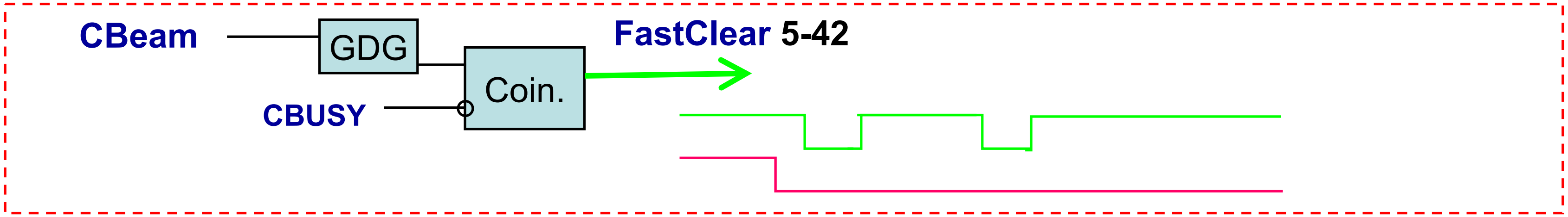
GDG

stop

OR

BUSY

CBUSY 3-39



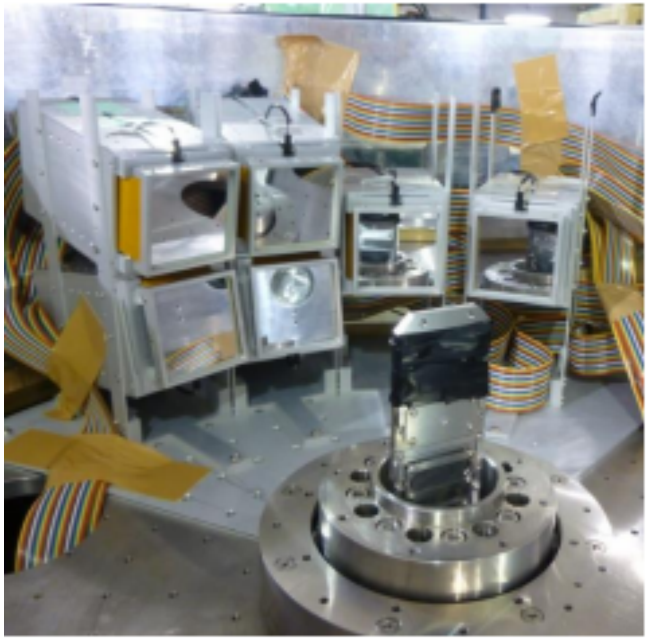
CBeam

GDG

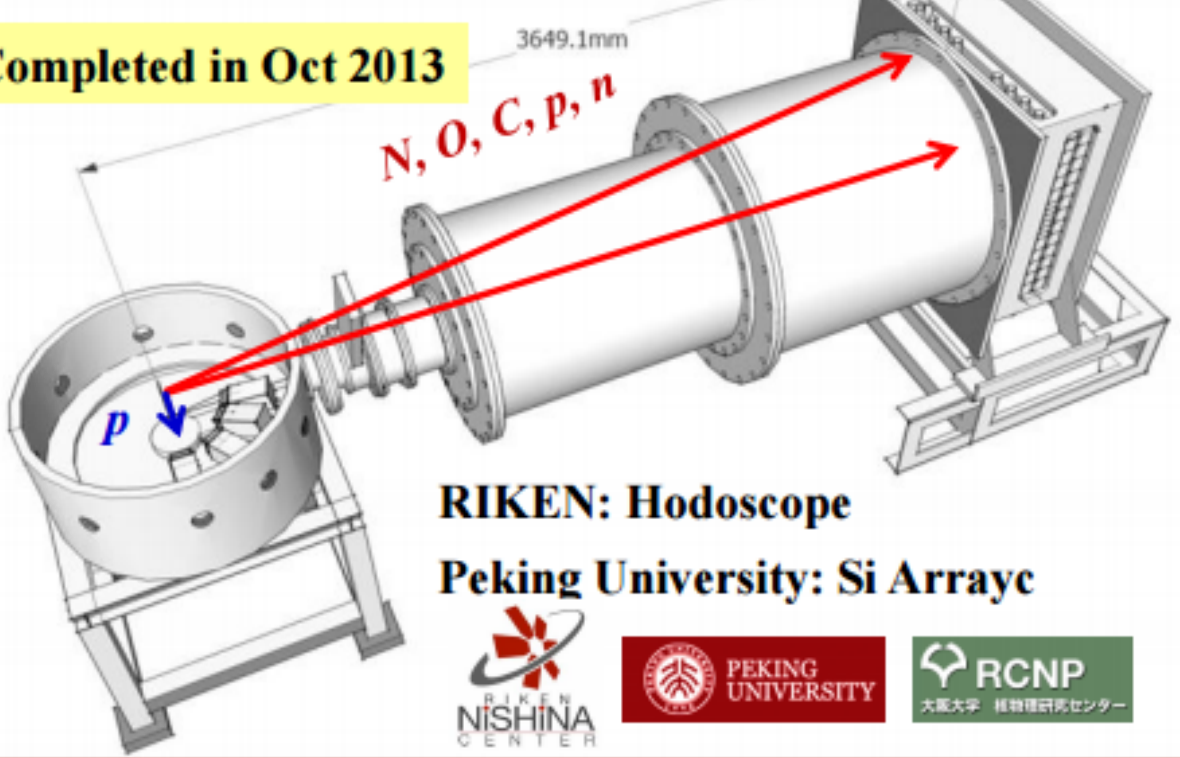
CBUSY

Coin.

FastClear 5-42

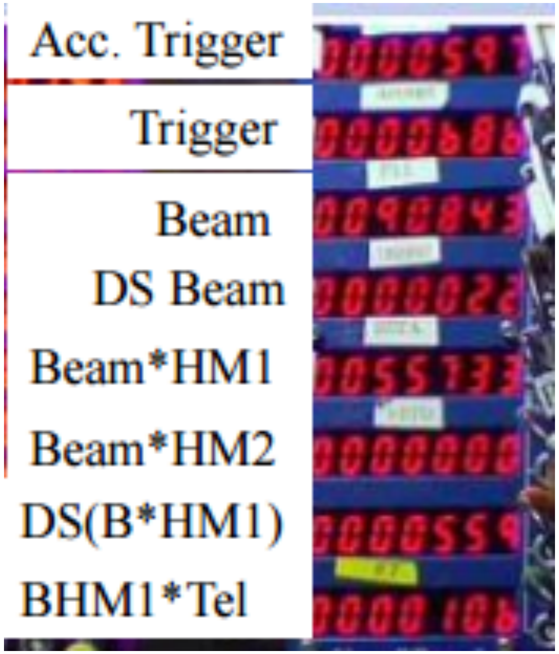


Completed in Oct 2013



RIKEN: Hodoscope

Peking University: Si Arrayc



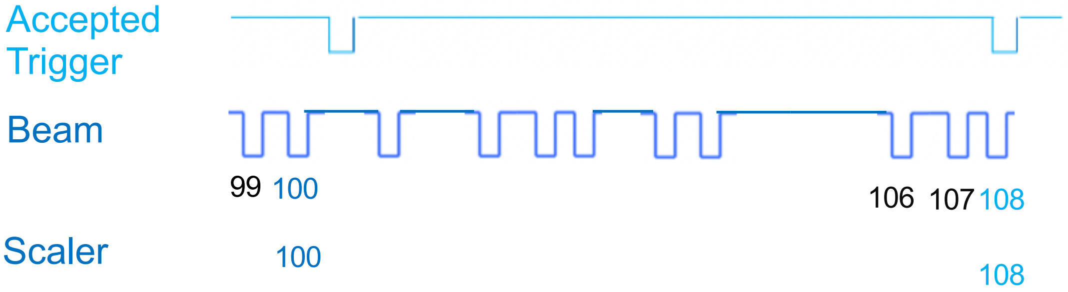
Visual Scaler-1

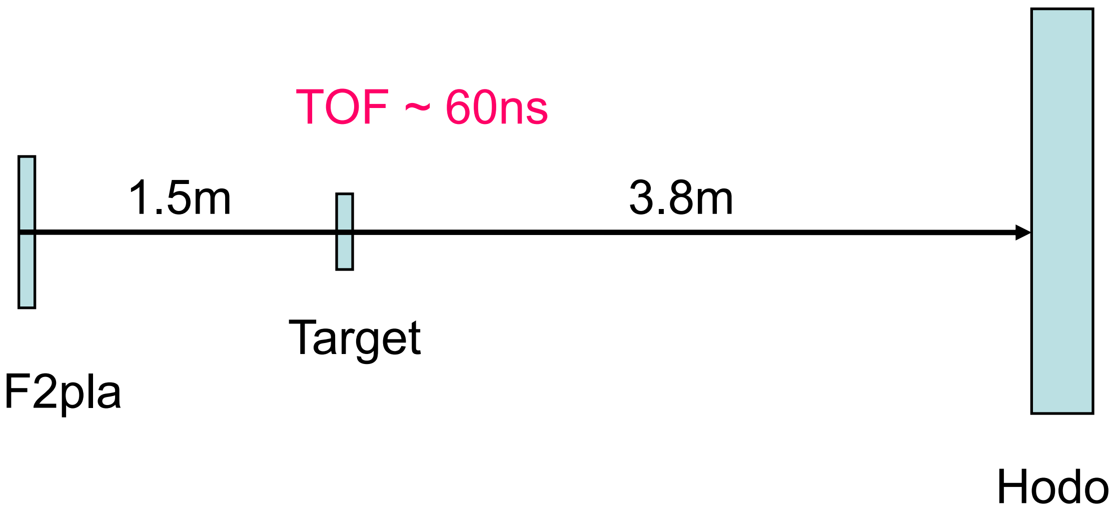
1. Trigger
2. Accepted Trigger
3. Beam
4. DB
5. B x HSingle
6. B x HMulti
7. 14O
8. B x Hodo x Tel

V1190(TDC)

33. Beam
34. DB
35. B x HSingle
36. B x HMulti
37. B x Tel
38. Beam x !Busy
    for deadtime
    of FCLR
64. Reference

To label trigger pattern





TOF ~ 60ns

1.5m

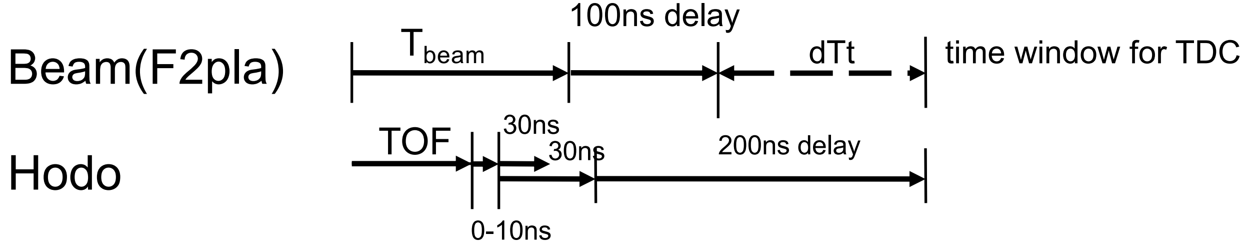
3.8m

Target

F2pla

Hodo

T_{Beam} =30ns(cable)+30ns(FastAmp+Disc.)
+50ns(cable)+20ns(Fan-I/O)
=130ns



Beam(F2pla)

T_{beam}

100ns delay

dTt

time window for TDC

Hodo

TOF

30ns

30ns

200ns delay

0-10ns

T_{HodoT}: 60+(0-10)+30+200+(30)=300-340ns

T_{HodoE}: 60+(0-10)+30+200=300-310ns

$dTt=T_{HodoT}-(T_{Beam}+100ns)$=70-110 ns
$dTe=T_{Hodoe}-(T_{Beam}+100ns)$=70-80 ns, Width: 230ns

Data Analysis - calibration

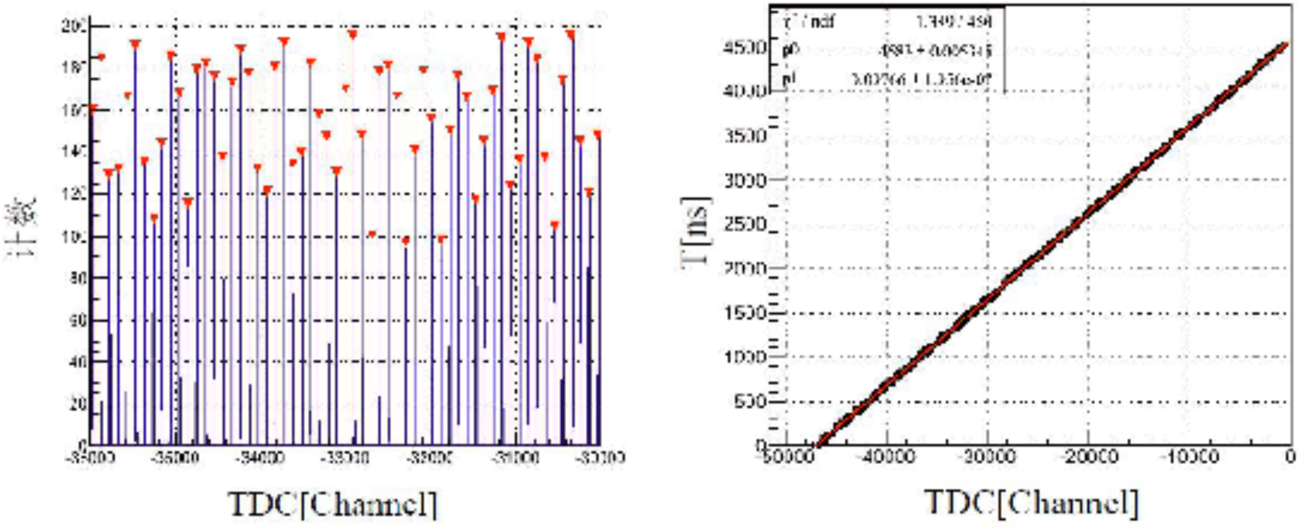


图 3.1-2　V1190 时间刻度

TDC:

0.9766 ns/ch

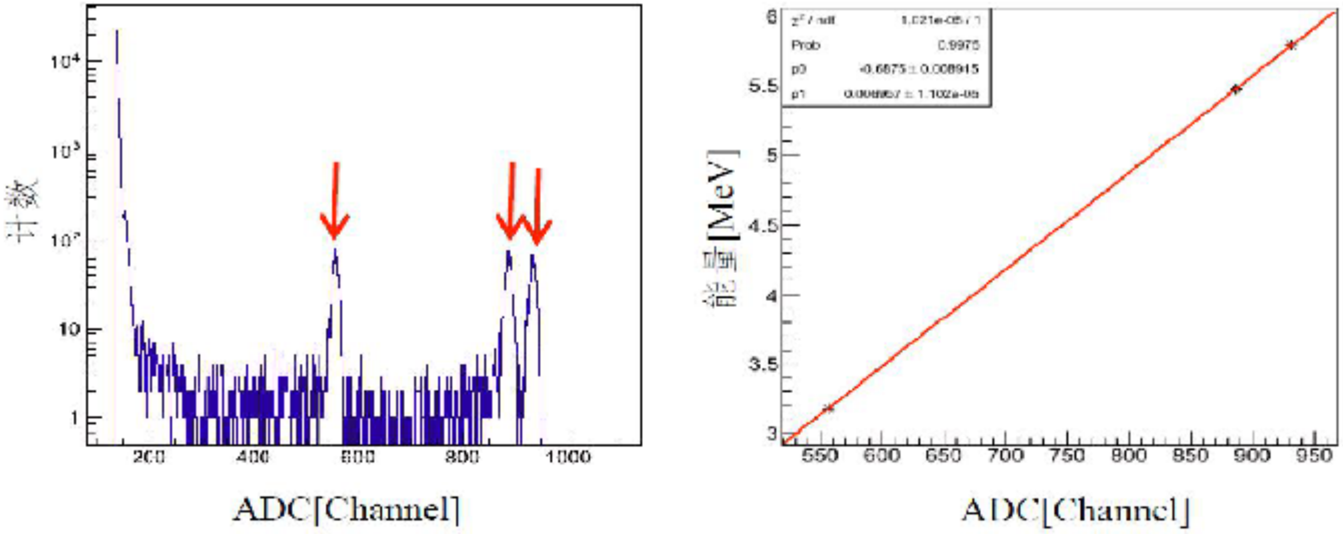


图 3.2-1　DSSD 能量刻度

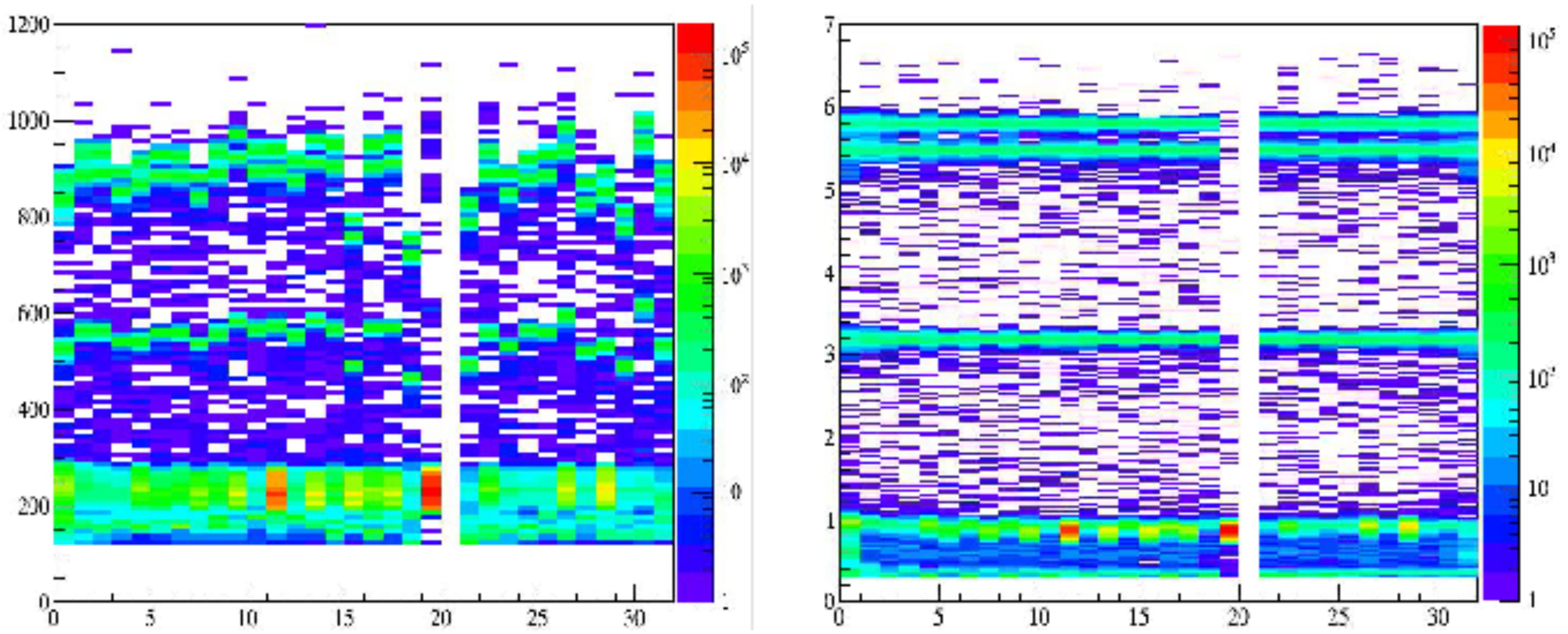
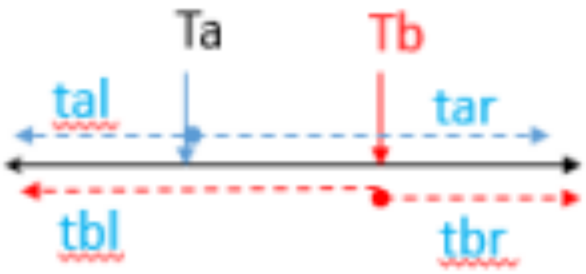


图 3.2-2　DSSD 能量刻度前后，左图：道值对硅条编号；右图：能量对硅条编号

PPAC beam x,y

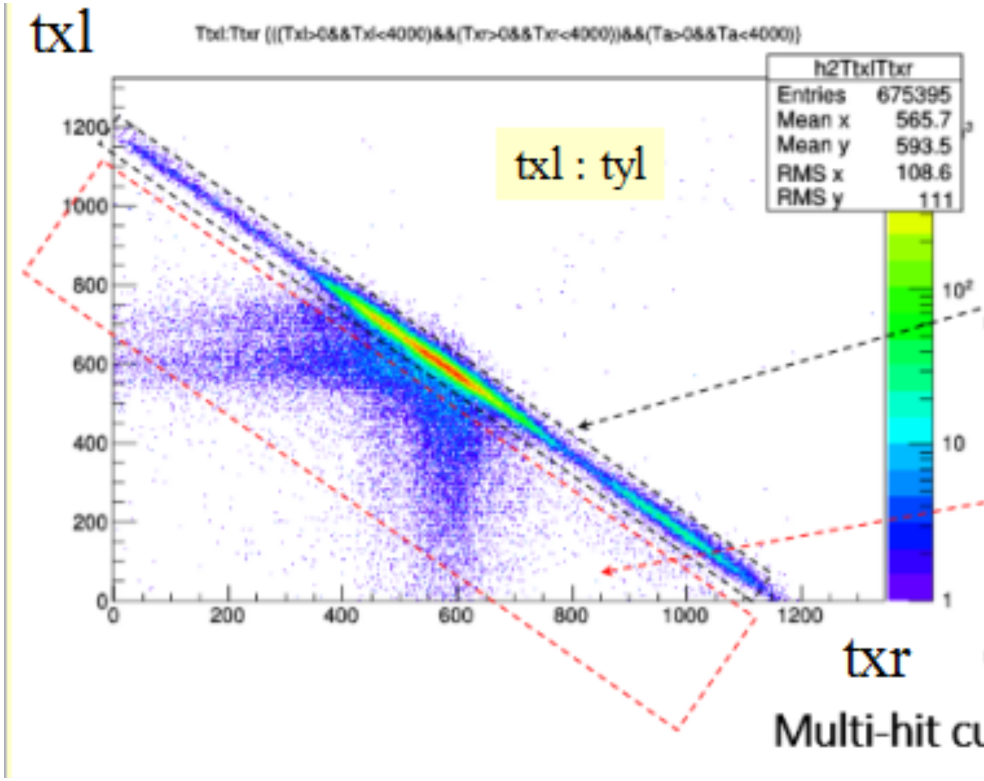
$$x = c_x(t_{xl} - t_{xr})$$

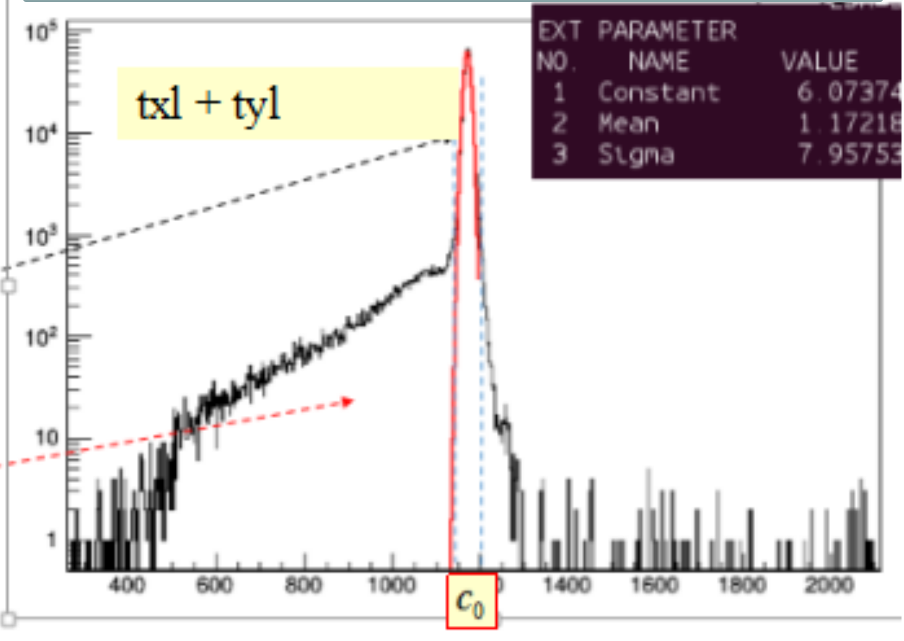
$$t_{xl} + t_{xr} = c_0$$



$$t_{xl} = t_{al}; \quad t_{xr} = t_{br}$$

$$t_{xl} + t_{xr} < c_0 \quad for \quad multi-hit \quad events$$





Multi-hit cut `"abs(Ttxl+Ttxr-1172)<24"`

beam at target

$$\sigma = \frac{N_{11C}}{\boxed{N_{14O}} N_s}$$

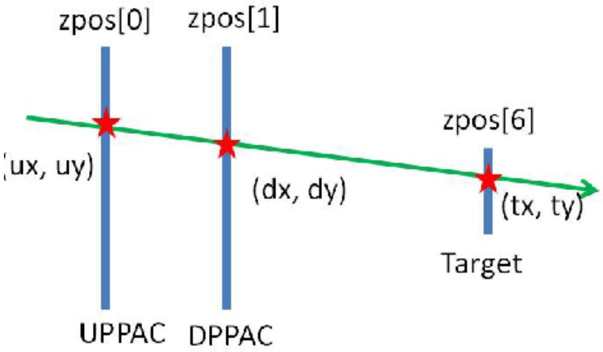


图 3.3-8　PPAC 位置追踪

$$N_{14O} = N_{beam} \times \varepsilon_{14O\_purity} \times \frac{N_{target}}{N_{beam}}$$

N_{beam}: Scaler

ε_{14O}: DB trig

N_{target}: Dbtrig with tracking

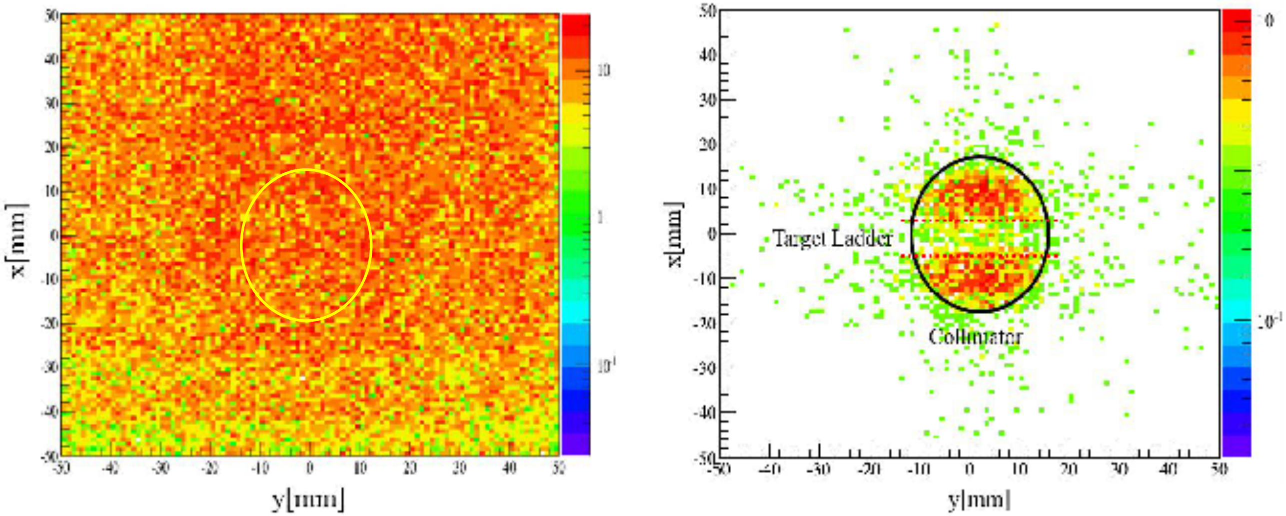
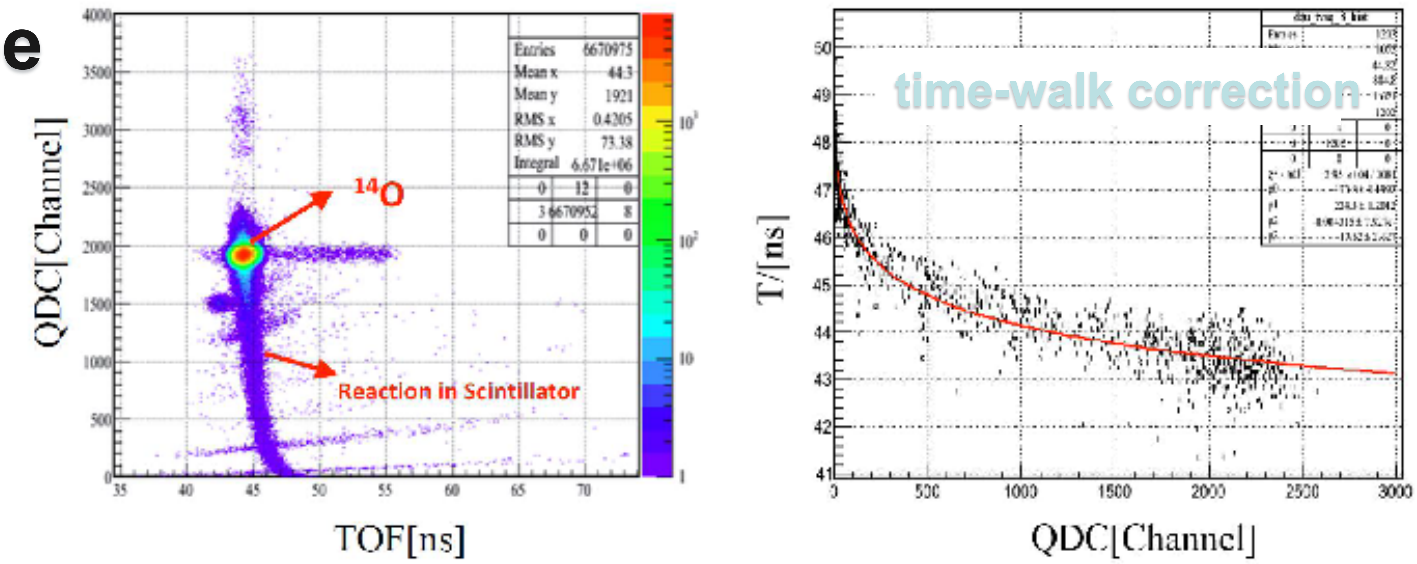


图 3.3-9　靶上束流的位置分布，左图束流子触发的结果，右图选择束流和 HODOSCOPE 符合的结果

Hodoscope



time-walk correction

图 3.4-3 WLAK 修正

position calibration

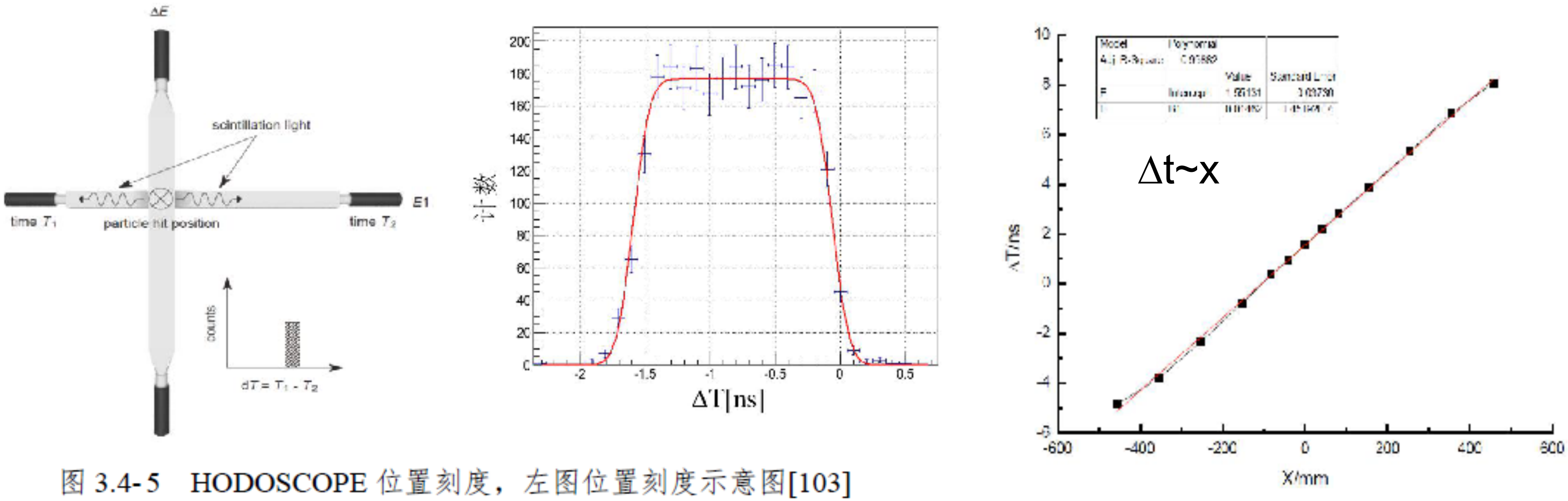
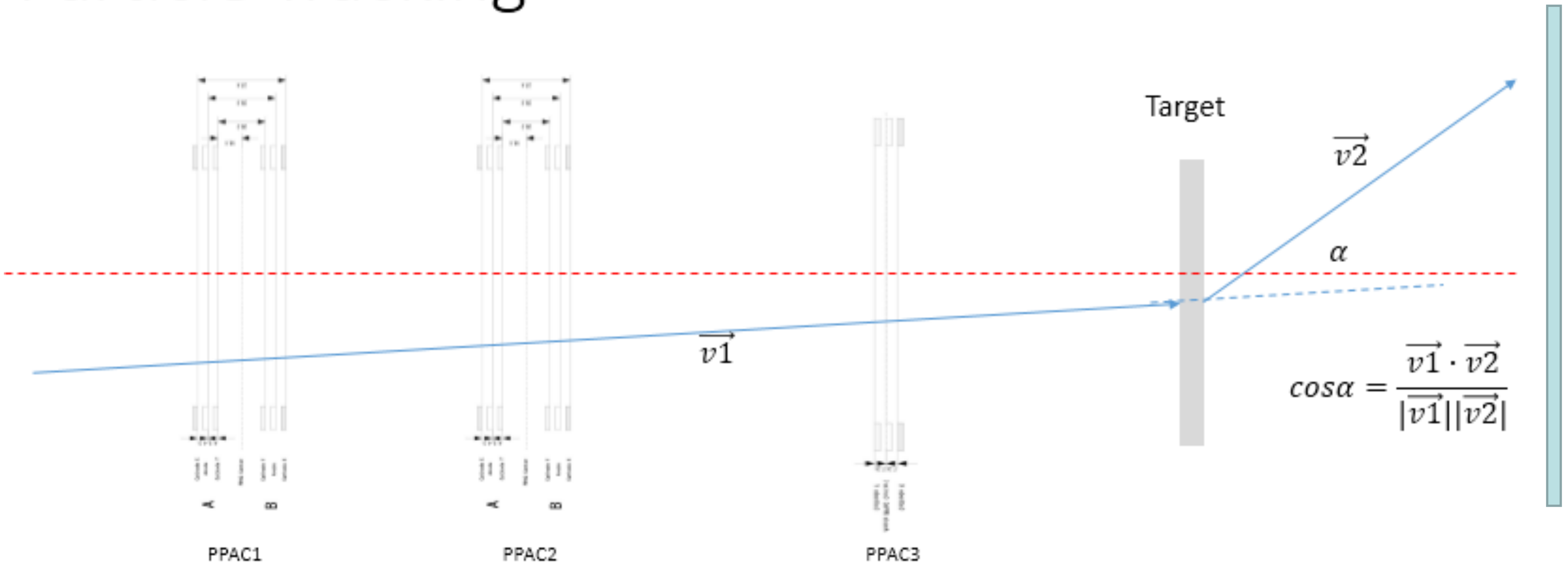


图 3.4-5 HODOSCOPE 位置刻度，左图位置刻度示意图[103]
右图打在一个格点上的事件的时间差谱，红线是拟合结果

Particle Tracking

Online
- Beam tuning (position, direction)
- beam profile at target position

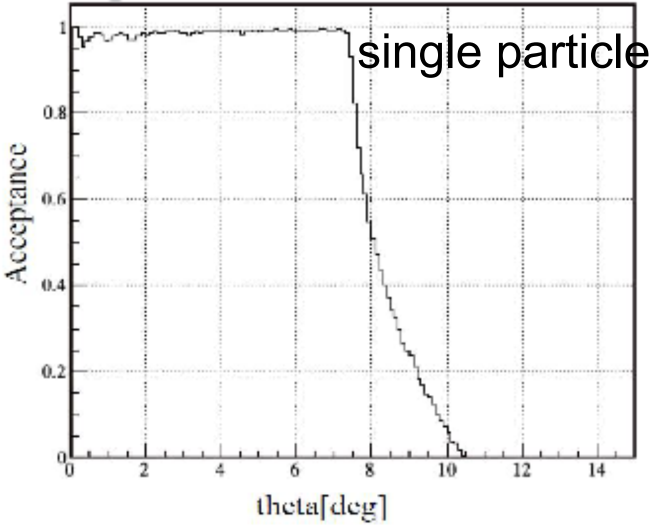
Offline
- reaction dynamics (Scattering angle)



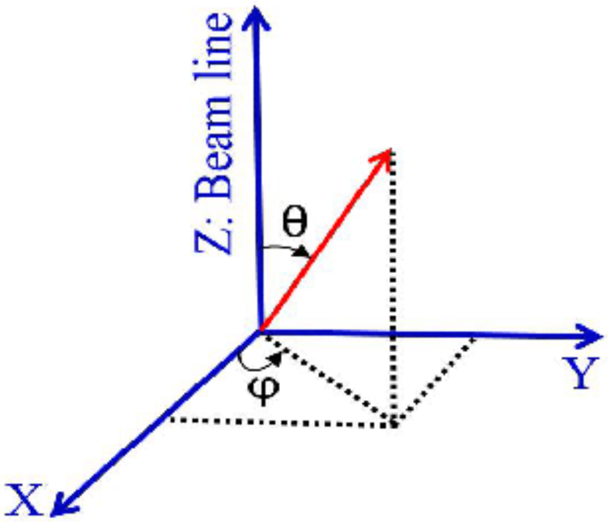
$$cos\alpha = \frac{\overrightarrow{v1} \cdot \overrightarrow{v2}}{|\overrightarrow{v1}||\overrightarrow{v2}|}$$

Hodoscope-Acceptance

MC simulation



single particle



$$M^2=\left\{\sum_i (m_i+T_i)\right\}^2-\left|\sum_i \overrightarrow{p_i}\right|^2$$

$$E_{decay}=M-\sum_i m_i$$

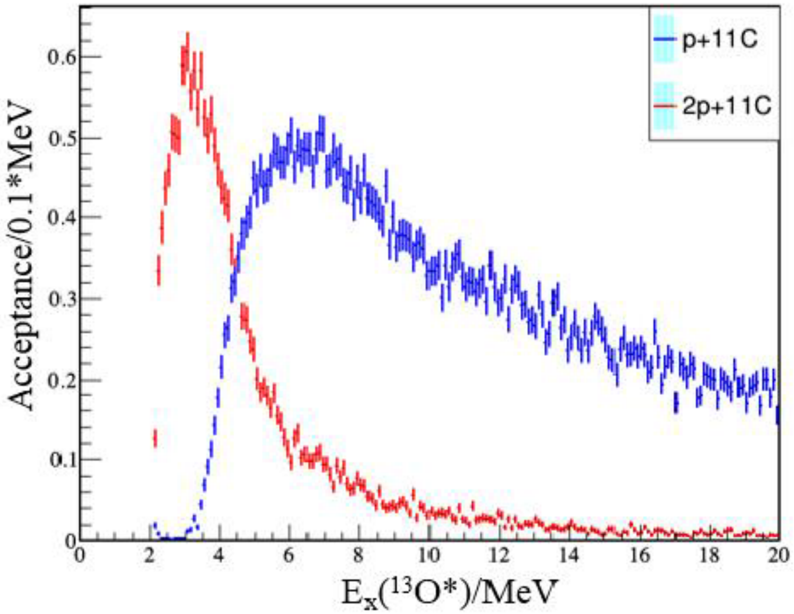


图 3.4-18　^{13}O 激发态三体直接衰变到 2p+^{11}C，HODOSCOPE 测到两体(p+^{11}C，蓝线)和三体(2p+^{11}C，红线)的接收度

Telescope-Acceptance

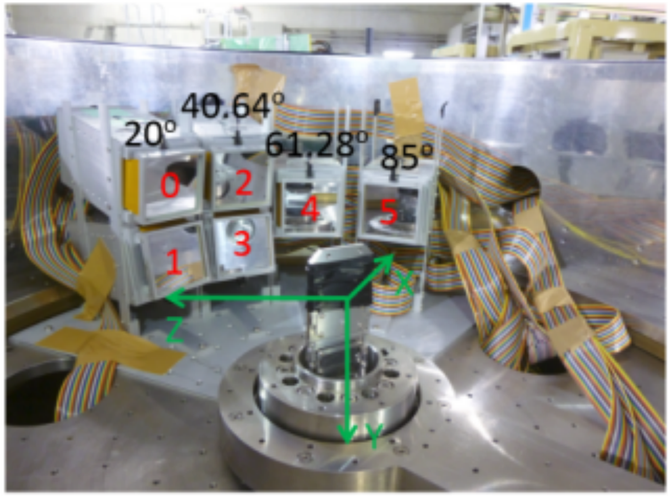


图 2.2-9　靶室内望远镜阵列设置
图中数字为望远镜编号(红色)以及中心和 Z 束流线的夹角(黑色)
图中的绿线标示了坐标系的定义

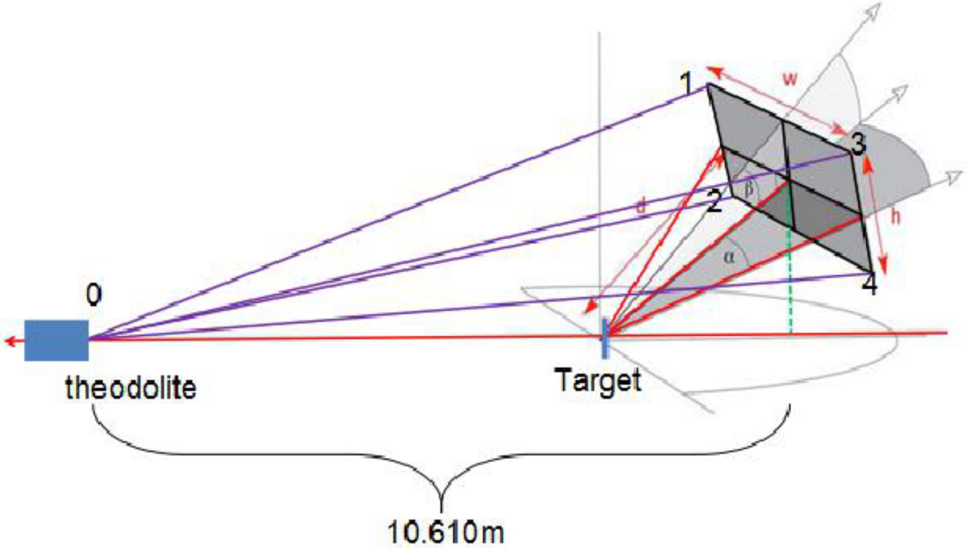


图 3.5-5　TELESCOPE 阵列定位

MC simulation

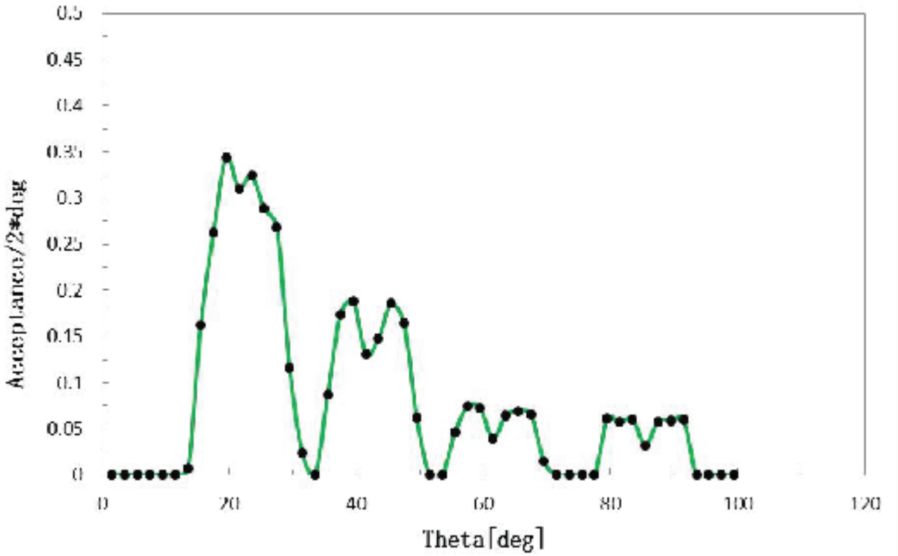


图 3.5-6　TELESCOPE 每 2 度的接收度

Reaction in Detector

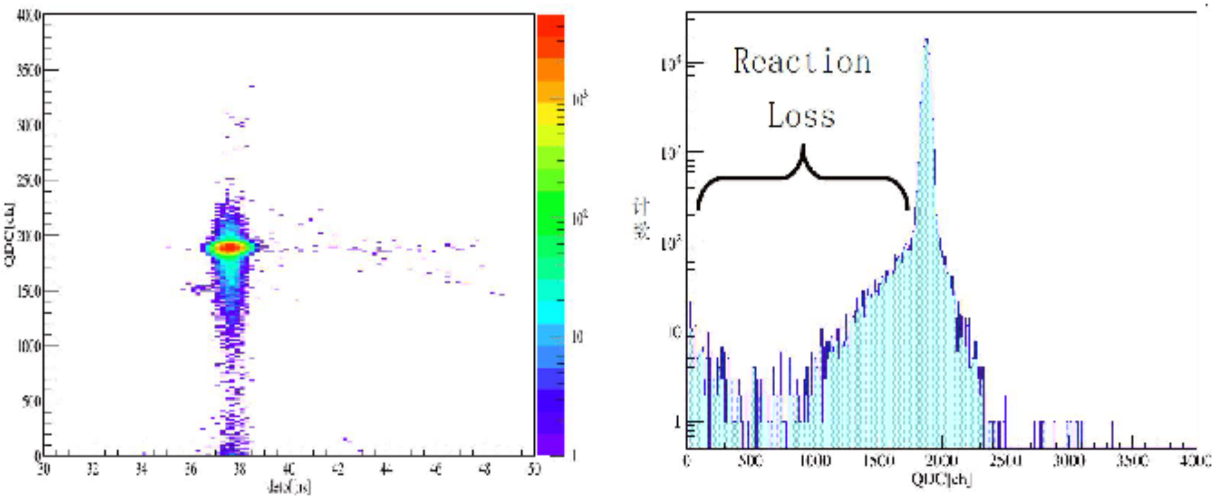


图 3.6-6 空靶时 ^{14}O 在 HODOSCOPE 上的反应损失

对 QDC 和 TOF 取其中心值±3sigma，范围之外的认为是在 HODOSCOPE 上的反应损失带来的。计算得到的反应损失为 10.5%±0.1%。

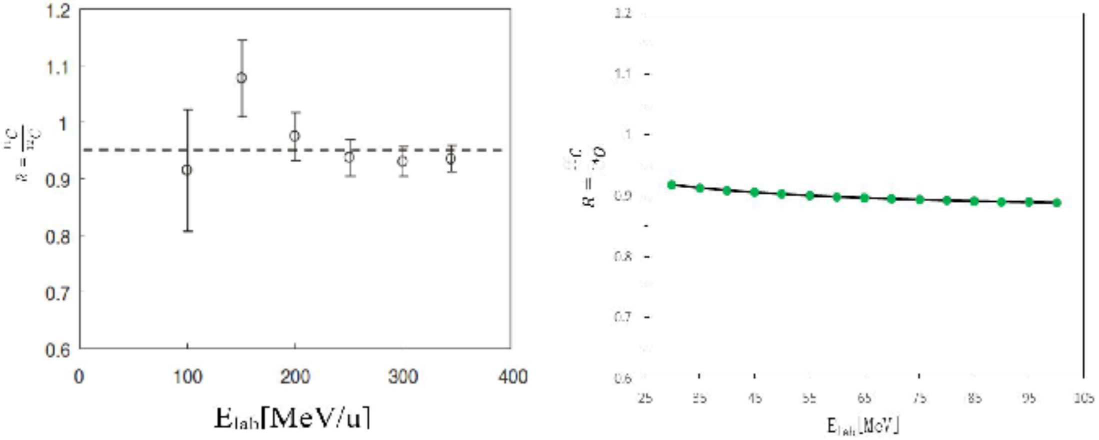
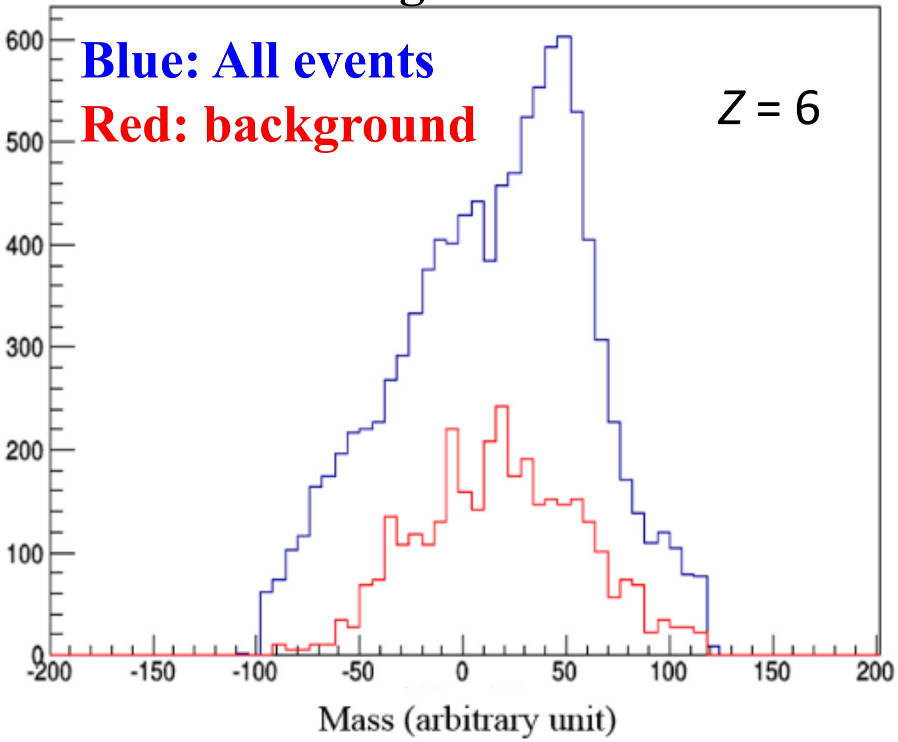


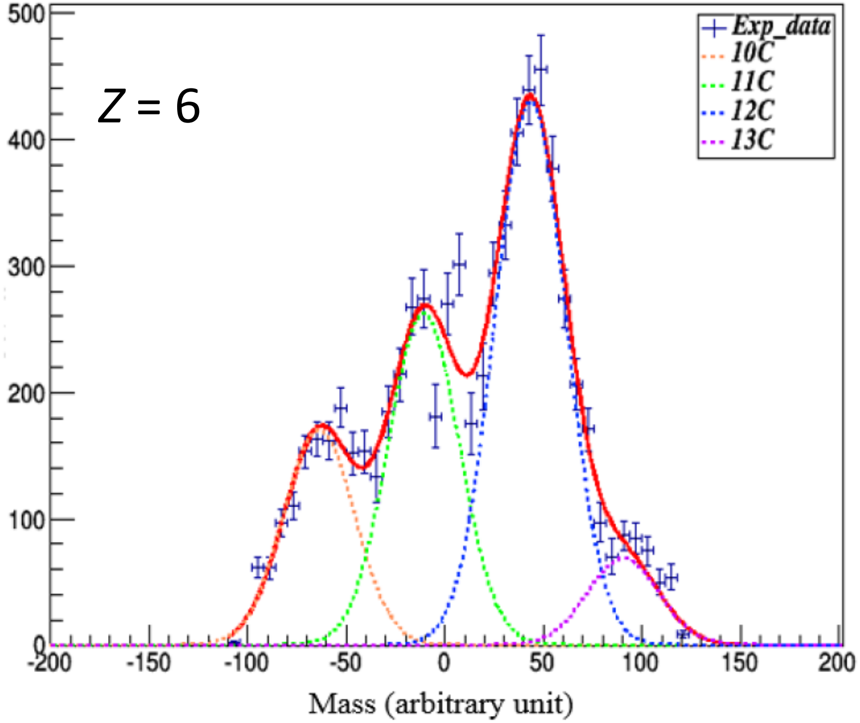
图 3.6-7 反应损失的比值，左图为 ^{11}C 和 ^{12}C 在塑闪中的反应截面的比值，取自文献[109]；右图为 Kox 公式计算得到的 ^{11}C 和 ^{14}O 在塑闪中反应截面的比值

Background estimation with empty target

Before background subtraction



After background subtraction



$$\sigma = \frac{R'_s}{R'_i * 1/F * N_s * (1-R_{^{11}C})}$$

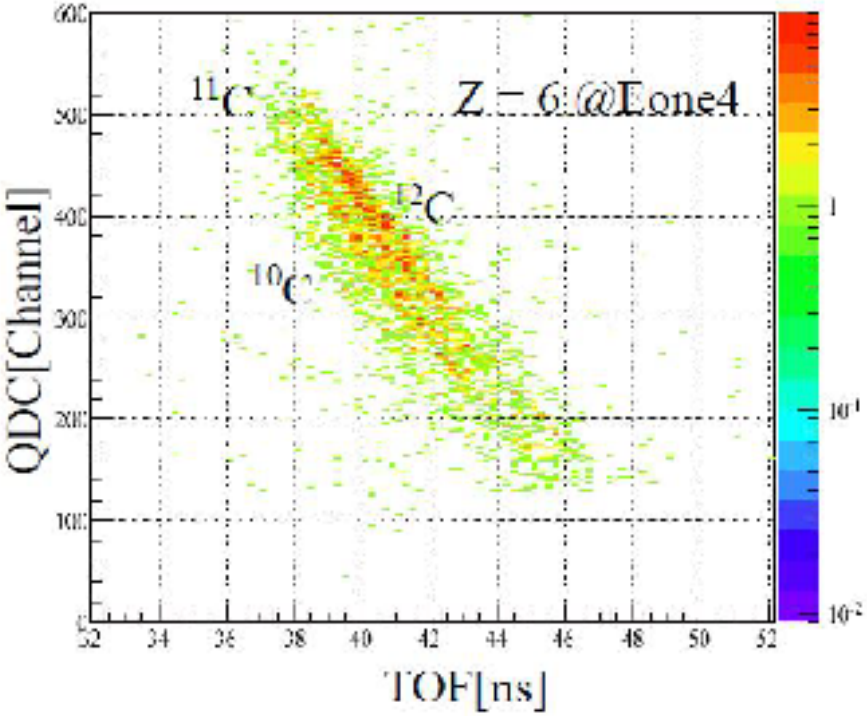
Reaction loss at hodo

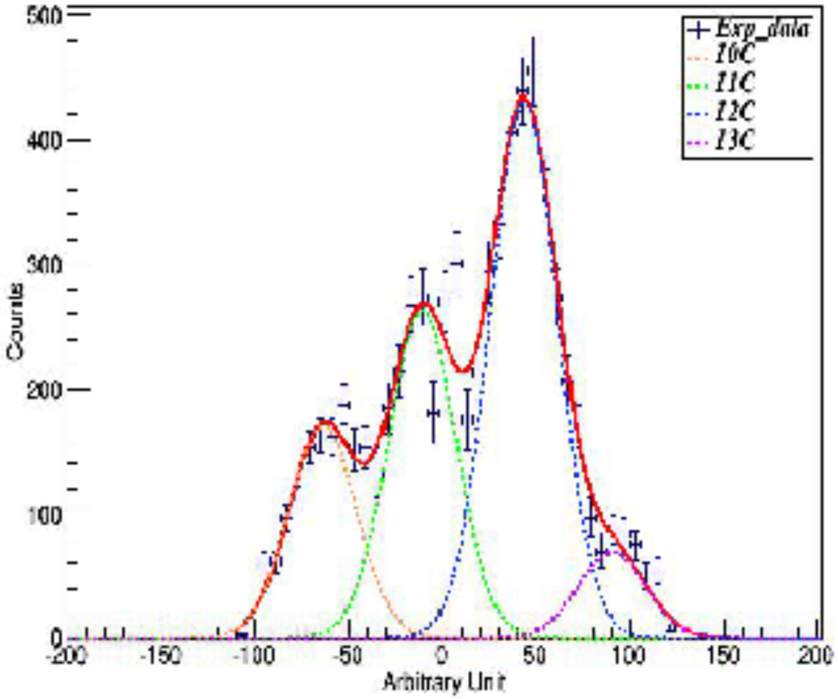
$$\left(\frac{\delta_\sigma}{\sigma}\right)^2 = \left(\frac{\delta_{R'_s}}{R'_s}\right)^2 + \left(\frac{\delta_{R'_i}}{R'_i}\right)^2 + \left(\frac{\delta_{1/F}}{1/F}\right)^2 + \left(\frac{\delta_{N_s}}{N_s}\right)^2 + \left(\frac{\delta_{R_{^{11}C}}}{R_{^{11}C}}\right)^2$$

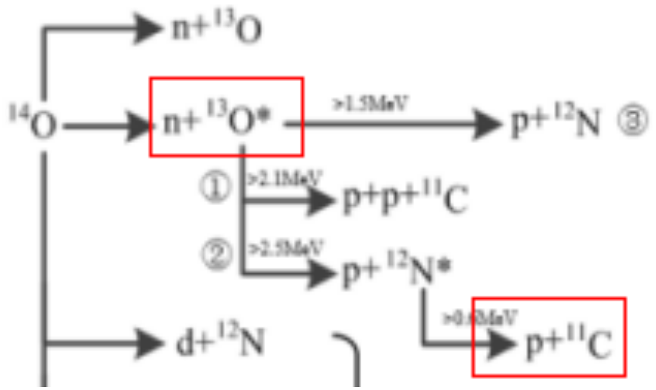
14.3% 0.2% 0.06% 0.4% 2%

60 MeV/u $^{14}O \rightarrow {}^{11}C$ cross section 60±9 m

$$\sigma = \frac{\boxed{N_{11C}}}{N_{14O}N_s}$$







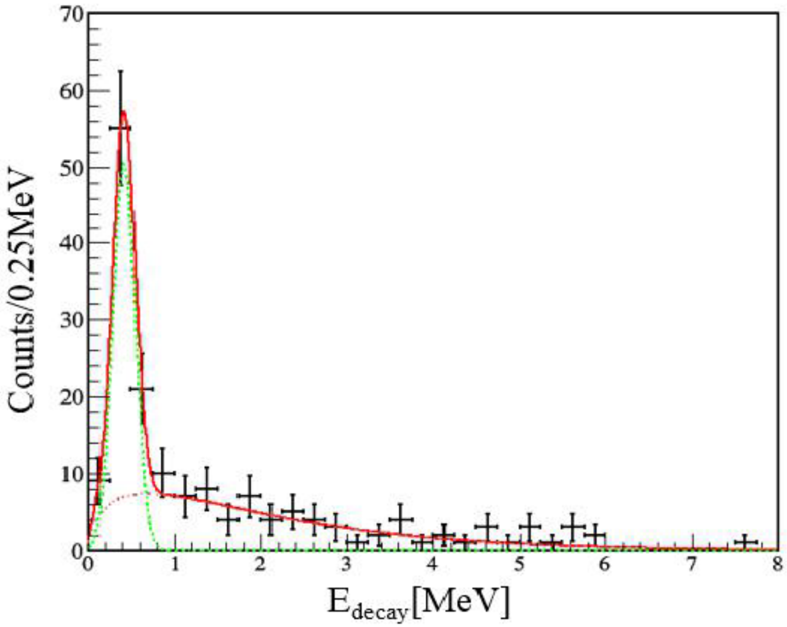


图 3.6-10　选择 ^{11}C 和质子重建的 ^{12}N 的衰变能谱

^{13}O*主要通过中间态的 ^{12}N*衰变到 ^{11}C，参考式(3-65)该过程的截面

$$\sigma = \frac{R_s^{'}}{R_i^{'} * 1/F * N_s * \varepsilon * (1 - R_{^{11}C}) * (1 - R_H)}$$

$R_s^{'}$ 为质子和 ^{11}C 重建得到的 ^{12}N*(2+)的计数约为 230±25，$R_i^{'}$ 为入射的 ^{14}O 数目；ε为 HODOSCOPE 仅测到两体的接收度，因为实验中仅观测到少量的三体符合事件，因此可假设 ^{13}O 处在较高的激发态，这样ε值约为 0.73(参考 3.6.2 节)，^{11}C 和质子在 HODOSCOPE 上的反应损失分别取 10%和 7%。由于实验测到的 p+^{12}N 的符合事件仅有 p+^{11}C 符合事件的十分之一，因此我们忽略 ^{13}O 激发态衰变到 ^{12}N 基态的截面，计算得 ^{13}O 激发态的上限约为 10±1mb。