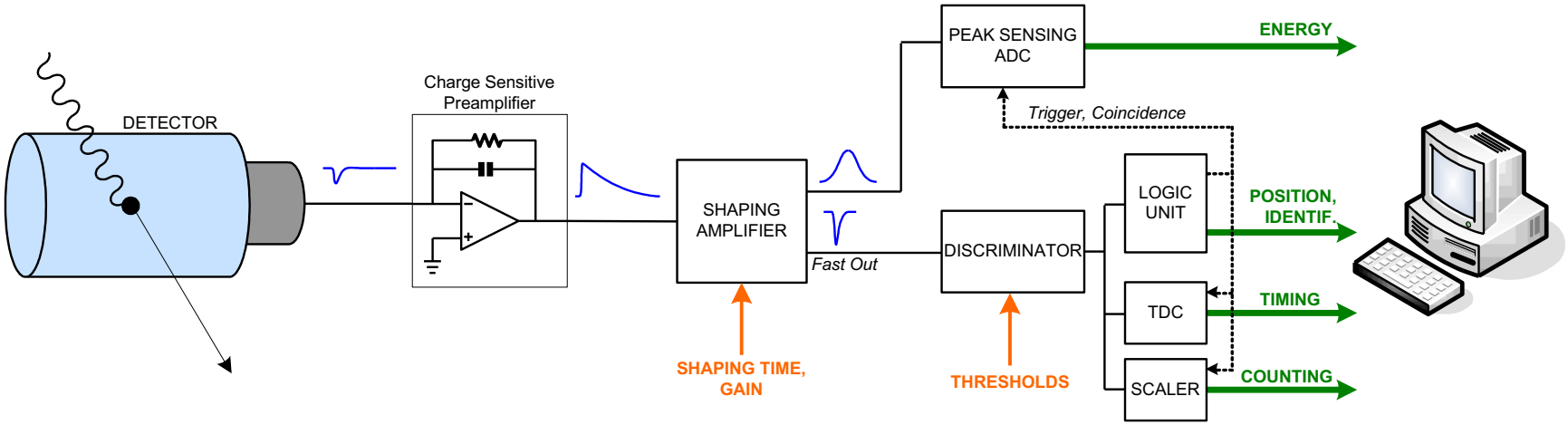
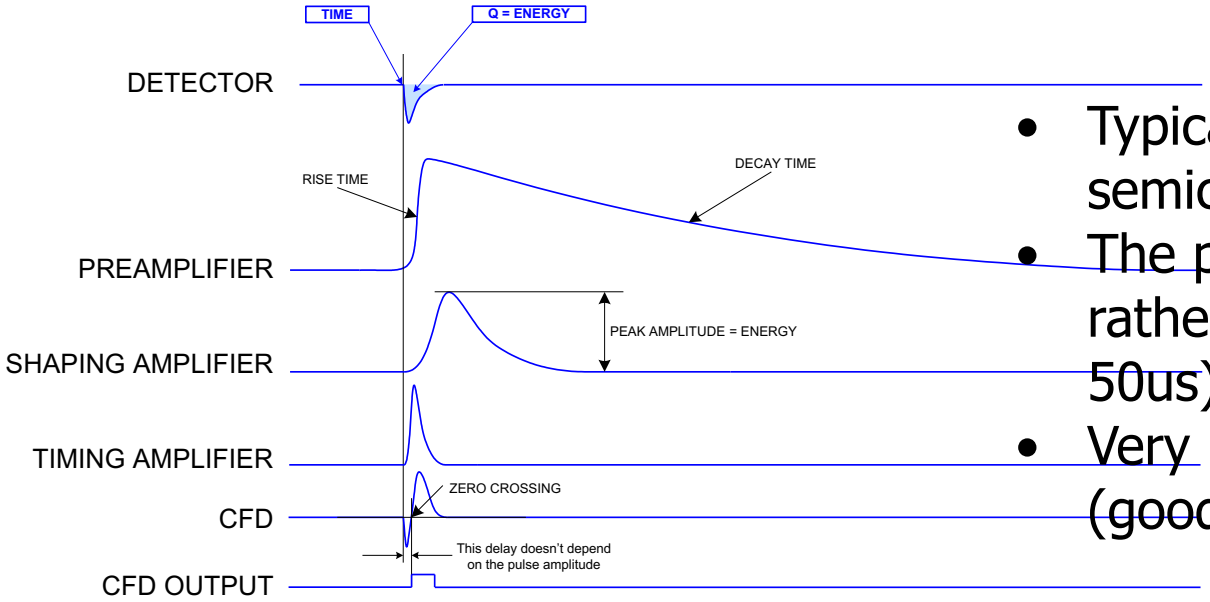
Digital Pulse Processing in Nuclear physics

Traditional chain: example
charge sensitive preamplifiers

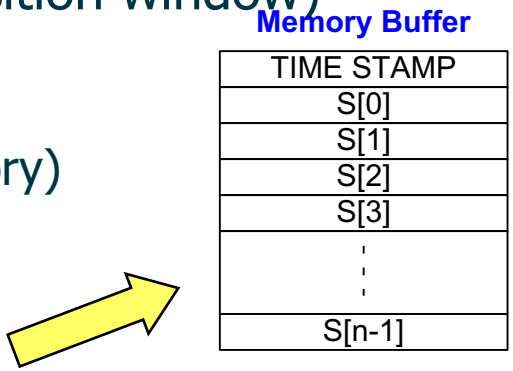


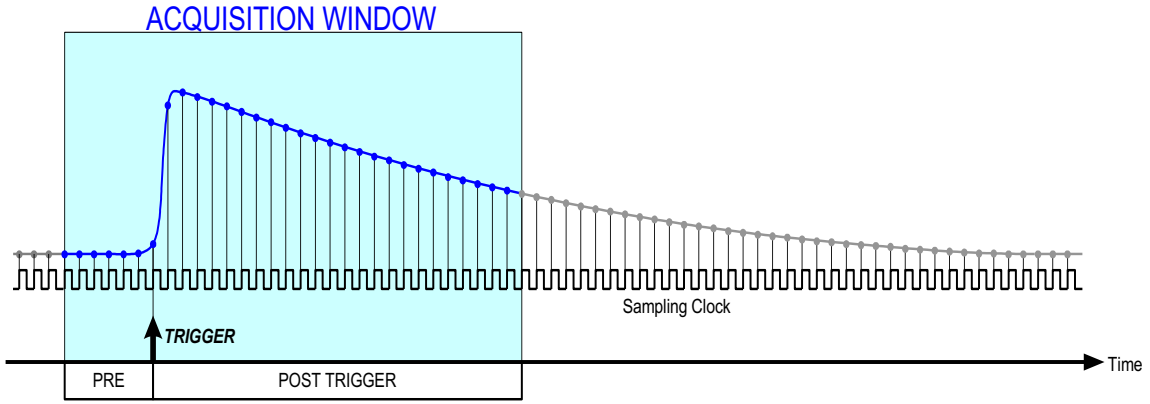


- Typically used with semiconductor detectors (Si, Ge)
- The preamp. output signal is rather slow (typ. decay time = 50us)
- Very high energy resolution (good S/N ratio)

Digitizers（flash ADC） vs Oscilloscopes

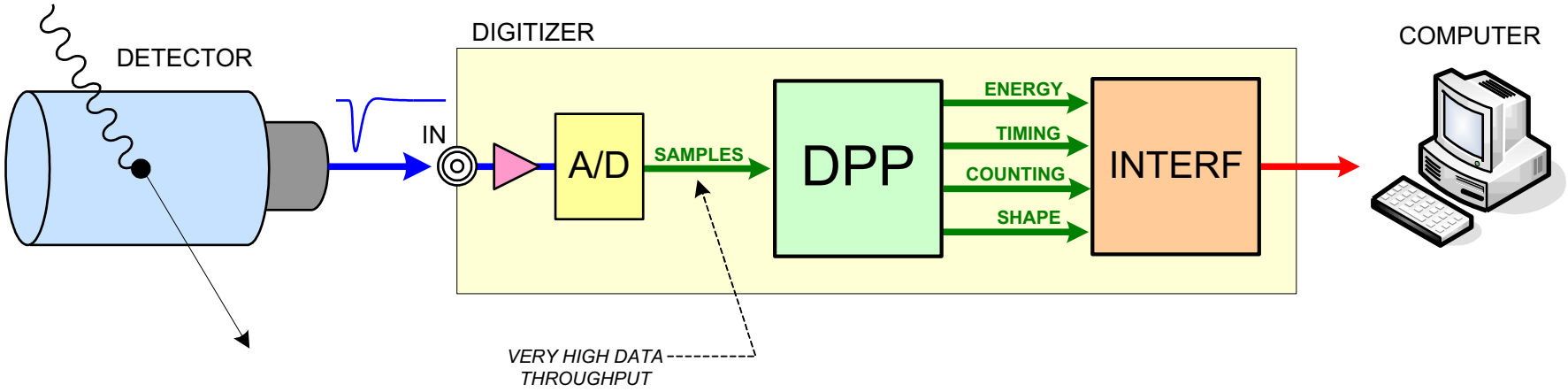
- The principle of operation of a waveform digitizer is the same as the digital oscilloscope: when the trigger occurs, a certain number of samples is saved into one memory buffer (acquisition window)
- However, there are important differences:
  - no dead-time between triggers (Multi Event Memory)
  - multi-board synchronization for system scalability
  - high bandwidth data readout links
  - on-line data processing (FPGA or DSP)

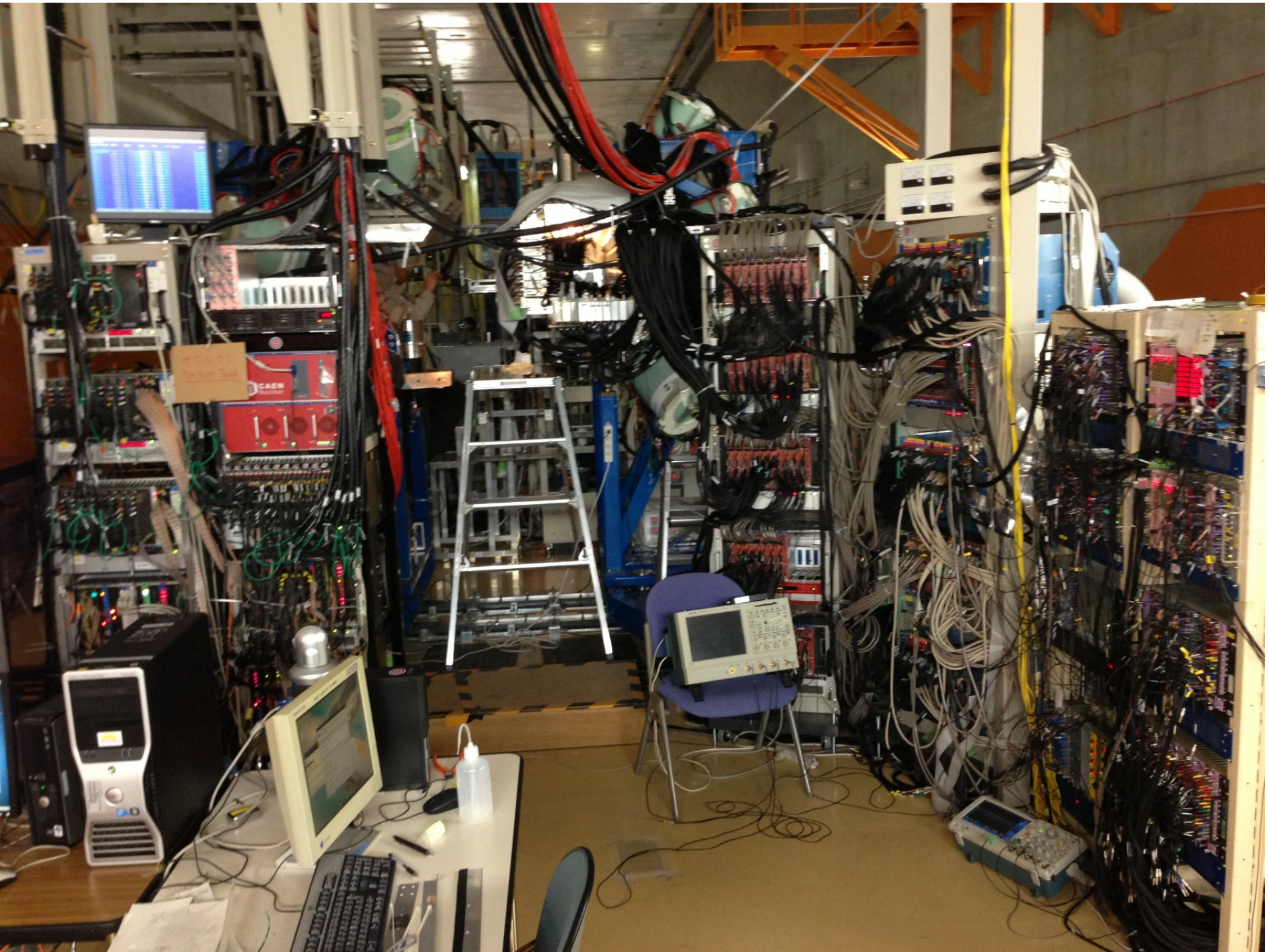




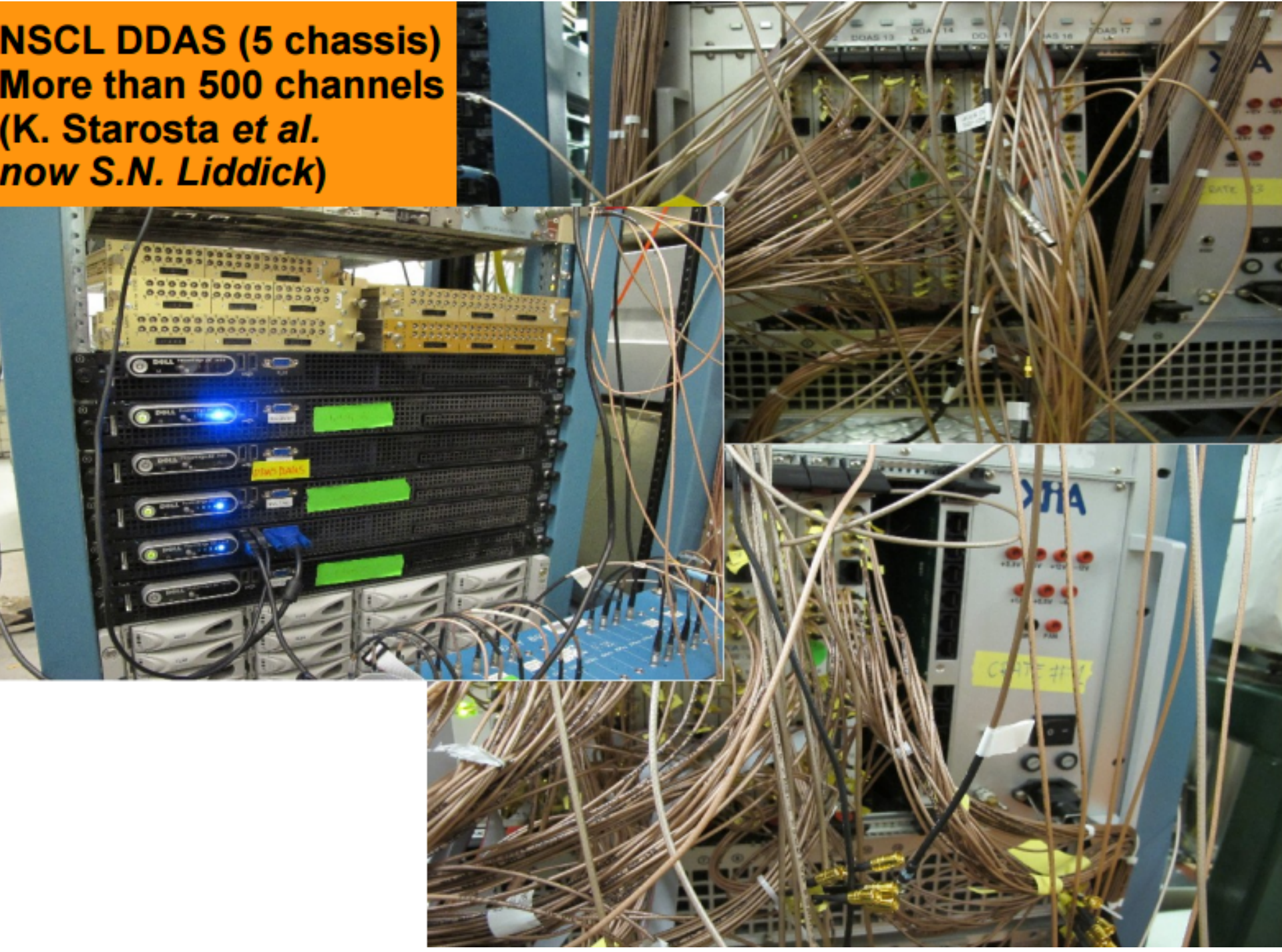
Benefits of the digital approach

- One single board can do the job of several analog modules
- Full information preserved: *A/D conversion as early as possible, data reduction as late as possible*
- Reduction in size, cabling, power consumption and cost per channel
- High reliability and reproducibility
- Flexibility (different digital algorithms can be designed and loaded at any time into the same hardware)





NSCL DDAS (5 chassis)
More than 500 channels
(K. Starosta *et al.*
***now S.N. Liddick*)**

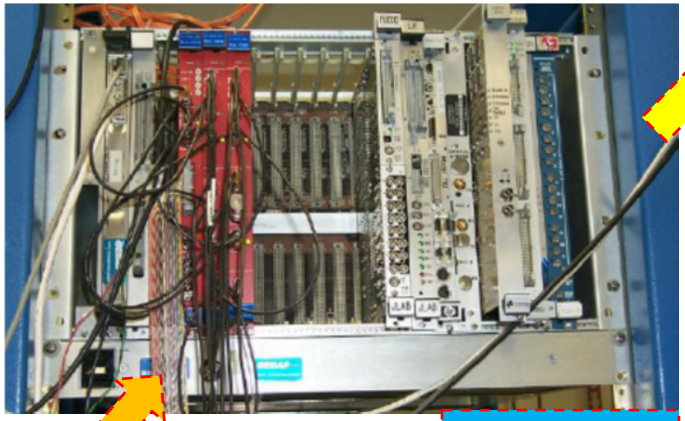


Evolution of DAQ

>20000cps

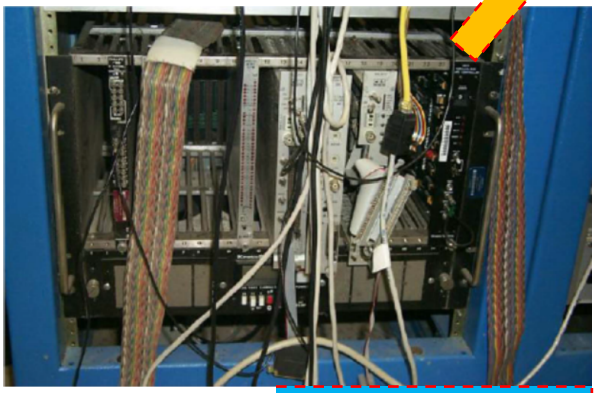
Digital

~ 5000cps



VME

~ 800cps



CAMAC

- NSCL DDAS DAQ
  - iThemba LABS DAQ
- GRITINA DAQ （ASIC）
- HiRA DAQ （ASIC）
- …

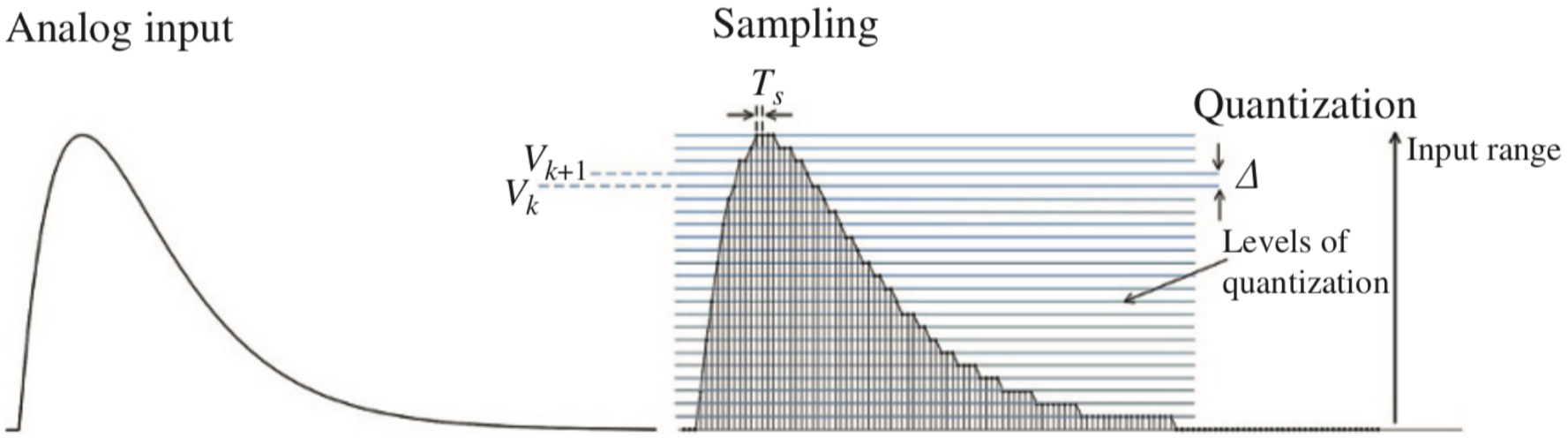
Digitization

Analog:

Continuous function V of continuous variable time t: V(t)

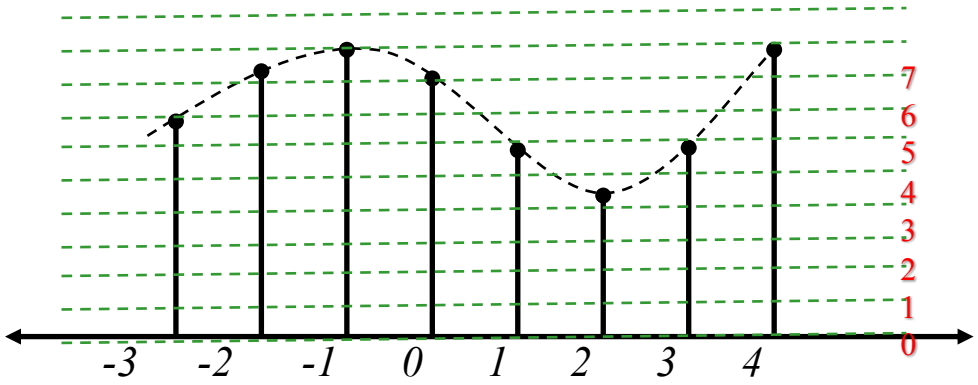
Digital:

Discrete function V_k of discrete sampling variables t_k with k= integer: $V_k=V(t_k)$



Periodic (Uniform) Sampling

1)Sampling is a continuous to discrete-time conversion



Most common sampling is periodic

$$x[n] = x(nT_s) \qquad -\infty < n < +\infty$$

Ccustomary in DSP

( ): for continuous variables

[ ]: for discrete variables

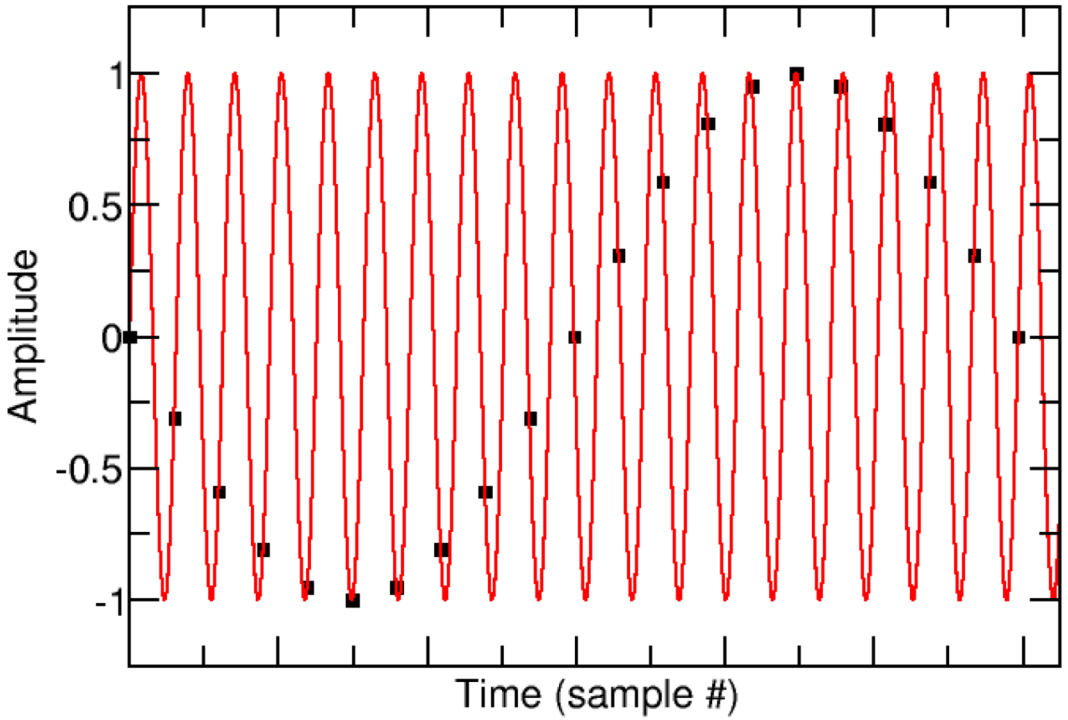
T_s is the sampling period in second

$f_s = 1/T_s$ is the sampling frequency in Hz

Sampling frequency in radian-per-second $\Omega_s = 2\pi f_s$ rad/sec

Sampling Theorem: Aliasing Error

Continuous, sinusoidal signal frequency f sampled at frequency f_s ($f_s < f$)



Aliasing: 混淆，混叠

Aliasing misrepresents the frequency as a *lower* frequency $f < 0.5f_s$

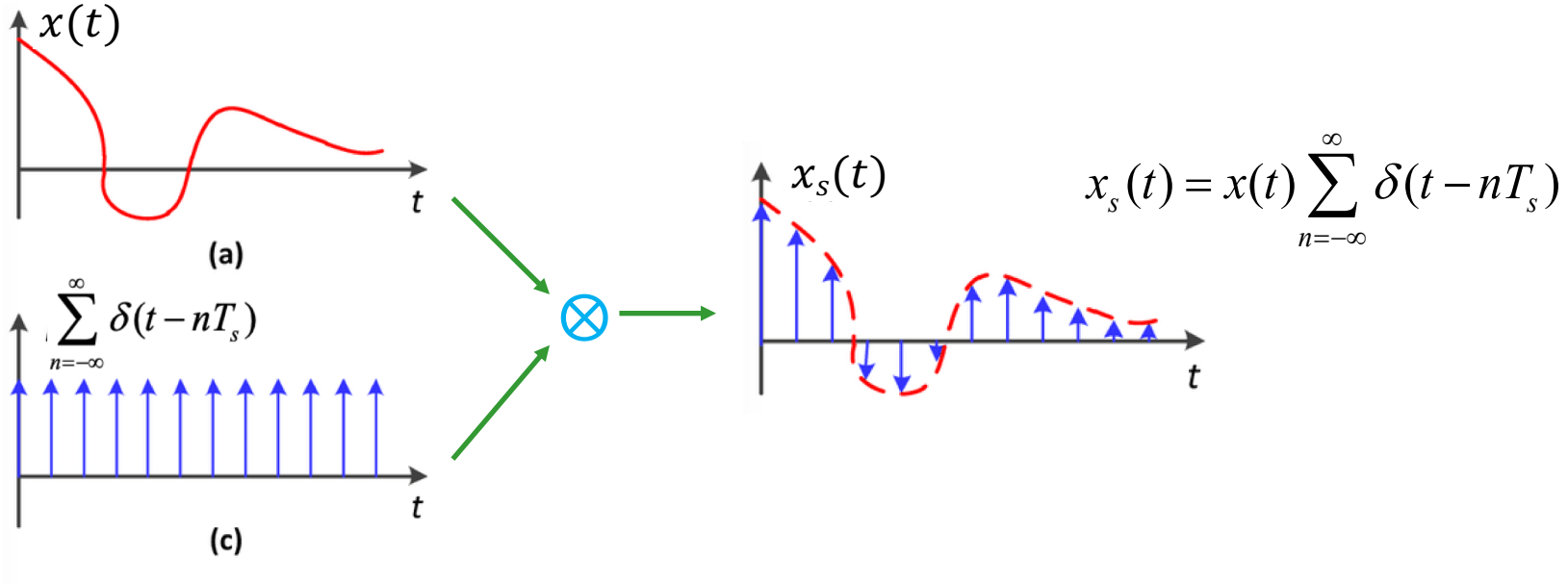
the aliasing error: If $f_s<f$, another frequency component with the same set of samples as the original signal appears in the sampled signals. Thus, the frequency component can be mistaken for the lower frequency component.

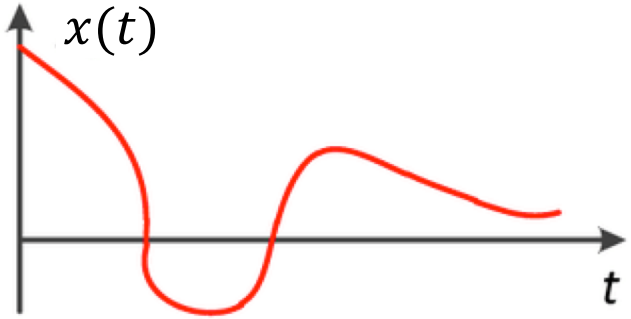
Sampling theorem

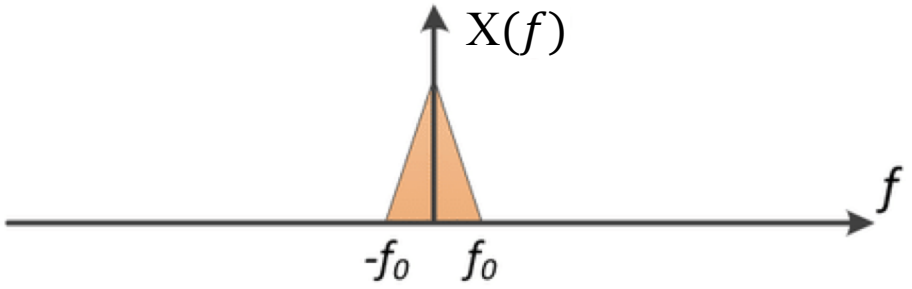
A continuous-time signal x(t) with frequencies no higher than f_{max}(Hz) can be reconstructed exactly from its sample x[n]=x(nT_s), if samples are taken at a rate $f_s=1/T_s$ that is greater than $2f_{max}$

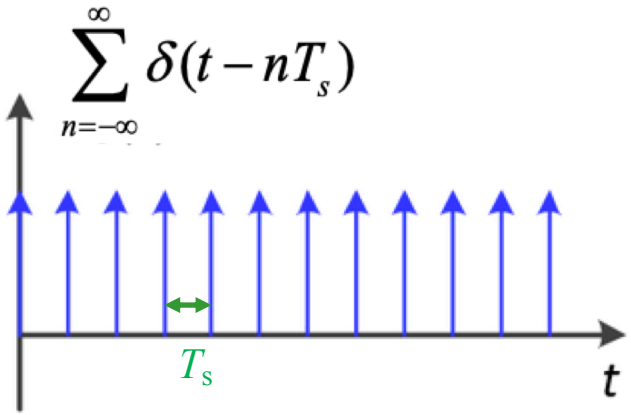
- Consider a band-limited signal x(t) with Fourier Transform X(ω)

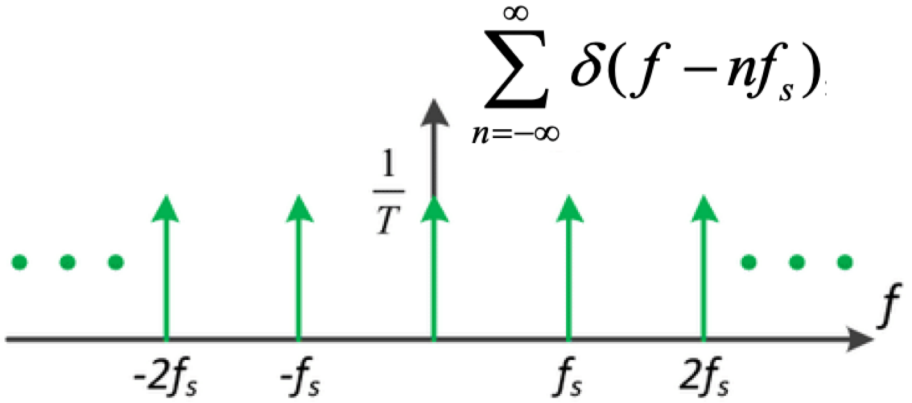
- Sampling x(t) is equivalent to multiply it by train of impulses:

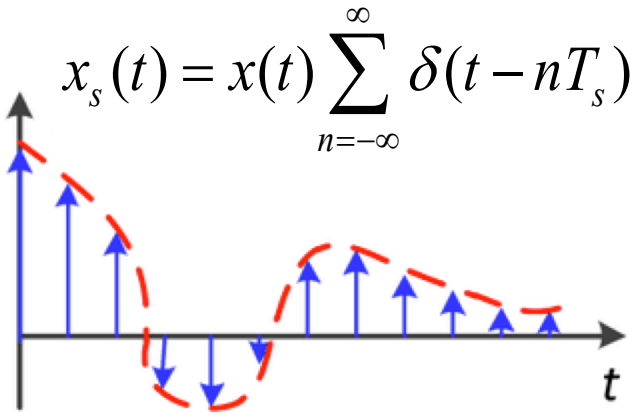






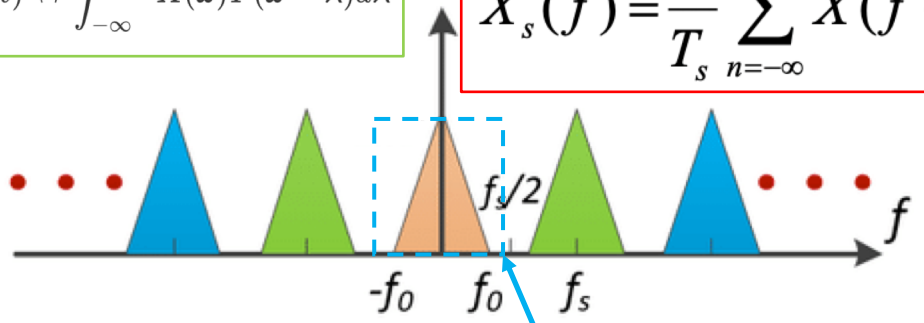






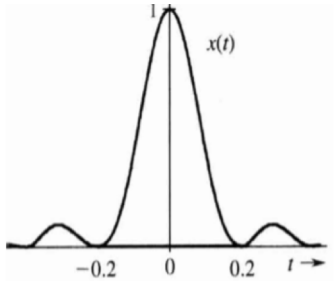
$$x(t)y(t) \leftrightarrow \int_{-\infty}^{+\infty} X(\omega)Y(\omega-\lambda)d\lambda$$

$$X_s(f) = \frac{1}{T_s}\sum_{n=-\infty}^{\infty} X(f-nf_s)$$

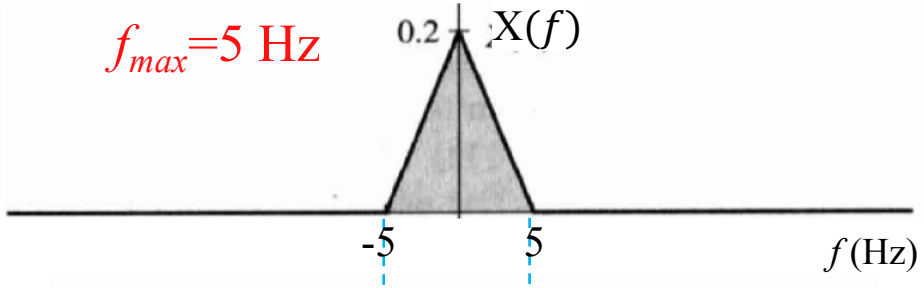


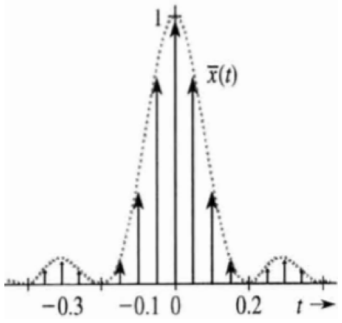
- to reconstruct the original signal x(t), we can use an ideal lowpass filter(LPF) on the sampled spectrum

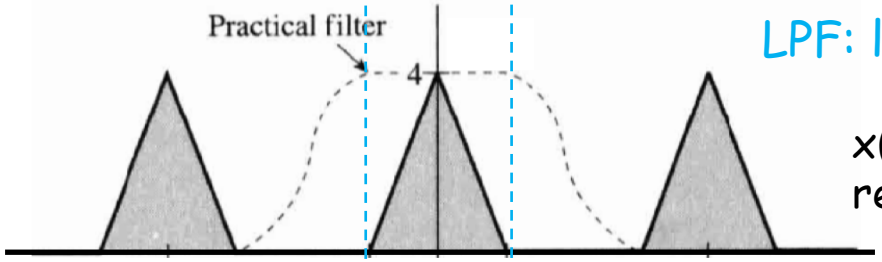
Example



f_{max}=5 Hz



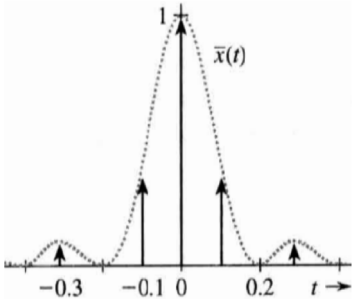


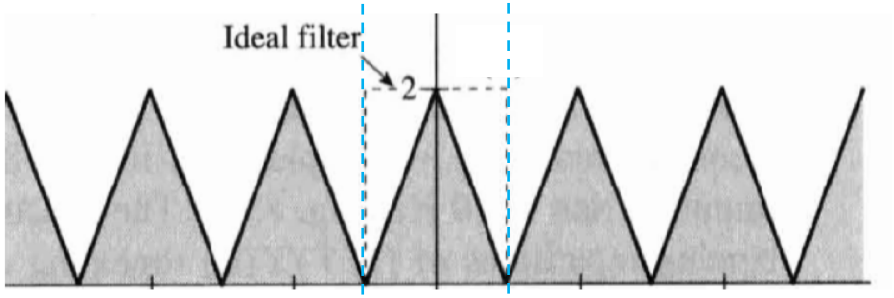


f_s=20 Hz

LPF: low pass filter

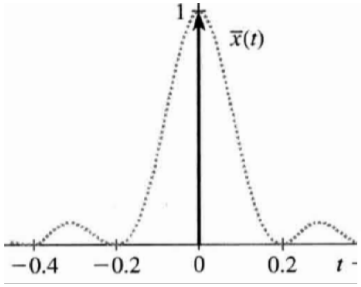
x(t) can be easily recovered by LPF

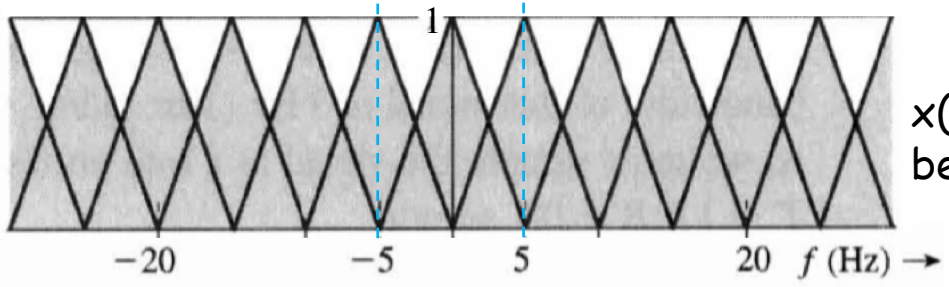




f_s=10 Hz

x(t) can be recovered by sharp LPF





f_s=5 Hz

x(t) can not be recovered

If $f_s < 2f_{max}$ sampling is irreversible due to aliasing error.

reconstructing the original signal x(t) is only possible if the shaded parts do not overlap. This means that fs must be more than TWICE that of $f_{BW}(=f_{max})$.

$f_s=2f_{BW}$ is generally known as the Nyquist Frequency 尼奎斯特频率
The minimum sampling rate that must be exceeded is known as the Nyquist Rate

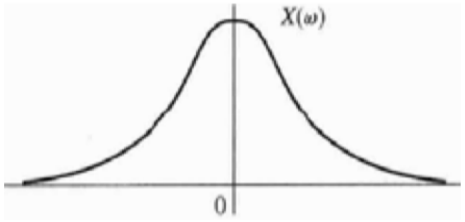
Note:
in practice the sampling frequency is usually >*5x* the signal bandwidth

Semiconductor(Ge,Si+CSP) : f_s >60 MHz(energy)
Plastic scintillator(PMT) : f_s >500MHz(timing)

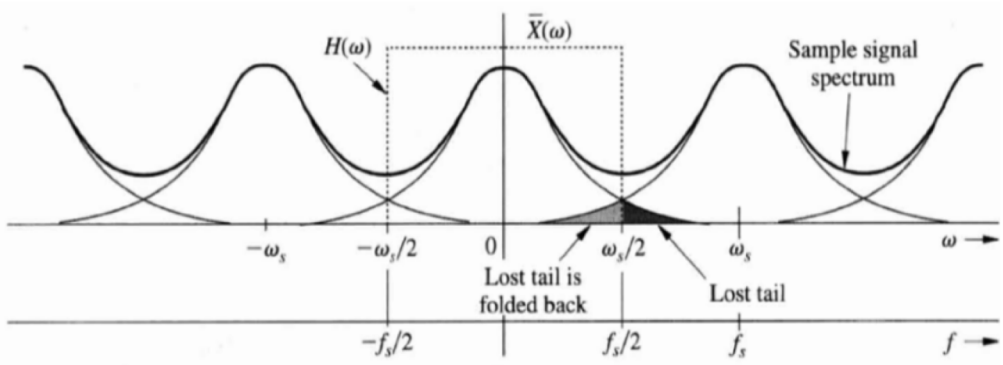
Anti-aliasing Filter

The bandwidth of any real life analog signal is infinite.

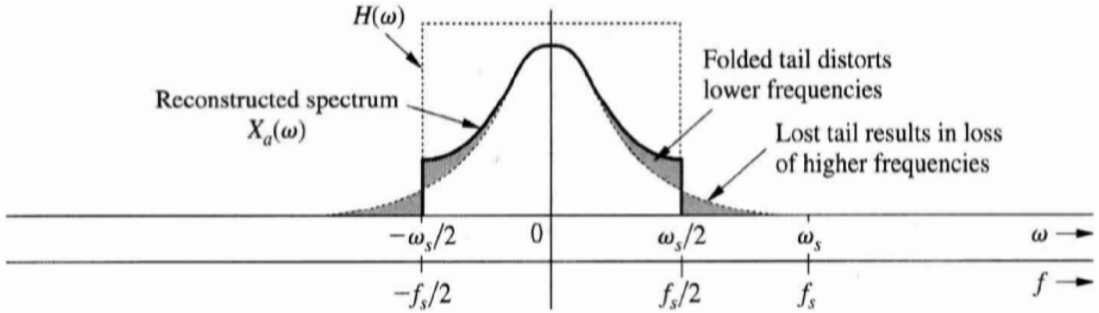
$f_{BW} \rightarrow \infty$



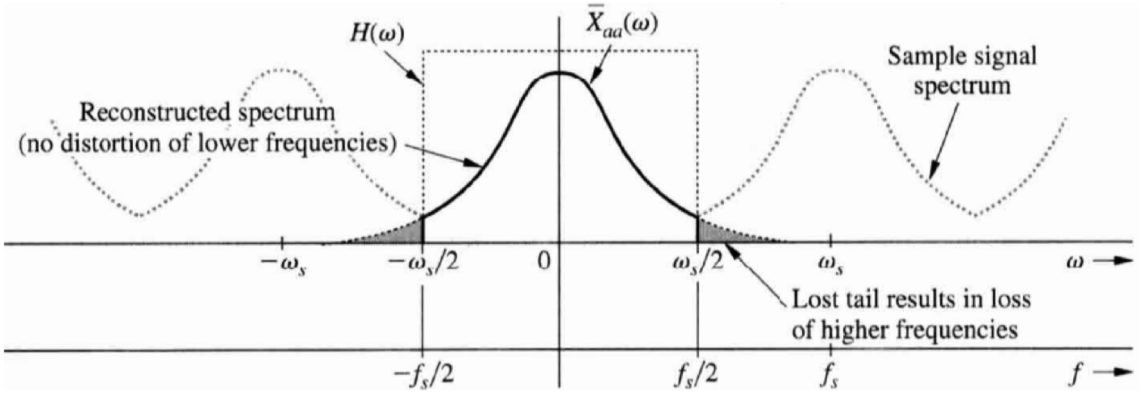
After sampling with f_s:



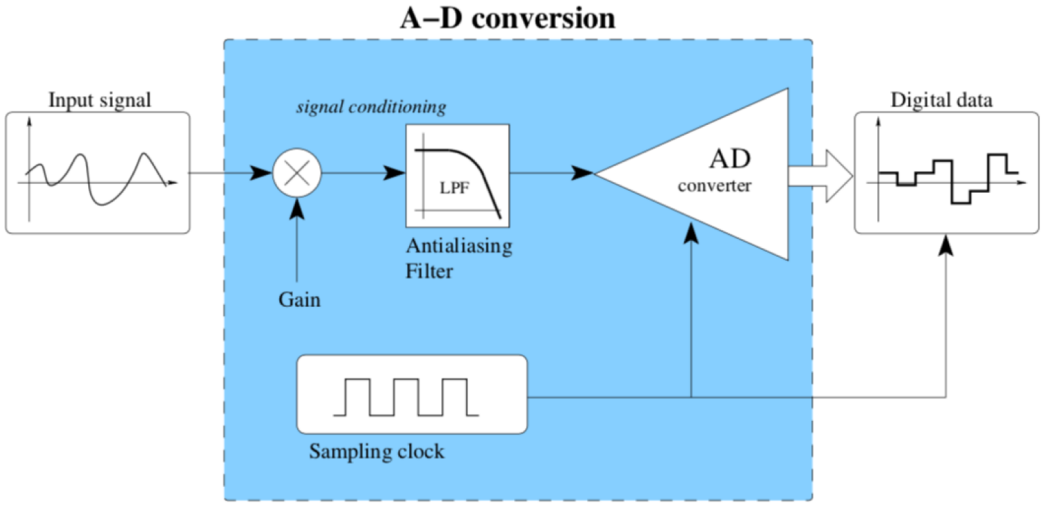
After reconstruction:



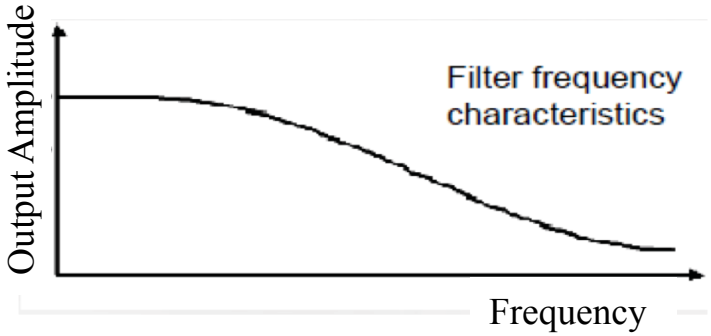
Use low-pass filter to restrict bandwidth of input signal to satisfy Nyquist criterion, $f_s > f_{BW}$. Then reconstruction can be done without distortion or corruption to lower frequencies

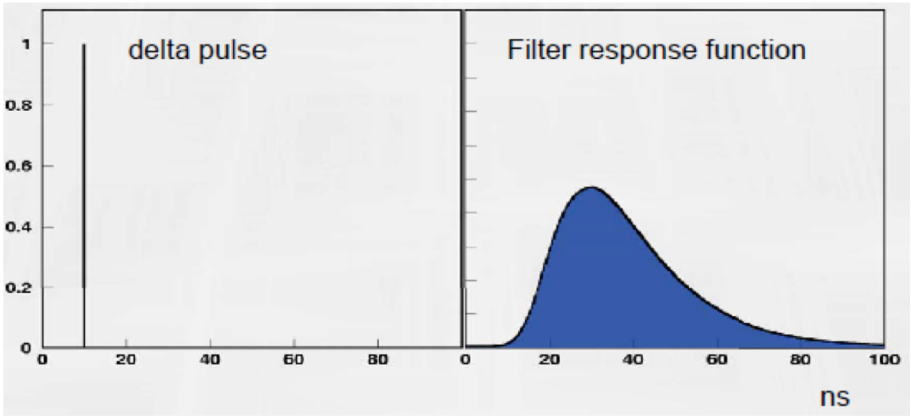


Typical ADC configuration: The input signal is first amplified or attenuated in order to have an optimal match with the input range of the AD converter. A proper antialiasing filter is then applied before the sampling.

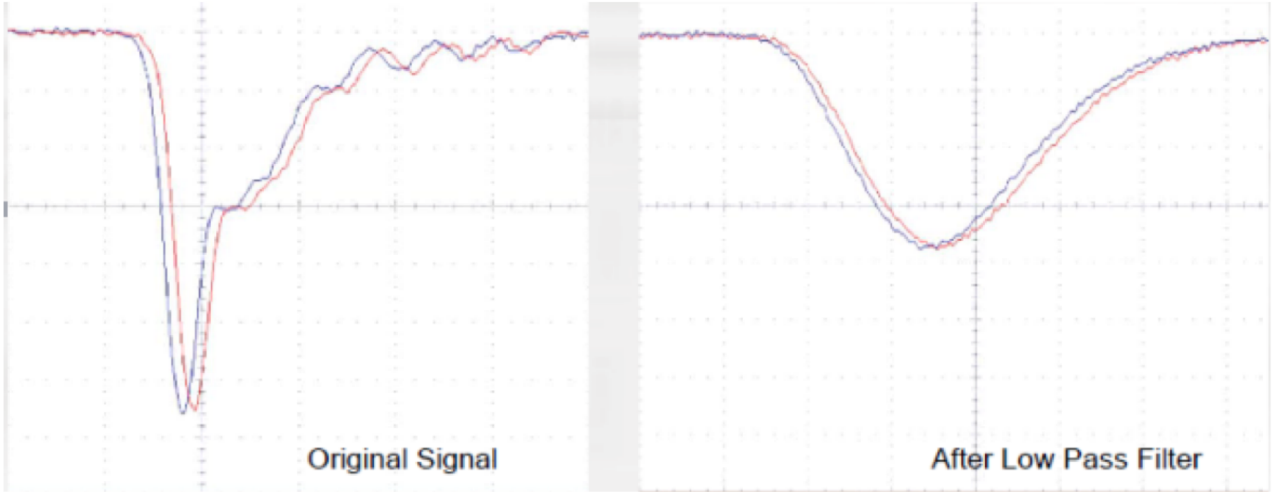


Low pass filter

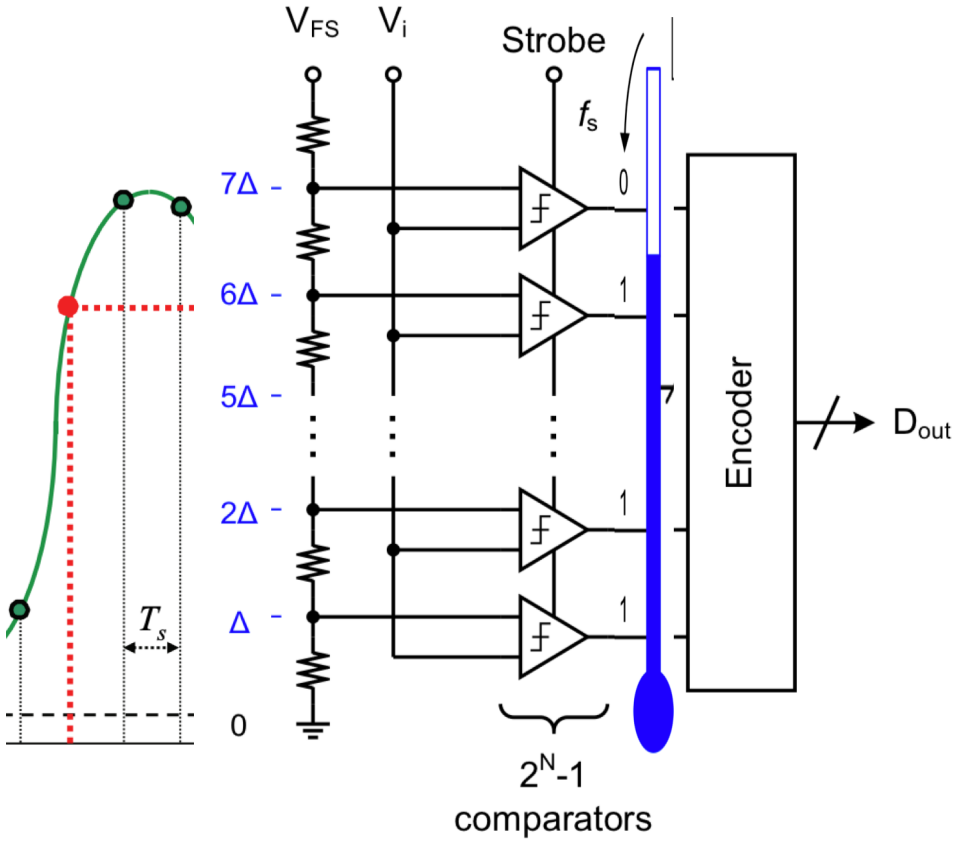




Effects of low pass filter



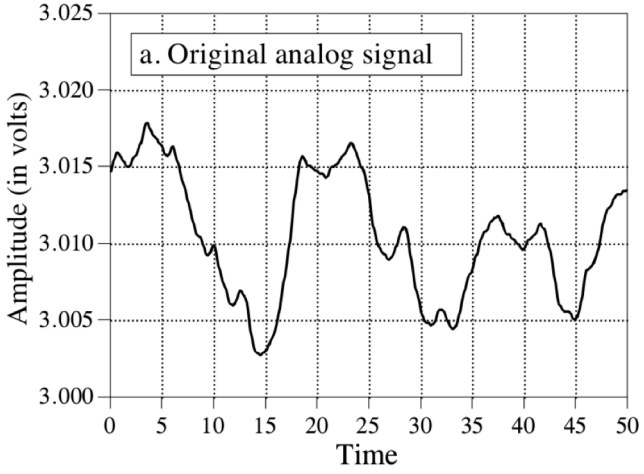
FLASH ADC



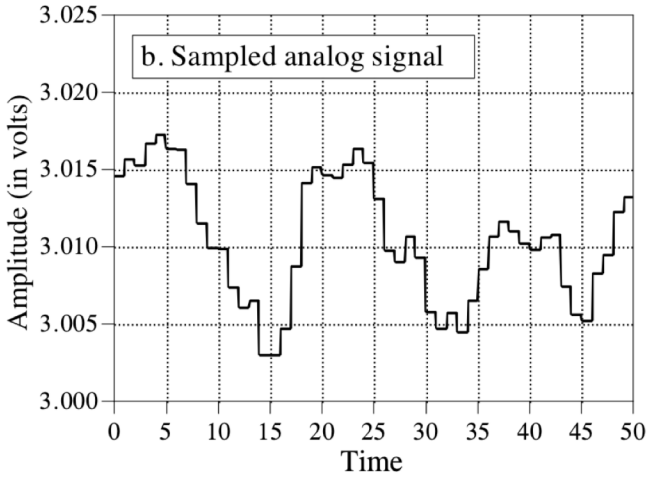
- Uses the 2^N resistors to form a ladder voltage divider, which divides the reference voltage into 2^N equal intervals.
- Use sthe2^{N-1} comparators to determine in which of these 2^N voltage intervals the input voltage V_i lies.
- The Combinational logic then translates the information provided by the output of the comparators
- This ADC does not require a clocks so the conversion time is essentially set by the settling time of the comparators and the propagation time of the combinational logic.

Very Fast (Fastest)

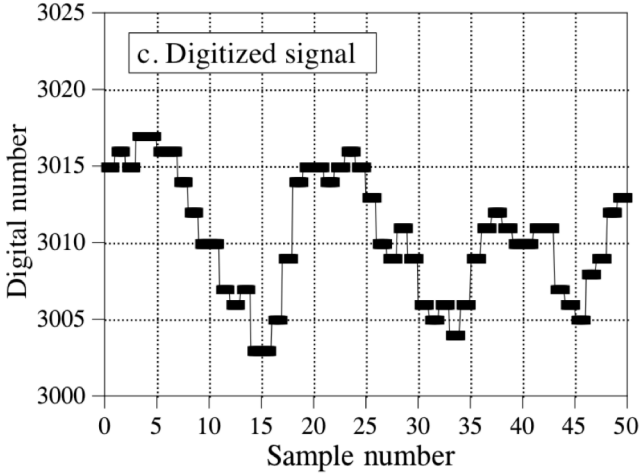
Quantization



S/H



ADC

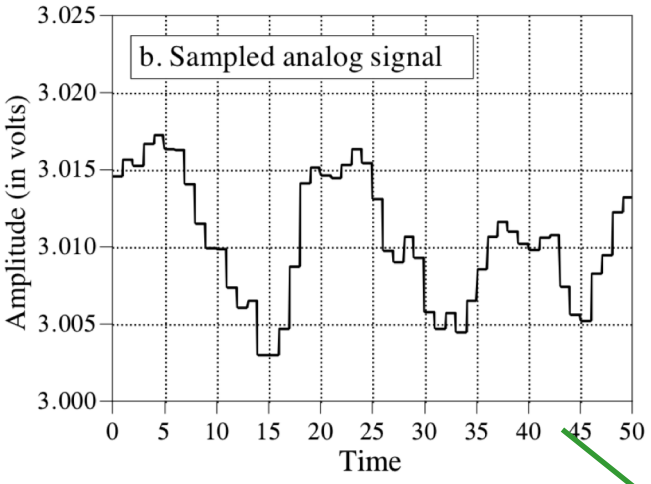


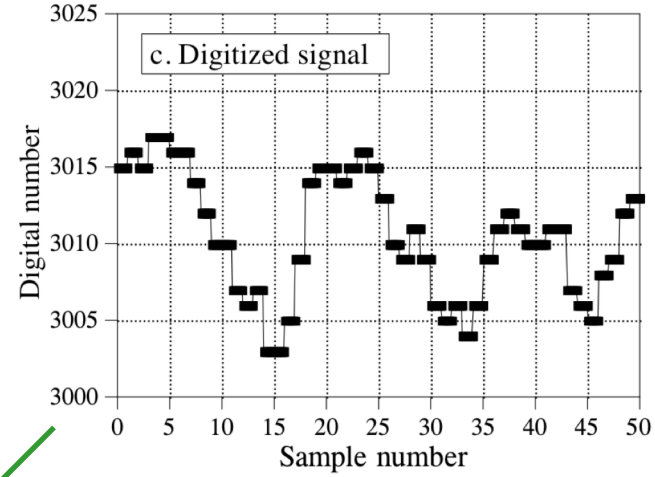
Sample-and-hold (S/H):
The only information retained is the instantaneous value of the signal when the periodic sampling takes place.

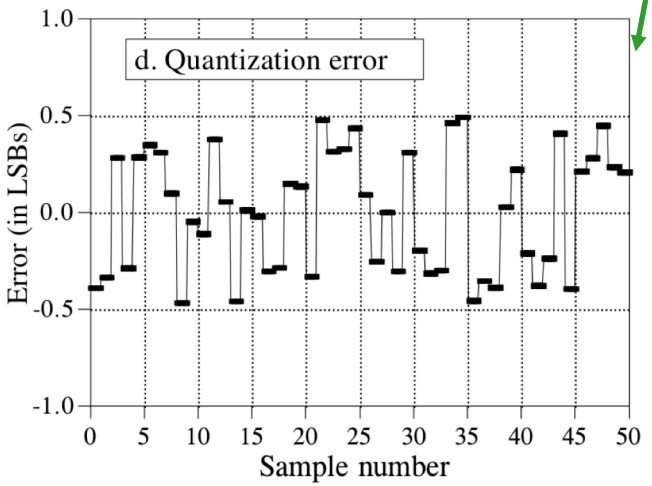
The ADC converts the voltage to the nearest integer number.

12bit digitizer:
0-4.095V -> 0-4095
LSB (Least Significant Bit) = **1 mV**

Quantization error







maximum quantization error: ±1⁄2 LSB

σ_D: SD of quantization noise ~0.29LSB

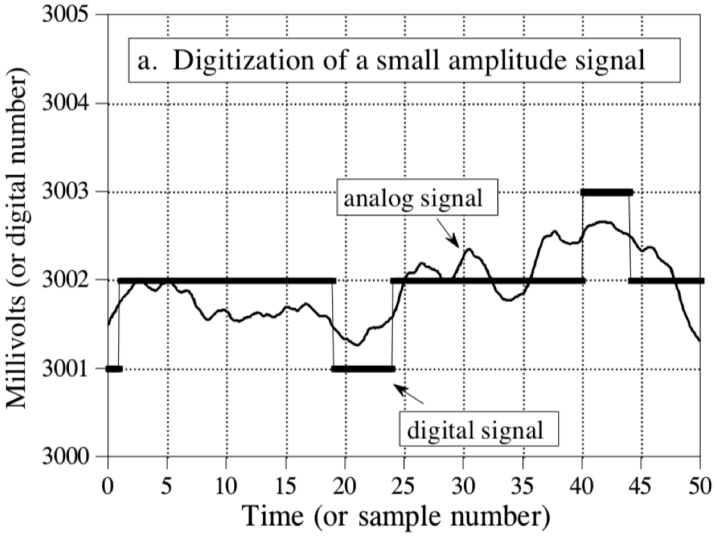
σ_A : SD of random noise in the analog signal

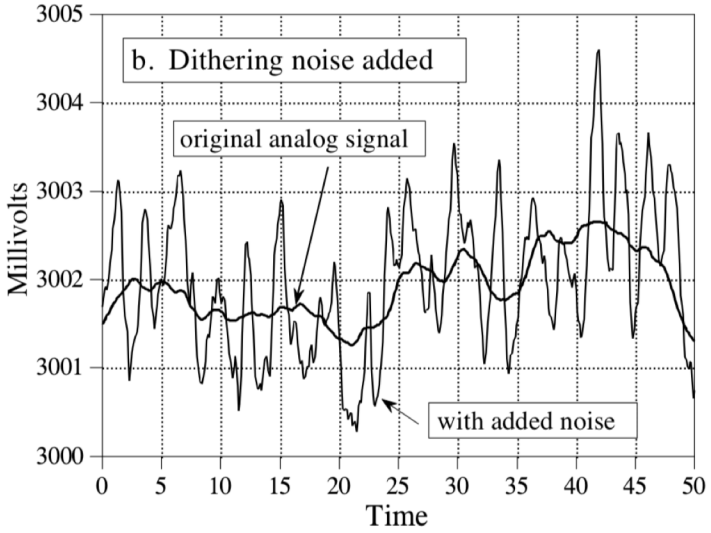
The total noise on the digitized signal

$$\sigma = \sqrt{\sigma_D^2 + \sigma_A^2}$$

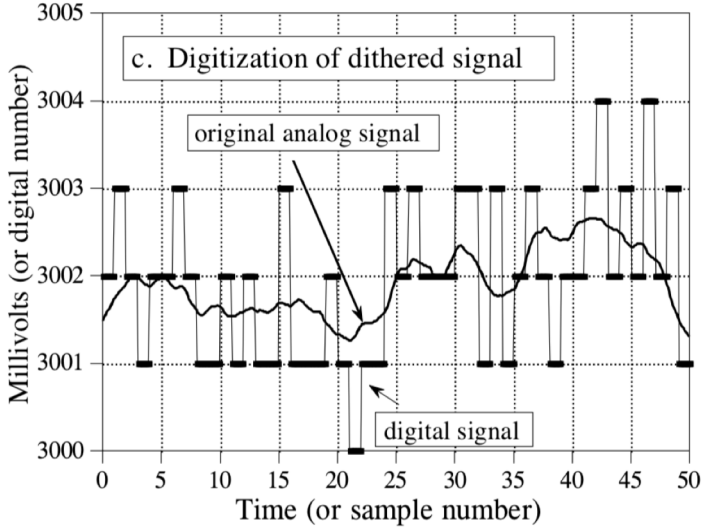
When faced with the decision of how many bits are needed in a system, ask two questions:
(1) How much noise is already present in the analog signal?
(2) How much noise can be tolerated in the digital signal?

An analog signal that varies less than ±1/2 LSB can become stuck on the same quantization level during digitization. **Dithering** is a common technique for improving the digitization of slowly varying signals.





SD of added noise
2/3 LSB

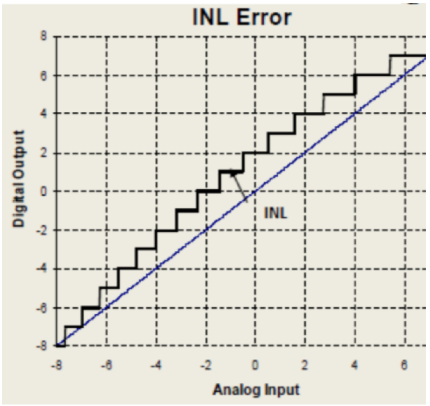


Dithering improves this situation by adding a small amount of random noise to the analog signal.
The added noise causes the digitized signal to toggle between adjacent quantization levels, providing more information about the original signal.

Sampling ADCs

- Bit resolution: 8-14
- Integral non-linearity

  The maximum deviation from this ideal linear behavior.
  A typical absolute value is 0.2−1 LSB.
- Dynamic range: ~2V
- Digitized speed: 40MSPS-1GSPS



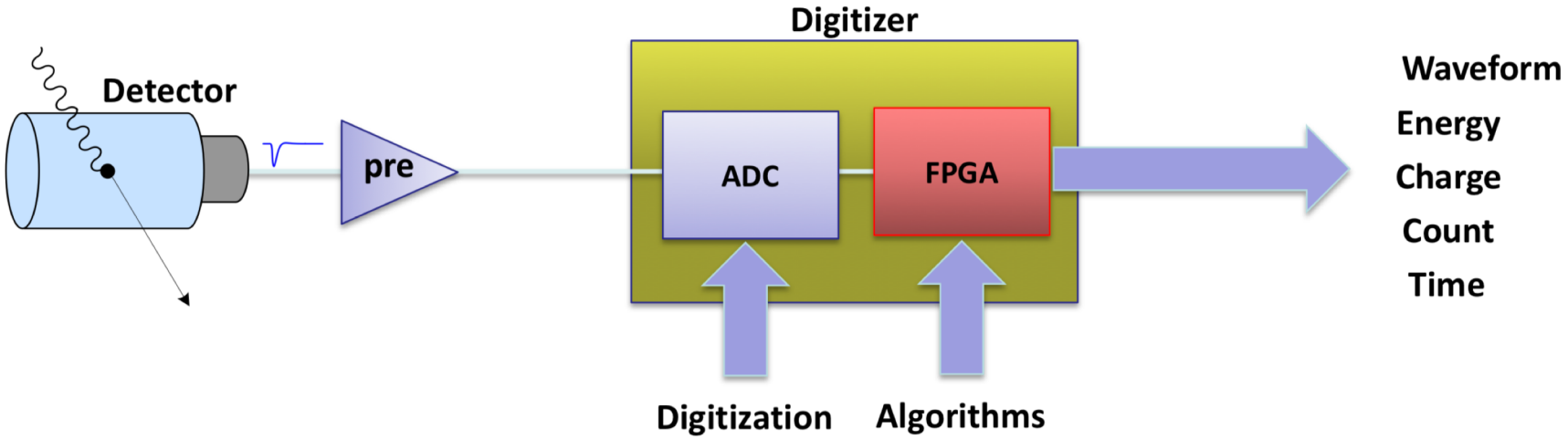
Series	Full scale Range (V)	AMC FPGA(1)	Input Type	Max. Sampling Rate	Bandwidth (MHz)	Resolution (bits)	Memory (MS/ch)
724	± 1.125 /± 5	EP1C4/ EP1C20	Single Ended Differential	100 MS/s	40	14	0.5/4
720	± 1	EP1C4	Single Ended Differential	250 MS/s	125	12	1.25/10
721	± 0.5	EP1C4	Single Ended Differential	500 MS/s	250	8	2
731	± 0.5	EP1C4	Single Ended Differential	0.5-1 GS/s	250/500	8	2-4
740	± 1/± 5	EP3C16	Single Ended	65 MS/s	30	12	0.19/1.5
751	± 0.5	EP3C16	Single Ended Differential	1-2 GS/s	500	10	1.8-3.6/ 14.4-28.8
761	± 0.5	EP3C16	Single Ended Differential	4 GS/s	Tdb	10	7.2/57.6
742(2)	± 0.5	EP3C16	Single Ended	5 GS/s	Tbd	12	0.128

- tradeoff: speed/resolution

Higher sampling rate
-> lower resolution

Typical values for high-speed ADCs are 1−2 bits below the “physical” number of bits.
ENOB(**Effective number of bits**)= 10~11 bits for 12-bit ADC.

Digital signal processing



The aim of the Digital Pulse Processing is to make a “all in digital” version of analog modules such as Shaping Amplifiers, Discriminators, QDCs, Peak Sensing ADCs, TDCs, Scalers, Coincidence Units, etc.

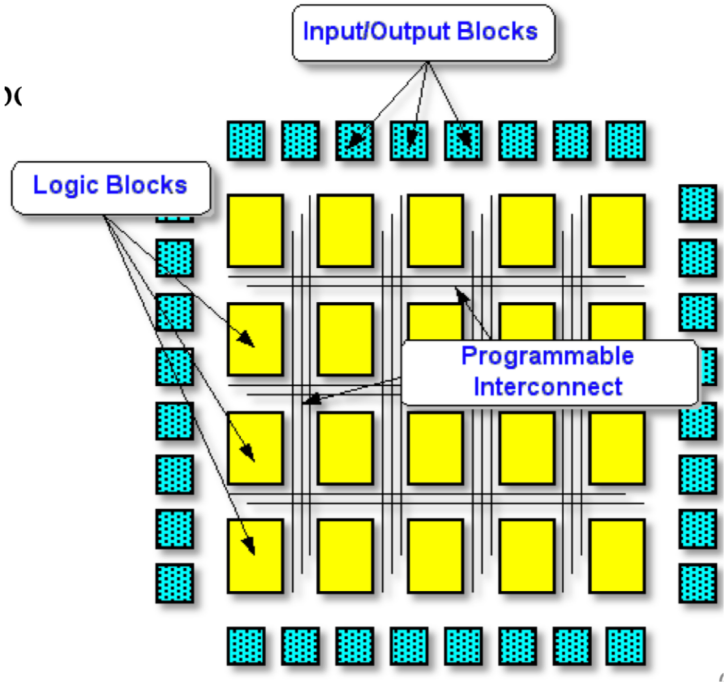
Algorithms: Trigger filter, energy filter, time filter etc.

Field-Programmable Gate Array (FPGA)

•FPGAs are an array of programmable logic cells interconnected by a network of wires and configurable switches.

•A FPGA has a large number of these cells available to form multipliers, adders, accumulators and so forth in complex digital circuits.

•FPGAs can be infinitely reprogrammed in-circuit in only a small fraction of a second.

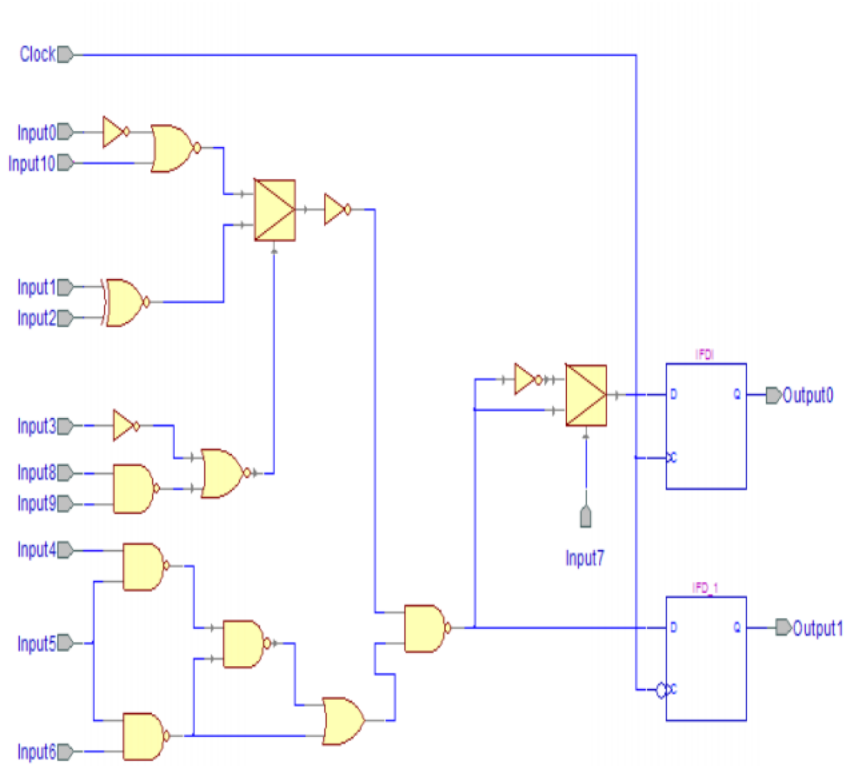


Implement your design using VHDL or Verilog

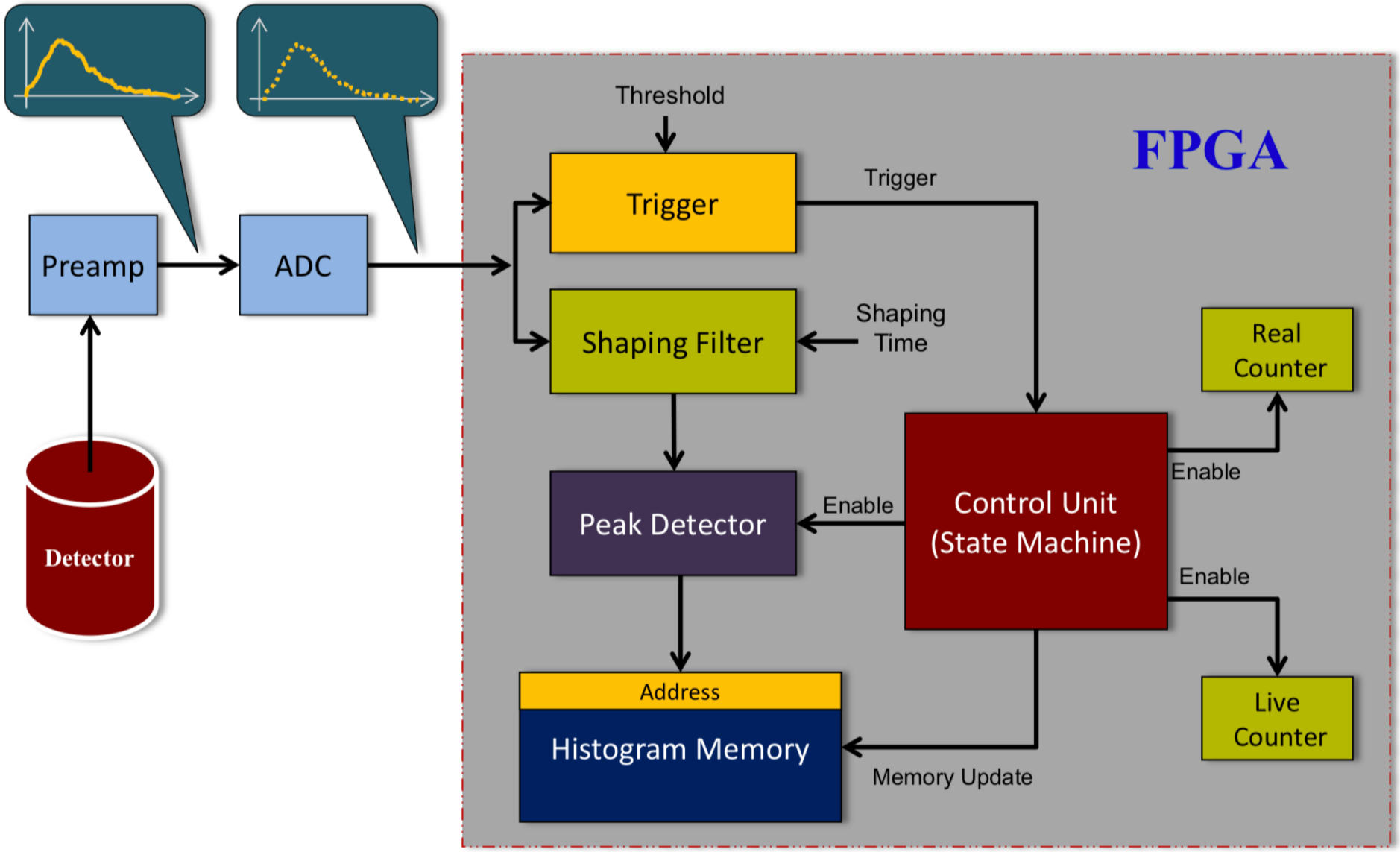
VHDL description

```
architecture MLU_DATAFLOW of MLU is

signal A1:STD_LOGIC;
signal B1:STD_LOGIC;
signal Y1:STD_LOGIC;
signal MUX_0, MUX_1, MUX_2, MUX_3: STD_LOGIC;

begin
                A1<=A when (NEG_A='0') else
                                not A;
                B1<=B when (NEG_B='0') else
                                not B;
                Y<=Y1 when (NEG_Y='0') else
                                not Y1;

                MUX_0<=A1 and B1;
                MUX_1<=A1 or B1;
                MUX_2<=A1 xor B1;
                MUX_3<=A1 xnor B1;

                with (L1 & L0) select
                                Y1<=MUX_0 when "00",
                                                MUX_1 when "01",
                                                MUX_2 when "10",
                                                MUX_3 when others;

end MLU_DATAFLOW;
```

Circuit netlist



Inside the FPGA



Digital Filters

shaper – modification of signal shape(time domain)
Filter – modification of signal bandwidth(frequency domain)
Shaper=Filter

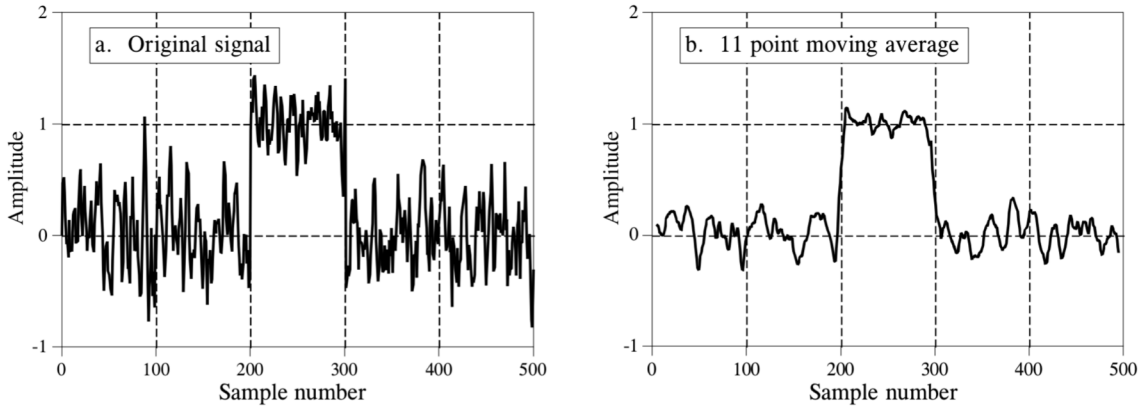
- Analog filters
  - Electronic components are cheap.
  - Large dynamic range in amplitude and frequency.
  - Real-time.
  - Low stability of resistors, capacitors and inductors due to temperature.
  - Difficult to get the components accuracy as calculated by the formula.

- Digital filters:
  - Better performance than analog filters
  - Digital filters are programmable.
  - The characteristics of DSP filters are predictable.
  - Unlike analog filters, the performance of digital filters is not dependent on the environment, such as temperature or voltage
  - In general, complex digital filters can be implemented at lower cost than complex analog filters.

The Moving Average as a Filter

The *moving average* is often used for smoothing data in the presence of noise. It is actually one of the most common filters in signal processing.

The moving average of length N can be defined as $$y[n] \equiv \frac{1}{N} \sum_{i=-N+1}^{0} x[n+i],$$



The filter is usually implemented recursively, in a very efficient way.

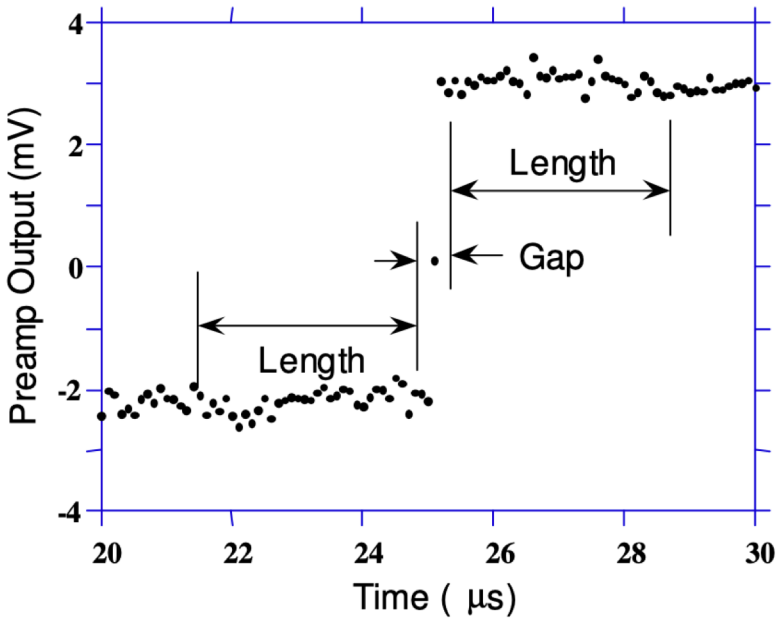
$$y[n] = x[n-N+1]/N + \ldots + x[n]/N$$

$$y[n+1] = x[n-N+2]/N + \ldots + x[n+1]/N,$$

$$\boxed{y[n+1] = y[n] + (x[n+1] - x[n-N+1])/N.}$$

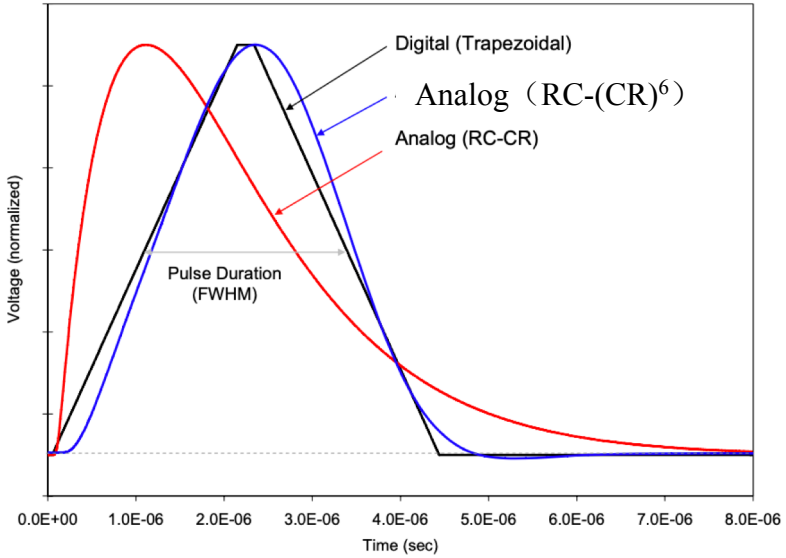
This recursive implementation will be *much* faster than convolution. Each new value of y can be computed with only two additions, instead of the N additions that would be necessary for a straightforward implementation of the definition.

Trapezoidal Filter -Energy



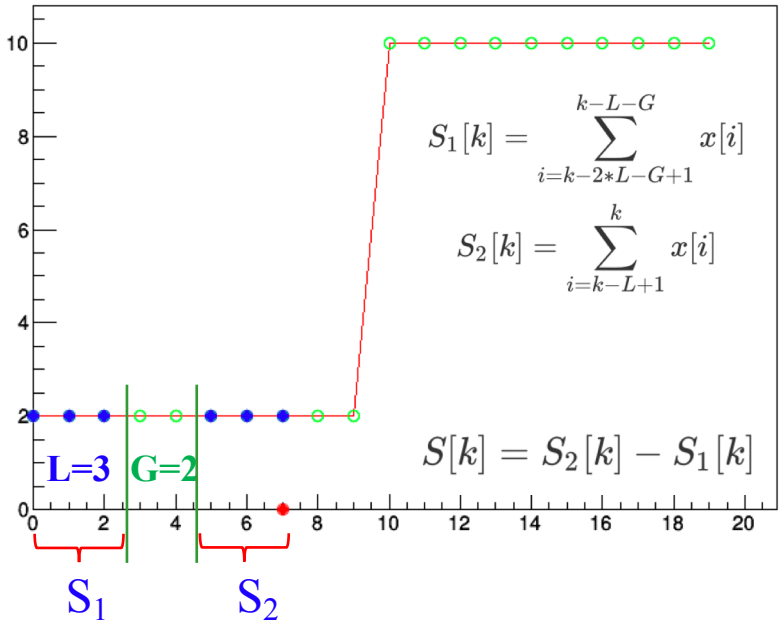
$$V_{x,k} = -\sum_{i(before)} W_i V_i + \sum_{i(after)} W_i V_i$$

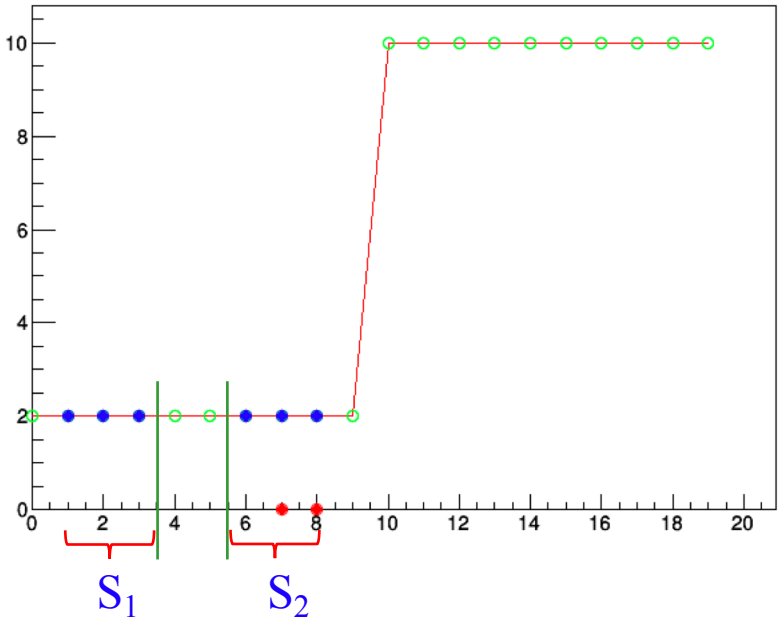
Moving average Moving average

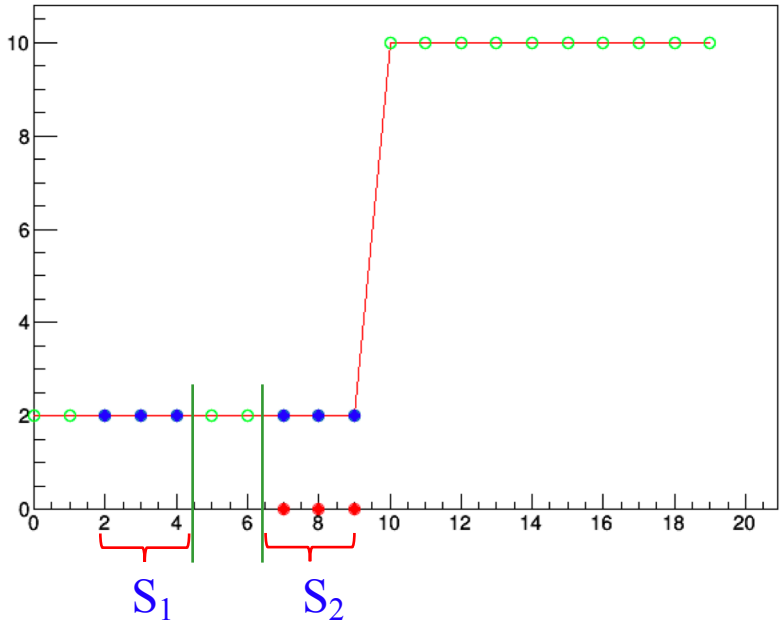


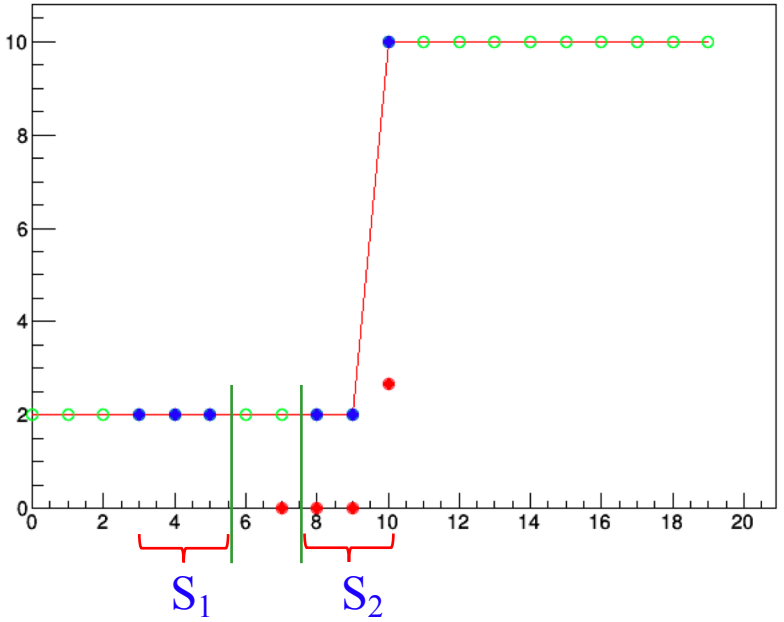
- the digital shaper has less pile-up (even with the same FWHM duration).
- the pile-up timing for the digital system is very clear: due to the pulse symmetry, there is no pile-up after a fixed time.

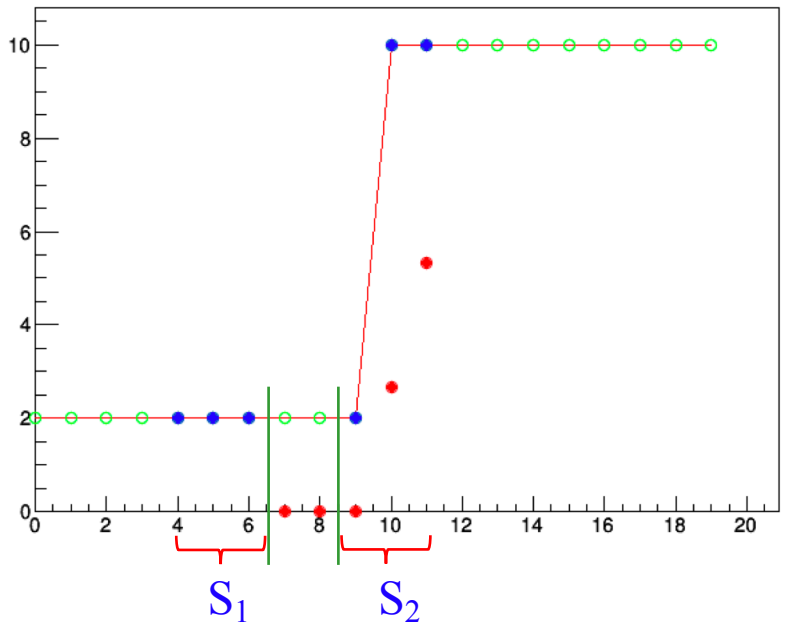
Trapezoidal Filter Algorithm

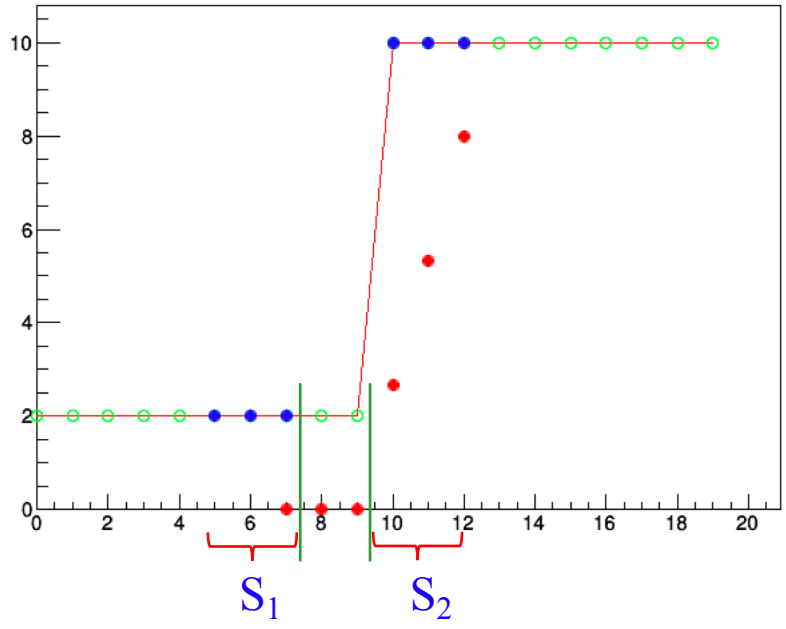


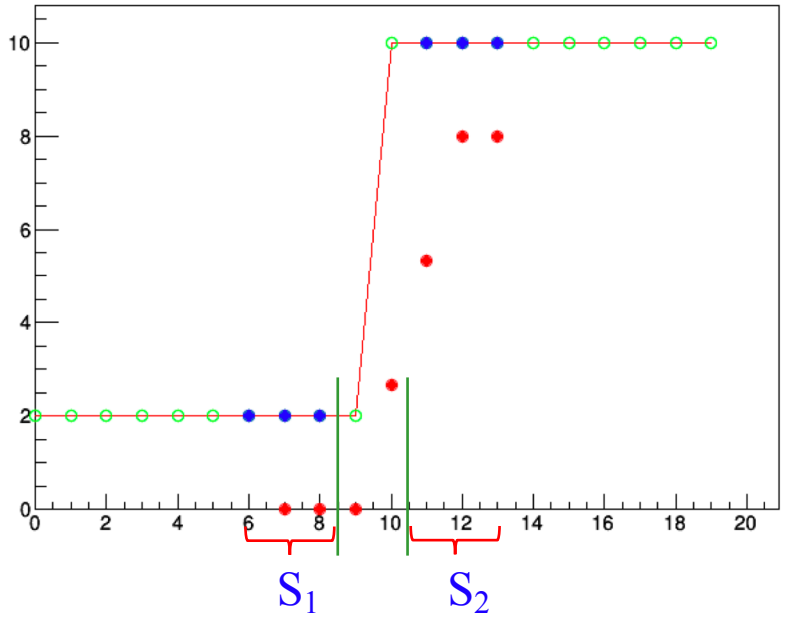


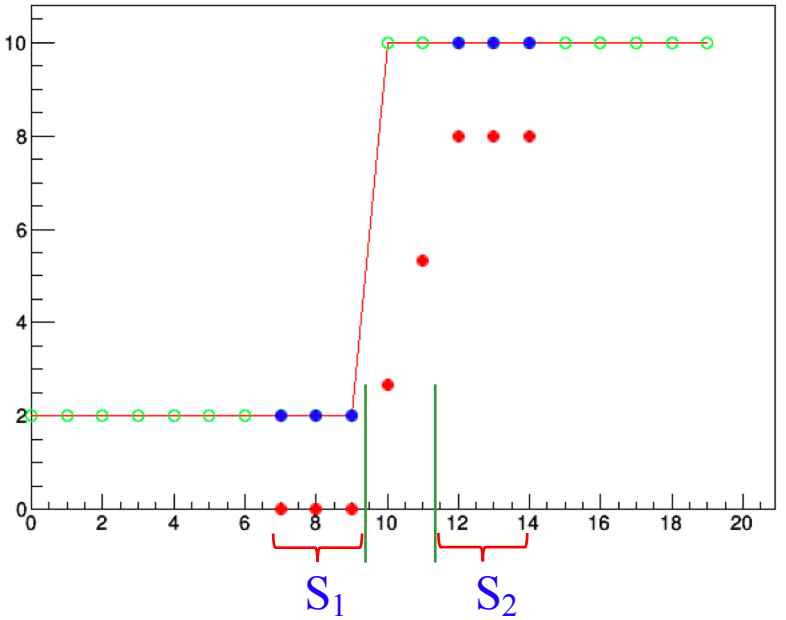


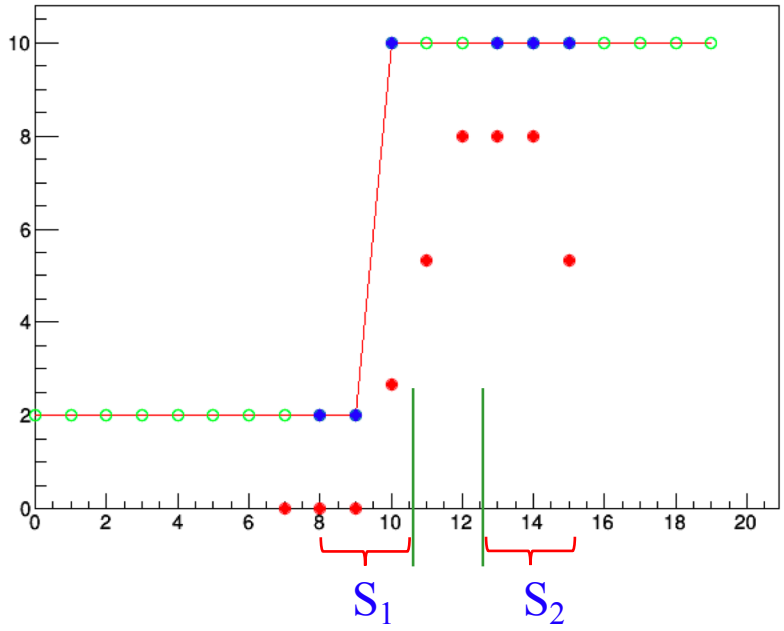


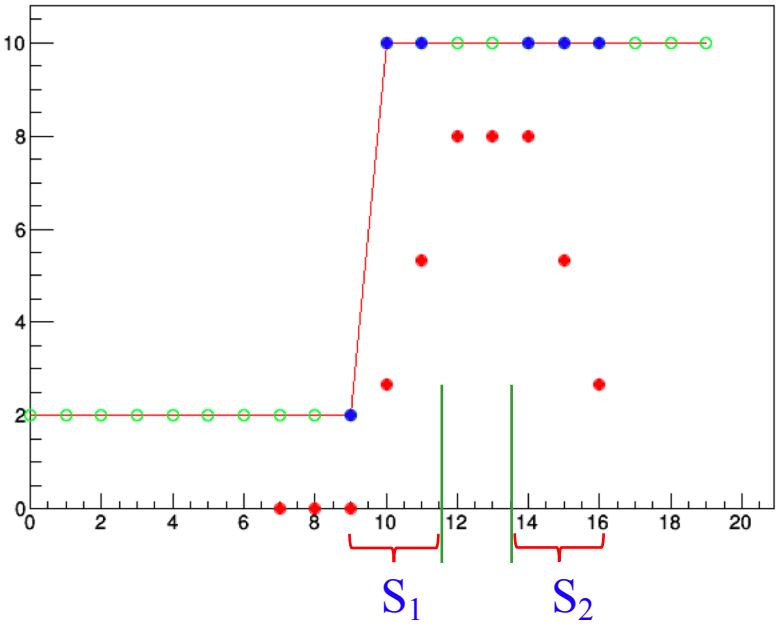

S1
S2


S1
S2


S1
S2


S1
S2


S1
S2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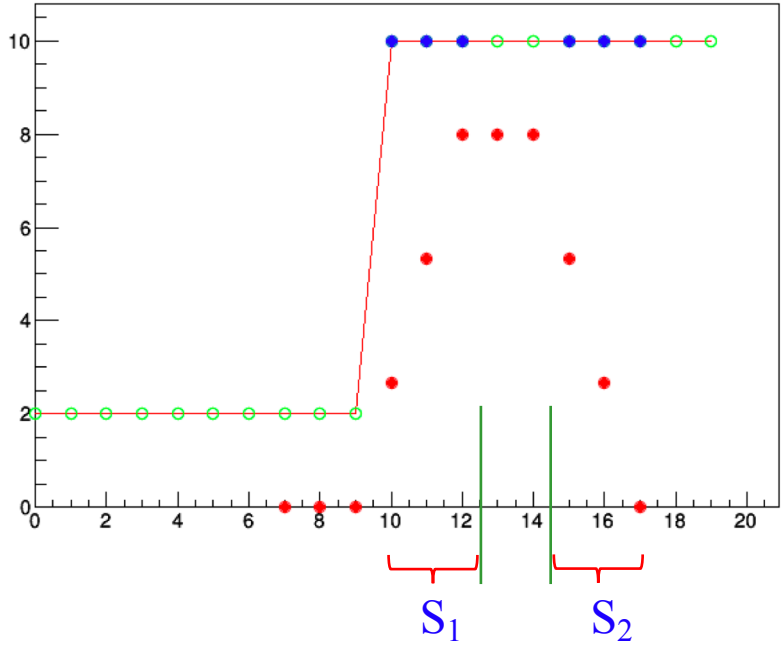
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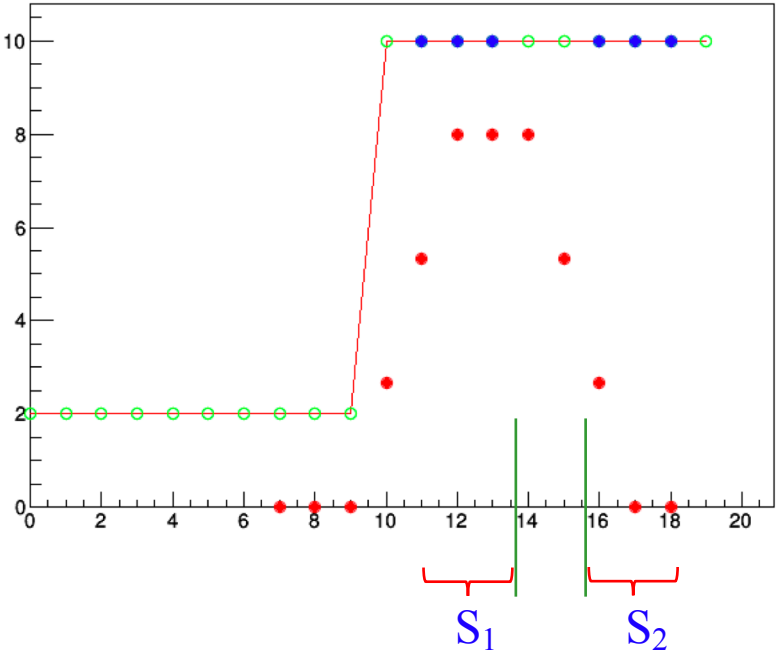
S1
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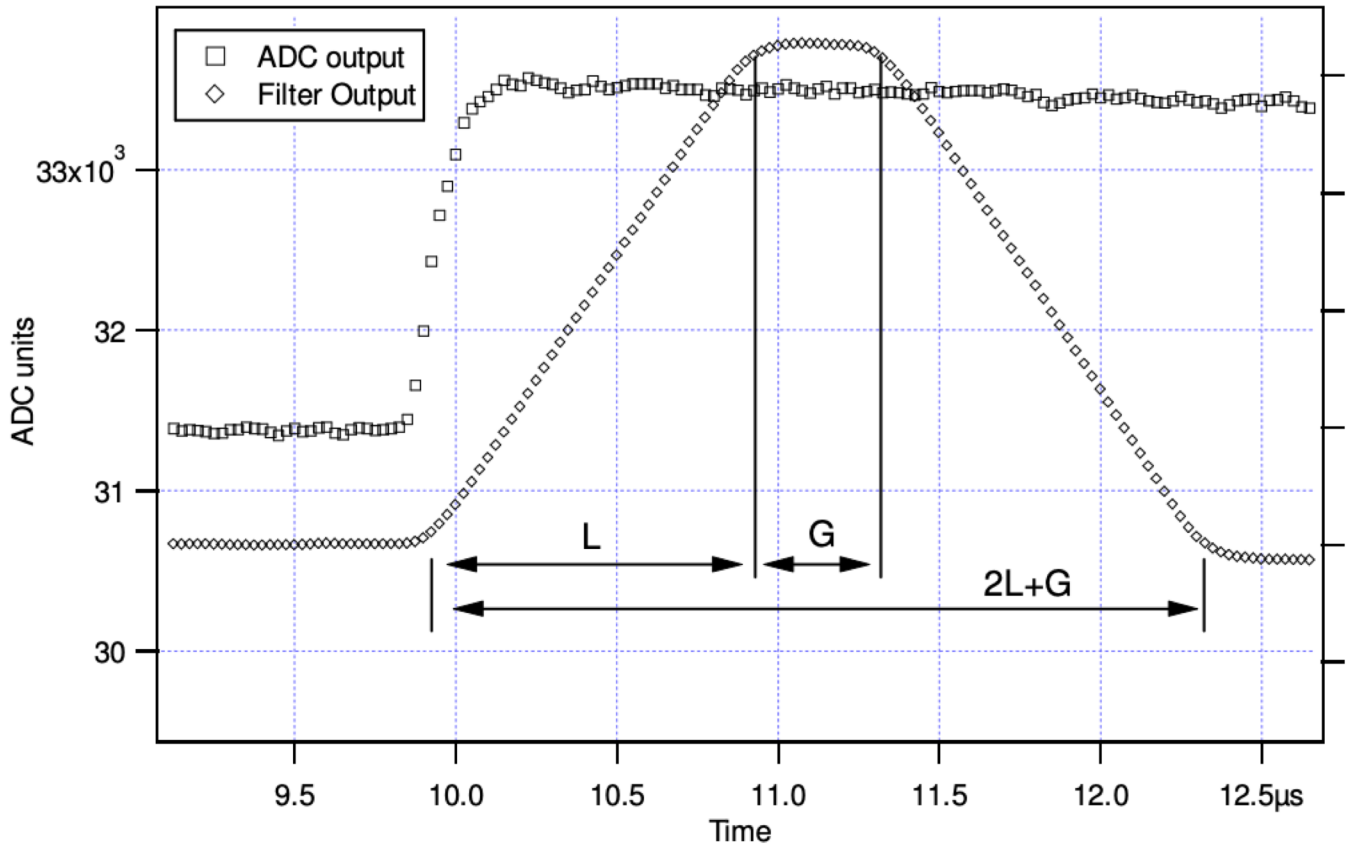


$$S[k] = \sum_{i=k-L+1}^{k} x[i] - \sum_{i=k-2*L-G+1}^{k-L-G} x[i]$$

$$S[k] = S[k-1] + x[k] - x[k-L] + x[k-2*L-G] - x[k-L-G]$$

Preamplifier decay time and Baseline

With a RC-type preamplifier, the slope of the preamplifier is rarely zero.
Every step decays exponentially back to the DC level of the preamplifier.

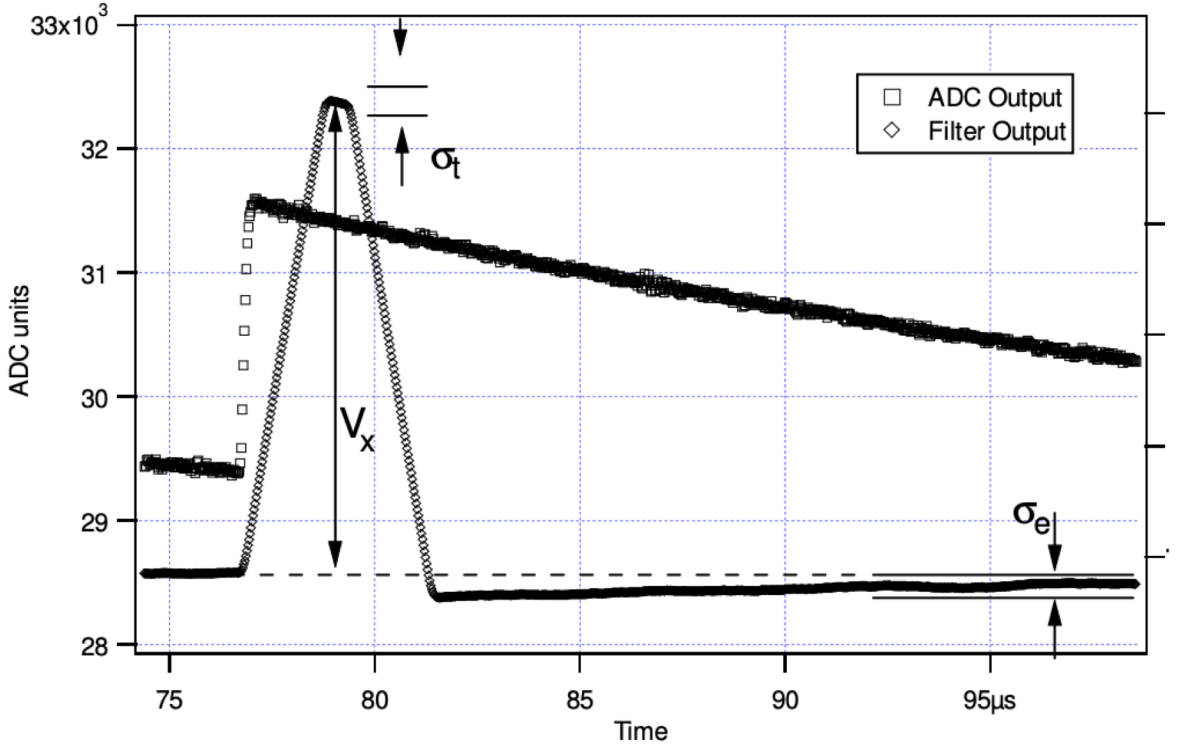


Figure 6.4: A γ-ray event displayed over a longer time period to show baseline noise and the effect of preamplifier decay time.

σ_s : Statistical fluctuation in Q

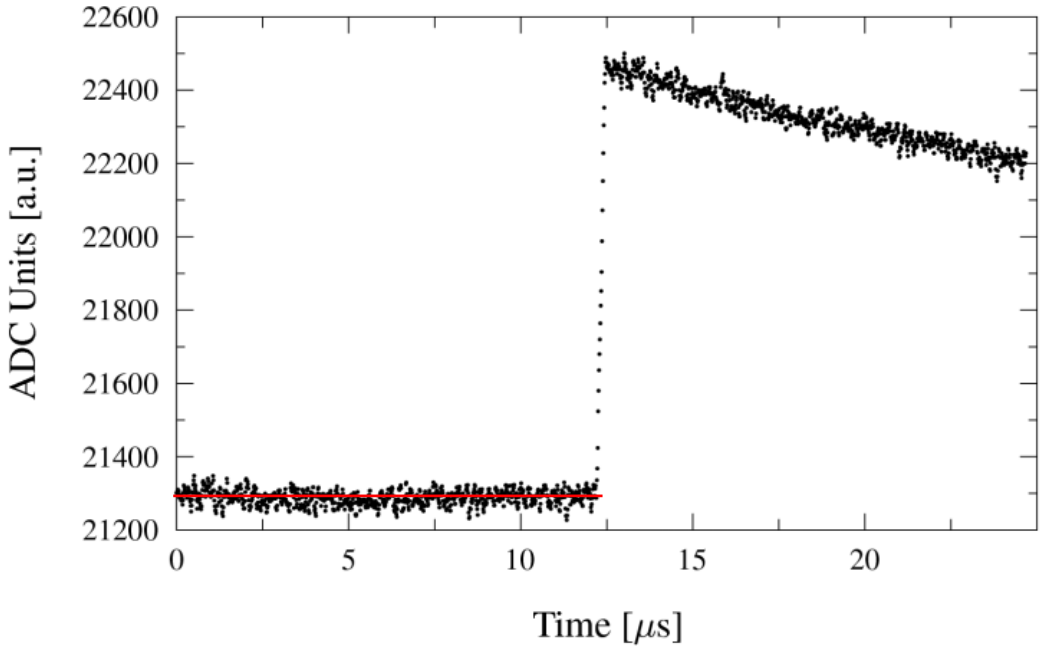
σ_e : Fluctuation in the baseline

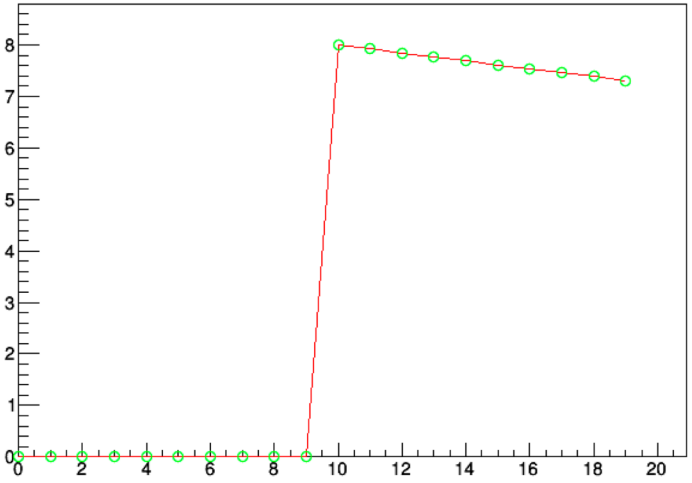
$$\sigma_t^2 = \sigma_s^2 + \sigma_e^2$$

Baseline Correction

The baseline offset can be corrected by calculating the average baseline at the start of the trace (e.g. over first 100 samples) and subtracting that average from the raw signal:

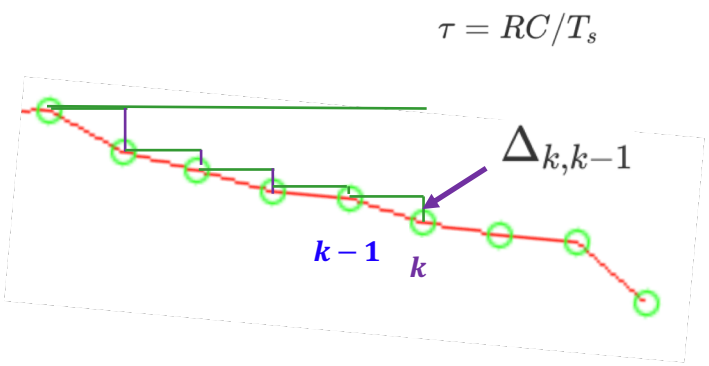
$$x[k] = raw[k] - \frac{1}{100}\sum_{i=0}^{99} raw[i]$$





Pole-Zero Correction

Using the decay constant τ, the baselines can be mapped back to the DC level.
This allows precise determination of energy, even if the pulse sits on the falling slope of a previous pulse.



Offset due to decay time:

$$\Delta_{k,k-1} = x[k] - x[k-1]e^{-1/\tau}$$

$$x'[k] = x[0] + \sum_{i=1}^{k}(x[i] - x[i-1]e^{-1/\tau})$$

$$x'[k-1] = x[0] + \sum_{i=1}^{k-1}(x[i] - x[i-1]e^{-1/\tau})$$

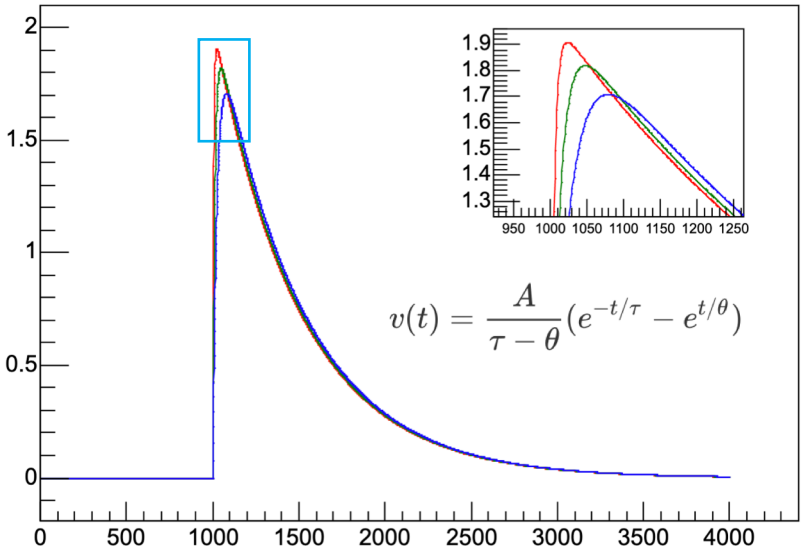
$$x'[k] = x'[k-1] + x[k] - x[k-1]e^{-1/\tau}$$

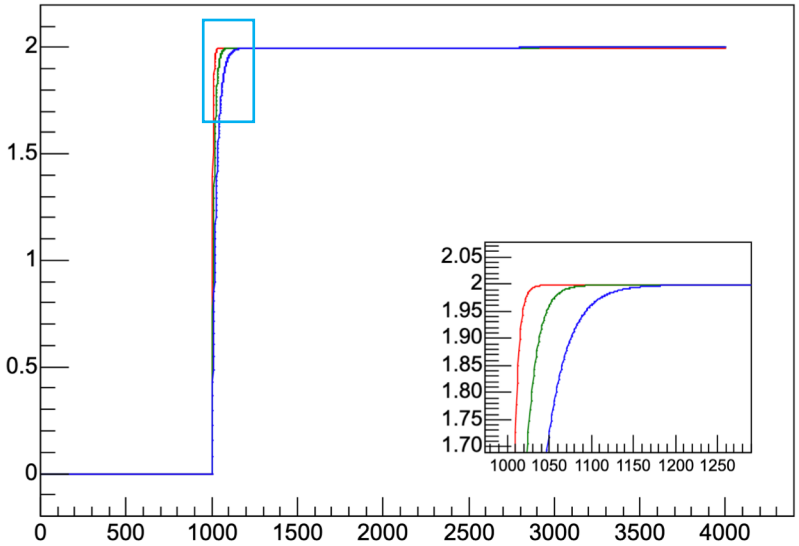
$$x'[k] = x'[k-1] + x[k] - x[k-1](1 - \frac{1}{\tau}) \qquad e^{-1/\tau} \approx 1 - \frac{1}{\tau}$$

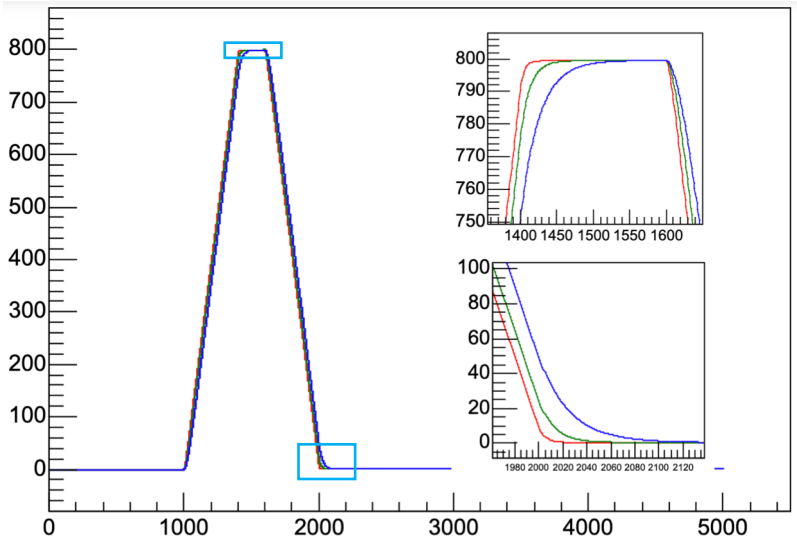
Trapezodial Filter

$$S[k] = S[k-1] + x'[k] - x'[k-L] + x'[k-2*L-G] - x'[k-L-G]$$

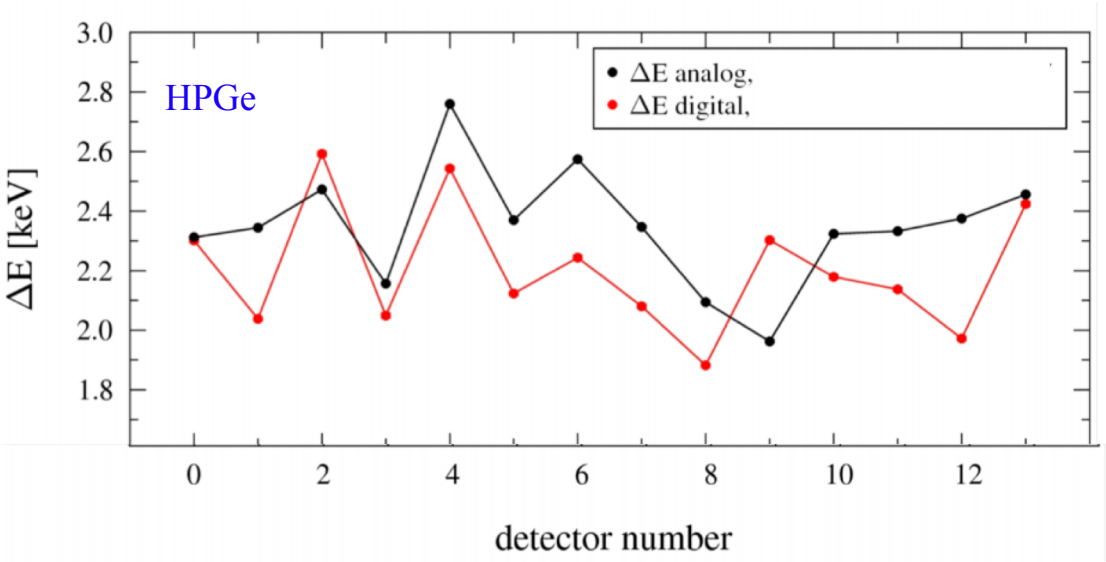
Exponential pulses with different rise time and the corresponding trapezoidal pulse shapes

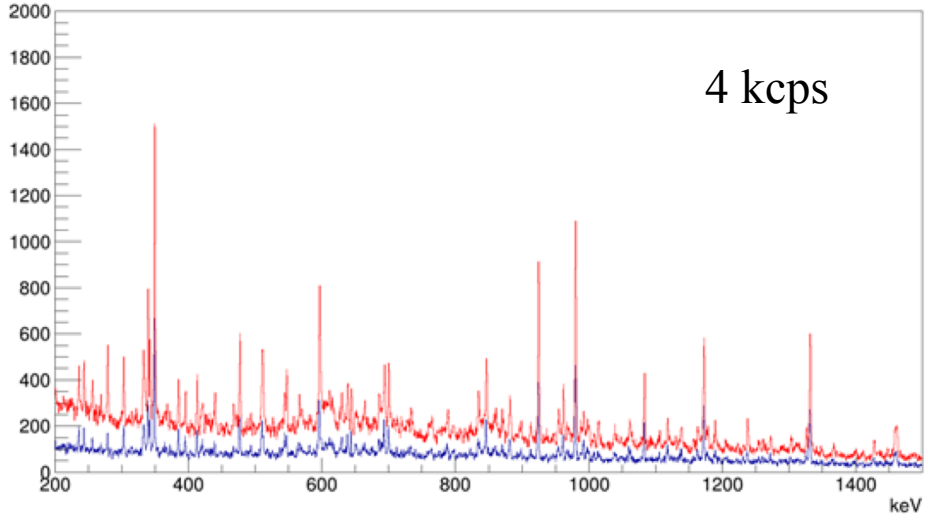


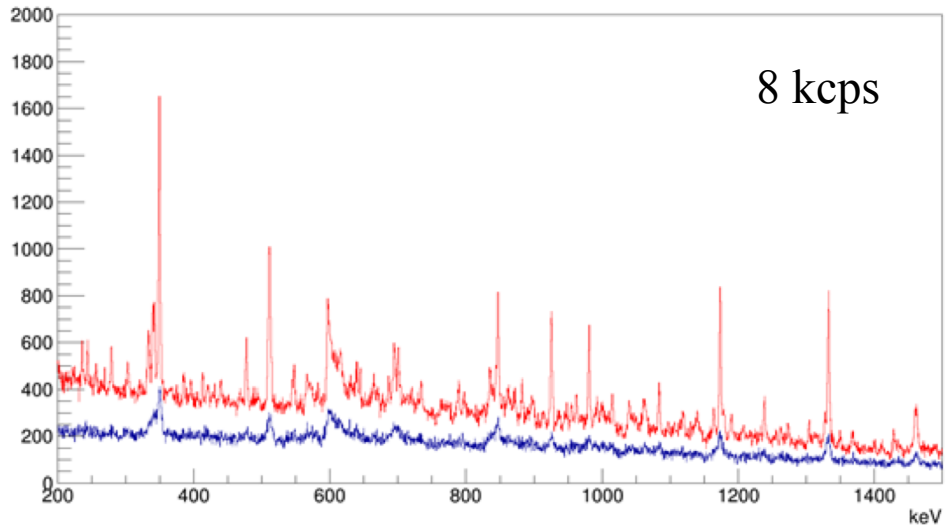




The digital spectroscopy can offer similar or even better energy resolution especially for very high count rates, compare to conventual techniques.







Trigger Filter

- trigger data acquisition
- determine the time window of wave caputure

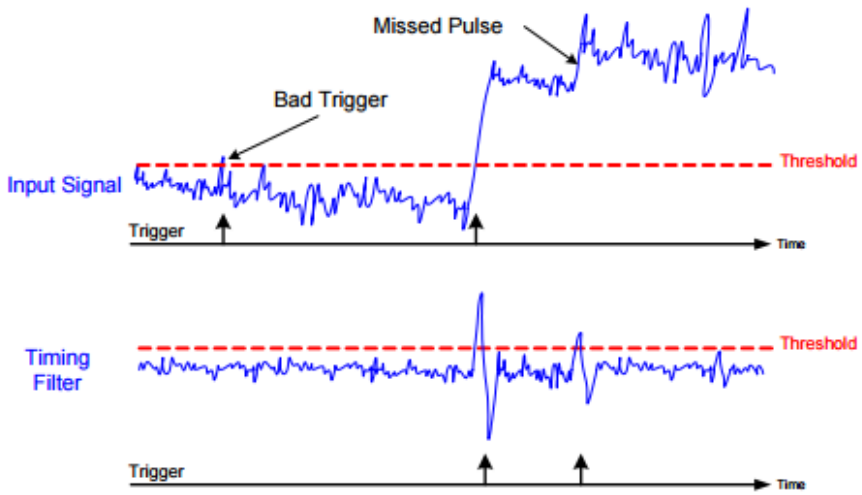
  - time window before/after trigger

Self-trigger for oscilloscopes:

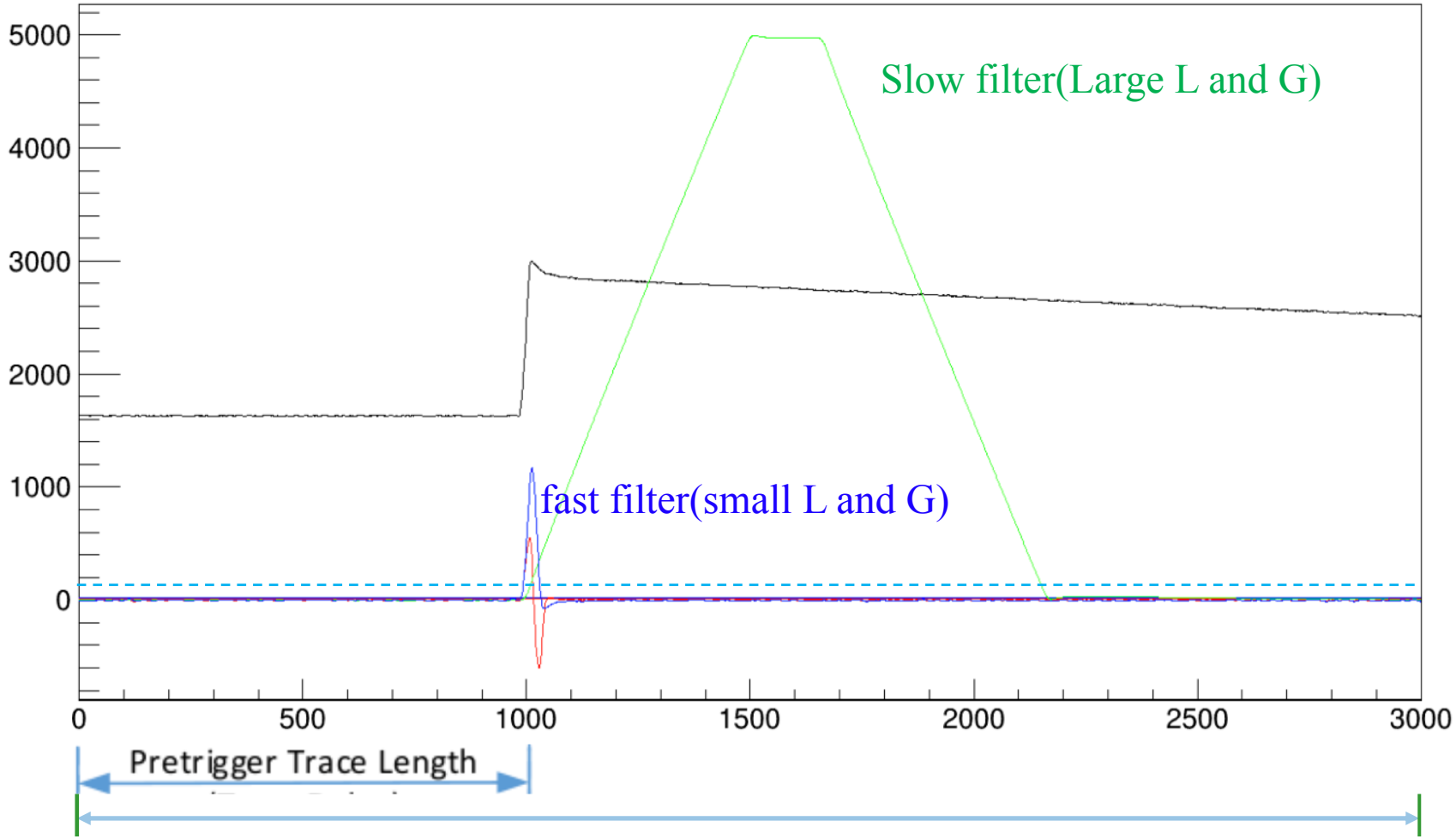
the trigger is generated as soon as the input signal crosses that threshold.

- False triggers from base-line fluctuation or pile-up can cause loss of important events

The digital filters are able to reject the noise, cancel the baseline and to do shape and timing analysis for this purpose.



- Slow filter: Energy determination → filter amplitude
- Fast filter: Time determination → leading edge trigger
  Trigger to select events of interest (e.g. Pile-up rejection)



Trigger Modes(CAEN)

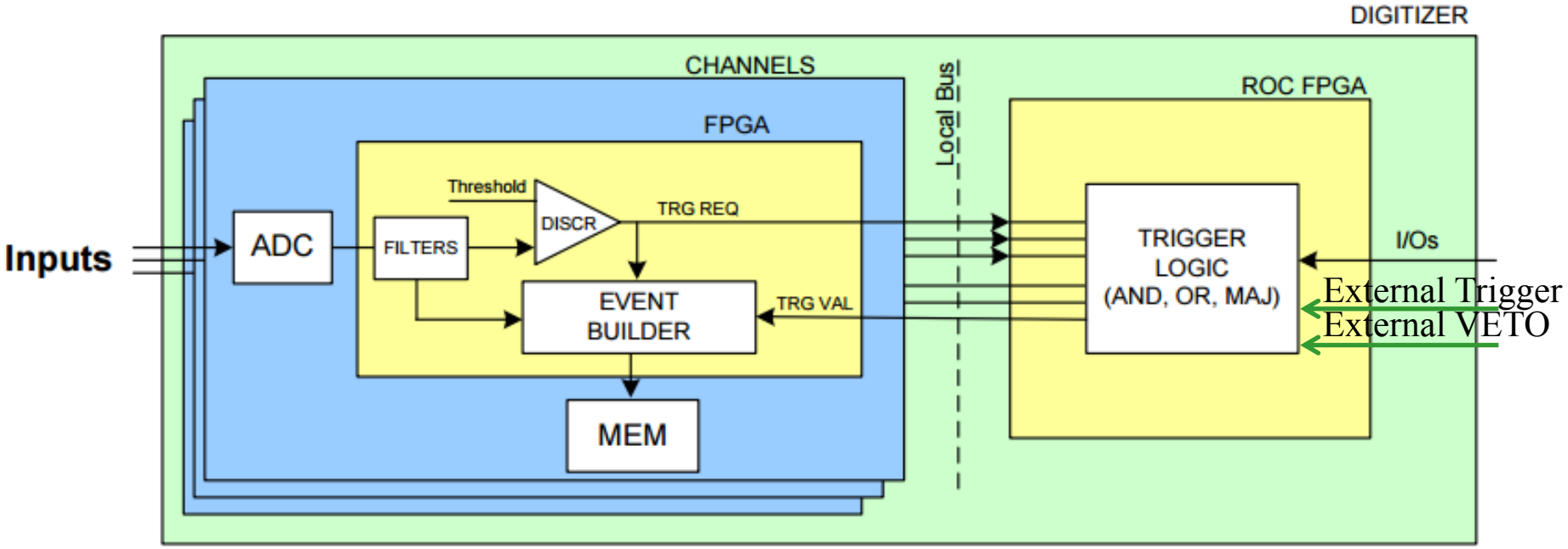


Fig. 4.1: Schematic chain of the trigger architecture of a DPP system

- Each channel has a digital discriminator that generates a **Trigger Request** (TR); the TRs of all channels are combined in the mother board (Mask + AND, OR, Majority) in order to generate a **Trigger**

Digital timing measurements

Trigger filter(default): leading edge discrimination with interrelation

CFD filter：

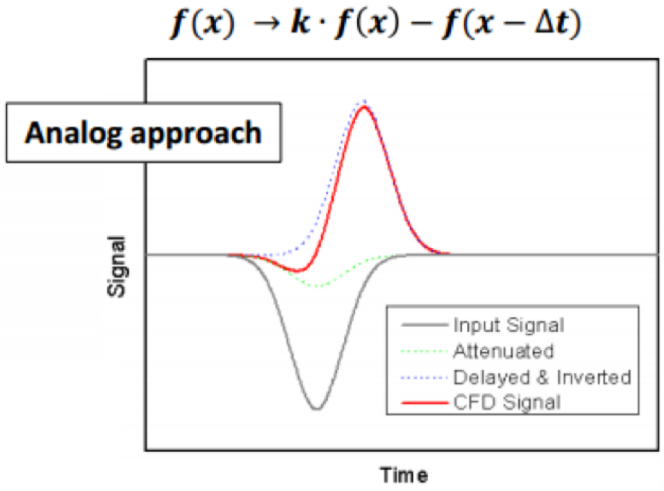
Trace[k]: sample of trigger filter

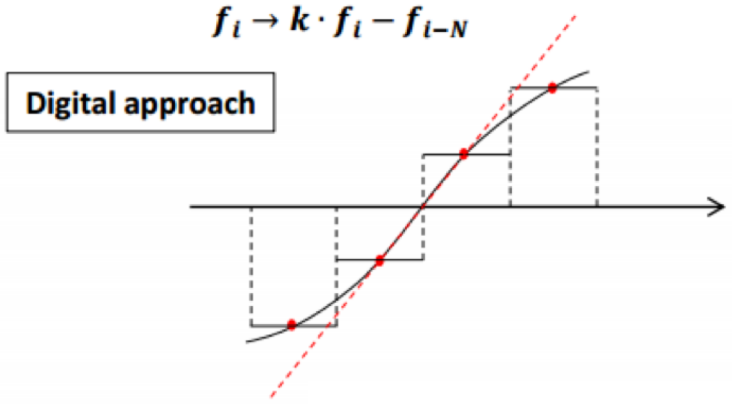
$$\mathrm{CFTrace}[k] = \sum_{i=1}^{L} \{\mathrm{F} * \mathrm{Trace}[k-i] - \mathrm{Trace}[k-i-D]\}.$$

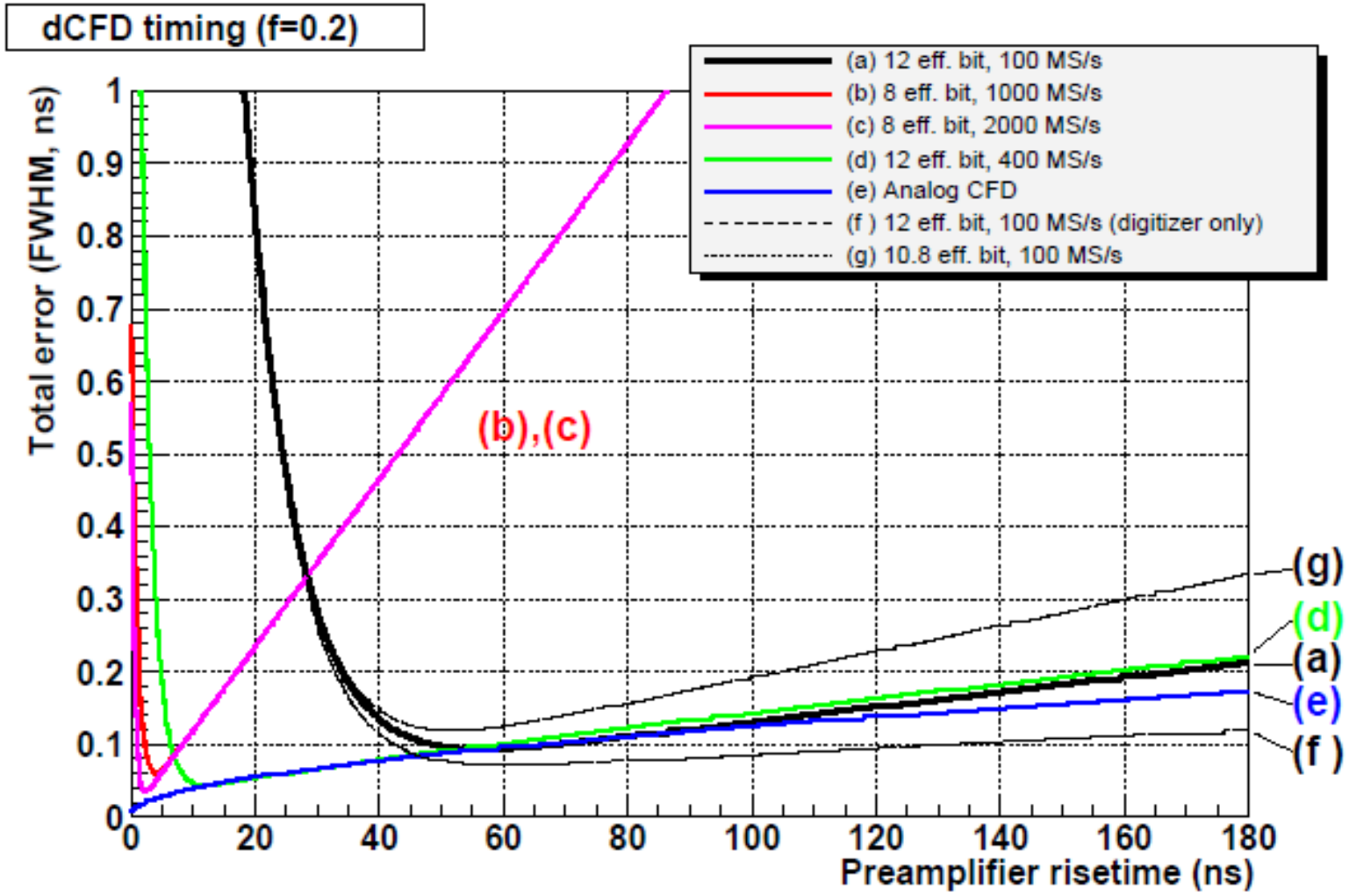
D: time delay

F: fraction

L:The running averaging of length for noise reduction



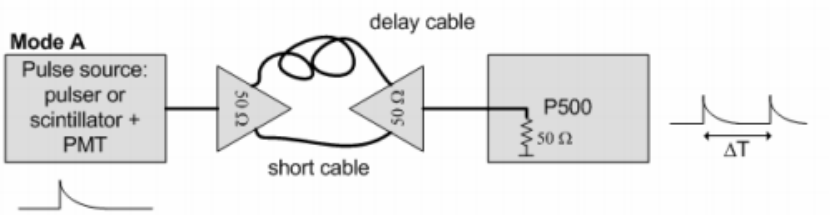




Total error on digital Constant Fraction timing (f =0.2) performed by various digital sampling systems

Fast timing with Digital CFD

12-bit 500MHz flashADC



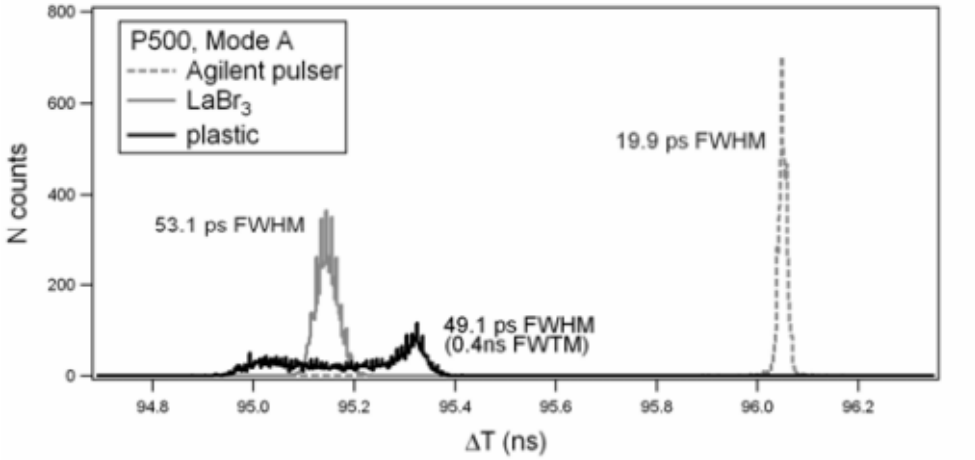
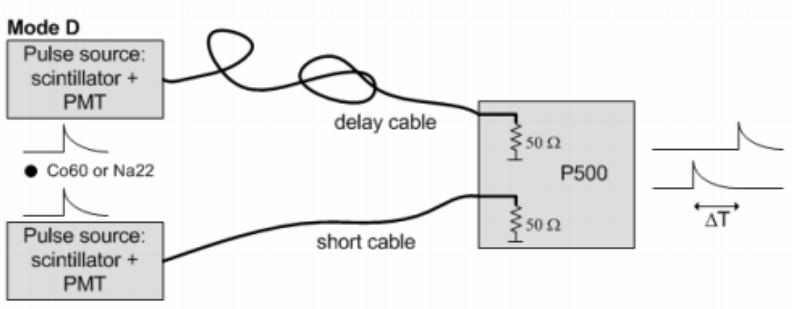


Fig. 8. Histograms of measured time difference ΔT between the two rising edges of a double pulse using P500.



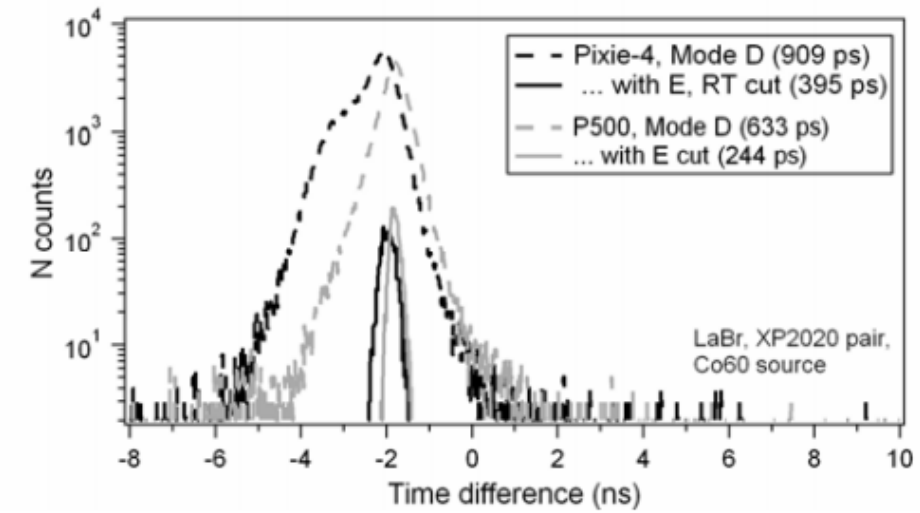
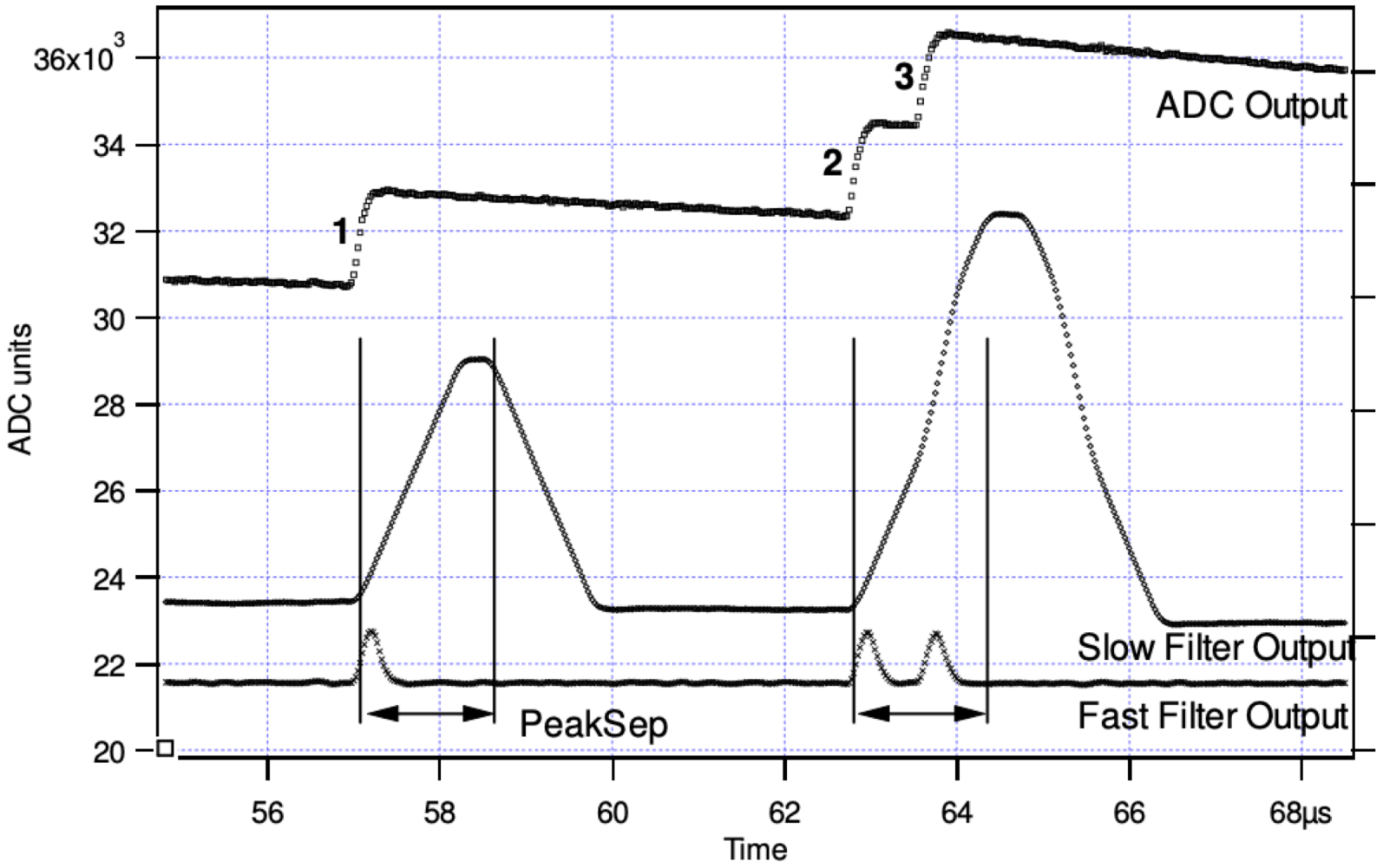


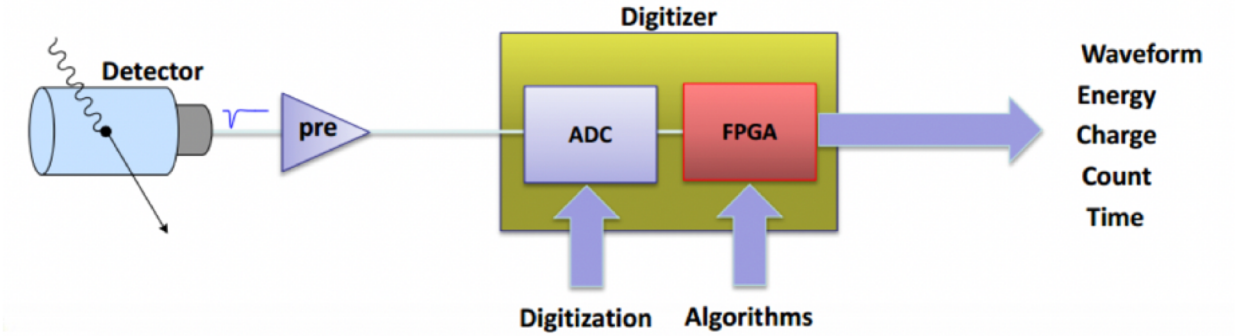
Fig. 11. Histograms of measured time difference ΔT between two coincident ^{60}Co pulses acquired with a pair of $LaBr_3$ crystals and fast PMTs.

http://www.xia.com/Papers/P500_TNS.pdf

Pile-up Rejection



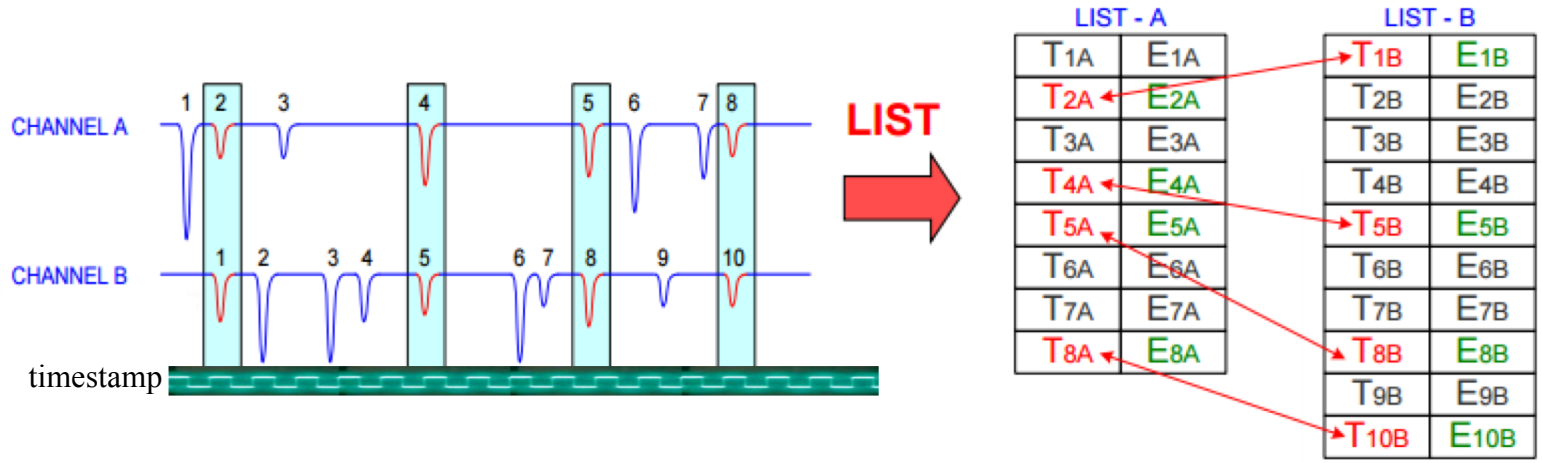
Full digital acquisition chain



The aim of the Digital Pulse Processing is to make a "all in digital" version of analog modules such as Shaping Amplifiers, Discriminators, QDCs, Peak Sensing ADCs, TDCs, Scalers, Coincidence Units, etc.

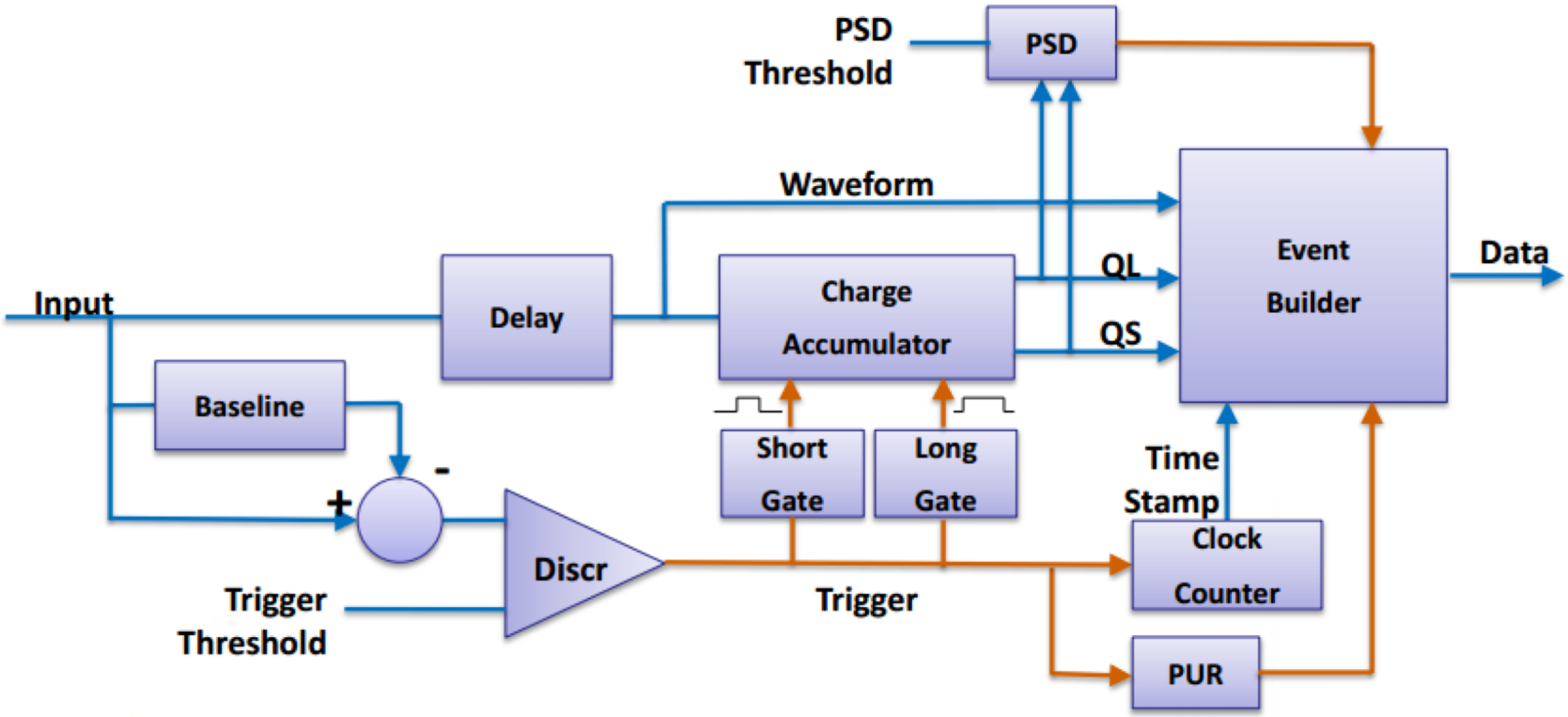
waveform : 500Hz of 1us long traces(12bit) at 100MSPS,

Data stream： ~100kB/second/channel=360MB/hour/channel！



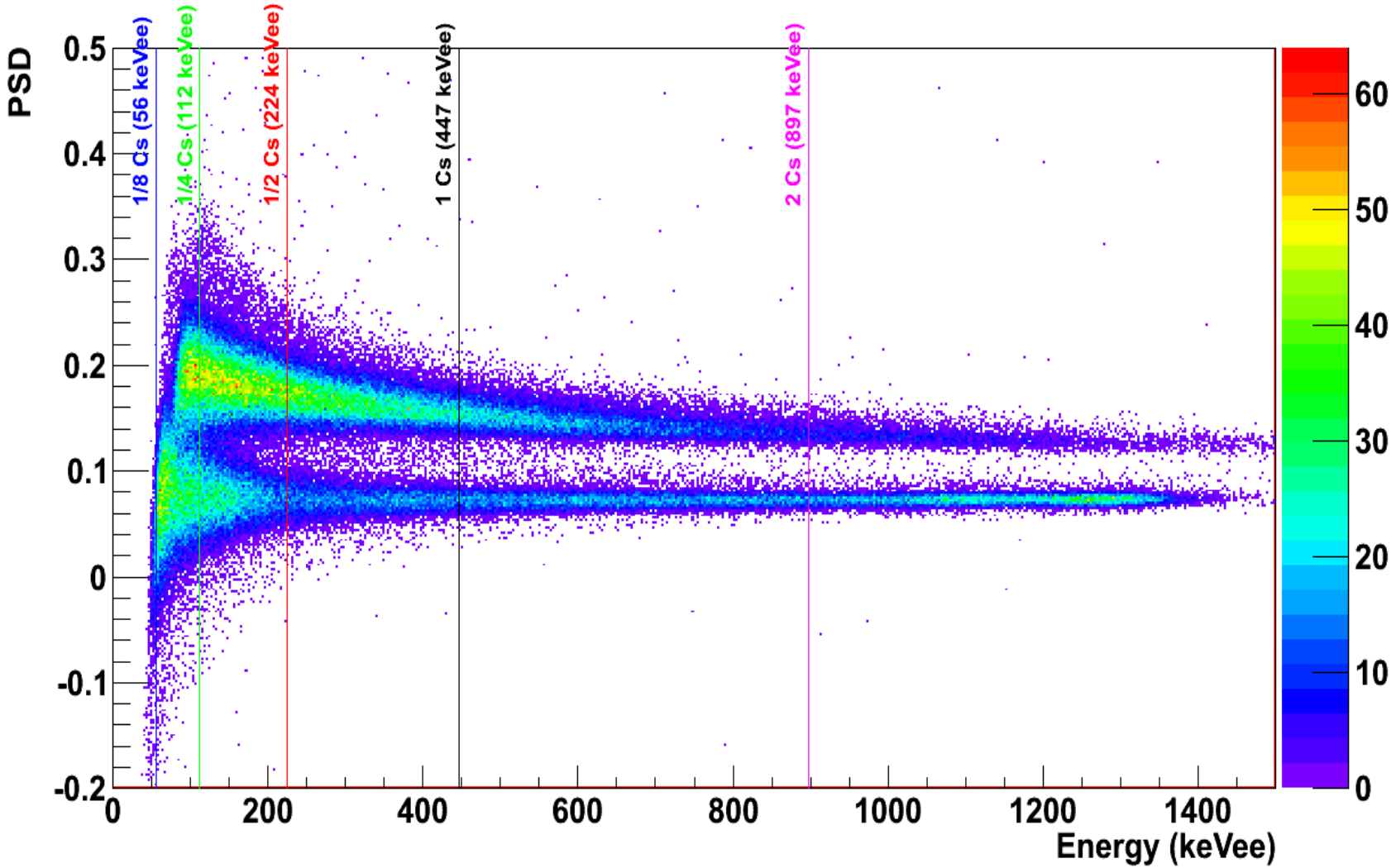
Digital system is implicitly synchronized. Any correlation can be measured with precision only given by the accuracy of the clock

Pulse Shape Discrimination: Block Diagram

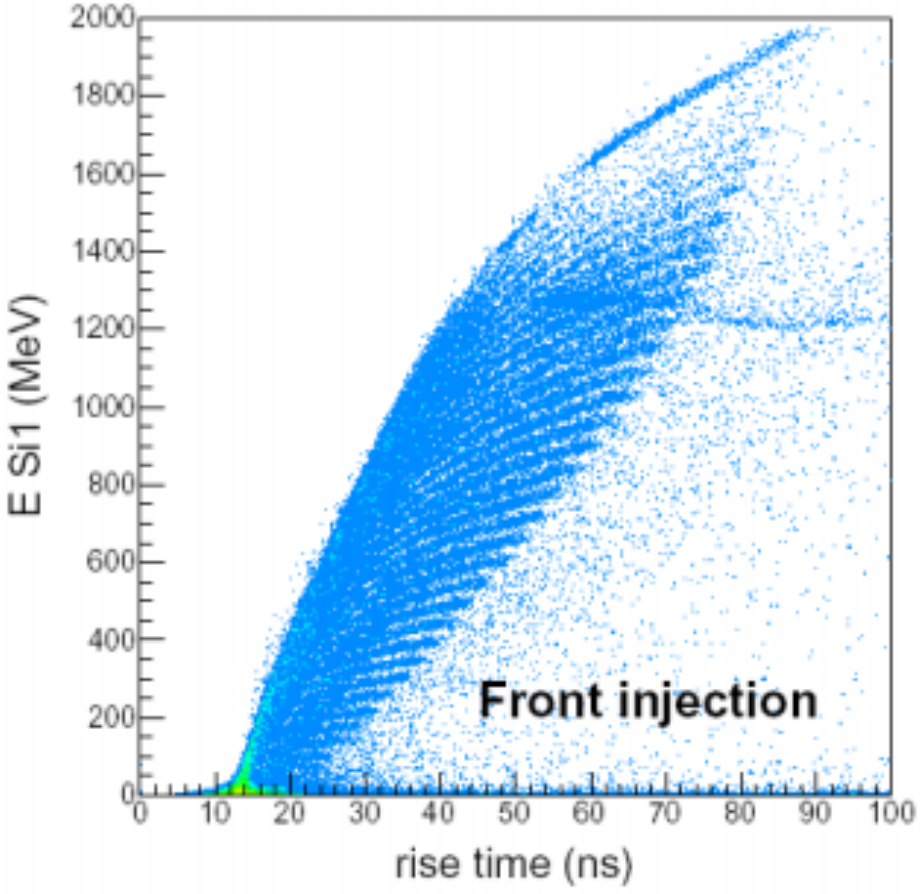


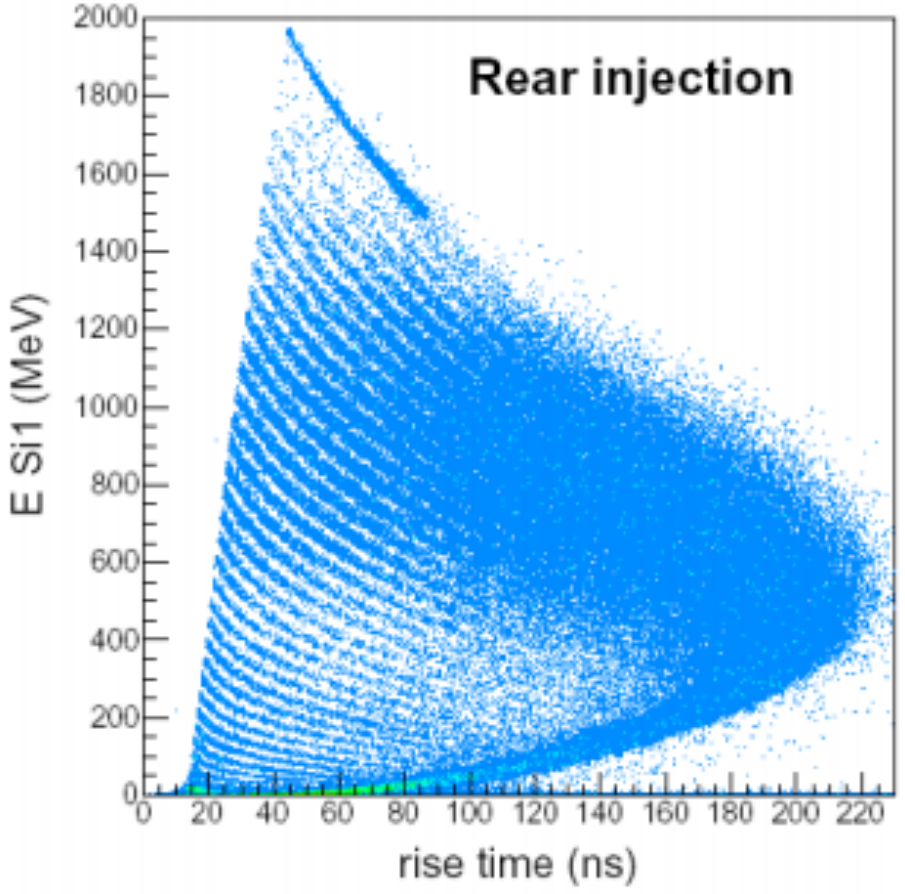
Pulse Shape Discrimination: Block Diagram

γ-n Discrimination: test results



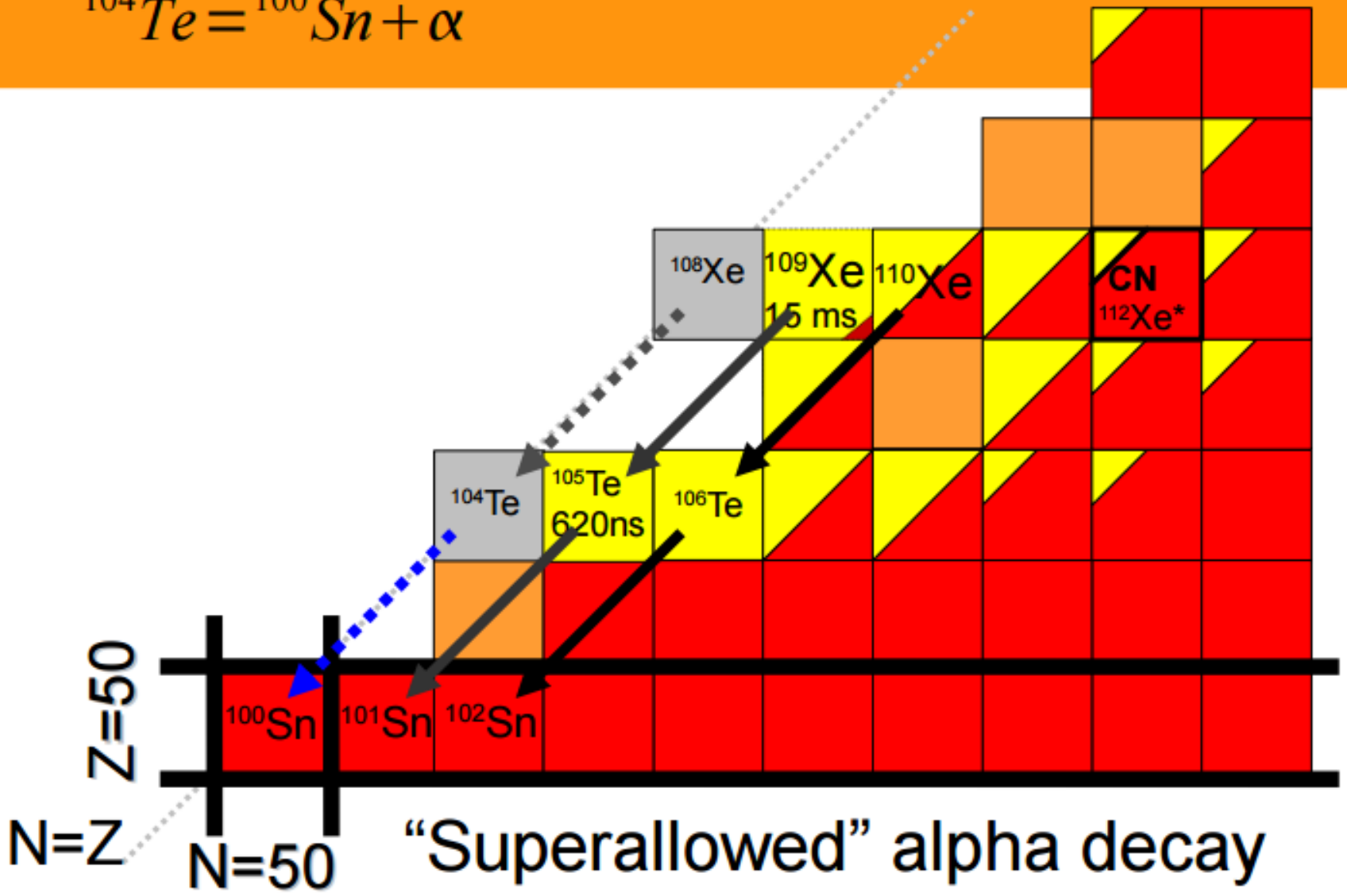
Pulse Shape Discrimination in Silicon



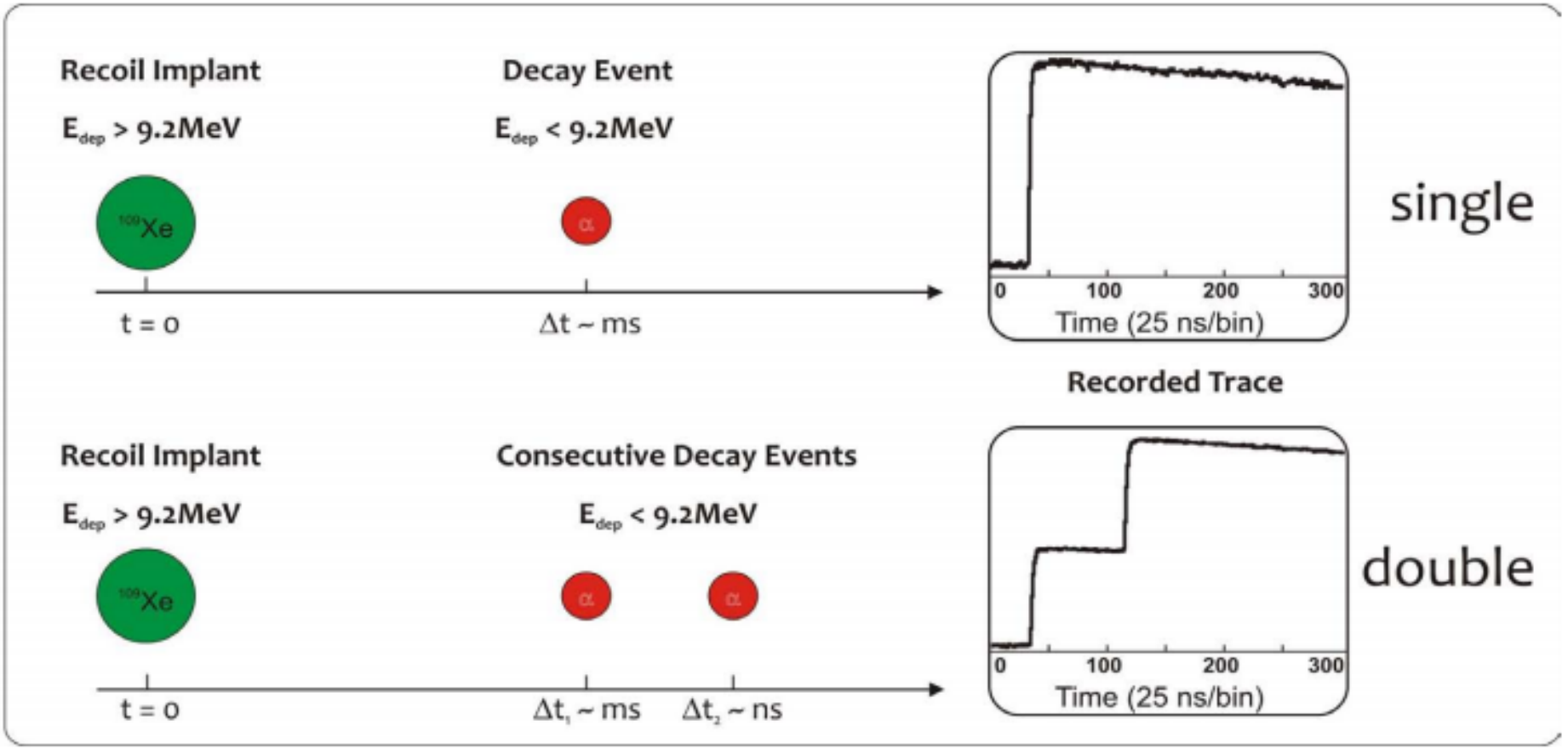


Nuclear molecules?

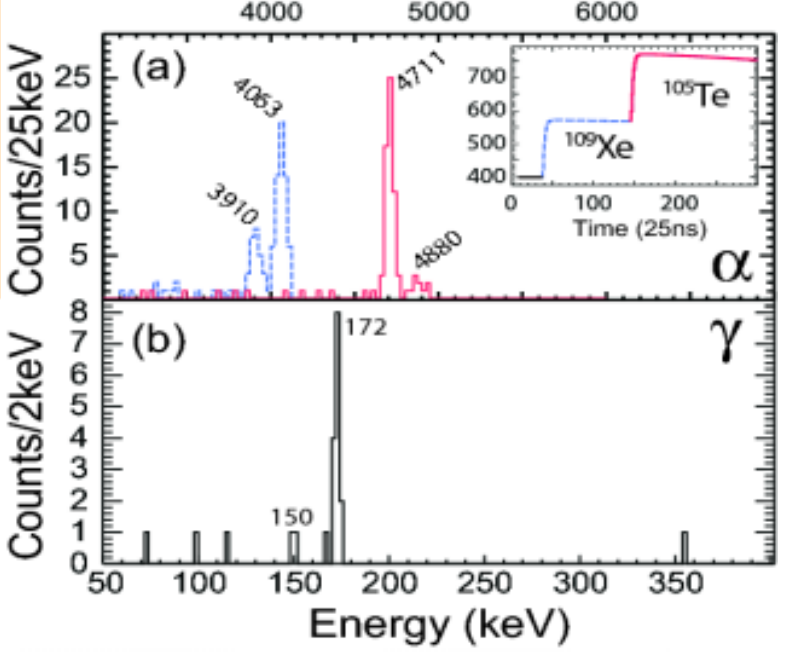
$$^{104}Te = {}^{100}Sn + \alpha$$



Macfarlane and Siivola, PRL 14,114,1965


Recoil Implant
E_{dep} > 9.2MeV
Decay Event
E_{dep} < 9.2MeV
^{109}Xe
α
t = 0
Δt ~ ms
0
100
200
300
Time (25 ns/bin)
single
Recorded Trace
Recoil Implant
E_{dep} > 9.2MeV
Consecutive Decay Events
E_{dep} < 9.2MeV
^{109}Xe
α
α
t = 0
Δt_1 ~ ms
Δt_2 ~ ns
0
100
200
300
Time (25 ns/bin)
double

Experimental results
Main decay path: $^{105}Te \rightarrow {}^{101}Sn^{*}$



13ms

$^{109}Xe_{55}$

E_α = 3910 keV

b_α = 31%

$\Delta l = 0$

E_α = 4063 keV

b_α = 69%

$\Delta l = 2$

E_γ = 150 keV

0.62μs

$^{105}Te_{53}$

E_α = 4711 (4)(10) keV

$\Delta l = 0$

b_α = 89%

E_α = 4880(12)(10) keV

b_α = 11%

$\Delta l = 2$

E_γ = 172 keV

$^{101}Sn_{51}$

To DSP or not to DSP?

Use DSP for …

resolution & throughput optimisation
variable detector pulse shapes

Use analogue signal processing for …

fast shaping
systems not sensitive to, or with fixed, detector pulse shapes
high density (low area, low power) applications

Expect …

ADCs with higher precision, speed & density
lower power & cost

more powerful FPGAs
an expanding range of applications