2021年湖州暑期讲习班

高能物理中的像素探测器及芯片设计

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Pixel Detector in HEP

State-of-the-art and future trends

OUTLINE

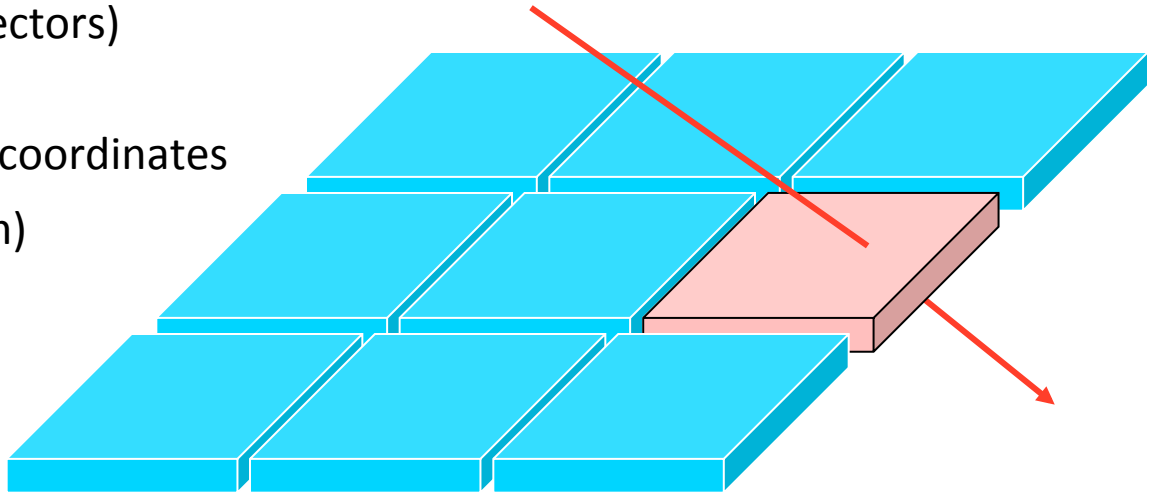
- Use of silicon for the detection of charged particles
- PN diode detector, strip detectors and pixel detector principles
- Hybrid Pixel Detectors
- Hybrid Pixel Detectors at LHC
- Monolithic Pixel Detectors
- Future perspectives

Silicon Pixel Detector

- Solid state detectors
- made of silicon
- in which a passing charged particle or gamma ray produces a signal by ionization
- The 2D-matrix allows recording images or complex multi-particle events.

3.6 eV to generate an electron-hole pair
(compare to ~30eV in gas detectors)

- 2D matrix => unambiguous coordinates
- high granularity (10 – 50 µm)
- High speed
- High efficiency



Efficiency of silicon as detection medium

Silicon vs gas in terms of signal yield and material thickness

Gas	Z	A	Density 10^{-3} (g/cm^3)	E_x (eV)	E_i (eV)	w_i (eV)	$[dE/dx]_{mip}$ (keV cm^{-1})
He	2	2	0.178	19.8	24.5	41	0.32
Ar	18	39.9	1.782	11.6	15.7	26	2.44
Ne	10	20.2	0.90	16.6 7	21.56	36.3	1.56
Xe	54	131.3	5.86	8.4	12.1	22	6.76
CF_4	42	88	3.93	12.5	15.9	54	7
DME	26	46	2.2	6.4	10.0	23.9	3.9
CO_2	22	44	1.98	5.2	13.7	33	3.01
CH_4	10	16	0.71	9.8	15.2	28	1.48
C_2H_6	18	30	1.34	8.7	11.7	27	1.15
i-C_4H_{10}	34	58	2.59	6.5	10.6	23	5.93

E_x ≡ excitation potential

E_i ≡ ionization potential,

w_i ≡ mean energy for ion-electron creation

Silicon density: 2.33 gcm^{-3}

Silicon: ~ 60-80 e-h pairs / µm
Argon: ~ 9.3 x 10^{-3} e-ion pairs /µm

Silicon / Argon (signal): ~ 7 x 10^3

X_0 (Silicon): 9.4 cm
X_0 (Argon): 11 x 10^3 cm

Argon / Silicon (X_0): 1.25 x 10^3

Silicon / Argon (signal) x Silicon / Argon(X_0): 5.6

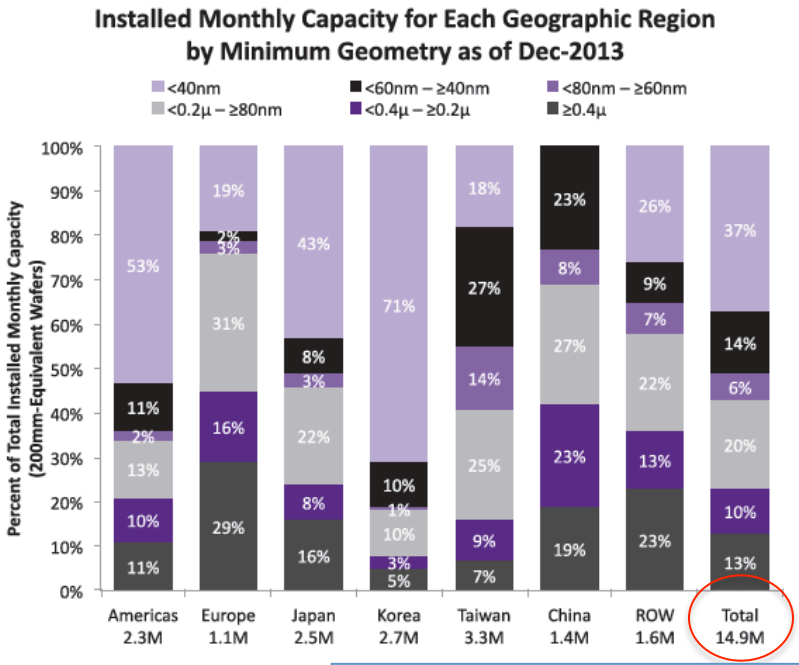
Silicon in industry

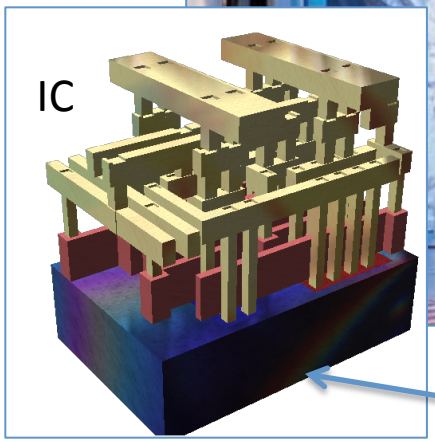
Monocrystalline silicon

main semiconductor used for the fabrication of Integrated Circuits (substrate)

Monocrystalline, high purity single crystals (Czochralski)

CMOS sub-micron fabs





~3.5$ / cm^2

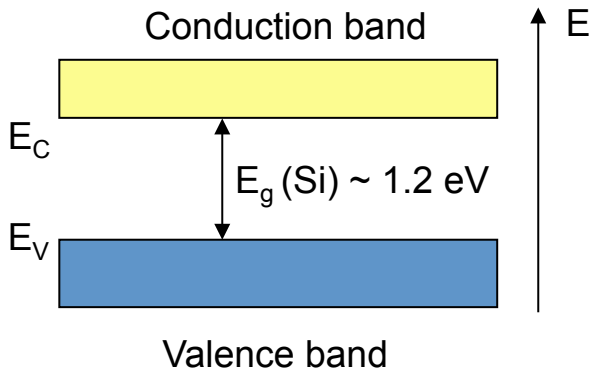
180 Million wafers / year

~ 9 x 10^6 m^2

Silicon properties

Bandgap energies for different materials at room temperature

Si	1.12eV
Ge	0.67eV
GaAs	1.42eV
Diamond	5.5eV

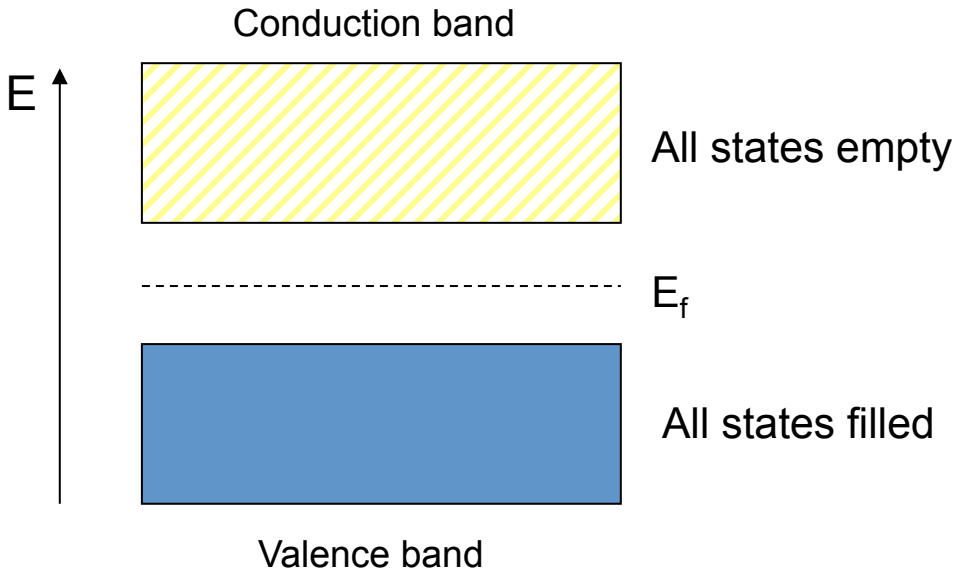


The band gap energy changes with temperature: E_g (Si) at 0K is 1.17eV

Note: in reality the band structure is more complex, depending on crystal momentum, crystal orientation, etc.

Silicon Properties

At absolute zero (-273.15°C)



E_f … Fermi Energy

If an electrical field is applied to the crystal no current can flow as this would require an electron to acquire energy. This is not possible because no higher energy states in the valence band are available.

At higher temperatures

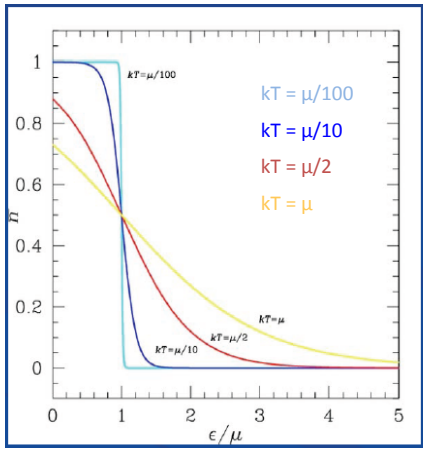
Electrons can gain energy due to thermal excitation

Probability that an electronic state is occupied by an electron follows the Fermi-Dirac statistics

$$F(E) = \frac{1}{1 + e^{(E - E_F)/kT}}$$

k ... Boltzmann constant

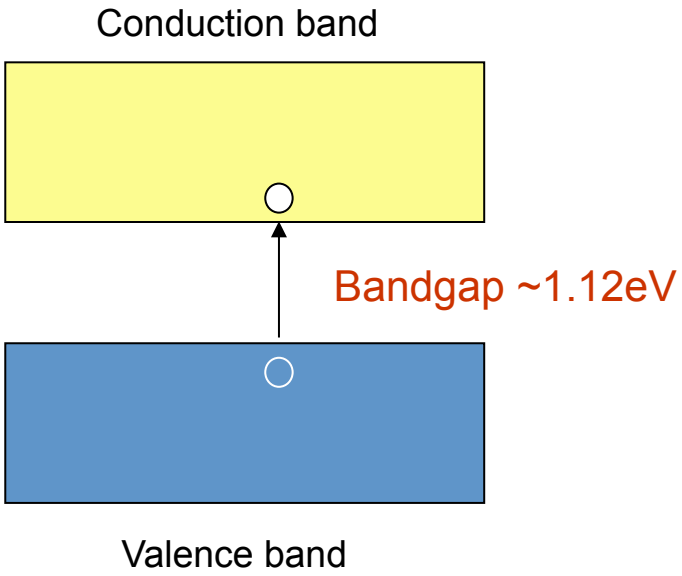
E_F is the energy at which the probability of occupation is 1/2.



Fermi-Dirac distribution. States with energy ε below the Fermi energy (μ) have higher probability n to be occupied, and those above are less likely to be occupied.

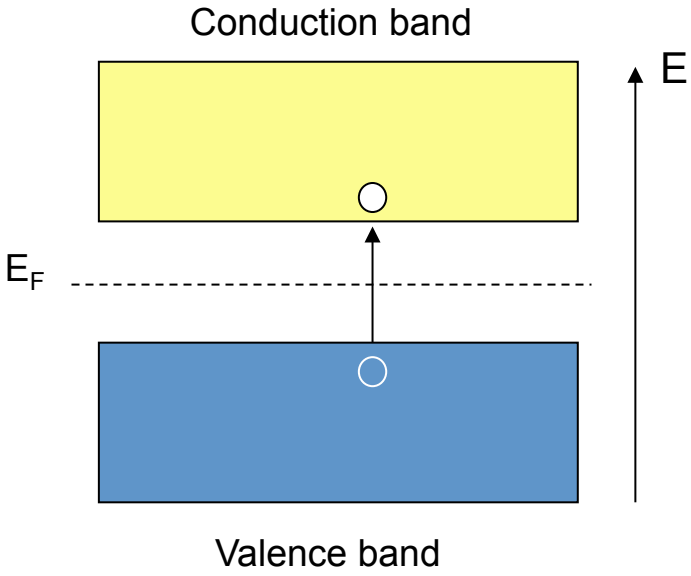
Silicon Properties

How much energy is required to generate an electron-hole pair?



Due to phonon scattering the average energy required to generate an electron-hole pair is 3.62 eV at room temperature.

Electrons and holes:



An electron moving to a state in the conduction band leaves an unoccupied state in the valence band = hole

Silicon properties

Intrinsic semiconductor: contains only small amounts of impurities compared to the thermally generated electrons and holes

$n = p = n_i$ n_i …intrinsic carrier density

$$E_F = E_i = \frac{E_C + E_V}{2} + \frac{kT}{2}\ln\left(\frac{N_V}{N_C}\right)$$

E_F lies very close to the mid band gap at RT

$$n_i = \sqrt{N_C N_V} \cdot e^{\left(-\frac{E_G}{2kT}\right)}$$

n_i (silicon at RT)=1.45 x 10^{10} cm^{-3}

N_V, N_C … effective densities of states in the valence band and conduction band

N_V=1.04x10^{19} cm^{-3} at RT

N_C=2.8x10^{19} cm^{-3} at RT

Compared to 1x10^{22} cm^{-3} atoms in a silicon crystal, only every 10^{12}th atom is ionized at RT

Silicon properties

For IC industry conductivity of semiconductors can be modified by adding impurities to the crystal: Doping

Dopants are classified as electron donors (donors) or electron acceptors (acceptors)

Silicon: 4 valence electrons
Donor atom: 5 valence electrons -> one weakly bound extra electron
Acceptor atom: 3 valence electrons → one missing bond = hole

Donors create an excess in negative charge: n-type silicon
Acceptors create an excess in positive charge: p-type sylicon

n-type silicon:
- excess of negative charge carriers (electrons)
- electrons=majority charge carriers
- holes=minority charge carriers

Dopants: group V elements, e.g. phosphorus

p-type silicon:
- excess of positive charge carriers (holes)
- holes=majority charge carriers
- electrons=minority charge carriers

Dopants: group III elements, e.g. boron

The doping concentration for silicon may range from 10^{13} cm^{-3} to 10^{18} cm^{-3}.

At RT usually all donors (acceptors) are ionized and thus the electron (hole) density n is equal to the concentration of donors N_D (acceptors N_A).

Silicon properties

Depends on concentration of free charge carriers and their mobility

$$\rho = \frac{1}{q(\mu_e n + \mu_h p)}$$

>> resistivity of intrinsic silicon ~ 235 kΩcm

>> silicon for pixel detectors ~ 1-6 kΩcm

>> silicon substrate for CMOS Ics ~ 0.1 – 10 Ωcm

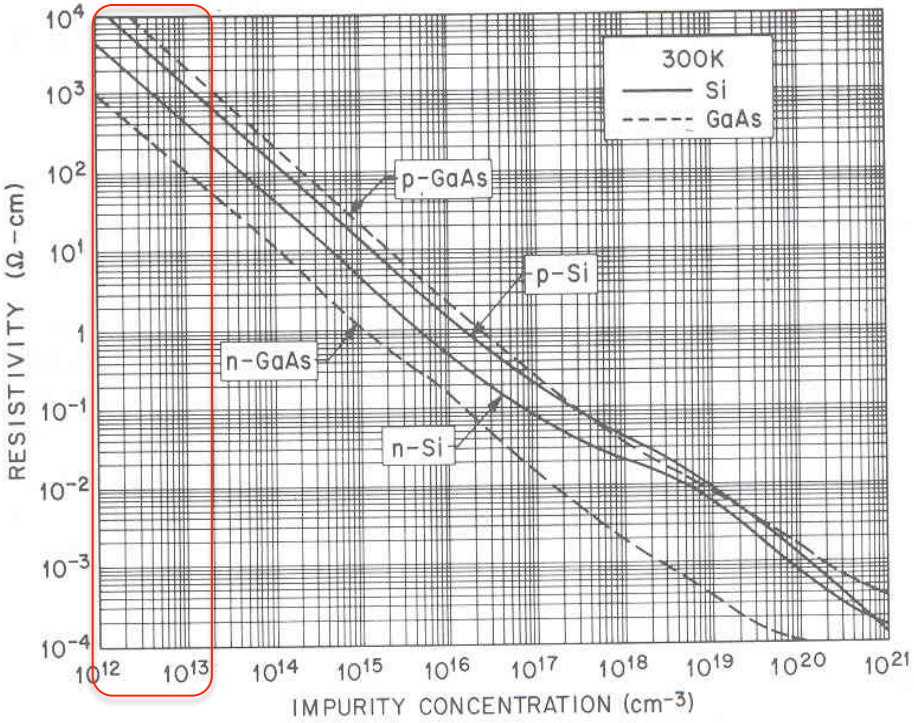


Fig. 7 Resistivity versus impurity concentration[4] for Si and GaAs.

From Sze, *Semiconductor Devices 1985*

Silicon properties

Free charge carriers can be seen as free particles - they are not associated with a lattice site

- Mean kinetic energy: 3/2 kT
- Mean velocity at RT: **~ 10^{11} µm/s**

The charge carriers scatter on **lattice imperfections** due to thermal vibrations, **impurity atoms** and **lattice defects** (e.g. radiation induced).

If no electric field is applied, the average displacement due to random motion is zero

Applying an electric field **E**:

Charge carriers will be accelerated in between random collisions in the direction determined by the electric field.

Average drift velocity (*):

$$v_e = -\mu_e E \qquad \mu_e \text{ electron mobility}$$

$$v_h = -\mu_h E \qquad \mu_h \text{ hole mobility}$$

(*) Holds for small fields E ("acceleration" is small compared to the thermal velocity.
If the electric field is high enough so that the carrier energies are larger
than the thermal energies, the drift velocities become independent of the electric field.

Carrier Transport

In the linear region of v(E) the charge carrier mobilities are

μ_e=1350 cm^2/Vs μ_h=480 cm^2/Vs

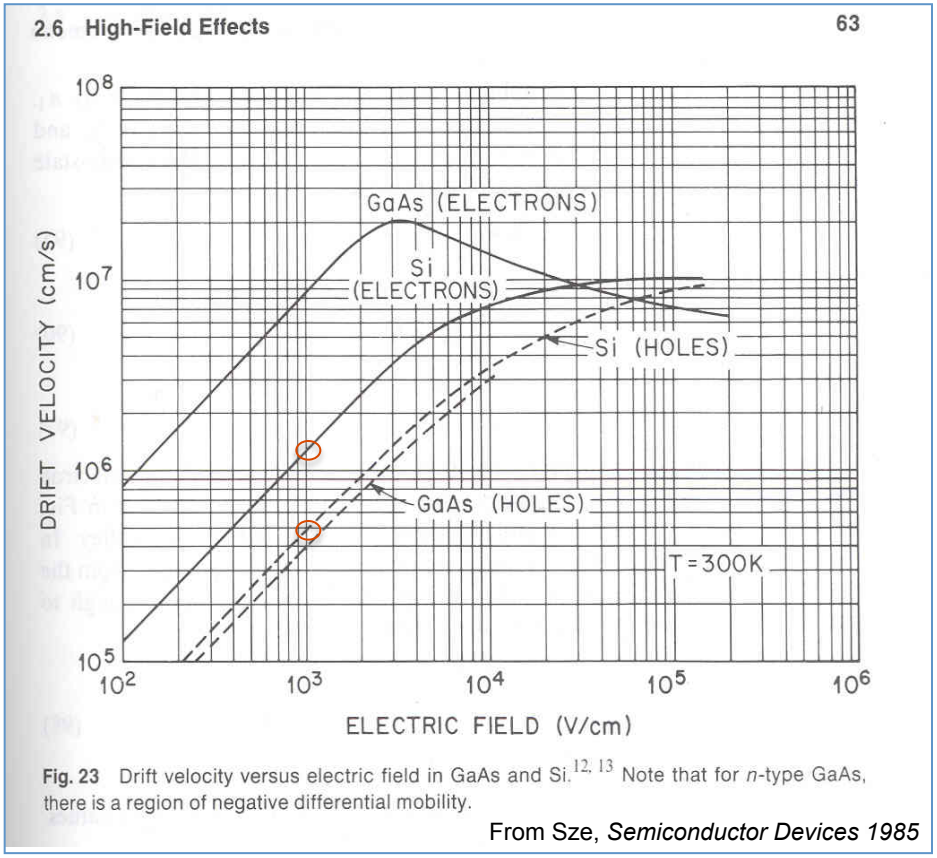
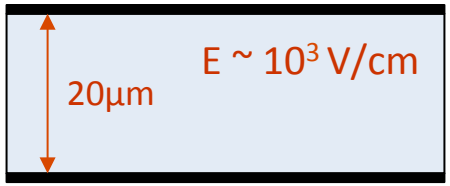


Fig. 23 Drift velocity versus electric field in GaAs and Si.[12, 13] Note that for *n*-type GaAs, there is a region of negative differential mobility.

From Sze, *Semiconductor Devices 1985*

2V is applied over 20µm



v_e ~ 10^{10} µm/s

v_h ~ 0.5 x 10^{10} µm/s

Charge collection time (e)

Ts = 2ns

How to build a detector?

P⁺N-Junction

Charge carrier diffusion across the junction due to difference in carrier concentration

opposite carriers recombine

Space charges remain in the junction region

generates electric field which counteracts the diffusion

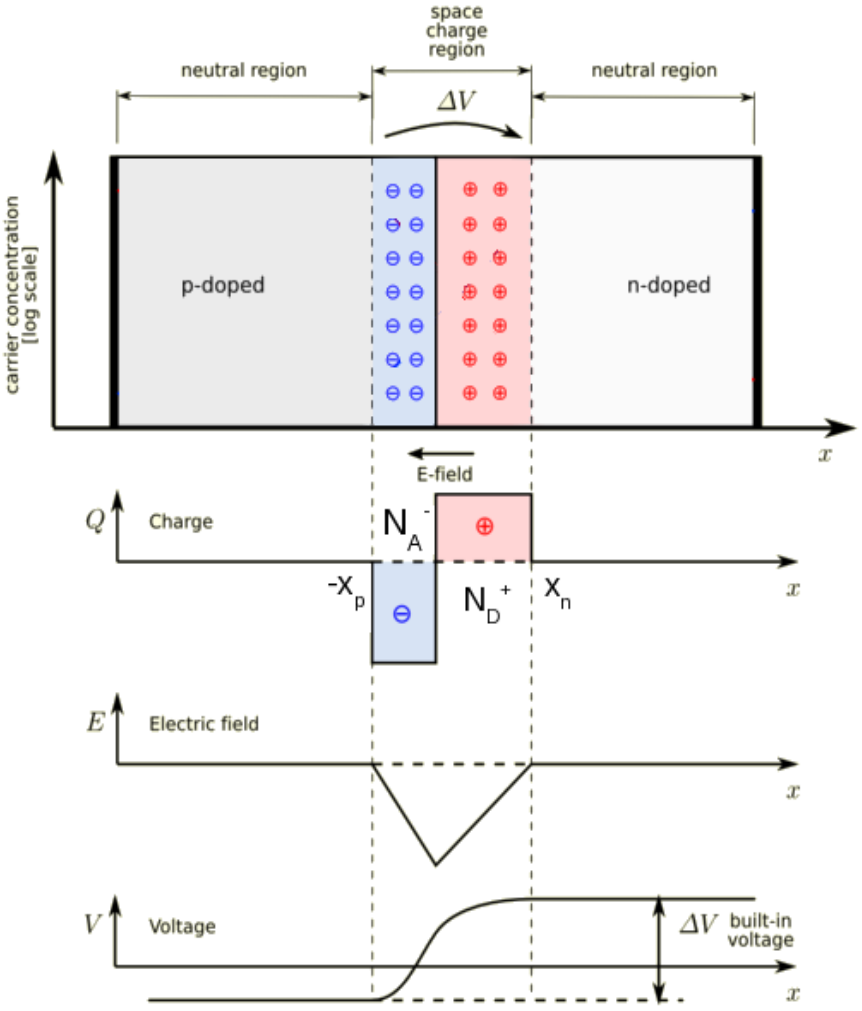
The corresponding potential is called built-in-voltage V_{bi}

$$V_{bi} = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2}$$

K ~ 8,6 x 10^{-5} eV/K

q ~ 1.6 x10^{-19}

kT/q ~ 26 mV (at RT)



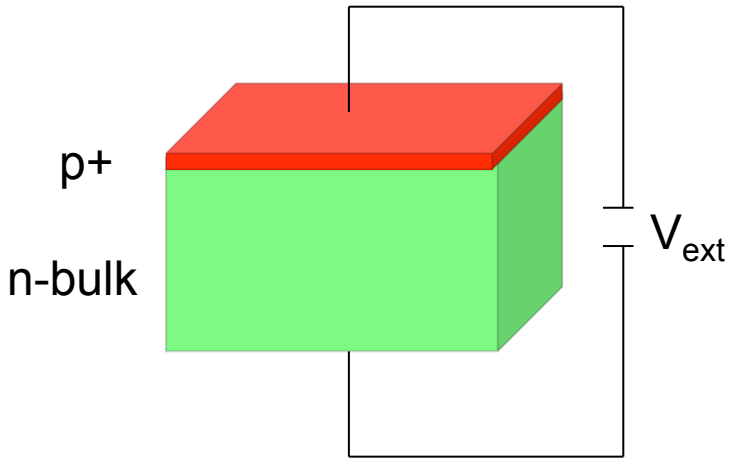
PN Junction Detector

- A passing charged particle or x-ray in the depletion region can create an e-h pair by ionisation ("ionization chamber")
- But the electric field (qV_{bi}) would be to small for good charge collection and the depleted region is too small for collecting sufficient charge (recombination)

Build a more realistic detector:

p^+n junction

thin highly doped (p+) and n-well doped bulk, and apply an external voltage to deplete the bulk volume of free charge carriers



Depletion width W

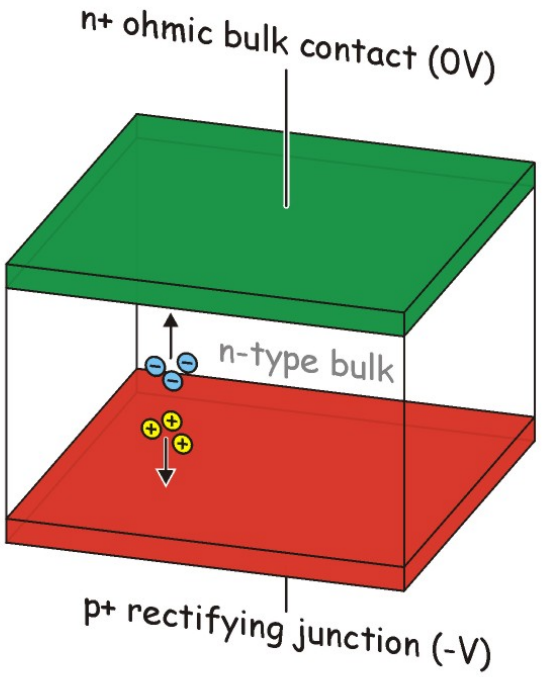
$$W = \sqrt{\frac{2\varepsilon_s (V_{ext} - V_{bi})}{qN_D}}$$

ε_s..product of rel. permittivity of silicon and of vacuum

PN Diode Detector

P⁺N diode detector:

- Reverse bias (positive voltage on n-bulk wrt p⁺-side)
- Increase bias to fully deplete the entire bulk of free charge carriers
- >> full volume is sensitive to a passing particle
- Highly n-doped layer to provide ohmic contact (n⁺)



Voltage at which full thickness of the diode is depleted

$$V_{fd} = \frac{e}{2\varepsilon_s}(N_D - N_A)d^2$$

d ..thickness

N_D-N_A=N_{eff}…effective doping concentration

e.g. $N_D = 10^{12}/cm^3$, d = 300µm

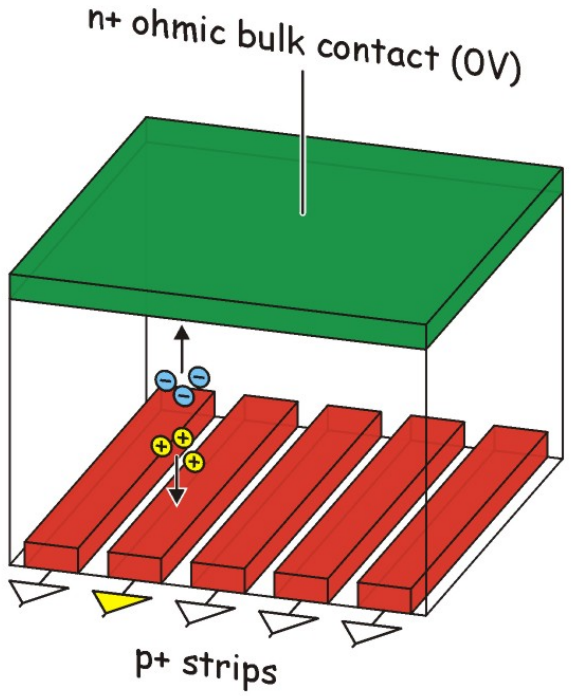
(ε_s = 11.7 x 8.8 x 10^{-12} F/m)

V_{fd} ~ 80 V

MPI

Strip Detector

How to achieve position resolution information? Segmentation



MPI

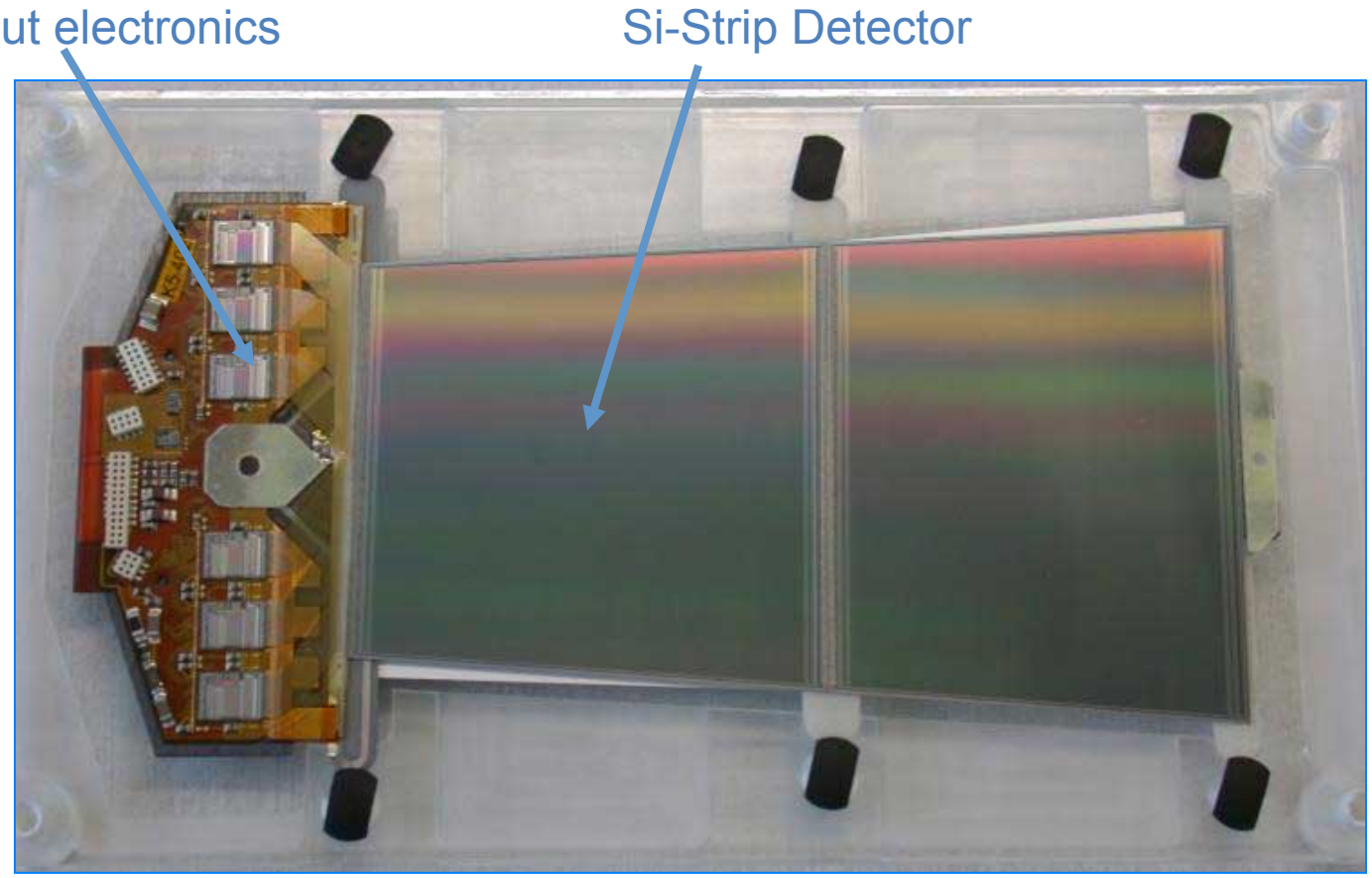
Each strip is connected to one electronic readout channel

First prototypes: ~ 1980

Strip pitch: ~10-100 µm

Position resolution: ~few µm due to charge sharing between neighboring strips (determine centroid of charge)

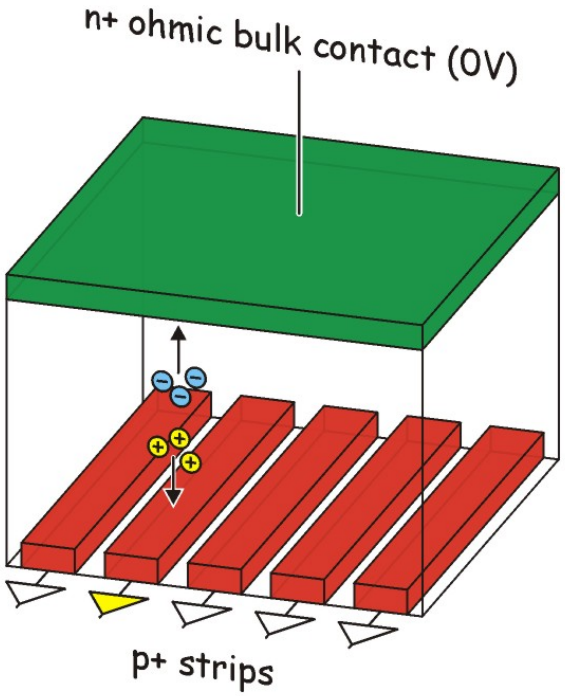
Strip Detector



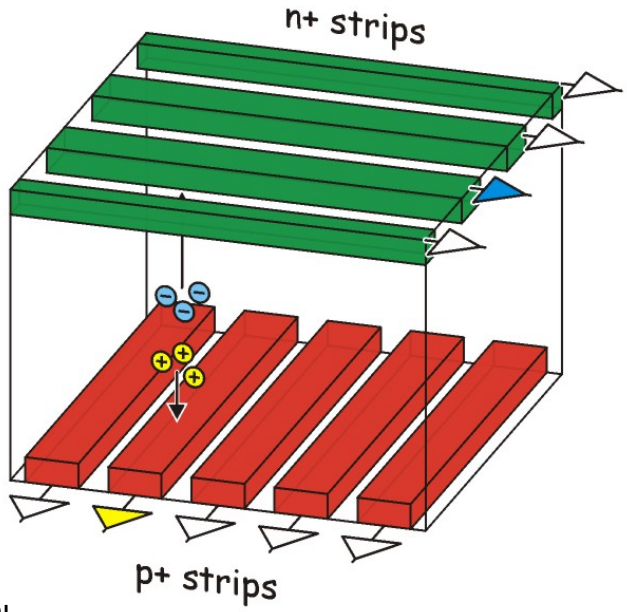
ATLAS strip detector, wedge shape, forward

Strip Detector

Double sided strip detector



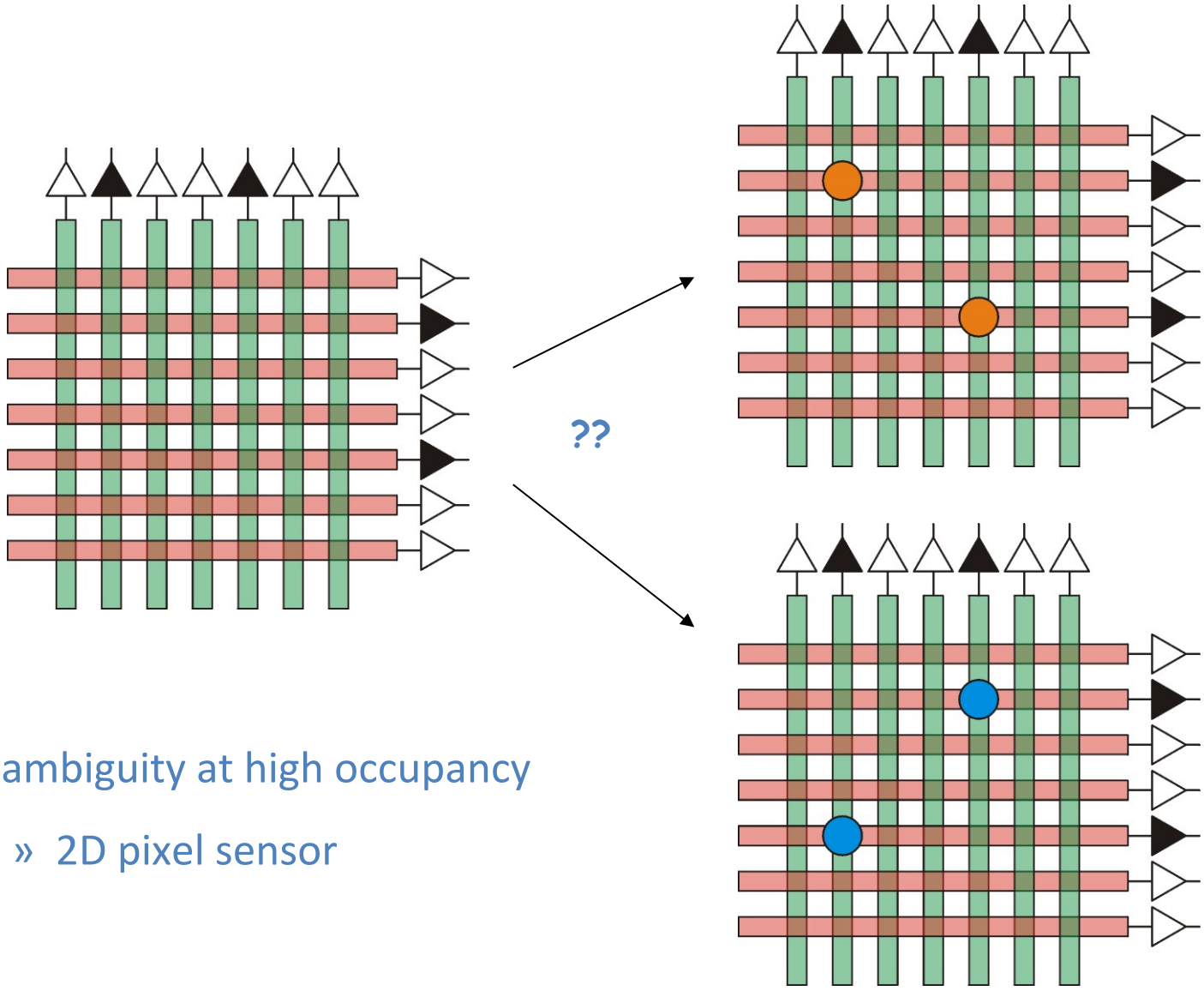
MPI



MPI

particle tracking 2D resolution

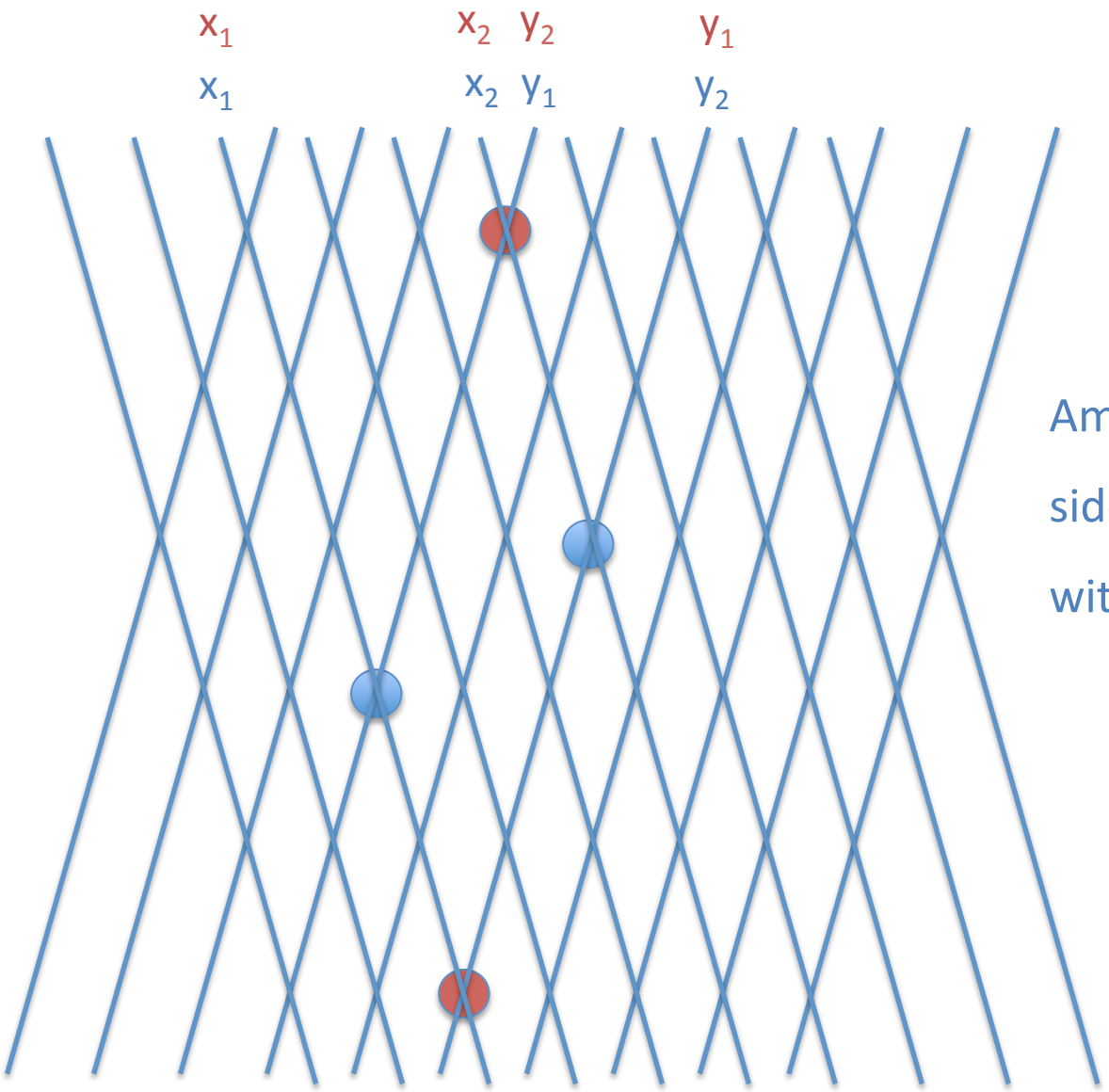
Strip Detector - Limitations



ambiguity at high occupancy

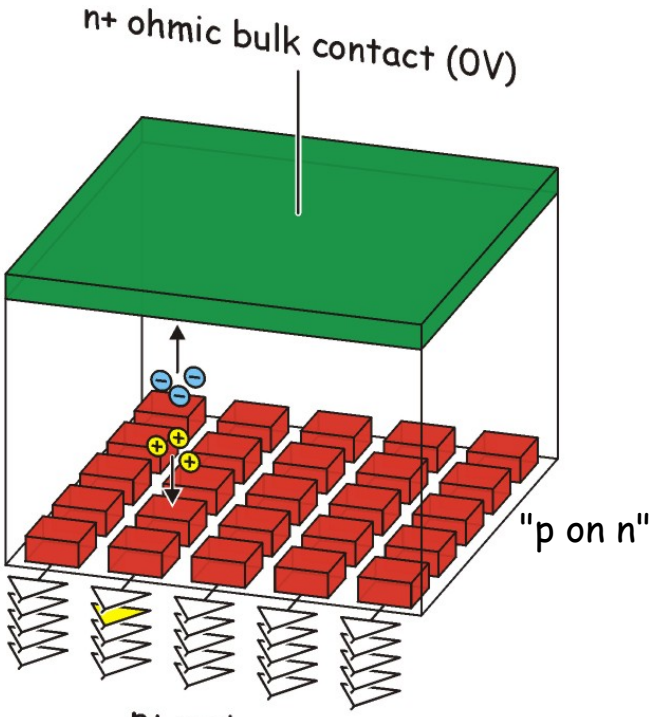
» 2D pixel sensor

Strip Detector - Limitations



Ambiguity in a double sided strip detector with stero angle

Pixel Detector



MPI

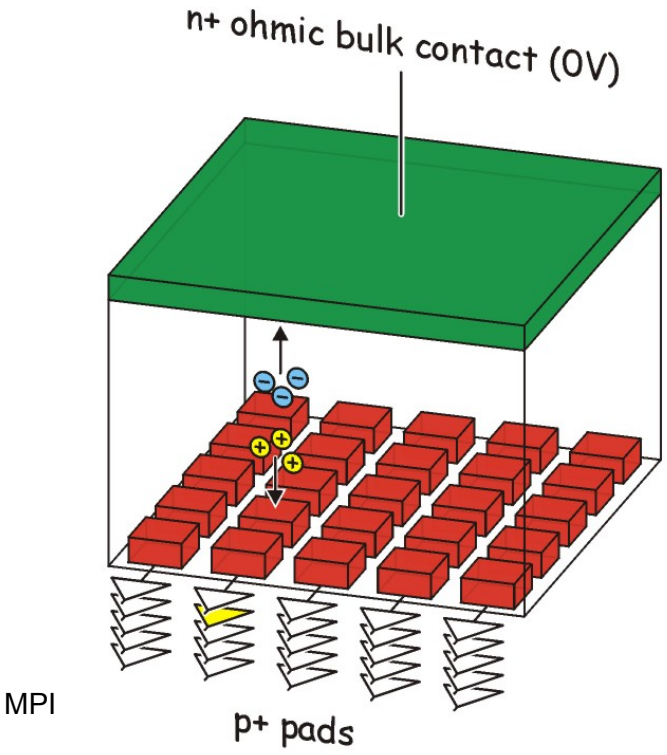
2D resolution

First prototypes ~1990

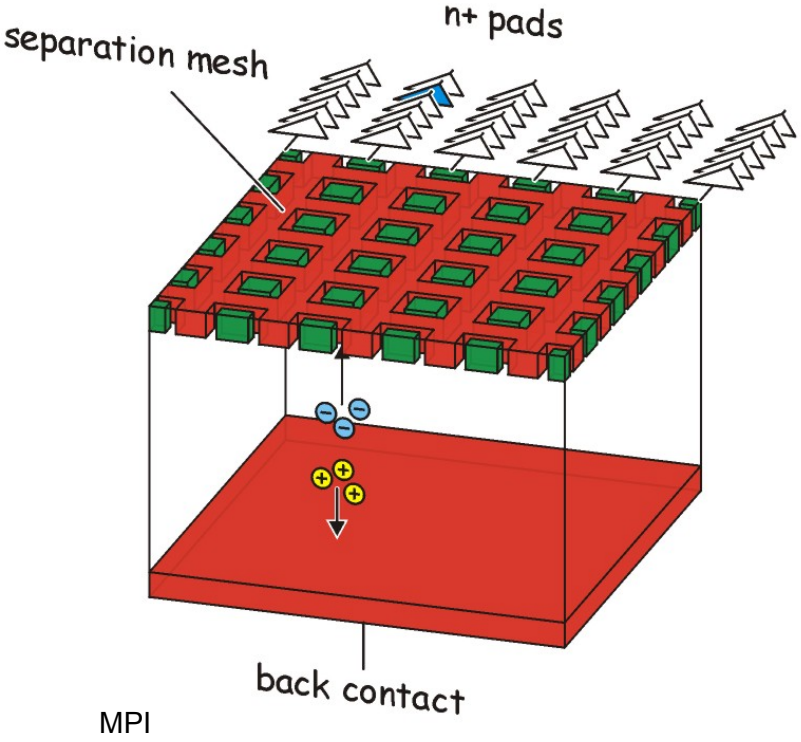
Can be used for tracking or imaging:

- particle tracking = detection of individual charged particles
- imaging = count / integrate particles or photons

Pixel Detector



”p on n"



"n on n"

Pixel Detectors in HEP – Short historical excursus

First use in HEP Experiments: CCDs used early 1980s in SLD/SLAC and NA11/32 CERN

"The silicon micropattern detector: a dream?"

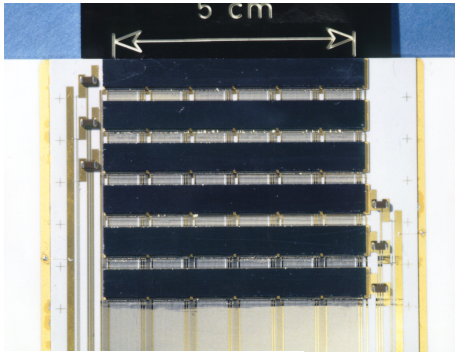
E.H.M Heijine, P. Jarron, A. Olsen and N. Redaelli , *Nucl. Instrum. Meth. A 273 (1988) 615*

"Development of silicon micropattern detectors"

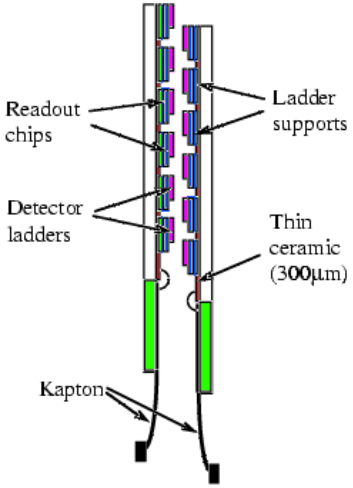
CERN RD19 collaboration, *Nucl. Instrum. Meth. A 348 (1994) 399*

1995 – First Hybrid Pixel detector installed in WA97 (CERN, Omega facility)

1996/97 – First Collider Hybrid Pixel Detector installed in DELPHI (CERN, LEP)

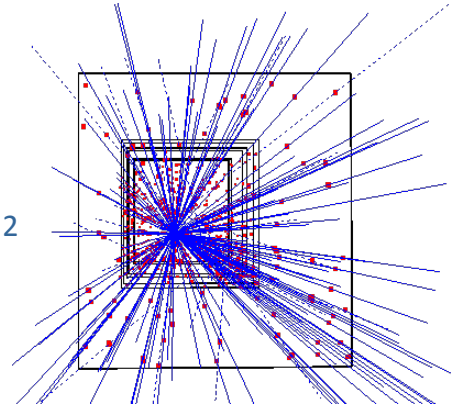


E. Heijne, E. Chesi



CERN – WA97 Experiment (1995)

- 5 x 5 cm^2 area
- 7 detector planes
- ~0.5 M pixels
- Pixel size 75 x 500 μm^2
- 1 kHz trigger rate
- Omega2 chip

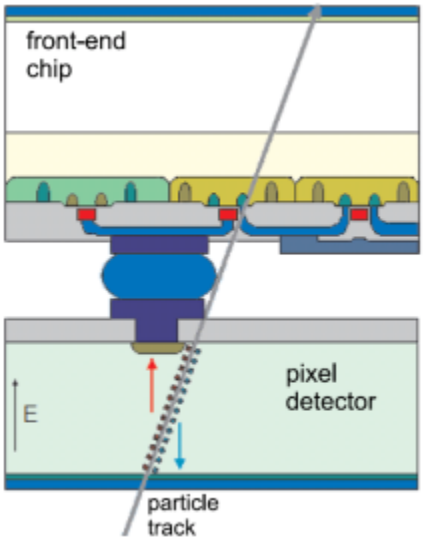


Work carried out by RD19 for WA97 and NA57/CERN

No-field, Pb-Pb, 153 reconstructed tracks

The world of Silicon Pixel Detectors

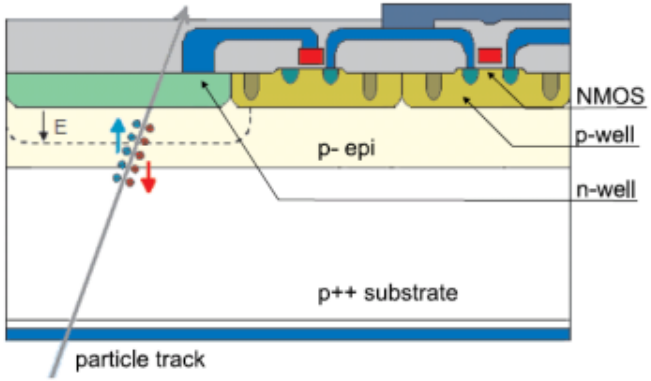
Hybrid Pixel Detector



N. Wermes (Univ. of Bonn)

- Sensor based on silicon junction detectors produced in a planar process
- High resistivity wafers (few kΩcm) with diameters of 4” – 6”
- Specialized producers (~10 world wide)
- Readout Chip: ASIC - CMOS sub-micron technology
- Interconnect technology based on flip-chip bonding

Monolithic Pixel Detector



N. Wermes (Univ. of Bonn)

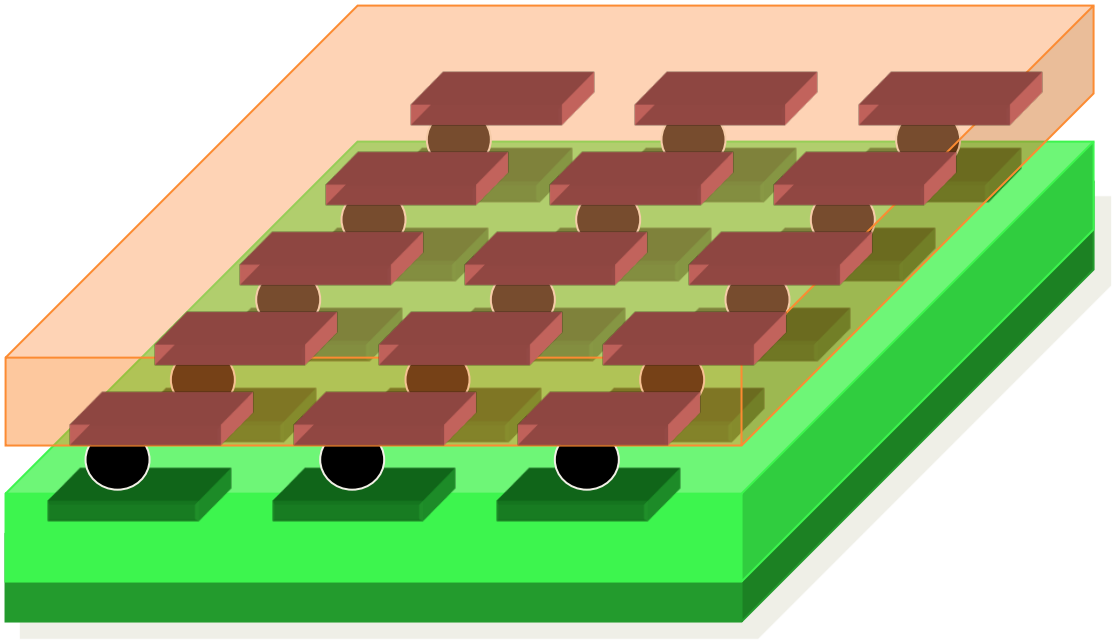
- Charge generation volume integrated into the ASIC
- Exist in many different flavours: CCDs, CMOS MAPS, HV/HR CMOS, DEPFET, SOI, …
- This talk will cover only CMOS Monolithic Active Pixel Sensors (CMOS MAPS) = CMOS Pixel Sensors (CPS)

Hybrid Silicon Pixel Detector

Readout Chip

Bump Bonds

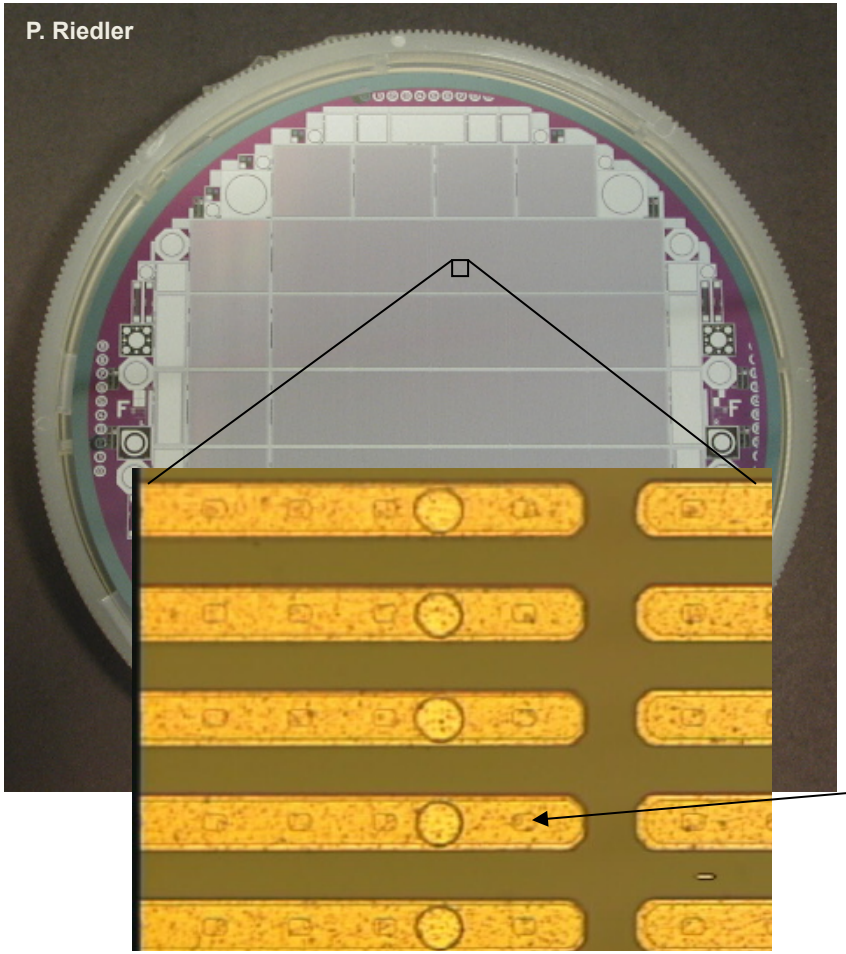
Si Sensor



Each pixel cell in the sensor is connected to a pixel cell in the readout chip via a bump bond.

Hybrid Silicon Pixel Detectors

1. Pixel Sensor



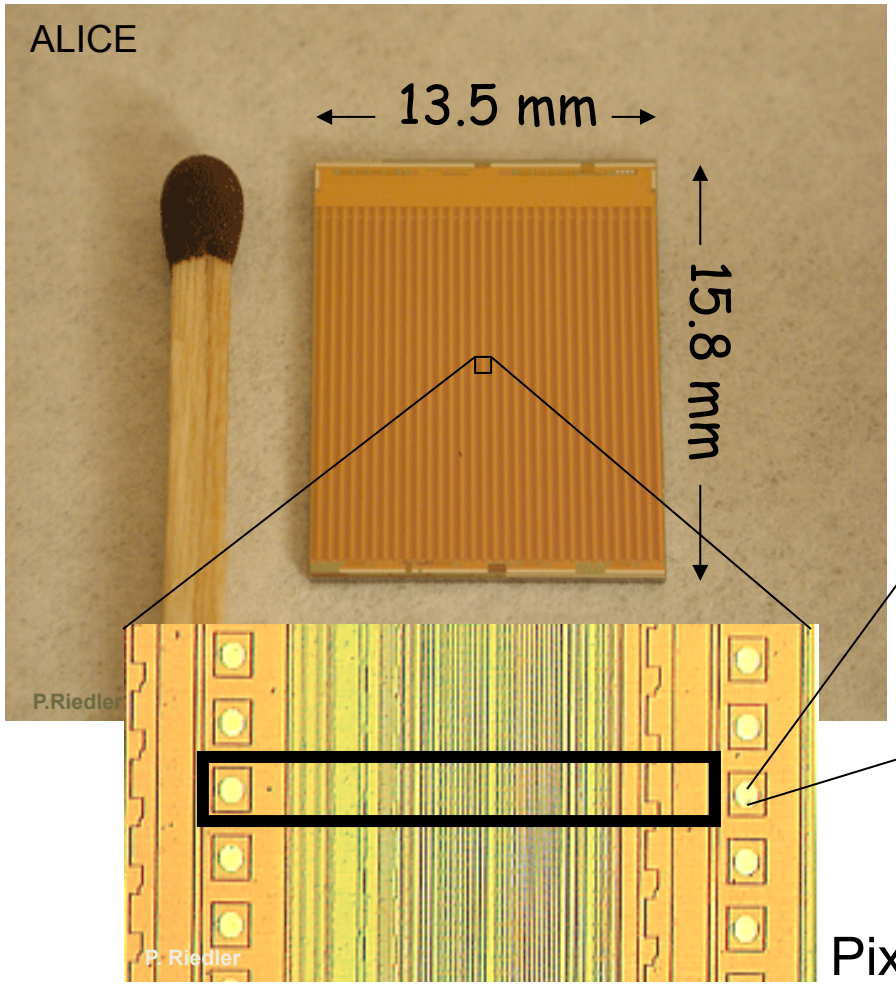
Different sensor materials can be used: Si, CdTe, GaAs, …

Depending on application (tracking, single photon counting, ..)

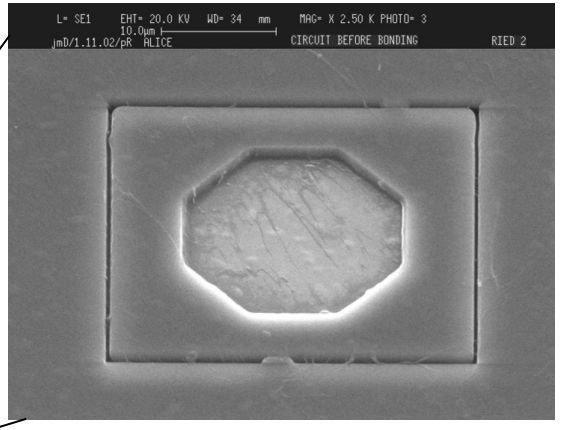
Usually several readout chips are connected to one sensor.

Hybrid Silicon Pixel Detectors

2. Pixel Chip



ASIC, custom design

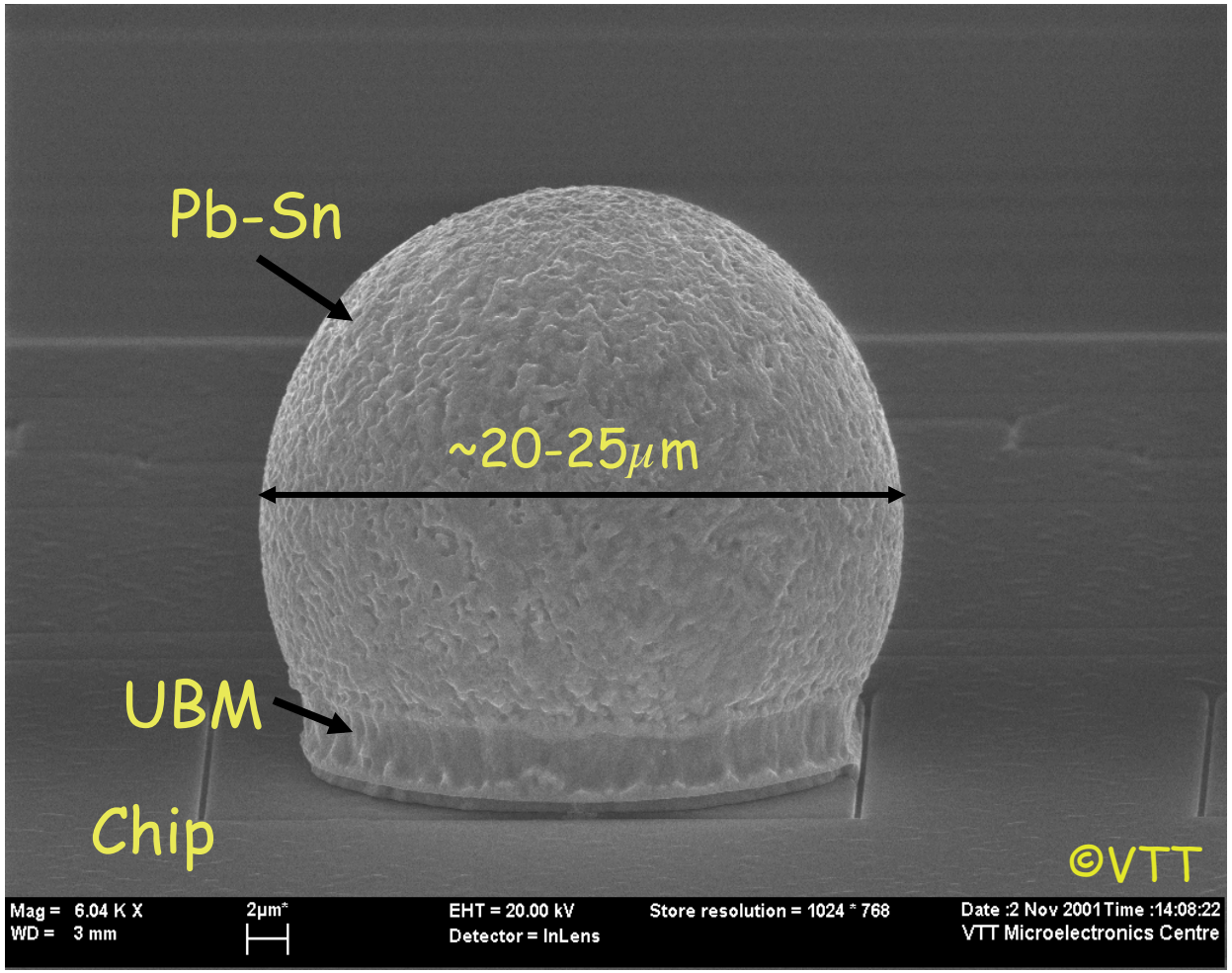


Bump bonding pad

Pixel cell (e.g. 50 µm x 425 µm)

Hybrid Silicon Pixel Detectors

3. Bump Bond



SEM picture of one Pb-Sn bump bond

Hybrid Silicon Pixel Detectors

How to efficiently cover large surfaces? Ladders (modules)

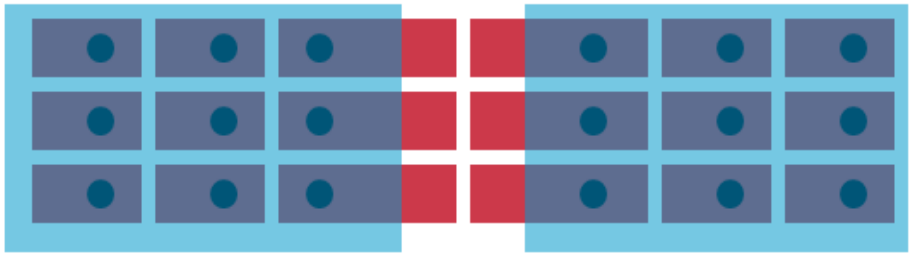
- sensor size limited by wafer size and bump bonding requirements (flatness!), LHC experiments: ~7 cm x 2 cm
- chip size limited by CMOS lithography
- larger chip -> lower yield in production

ATLAS, CMS

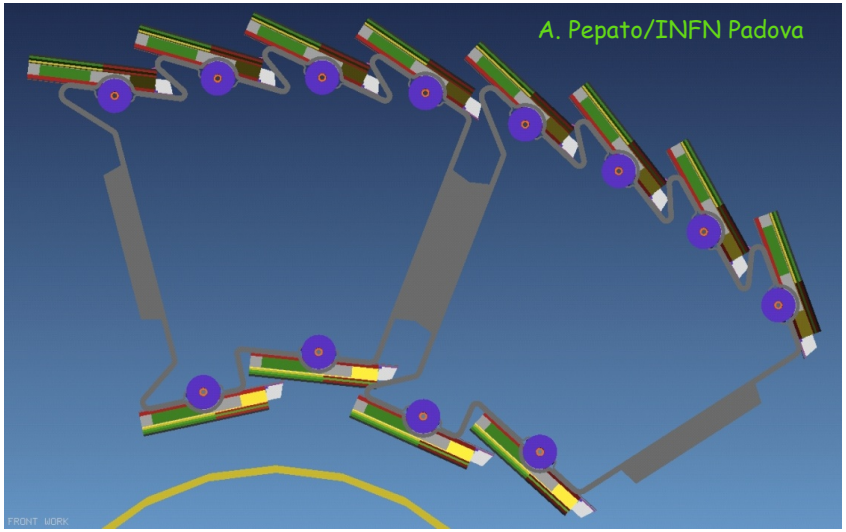
ALICE

Hybrid Silicon Pixel Detectors

To avoid dead areas between chips: long boundary pixels

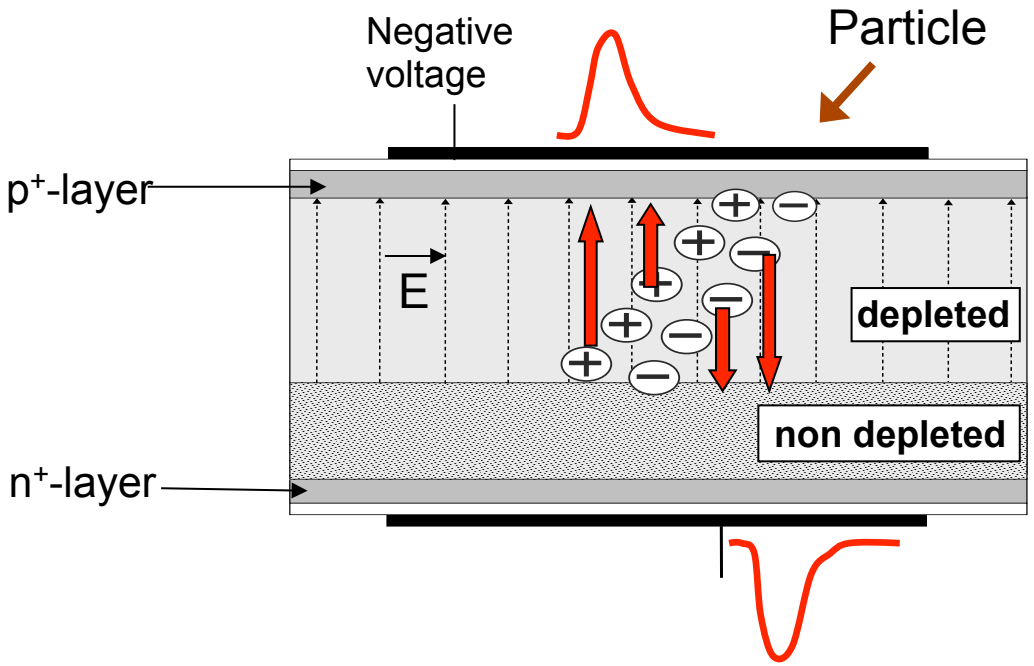


To avoid dead areas between ladders: turbine configuration
>> higher material budget in some regions

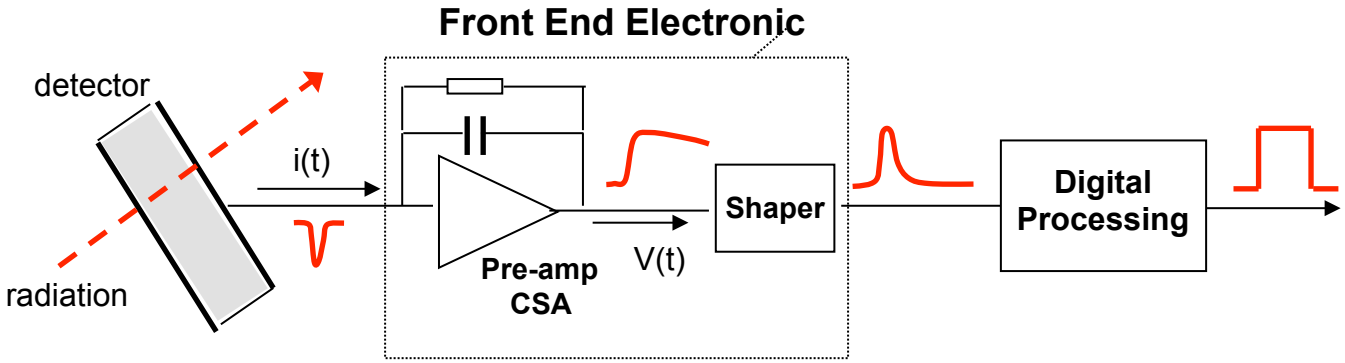


Hybrid Silicon Pixel Detectors – Signal formation

- Charge pairs generated in the detector volume move to the electrodes due to the electric field and due to diffusion
- The moving charge induces a signal current in the electrode



Hybrid Silicon Pixel Detectors – Signal formation



- Charge from the detector is integrated on the feedback capacitor
- The output voltage is proportional to the input charge

$$V_{out} = \frac{1}{C_f}\int_0^t I_{in}(t)dt = \frac{Q(t)}{C_f}$$

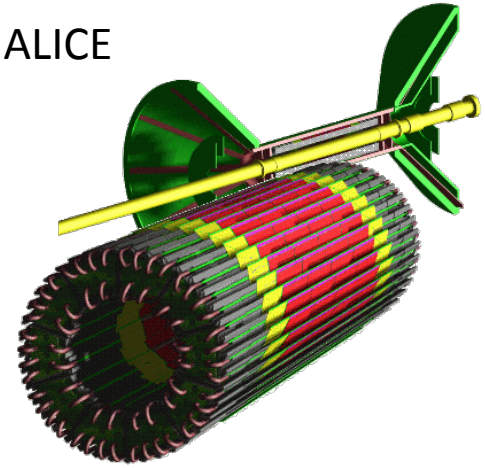
  - V_{out} remains constant for times >t
  - To avoid pile-up a feed-back resistor is added in parallel to C_f to discharge C_f

Pixel Detectors in HEP Experiments

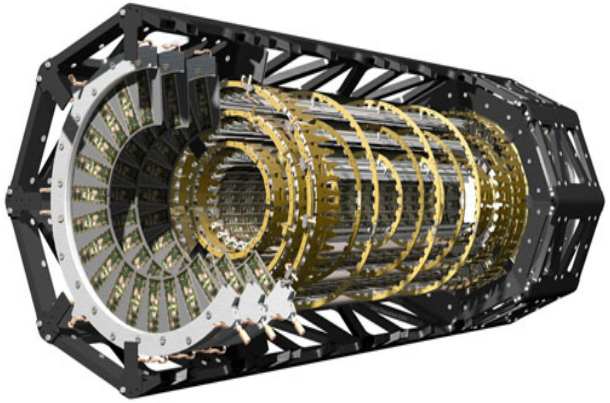
Hybrid Pixel Detectors at the heart of the LHC Experiments

Different sensor technologies, designs, operating condition

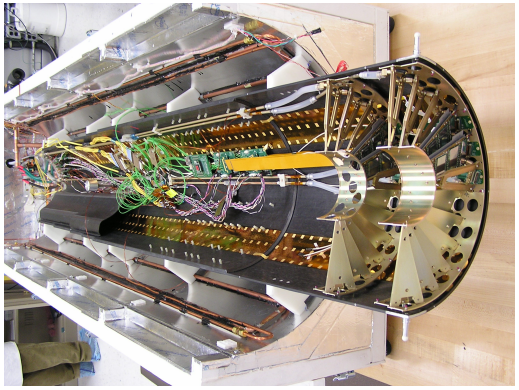
ALICE



ATLAS



CMS



Parameters	ALICE	ATLAS	CMS
Nr. layers	2	3	3
Radial coverage [mm]	**39** - 76	**50** - 120	**44** – 102
Nr of pixels	9.8 M	80 M	66 M
Surface [m^2]	0.21	1.7	1
Cell size ($r\phi$ x z) [μm^2]	50 x 425	50 x 400	100 x 150
Silicon thickness (sens. + ASIC) - x/X_0 [%]	0.21 + 0.16	0.27 + 0.19	0.30 + 0.19

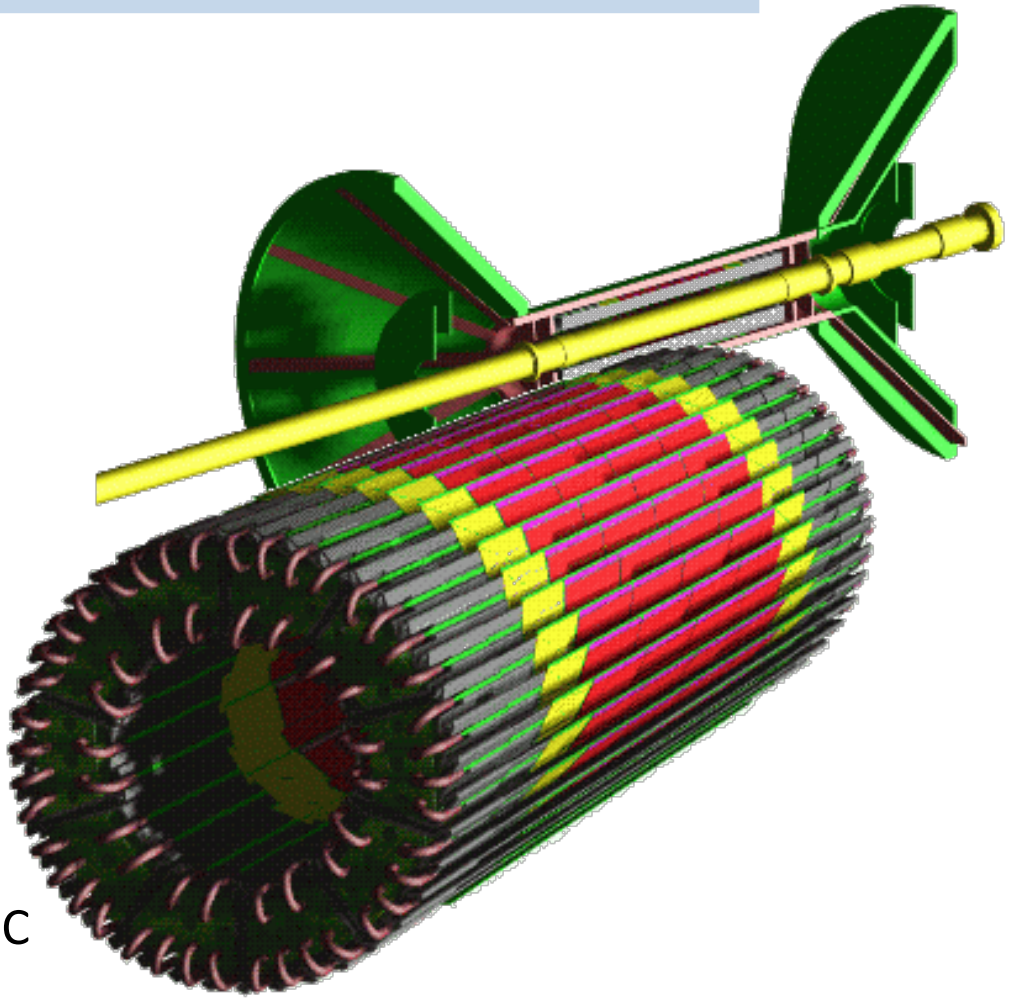
ALICE Pixel Detector

Two barrel layers:

- R= 3.9 cm
- R= 7.6 cm
- No forward disks

- 9.8 mio channels
- Area 0.21 m^2

- 120 modules
- 1200 pixel chips
- Environmental temperature ~ 27°C
- 0.5 T magnetic field



ALICE Pixel Detector

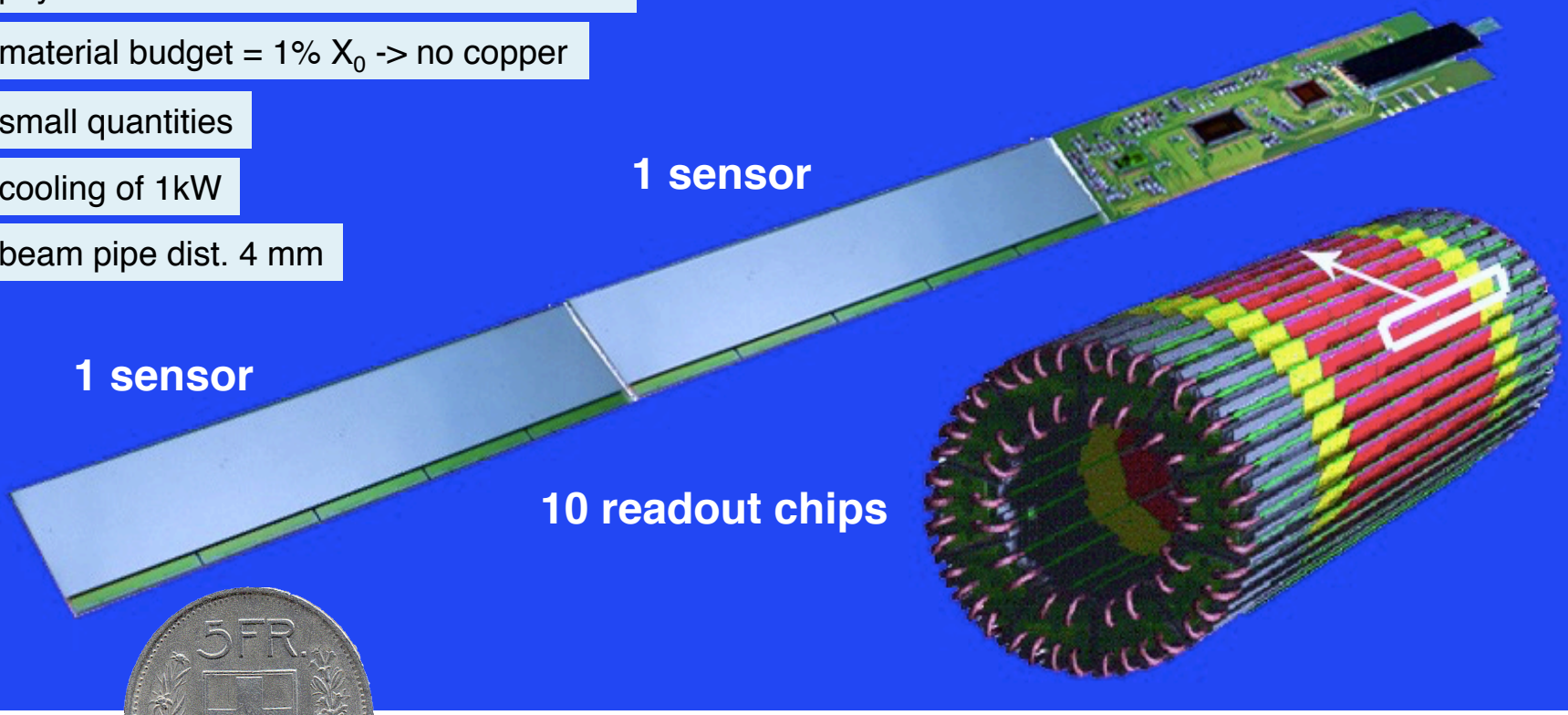
physical size = 200 mm x 15 mm x 2 mm

material budget = 1% X_0 -> no copper

small quantities

cooling of 1kW

beam pipe dist. 4 mm

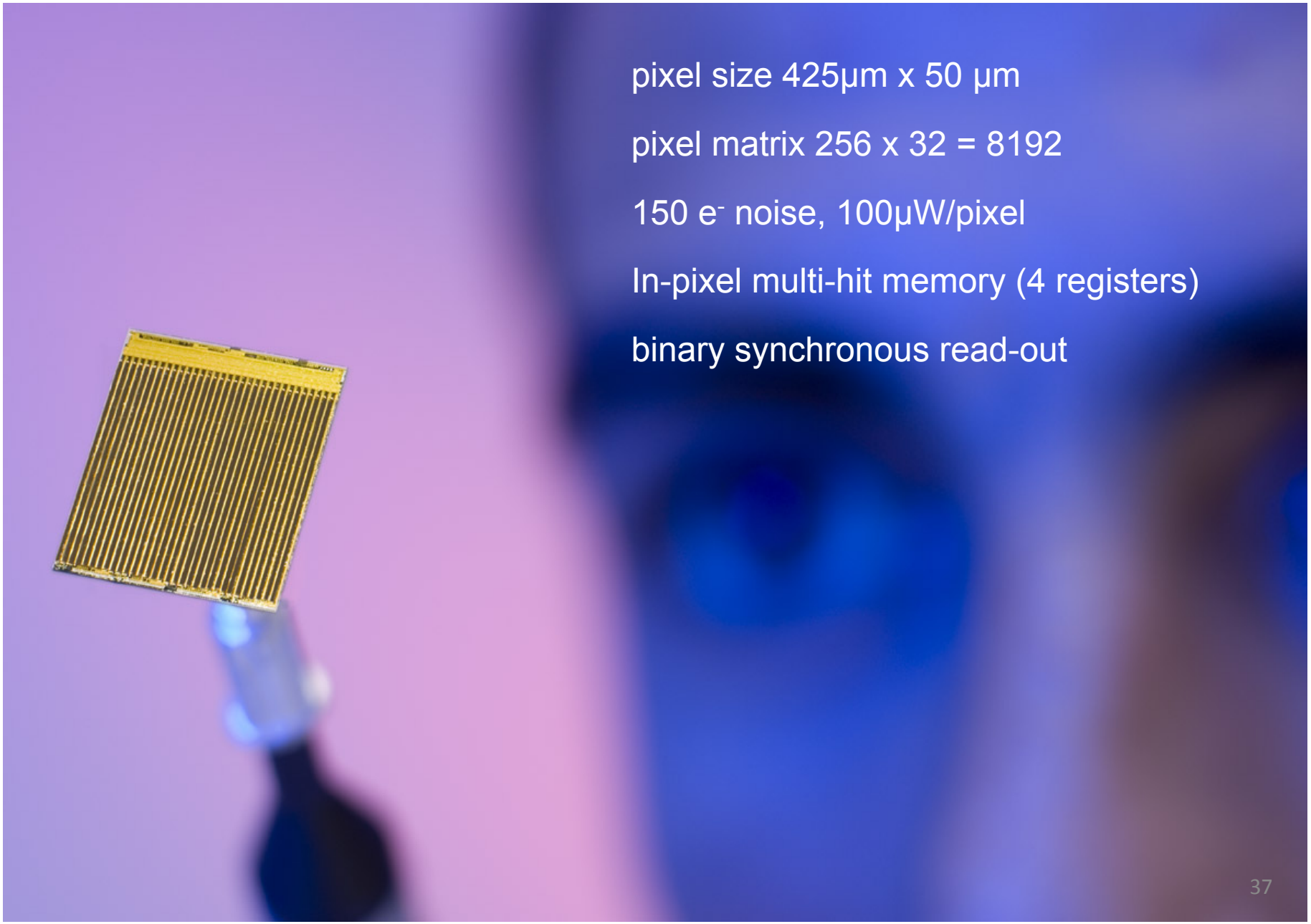


~10 million channels in 1200 pixel chips

120 detector modules – half staves

10 sectors

ALICE Pixel Detector – Pixel Chip



pixel size 425µm x 50 µm

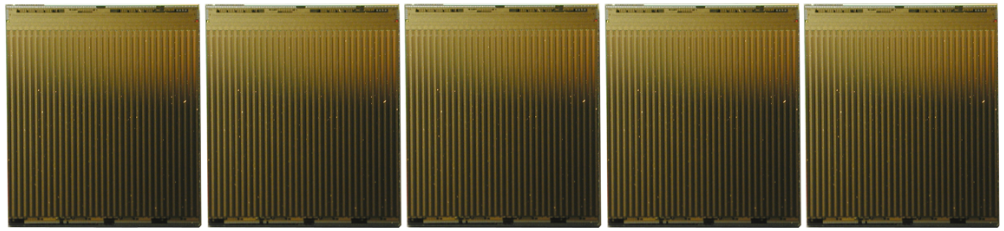
pixel matrix 256 x 32 = 8192

150 e^- noise, 100µW/pixel

In-pixel multi-hit memory (4 registers)

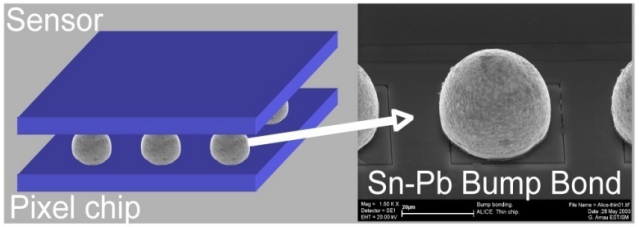
binary synchronous read-out

ALICE Pixel Detector – Sensor + Pixel Chip



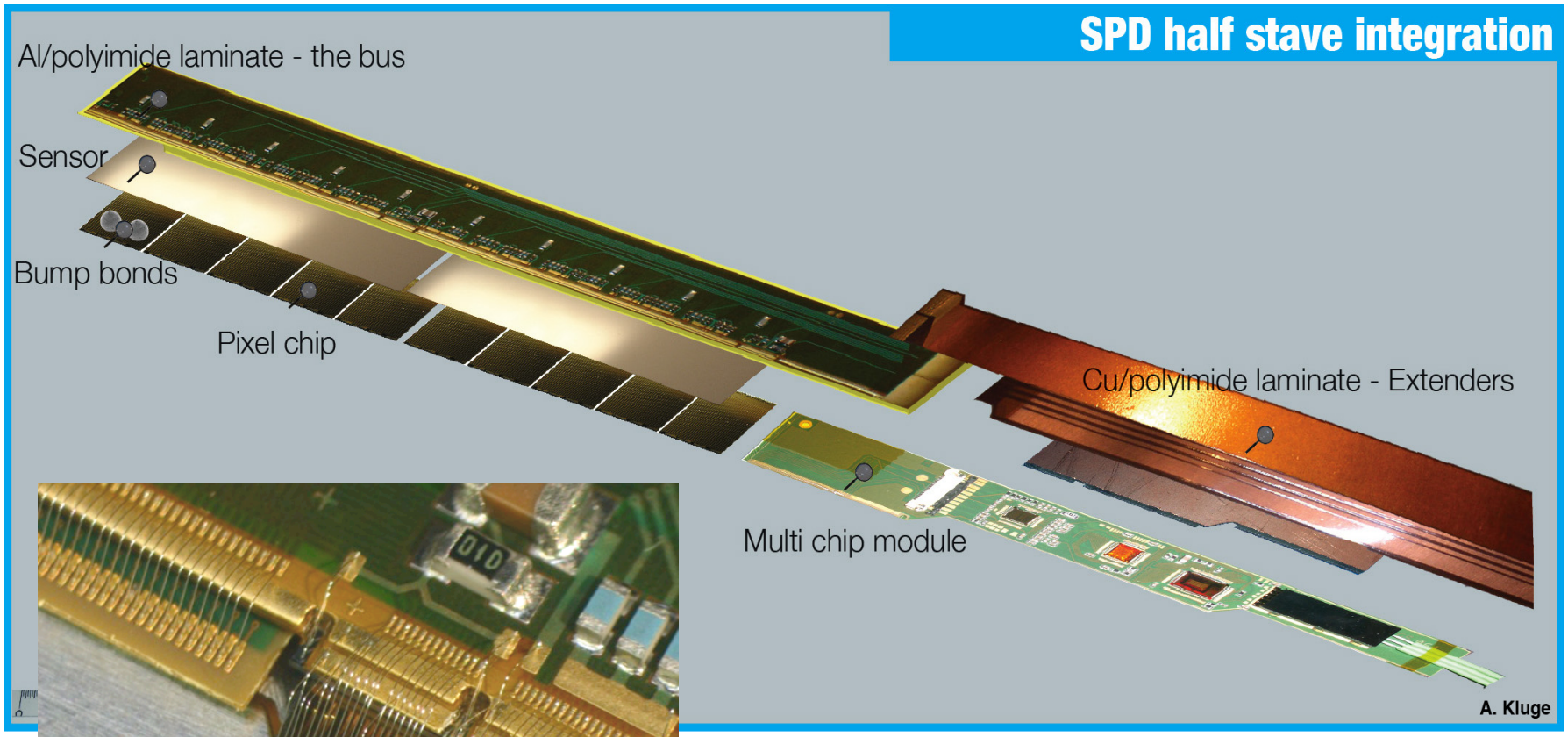
5 readout chips/sensor
0.25µm CMOS
13.68 mm x 15.58 mm
thinned to 150 µm

p-in-n silicon sensor
72.72 mm x 13.92 mm
200 µm thin

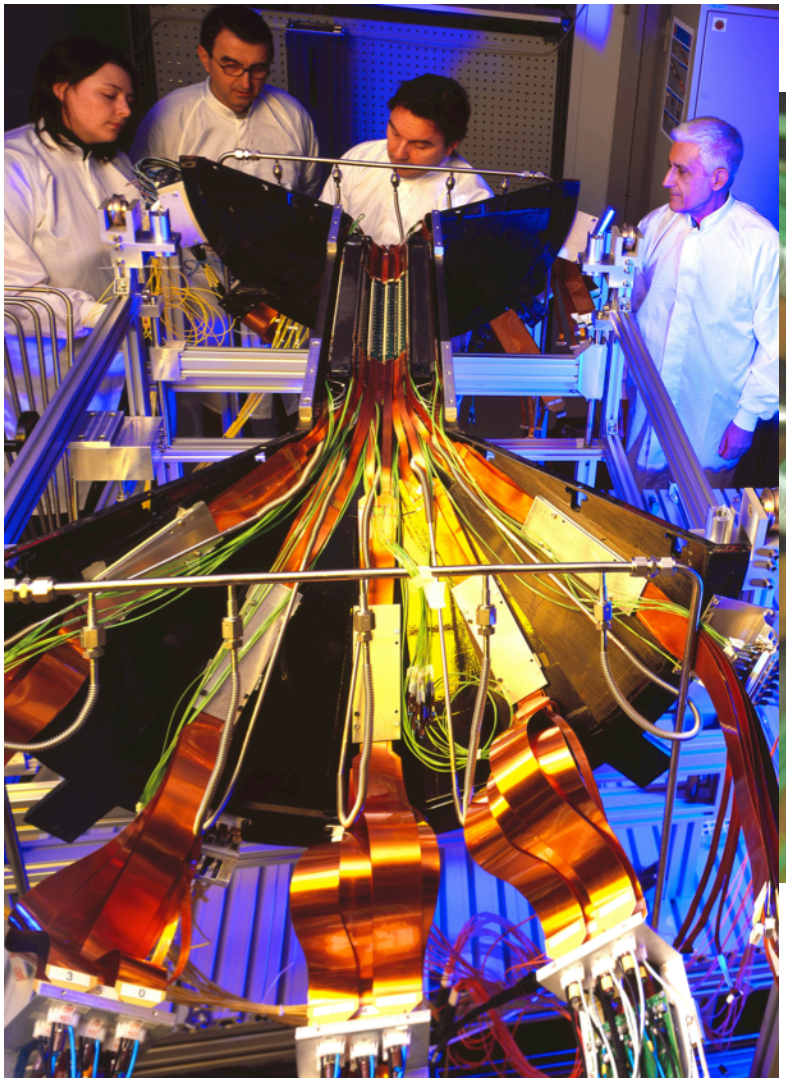


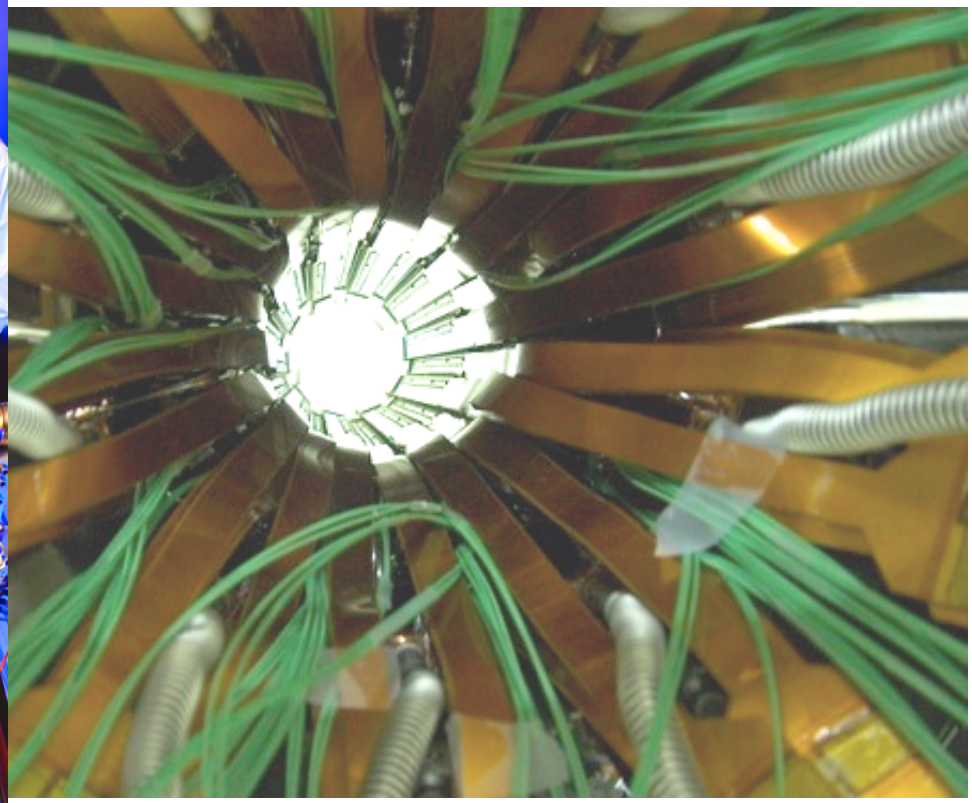
40960 bump bonds
~25 µm diameter
Stand-off:
~12 µm (Pb-Sn)

The ALICE SPD - Electronics Integration



ALICE Pixel Detector





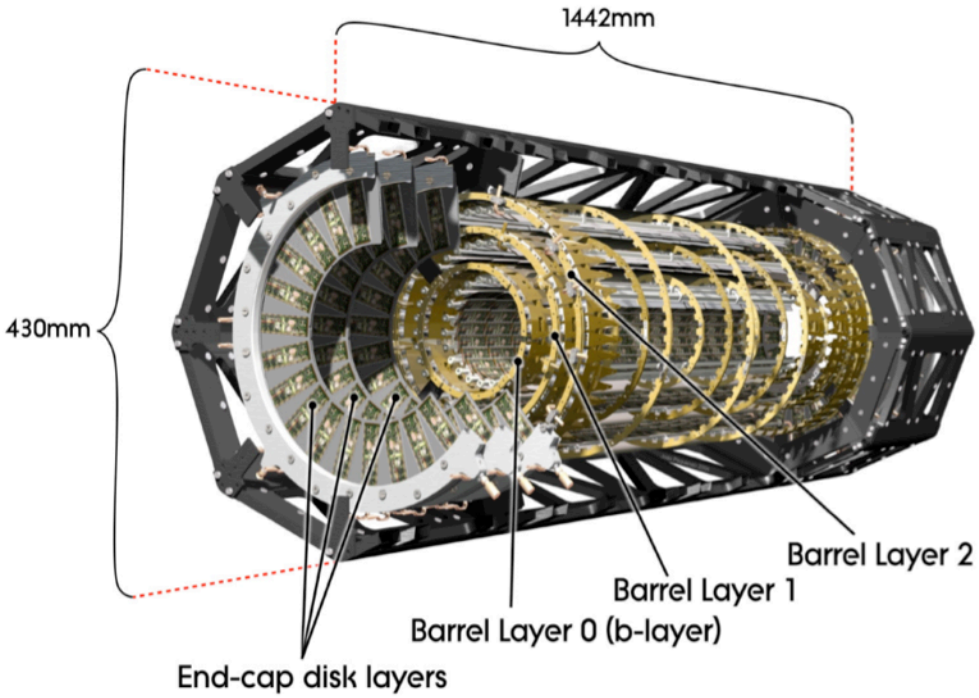
ATLAS Pixel Detector

Three barrel layers:

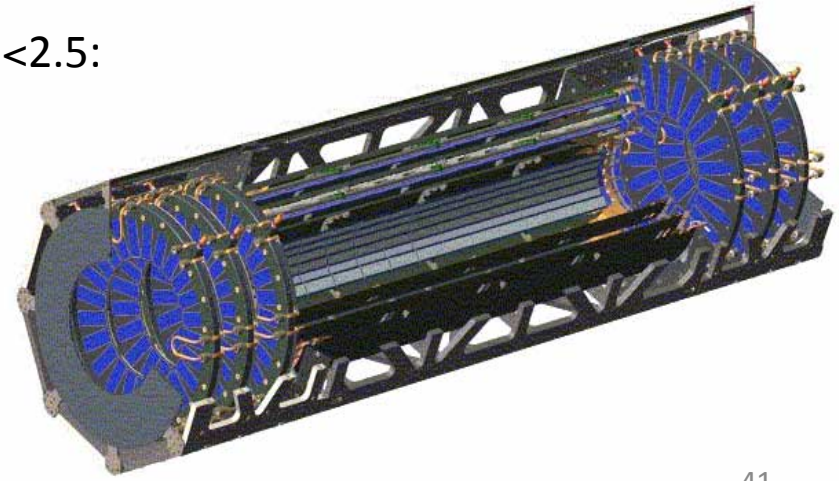
- R= 5 cm (B-Layer)
- R=9 cm (Layer-1)
- R=12 cm (Layer-2)
- 1456 barrel modules

Two endcaps:

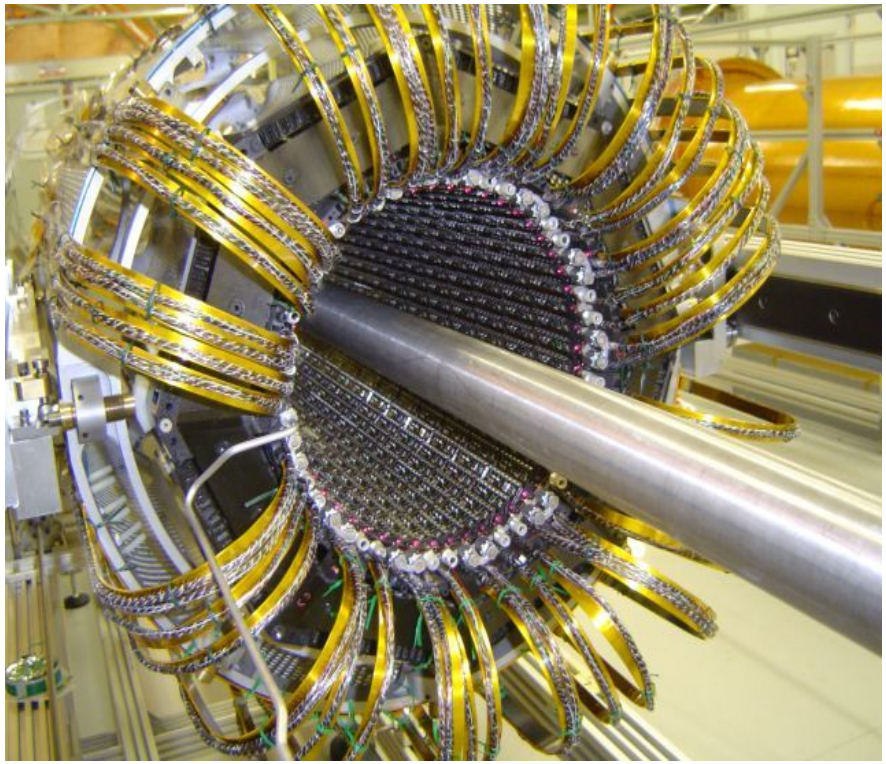
- three disks each
- 288 forward modules



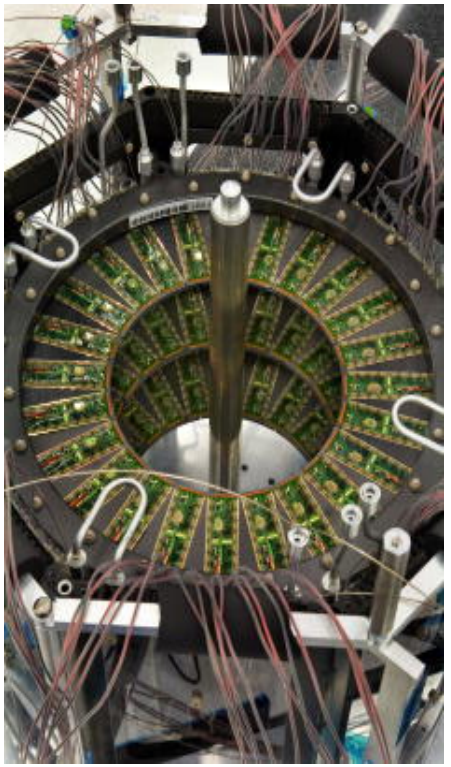
- 80 million channels
- sensitive area of 1.7 m^2
- Three precise measurement points up to $|\eta|<2.5$:
  - RΦ resolution:10 μm
  - z resolution: 115 μm
- Environmental temperature about -10 ºC
- 2 T solenoidal magnetic field.



ATLAS Pixel Detector



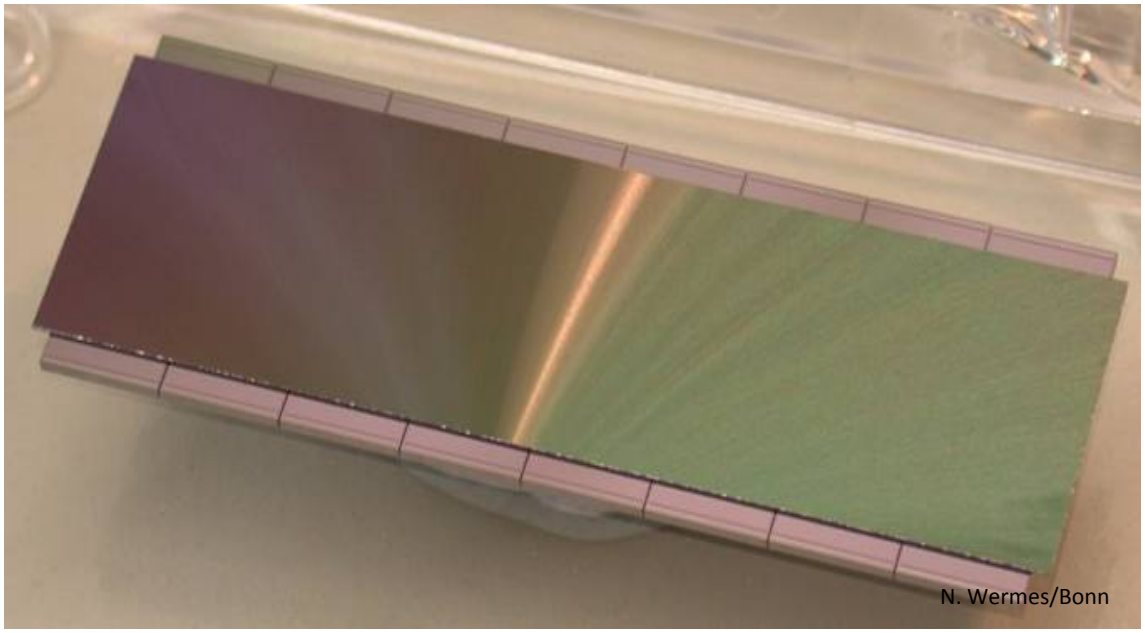
Layer 2



Disk

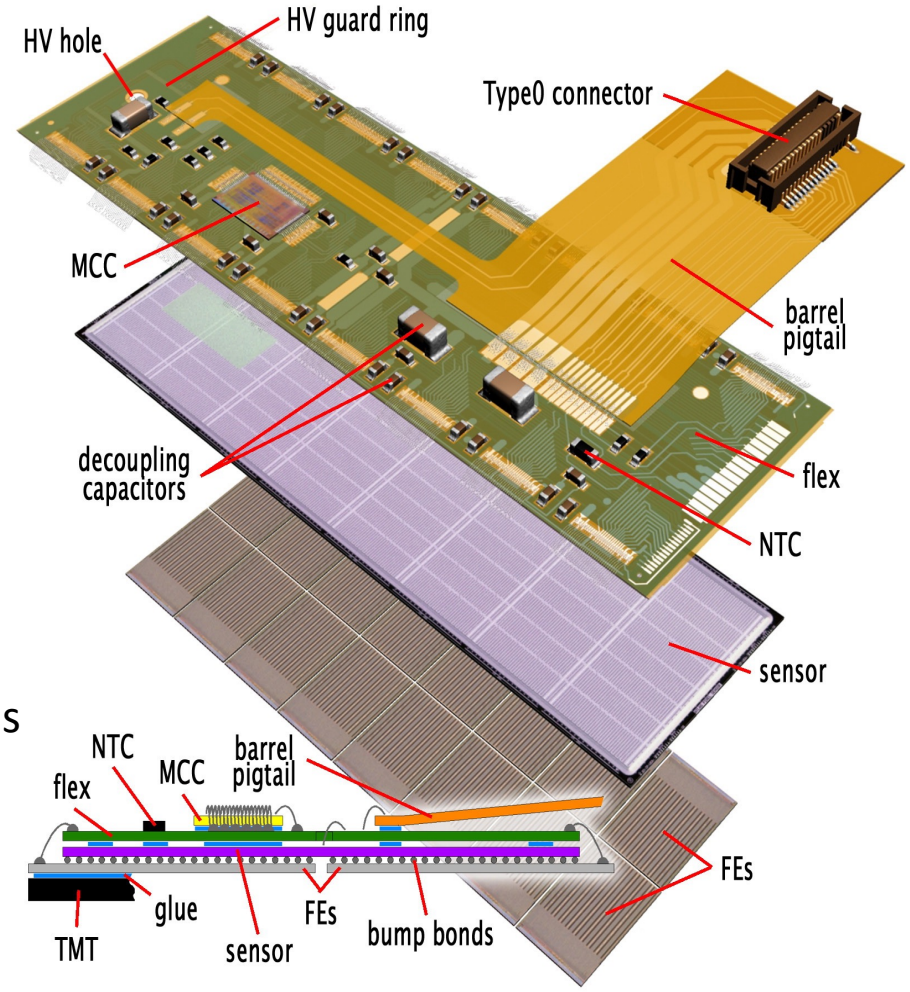
ATLAS Pixel Detector

- Hybrid silicon pixel detector
- 16 readout chips connected to 1 sensor (6.4 cm x 2.1 cm)



ATLAS Pixel Module

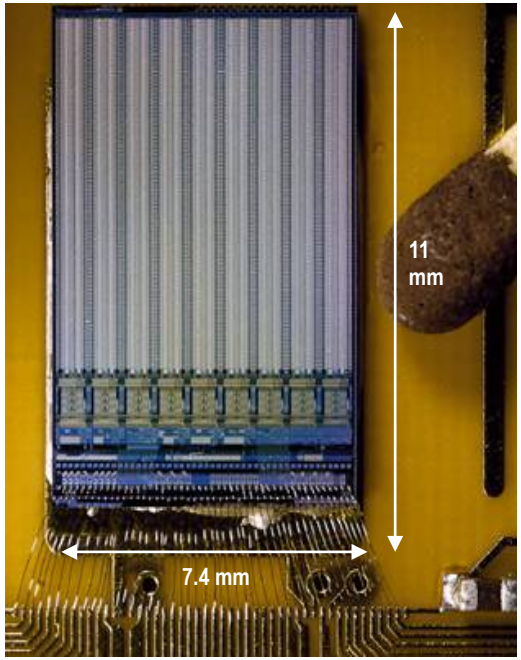
- **Sensor**
  - 47232 n-on-n pixels
  - 250 μm thickness
  - 50 μm (Rϕ) × 400 μm (z)
  - 328 rows (x_{local}) × 144 columns (y_{local})
- **16 FE chips**
  - bump bonded to sensor
- **Flex Hybrid**
  - passive components
  - Module Controller Chip
    to perform distribution of commands and event building.
- **Radiation-hard design:**
  - Dose >500 Gy
  - NIEL >10^{15} n_{eq}/cm^2 fluence



ATLAS Pixel Module

Front End Chips

- operation @ 40 MHz
- zero suppression in every pixel
- data buffering until trigger (2.5 µs later)
- amplitude via pulse width (ToT)
- noise ~160e^- (on module)
- thres. dispersion ~600e (< 100e after tuning)
- thinned to 180 µm



CMS (Compact Muon Solenoid) – Detector Layout

Three barrel layers:

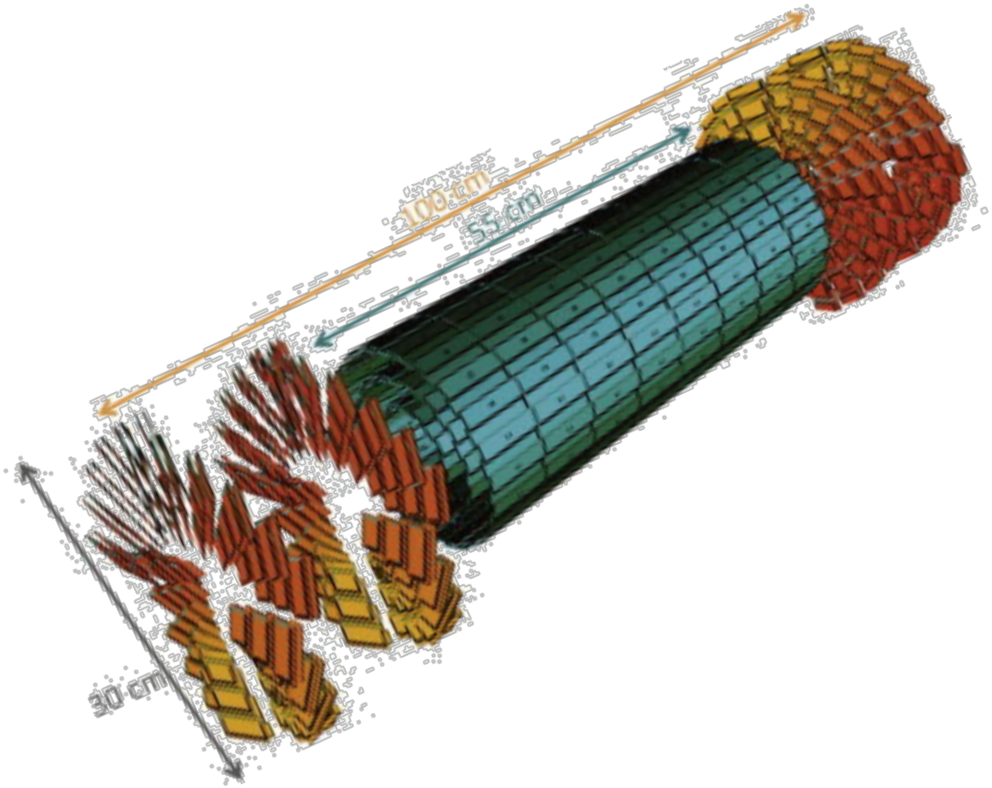
- R=4.4 cm
- R=7.3 cm
- R=10.2 cm

Forward disks:

- 2 forward disks on either side

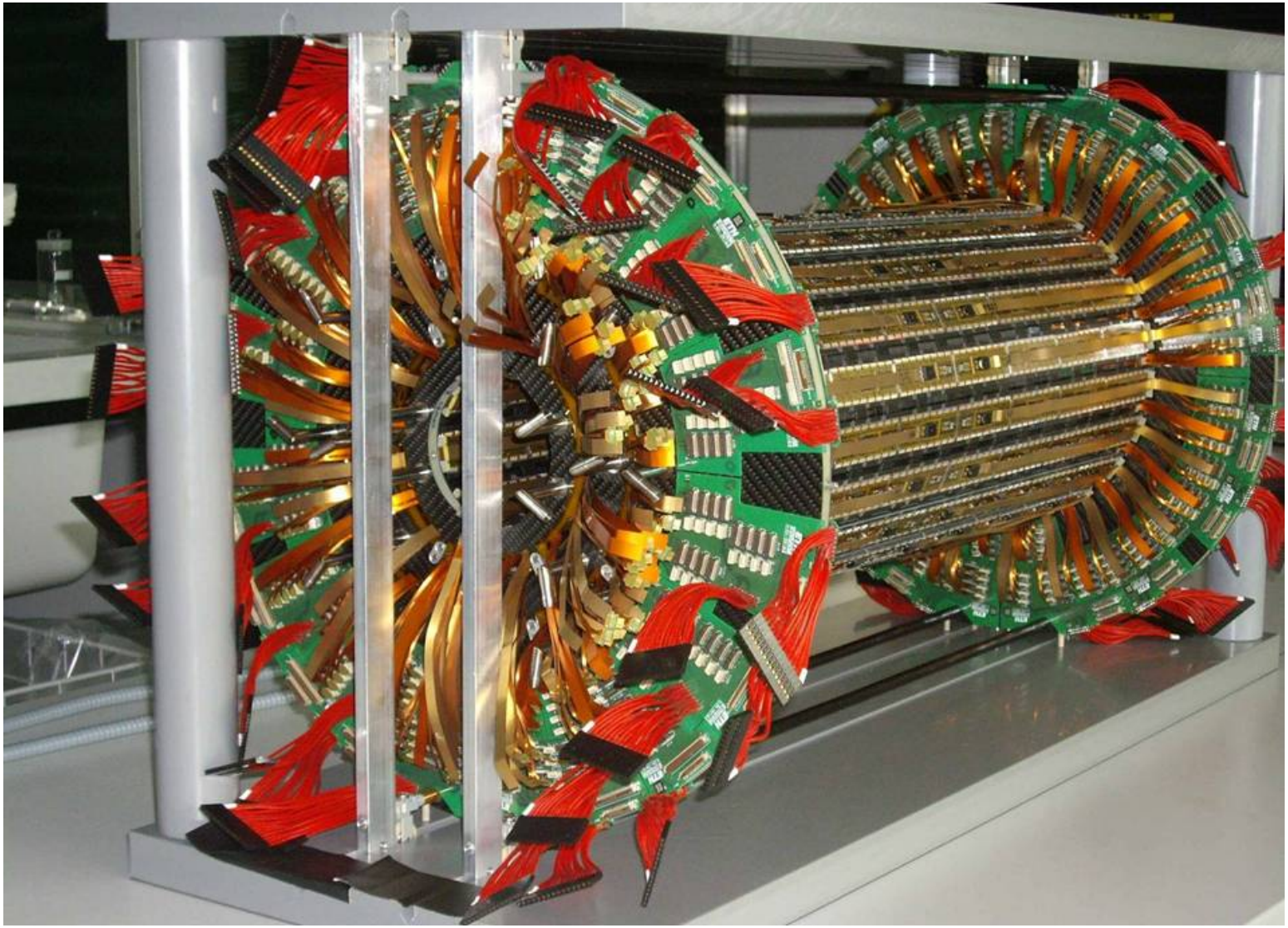
- 66 mio. channels
- Area ~1 m2

- 1440 modules
- 15840 readout chips
- Environmental Temperature: -8°C
- 4T magnetic field

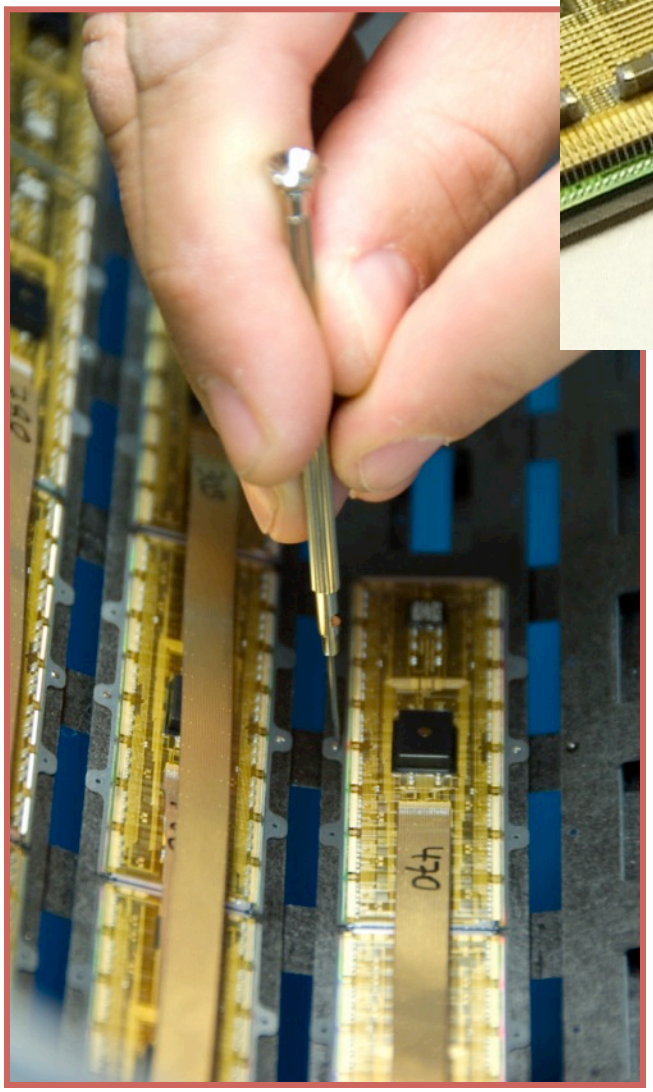


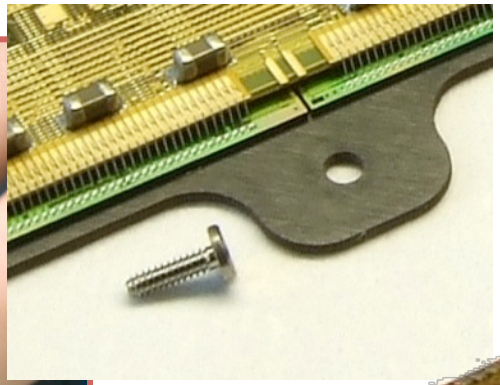
NIM A, 2013
http://dx.doi.org/10.1016/j.nima2013.04.001

CMS Pixel Detector



CMS Pixel Module





Kapton signal cable
21 traces, 0.3mm pitch

Alu-power cable
6 x 250μ ribbon

High Density Print
3 Layers, 48μ thick

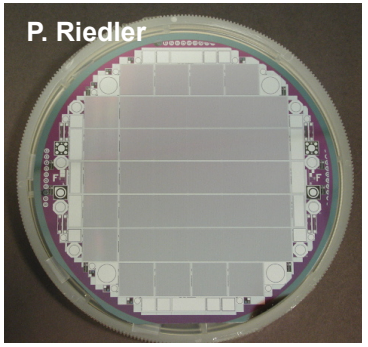
N-in-n Silicon Sensor
t=285μ
100μ x 150μ pixels

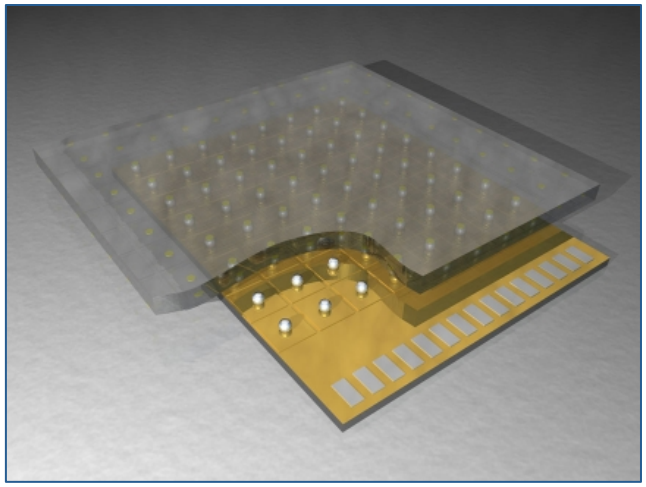
16 x Readout Chips
(CMOS) 175μ thick
4160 pixels/chip

SiN base strips
250μ thick, screw holes

Beyond Hybrid Pixel Detectors …

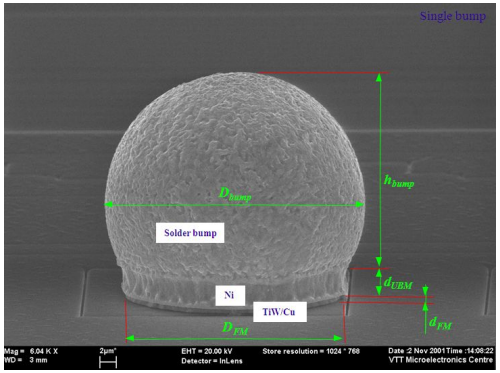
- Limited number of sensors producers (~10 world-wide)
- no industrial scale production ➔ high cost



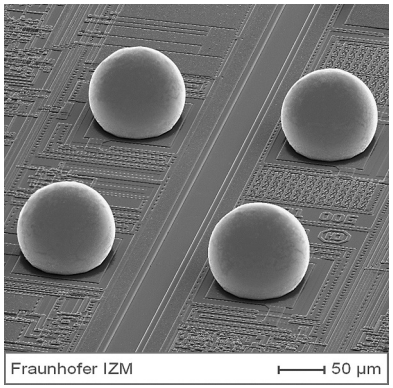


Azom.com

- Complex and costly interconnection between sensors and ASIC
- Interconnection technology (micro-bump bonding) limits:
  - pitch (currently ~30μm)
  - input capacitance ➔ power



VTT Microelectronics Centre



Fraunhofer IZM

Lower production cost

Higher integration (pitch, x/X_0)

Lower power (x/X_0, cost)

… Monolithic Pixel Detector

Monolithic pixel detectors for HEP exist in many different flavors, each with many different parameters …

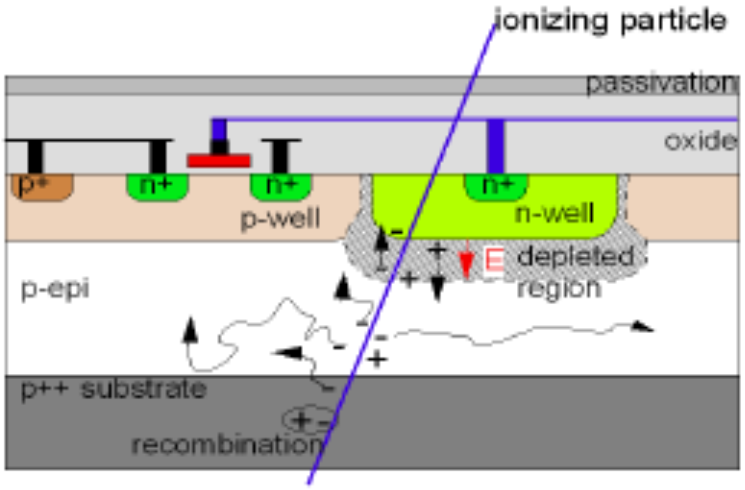
… for a comprehensive review of CMOS Pixel sensors see CPIX2014

Common points

- Profit from standard industrial CMOS processing (many foundries, larger wafer diameter, potentially **low cost per area**, stitching, …)
- **Thin detectors** (O(50μm Si)) ➔ low material budget
- **High granularity** (small cell size)
- **Low power** (small detector capacitance)
- No need for cost intensive chip-to-chip bump bonding

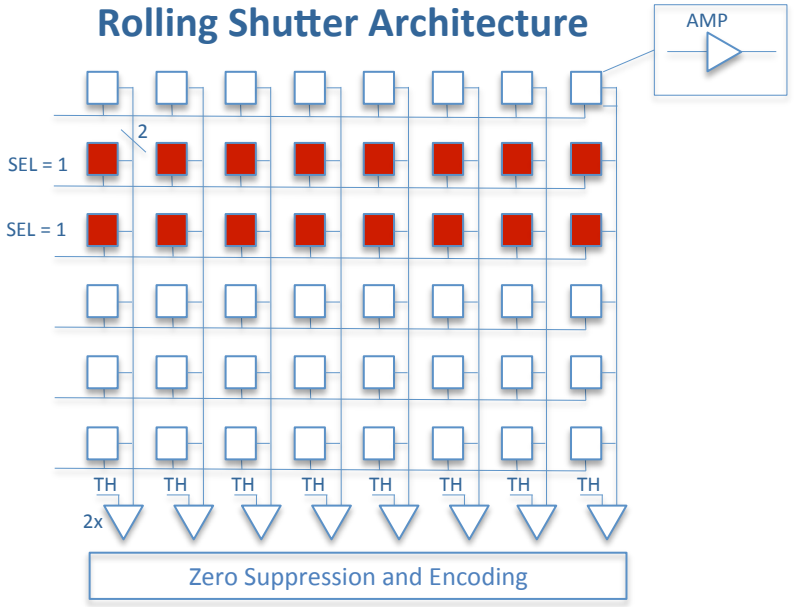
Classical CMOS Pixel Sensor

- n-well charge collector in p-type epitaxial layer
- Signal generated in a high-resistivity (> 1 kΩcm) epi-layer ~20μm thick (larger values possible)
- (Early versions with thin and low resistivity epi-layer)
- MIP produces ~80 e-h pairs per micron



M. Winter et al. (IPHC)

- epi-layer not fully depleted
- Charge collected by (mostly) diffusion and drift
- Longer charge collection time
- More sensitive to radiation induced displacement damage in the epi layer
- Only one transistor type in the active area (NMOS)
- Often use rolling shutter architecture for reading out the matrix



Pixel Detectors in HEP – Inner Tracking Region

	Inter. Rate (Hz)	Particle Rate [kHz/mm^2]	Fluence [n_{eq}/cm^2 per lifetime]	Ionization dose [Mrad per year]
LHC (10^{34} cm^{-2}s^{-1})	10^9	10^3	2×10^{15}	79
HL-LHC (10^{35} cm^{-2}s^{-1})	6×10^{10}	10^4	2×10^{15}	> 500
LHC HL-HI (6 x 10^{27} cm^{-2}s^{-1})	10^5	10	< 10^{13}	0.1
RHIC (8 x 10^{27} cm^{-2}s^{-1})	10^5	3.8	few 10^{12}	0.2
FAIR CBM	10^6		10^{13}	0.1
SuperKEKB (8 x 10^{35} cm^{-2}s^{-1})		400	3×10^{12}	10
ILC (10^{34} cm^{-2}s^{-1})		250	10^{12}	0.4

Monolithic Pixels
- Lower rates
- Lower radiation
- Smaller Pixels
- Less material

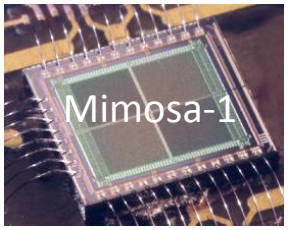
Examples: STAR HFT, BELLE II, CBM, ALICE Upgrade

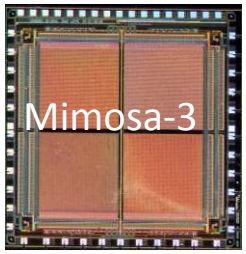
Hybrid Pixels
- High rates
- High radiation

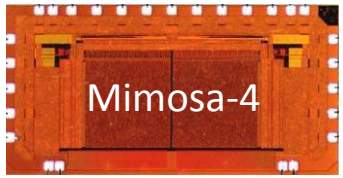
Examples: ATLAS, CMS, NA62

Monolithic Pixel Detectors in HI Experiments

Owing to the industrial development of CMOS imaging sensors and the intensive R&D work within the HEP community (IPHC, RAL, …)







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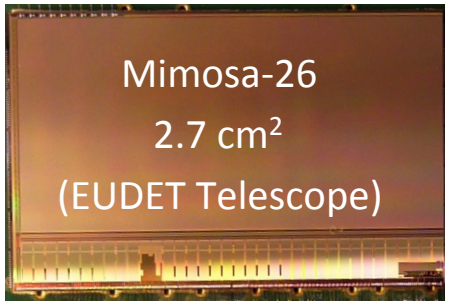
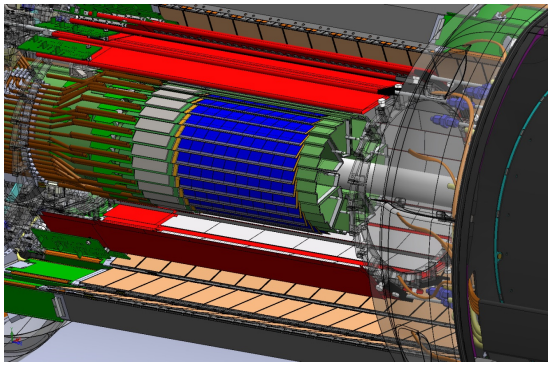
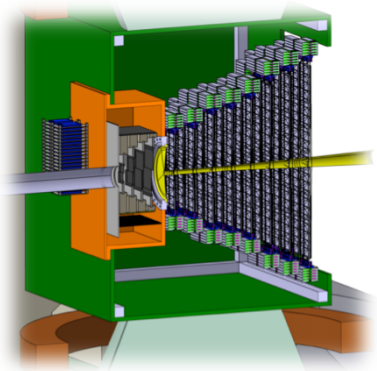


R. Turchetta, M. Winter

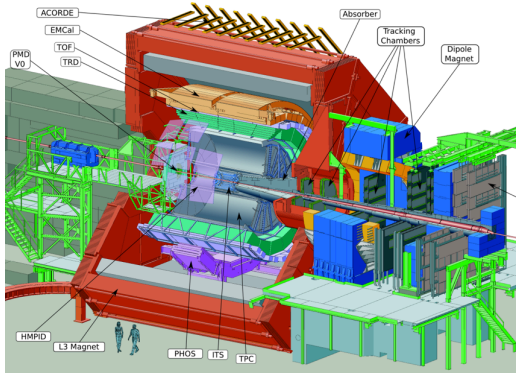
… several HI experiments have selected CMOS pixel sensors for their inner trackers



STAR HFT
0.16 m² – 356 M pixels



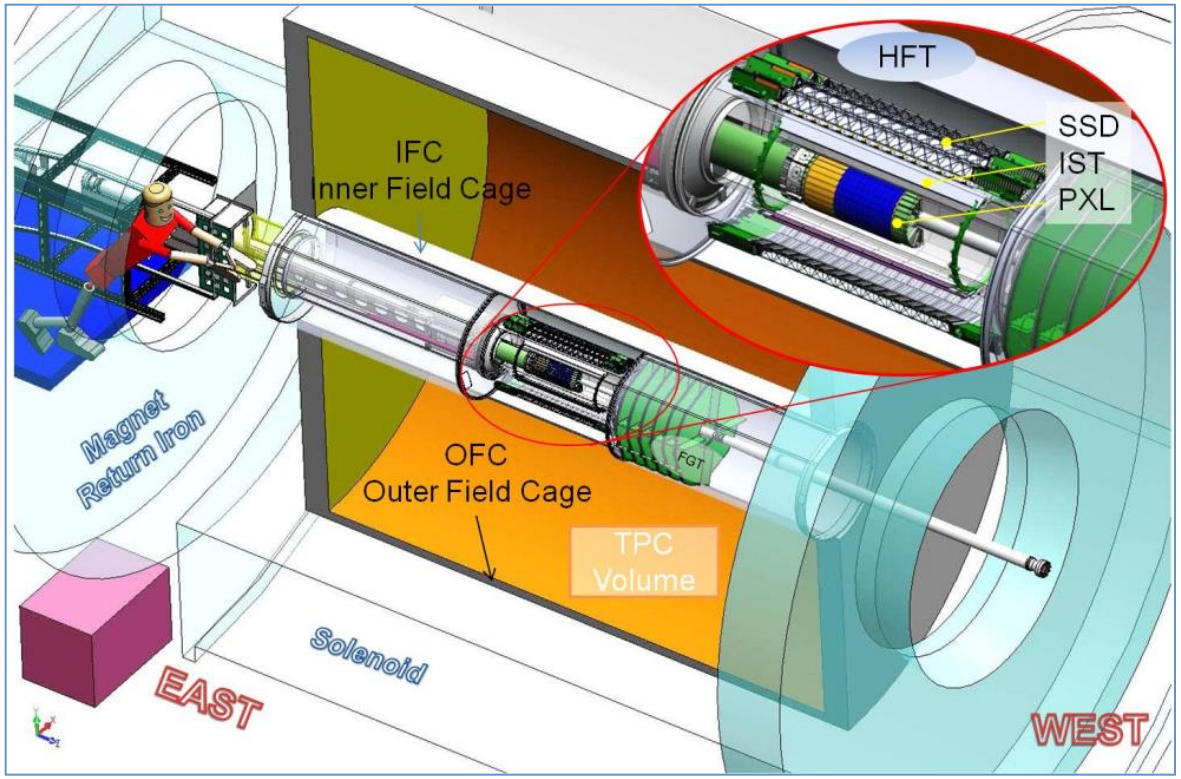
CBM MVD
0.08 m² – 146 M pixel



ALICE ITS Upgrade (and MFT)
10 m² – 12 G pixel

2014 - First CPS Detector

STAR Upgrade - Heavy Flavor Tracker (HFT)

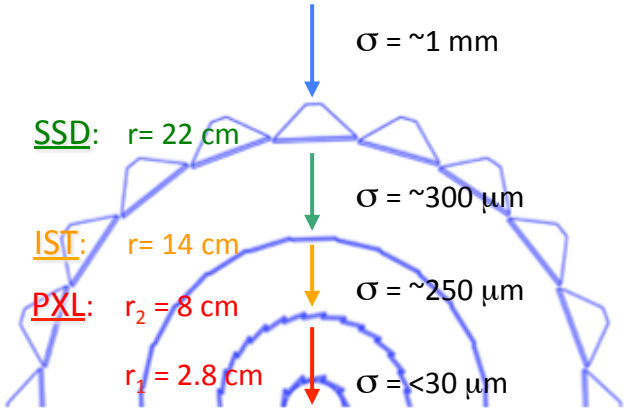


L. Greiner (LBL) / CPIX-2014

TPC – Time Projection Chamber
(main tracking detector in STAR)

HFT – Heavy Flavor Tracker

- SSD – Silicon Strip Detector
- IST – Inner Silicon Tracker
- PXL – Pixel Detector

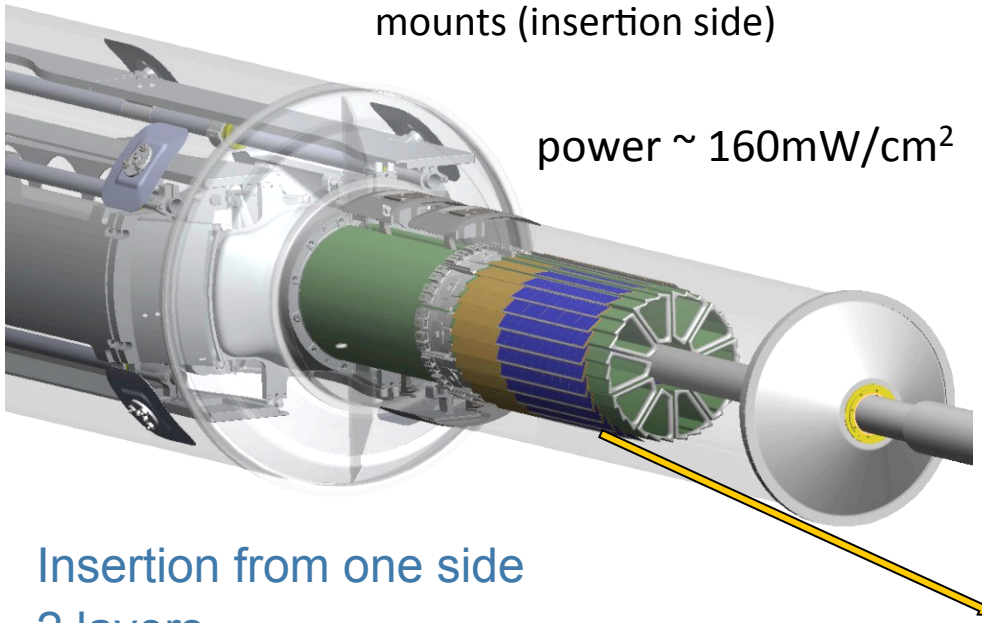


Tracking inward from the TPC with graded resolution

STAR Pixel Detector (PXL)

L. Greiner (LBL) / CPIX-2014

Mechanical support with kinematic mounts (insertion side)

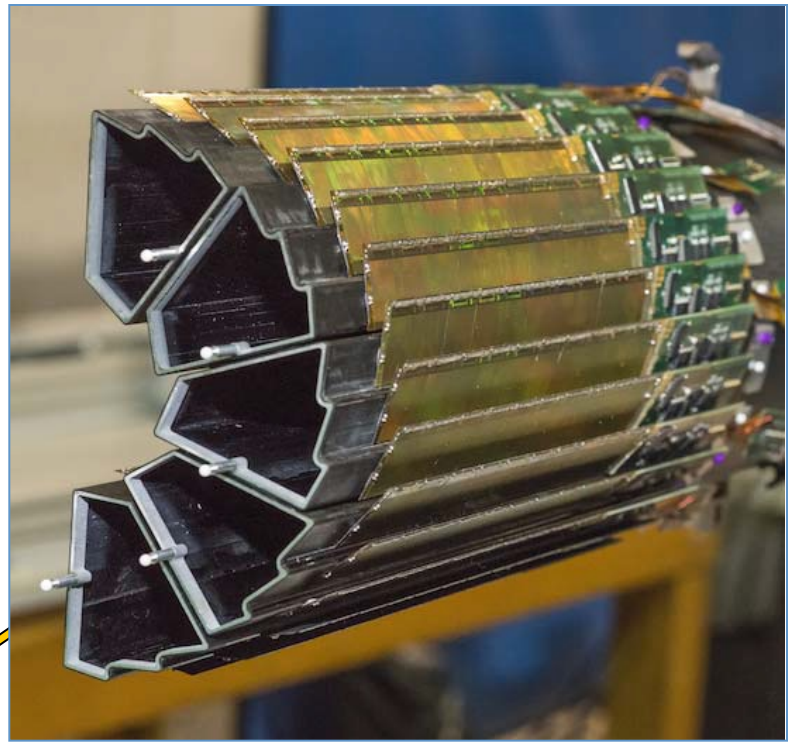


power ~ 160mW/cm^2

- Insertion from one side
- 2 layers
- 10 sectors total (in 2 halves)
- 4 ladders/sector

Key dates

- 3-sector prototype May 2013
- **Full detector Jan 2014**



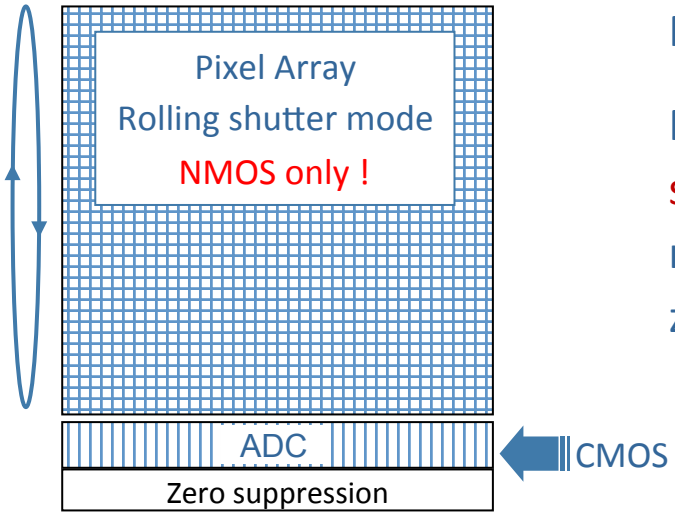
carbon fiber sector tubes
(~ 200 µm thick)

Ladder with 10 MAPS sensors (~ 2×2 cm each)

2-layer kapton flex cable with Al traces

20 cm

STAR PXL – CMOS Sensor



NMOS only in pixel array

RO architecture: rolling shutter column parallel readout with integrated zero suppression logic

Technology: AMS 0.35u

Reticle size (2x2 cm²)

Pixel pitch 20.7 µm

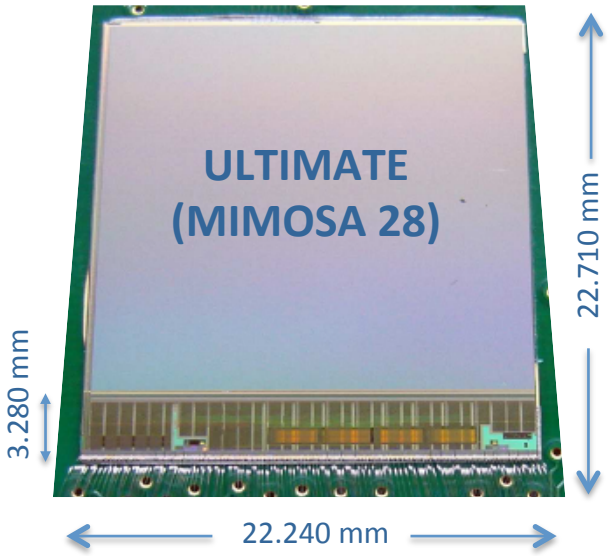
Array size: 928 x 960

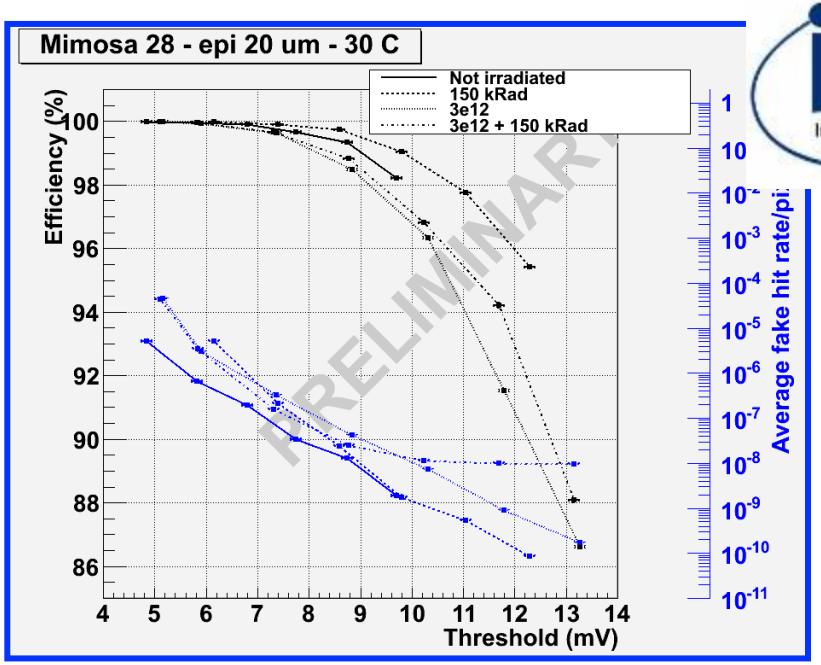
Integration time: 185.6 µs

In pixel CDS

Sensors thinned to 50 µm

High Res Si option





IPHC Institut Pluridisciplinaire Hubert CURIEN STRASBOURG

C. Hu (IPHC) / CPIX-2014

STAR PXL – Detector Design Characteristics

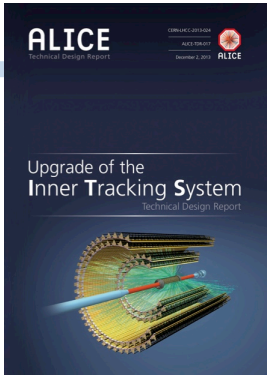
DCA Pointing resolution	$(12^{(*)} \oplus 24\ \text{GeV/p·c})\ \mu m$
Layers	Layer 1 at 2.8 cm radius Layer 2 at 8 cm radius
Pixel size	20.7 μm X 20.7 μm
Hit resolution	3.7 $\mu m^{(*)}$ (6 μm geometric)
Position stability	6 μm rms (20 μm envelope)
Radiation length first layer	x/X_0 = 0.39% (Al conductor cable)
Number of pixels	356 M
Integration time (affects pileup)	185.6 μs
Radiation environment	20 to 90 kRad / year $2*10^{11}$ to 10^{12} 1MeV n eq/cm^2
Rapid detector replacement	~ 1 day

356 M pixels on ~0.16 m^2 of Silicon

L. Greiner (LBL) / CPIX-2014

(*) Simple geometric component, cluster centriod fitting gives factor of ~1.7 better

ITS upgrade design objectives



CERN-LHCC-2013-24

1. Improve impact parameter resolution by a factor of ~3

- Get closer to IP (position of first layer): 39mm ➡ 23mm
- Reduce x/X_0 /layer: ~1.14% ➡ ~ 0.3% (for inner layers)
- Reduce pixel size: currently 50μm x 425μm ➡ O(30μm x 30μm)

J. Phys. G (41) 087002

2. Improve tracking efficiency and p_T resolution at low p_T

- Increase granularity:
  - 6 layers ➡ 7 layers
  - silicon drift and strips ➡ pixels

3. Fast readout

- readout Pb-Pb interactions at > 100 kHz and pp interactions at ~ several 10^5 Hz (currently limited at 1kHz with full ITS)

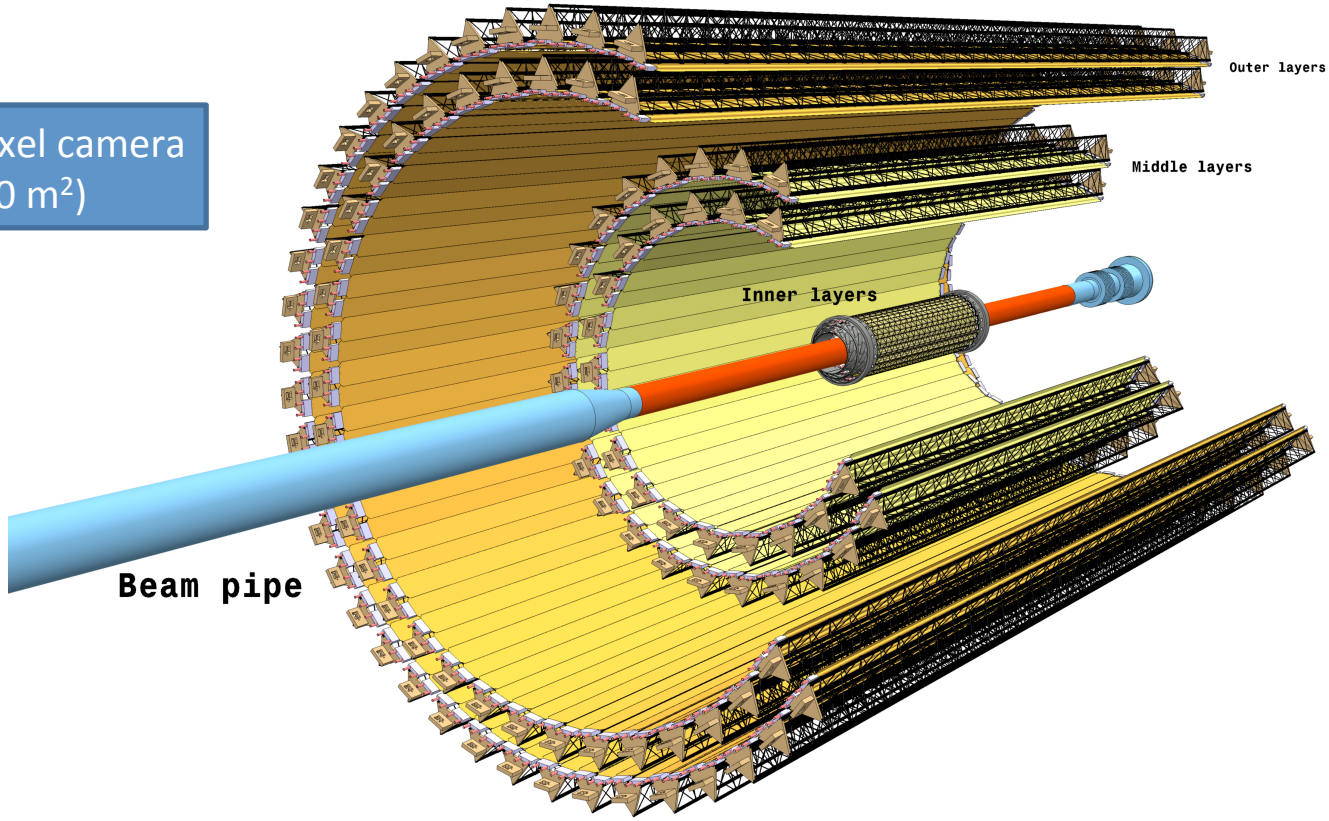
4. Fast insertion/removal for yearly maintenance

- possibility to replace non functioning detector modules during yearly shutdown

Install detector during LHCC LS2 (2018-19)

New ITS Layout

12.5 G-pixel camera
(~10 m^2)



7-layer barrel geometry based on MAPS

r coverage: 23 – 400 mm

η coverage: $|\eta| \leq 1.22$
for tracks from 90% most luminous region

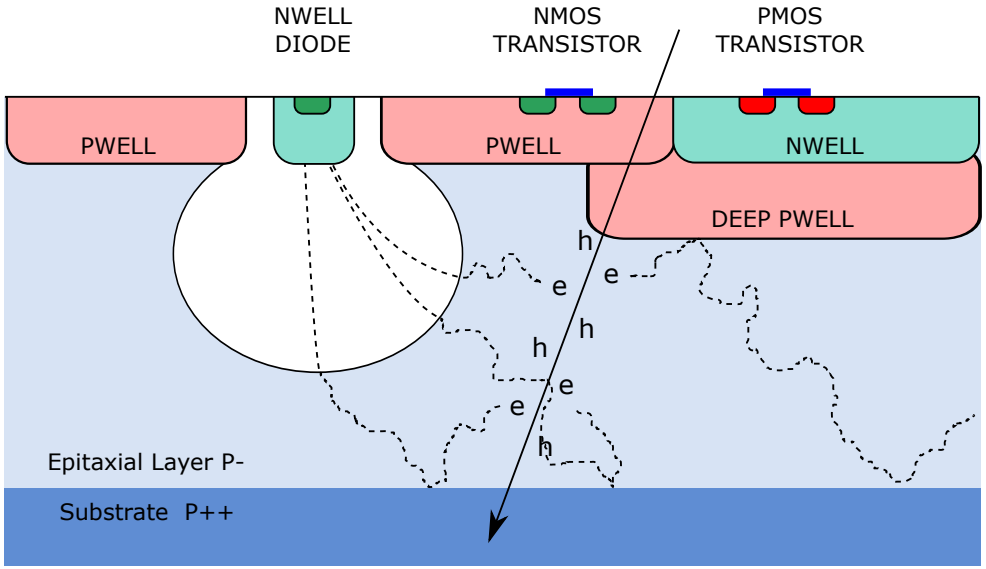
3 Inner Barrel layers (**IB**)

4 Outer Barrel layers (**OB**)

Material /layer : 0.3% X_0 (IB), 1% X_0 (OB)

ITS Pixel Chip – technology choice

CMOS Pixel Sensor using TowerJazz 0.18μm CMOS Imaging Process



Tower Jazz 0.18 μm CMOS

- feature size 180 nm
- metal layers 6

➔ Suited for high-density, low-power

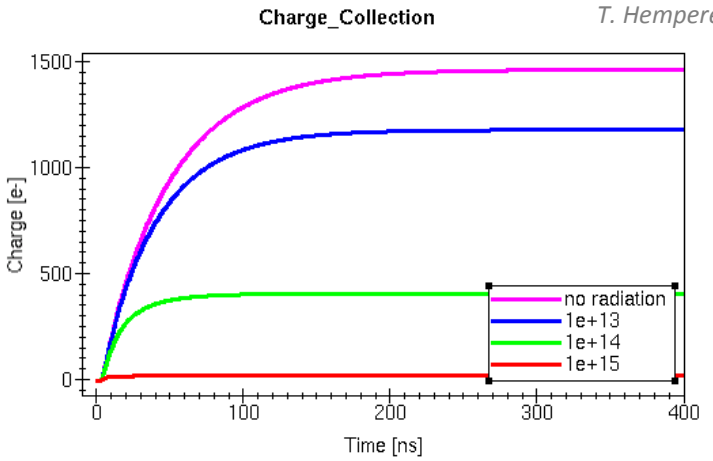
- Gate oxide 3nm

➔ Circuit rad-tolerant

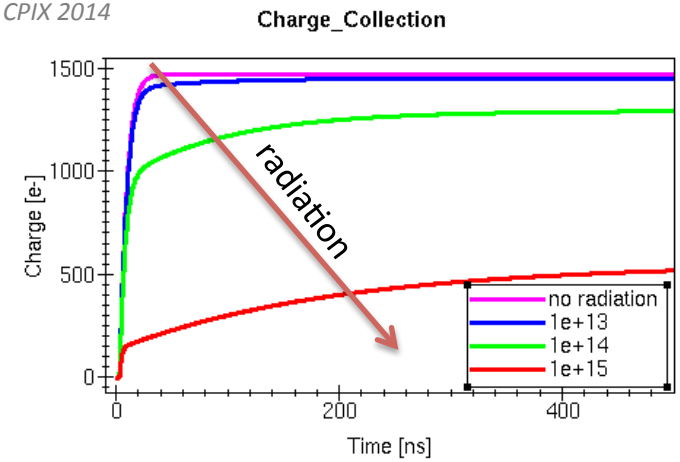
- High-resistivity (> 1kΩ cm) p-type epitaxial layer (20μm - 40μm thick) on p-type substrate
- Small n-well diode (2-3 μm diameter), ~100 times smaller than pixel => low capacitance
- Application of (moderate) reverse bias voltage to substrate can be used to increase depletion zone around NWELL collection diode
- Quadruple well process: deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area

ITS Pixel Chip – starting material

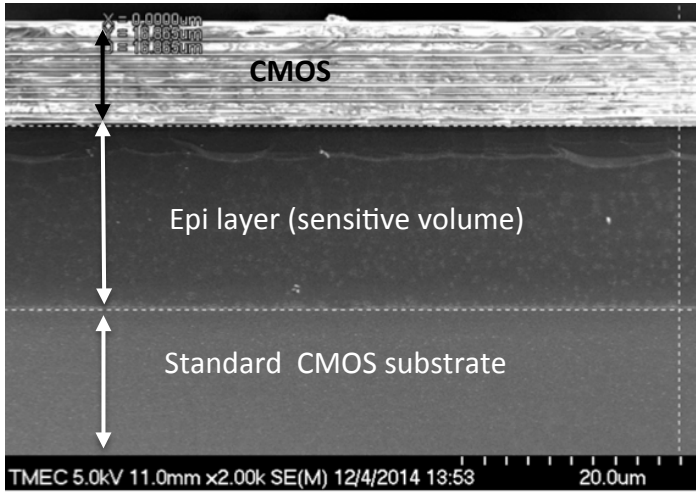
Charge collection time and recombination depend on doping concentration (Si resistivity) and radiation induced dislocations



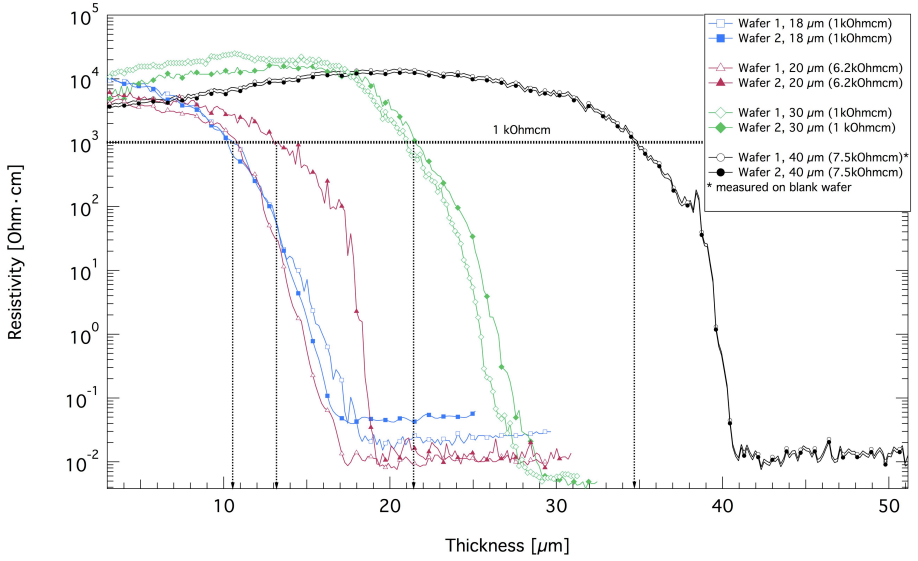
Substrate: 10 Ohm cm, NWELL: @1V PW: @ 0V



Substrate: 2k Ohm cm, NWELL: @1V PW: @ 0V

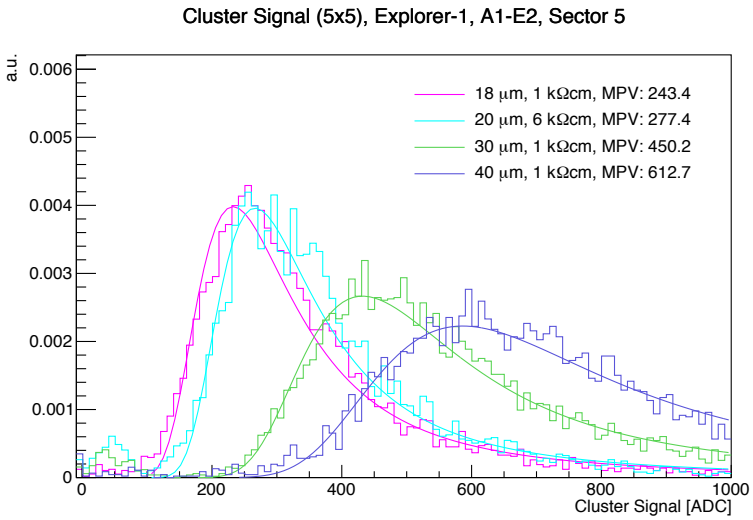


SEM picture: epi thickness 20µm



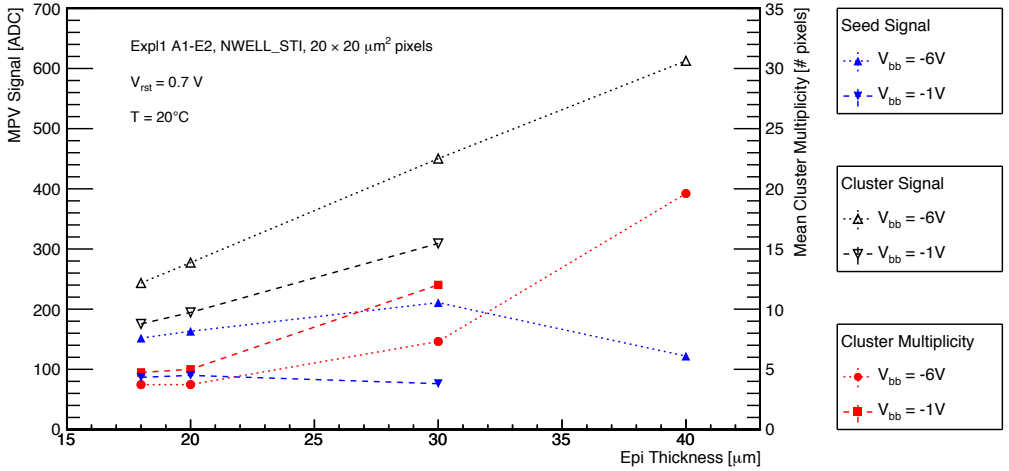
ITS Pixel Chip – starting material

Thicker epitaxial layers will yield more charge but … diffusion increases cluster size



J. Van Hoorne, TIPP2014

J. Phys. G (41) 087002



Measurements done at Desy test beam with 3.2 Gev/c positrons

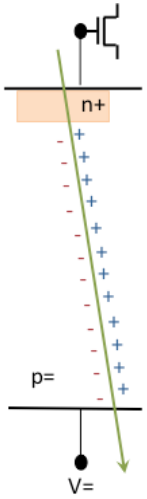
- Cluster charge increases linearly with epi-layer thickness
- Cluster size increases with epi-layer thickness

optimum epi thickness (maximum seed signal) increases by increasing depletion volume

ITS Pixel Chip – starting material

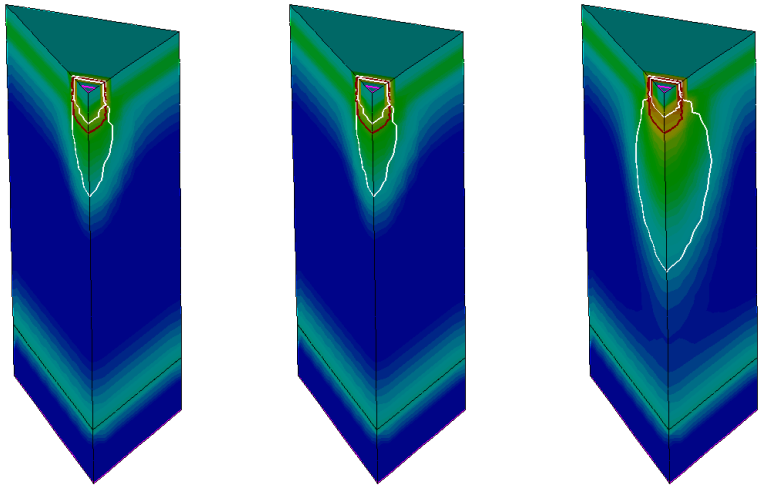
Low input capacitance decisive to achieve large S/N at low power

(W. Snoeys, NIMA 731 (2013) 125-130)



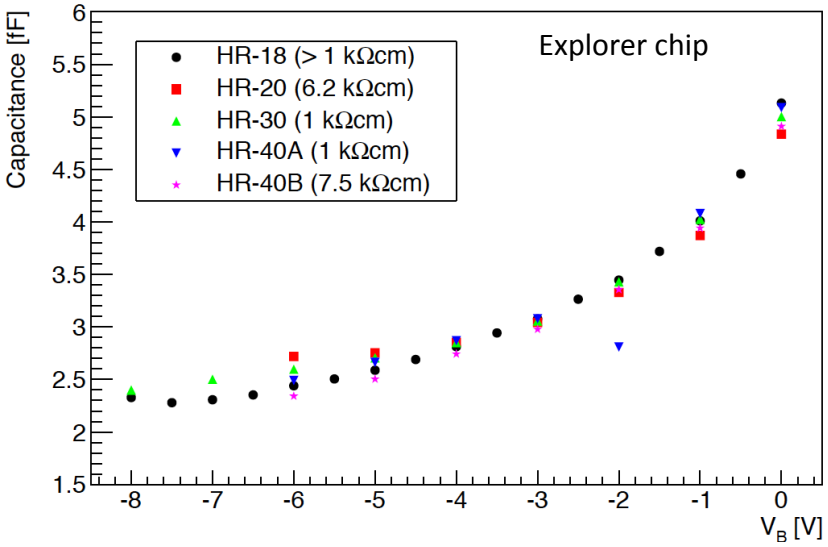
NWELL DIODE output signal = Q /C

- Minimize spread of charge over many pixels
- minimize capacitance:
  - ➡ small diode surface
  - ➡ large depletion volume



-1V, 1x10^{13} cm^{-3} -1V, 1x10^{12} cm^{-3} -6V, 1x10^{12} cm^{-3}

Diode 3µm x 3µm square n-well , White line: boundaries of depletion region



☞ Pixel input capacitance decreases with increasing reverse bias, in agreement with simulated size of depletion region

☞ Minor influence of epi resistivity for current pixel layout

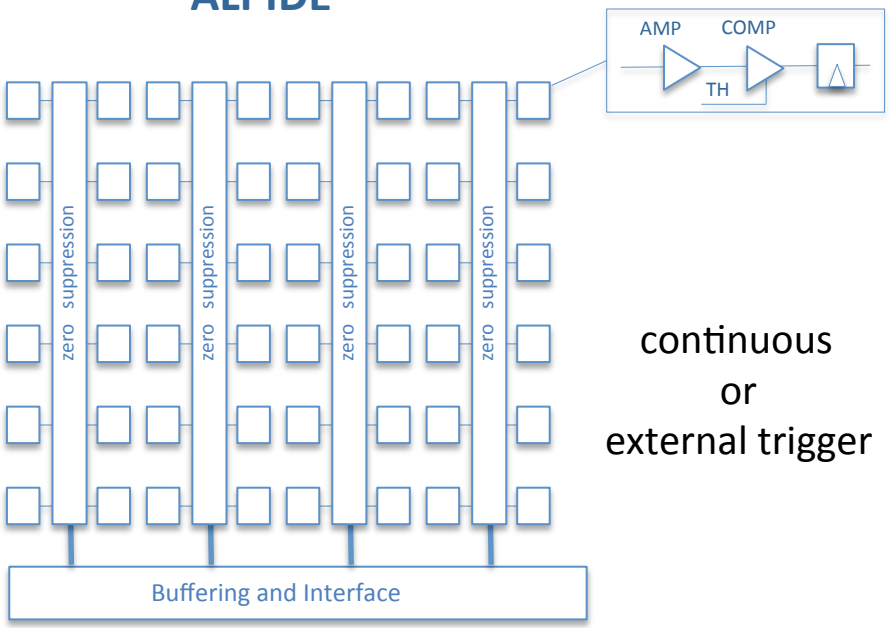
PIXEL Chip – General Requirements

Parameter	Inner Barrel	Outer Barrel
Silicon thickness	50 μm	
Spatial resolution	5 μm	10 μm
chip dimensions	15 mm x 30 mm	
Power density	< 300 mW/cm^2	< 100 mW/cm^2
Event time resolution	< 30 μs	
Detection efficiency	> 99%	
Fake hit rate	< 10^{-5} per readout frame	
TID radiation hardness (*)	2700 krad	100 krad
NIEL radiation hardness (*)	1.7x10^{13} 1MeV n_{eq}/cm^2	10^{12} 1MeV n_{eq} / cm^2

(*) 10 x radiation load integrated over approved programme (~ 6 years of operation)

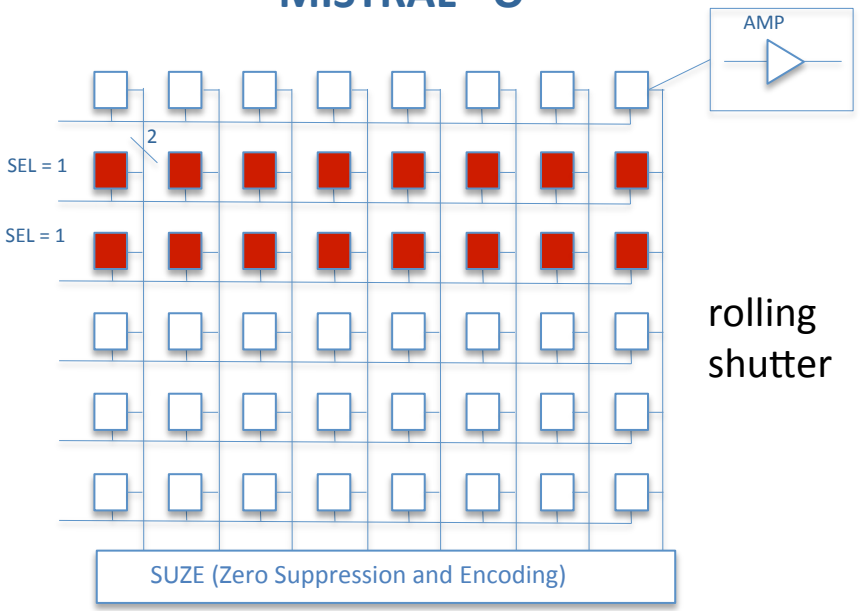
ITS Pixel Chip – two architectures

ALPIDE



continuous
or
external trigger

MISTRAL - O



rolling
shutter

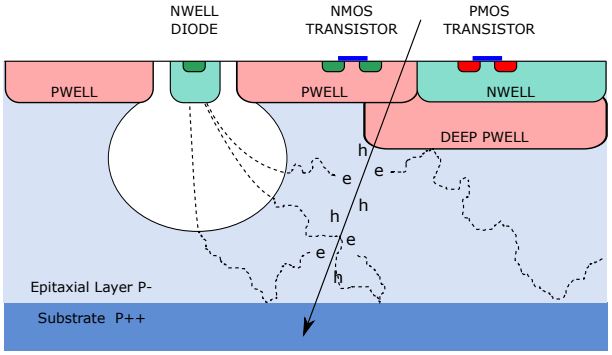
Pixel pitch	28μm x 28μm
Event time resolution	<2μs
Power consumption	39mW/cm^2
Dead area	1.1 mm x 30mm

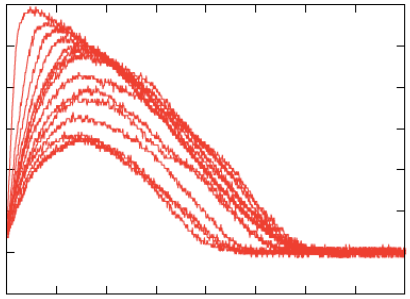
Pixel pitch	36μm x 64μm
Event time resolution	~20μs
Power consumption$^{(*)}$	97mW/cm^2
Dead area	1.7 mm x 30mm

ALPIDE and MISTRAL-O have same dimensions (15mm x 30mm), identical physical and electrical interfaces: position of interface pads, electrical signaling, protocol

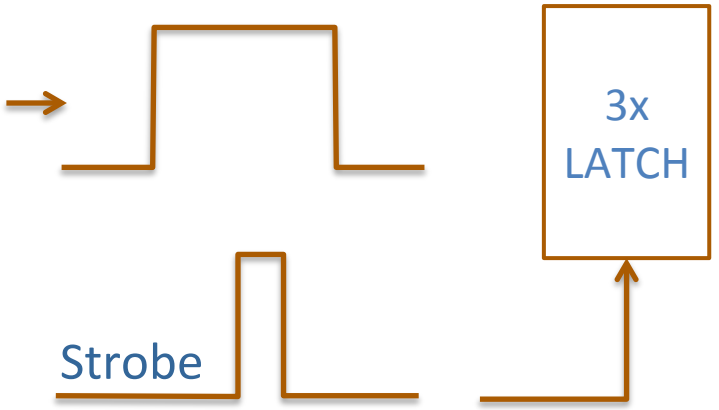
$^{(*)}$ might further reduce to 73mW/cm^2

ALPIDE Principle of Operation





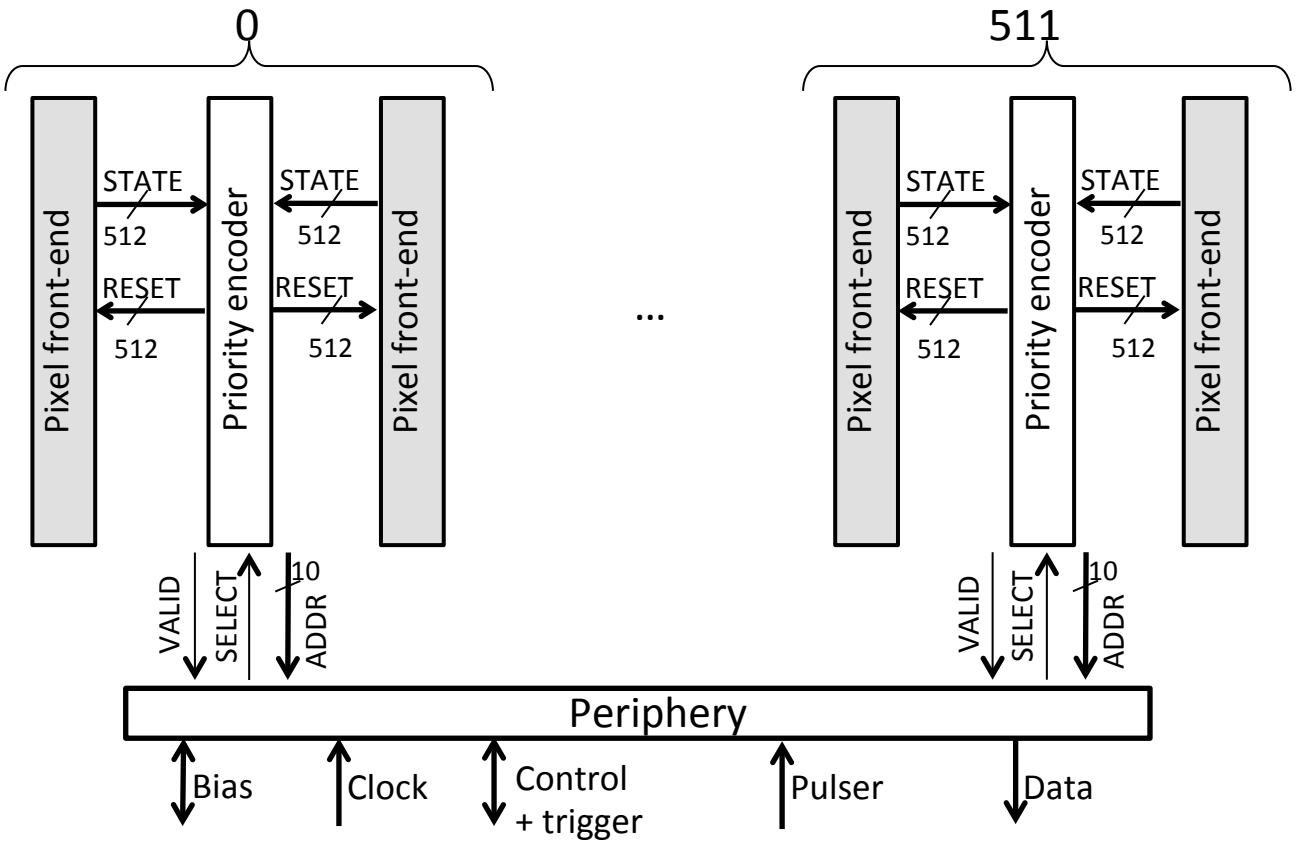
particle hit



Front-end acts as a delay line

- Sensor and front-end continuously active
- Upon particle hit front end forms a pulse with ~ 1-2 µs rise time
- Threshold is applied to form binary pulse
- Hit is latched into memory if strobe is applied during binary pulse

ALPIDE Principle of Operation



Hit driven architecture

- Priority encoder sequentially provides addresses of all hit pixels present in double column
- No activity if no hit ➔ low power

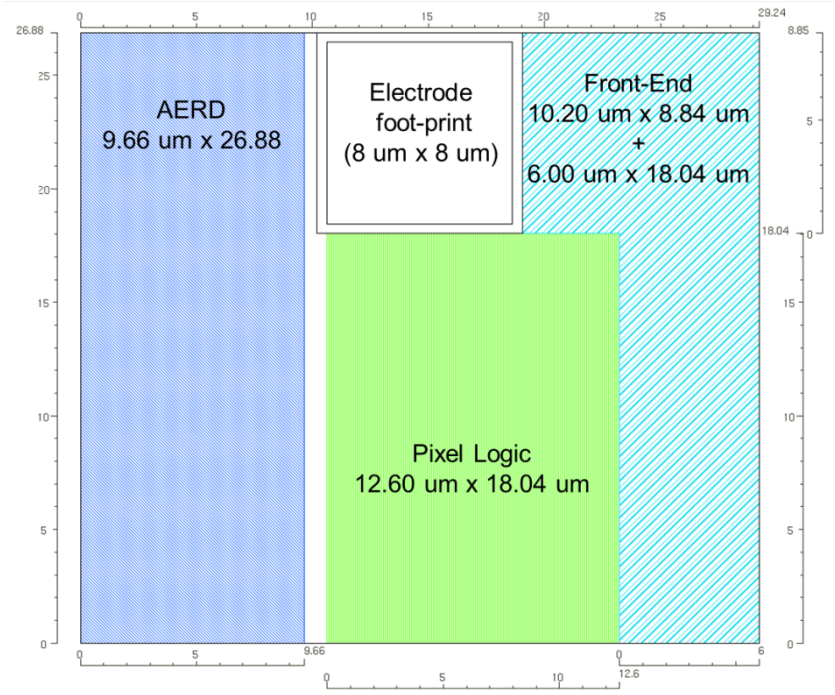
pALPIDE-3 - single pixel floorplan and laoyut

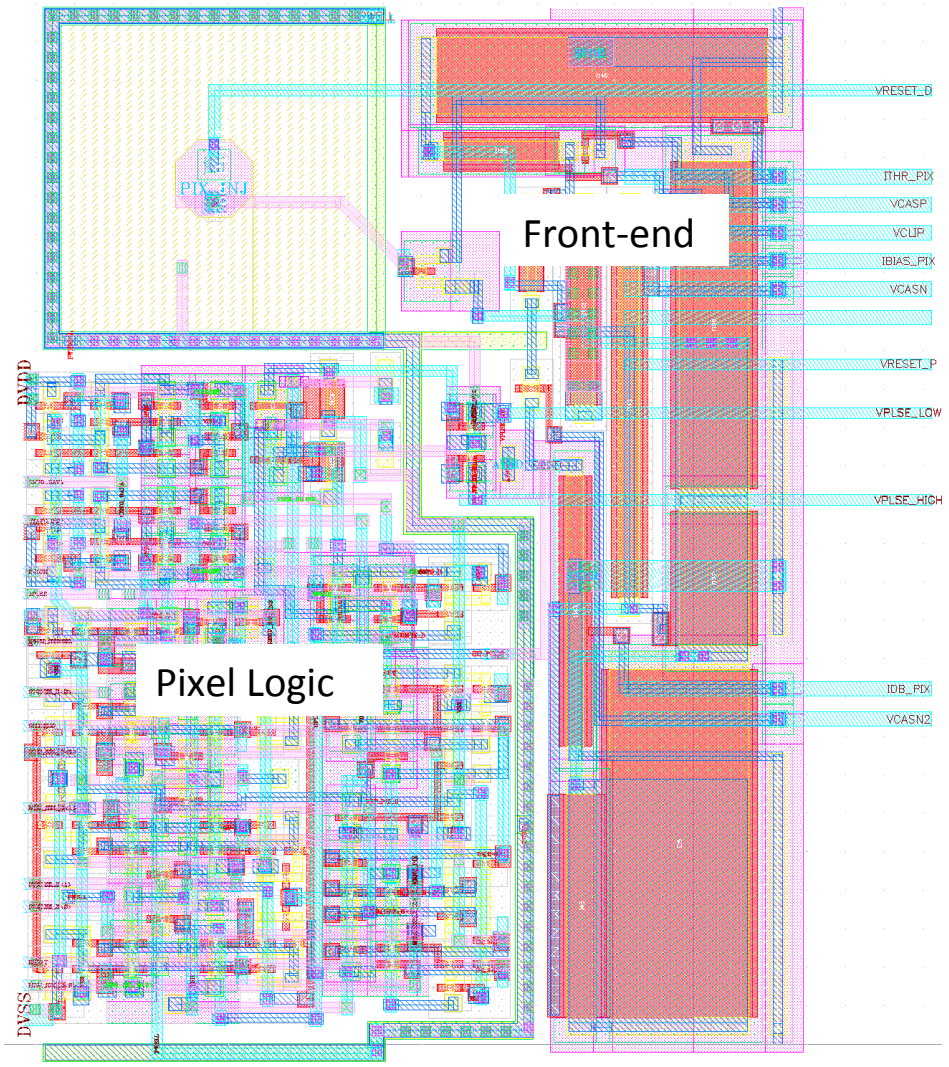
Final pixel size: 29.250 μm × 26.880 μm (w × h)

Collection diode 8 um
- 2 μm nwell width
- nwell-pwell spacing 3 μm

150 transistors

W 29.24 um
H 26.88 um

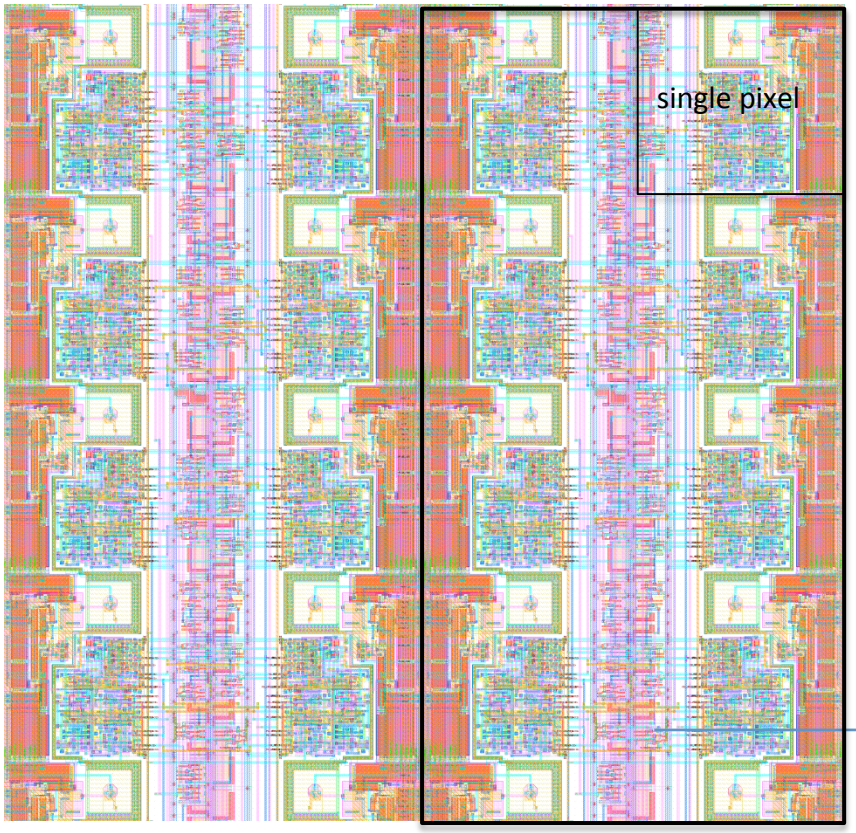




pALPIDE-3 – matrix layout

Pixel matrix (1024×512) size: 29.952 mm × 13.763 mm

4 x 5 pixels



Priority Encoder implemented with standard cells

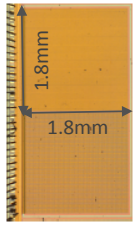
8 sectors
128 columns/sector
width 3.74 mm/sector

Pixel double column

ALPIDE Development

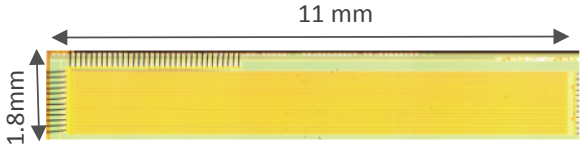
2012 — **Explorer**

- 20μm x 20μm and 30μm x 30μm pixels (analogue readout)
- pixel geometry, starting material, sensitivity to radiation



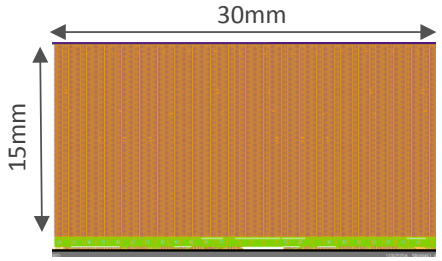
2013 — **pALPIDEss-0**

- Matrix with 64 columns x 512 rows
- 22μm x 22μm pixels
- (in-pixel discrimination and buffering)
- zero suppression within pixel matrix



May-2014 — **pALPIDE-1**

- **Full-scale prototype:** 1024 x 512
- 4 sectors with different pixels
- Final pixel pitch: 28μm x 28μm
- Interface pads over matrix
- 1 register/pixel, no final interface



Apr-2015 — **pALPIDE-2**

- Optimization of some circuit blocks
- Final interface: allows integration into ITS modules
- NO high-speed output link (1.2 Gbit/sec replaced by a 40Mb/s)

pALPIDE-1 – Main Design Features

ALICE

ALPIDE Full Scale prototype

- Dimensions: 30mm x 15 mm
- Pixel Matrix: 1024 cols x 512 rows
- Pixel pitch: 28μm x 28μm
- Peaking time (defines time res): <2μs
- Pulse length: 10-20μs
- In-pixel discriminator + 1 register
- Power consumption: < 40mW/cm^2
- 4 sectors with different pixels

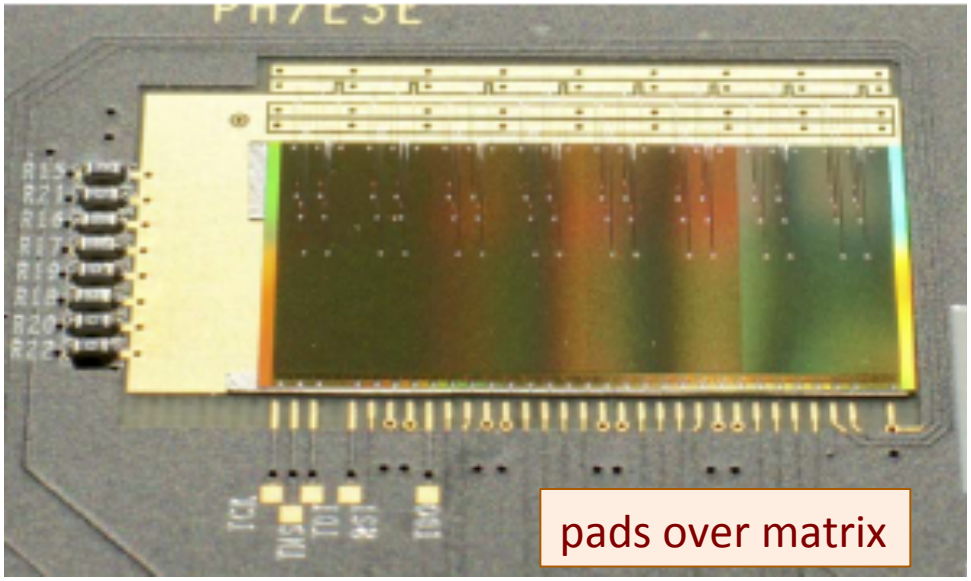
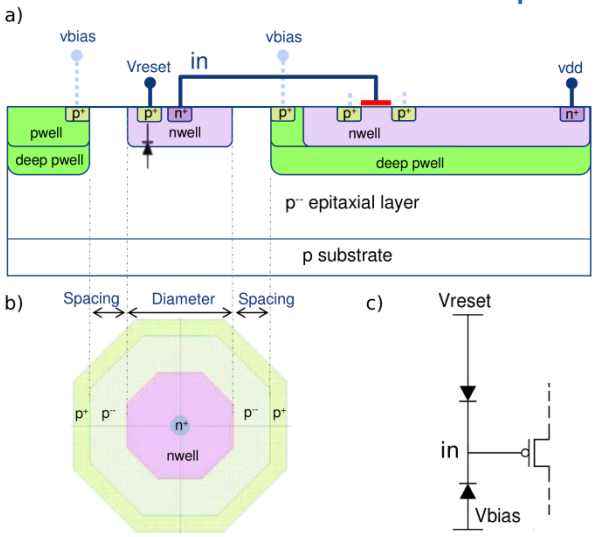


Figure: picture of pALPIDE-1



Sector	nwell diameter	spacing	pwell opening	reset
0	2μm	1μm	4μm	PMOS
1	2μm	2μm	6μm	PMOS
2	2μm	2μm	6μm	Diode
3	2μm	4μm	10μm	PMOS

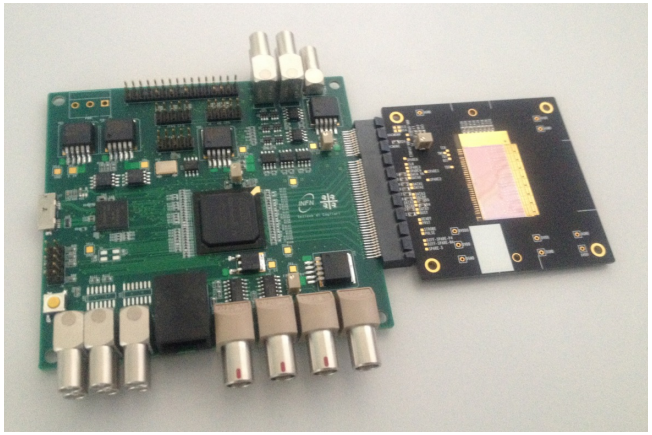
pALPIDE-1 Characterization

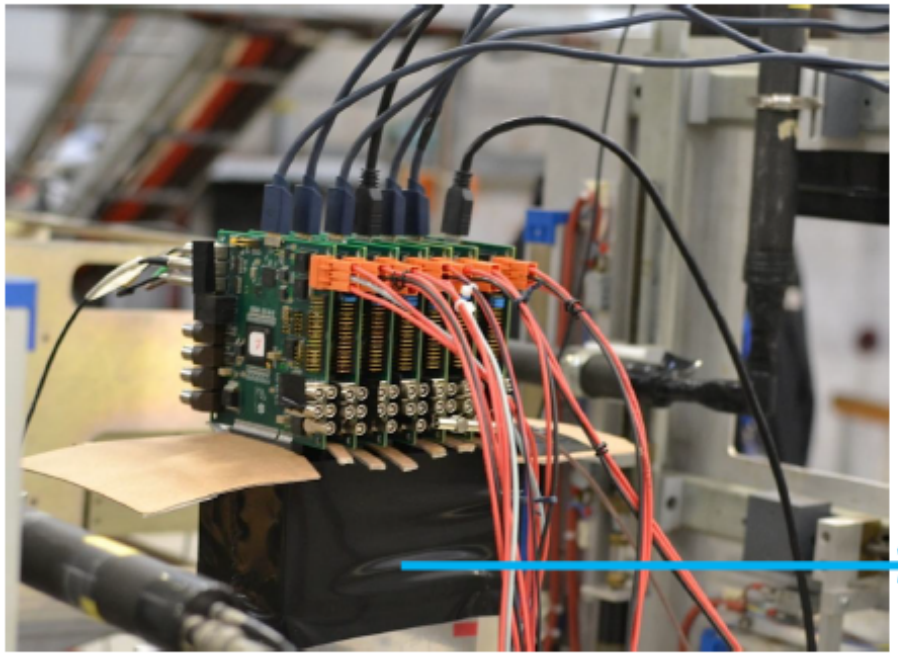
Intensive test beam campaign

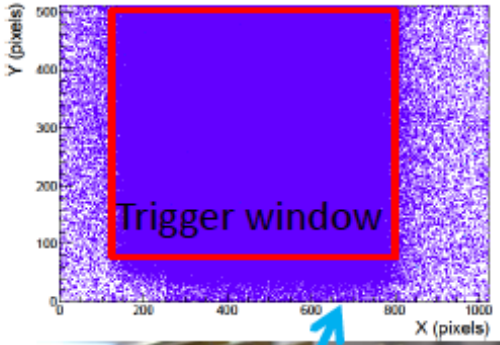
- PS: 5-7 Gev π^-
- SPS: 120 Gev π^-
- PAL (Korea): 60 MeV e^-
- BTF (Frascati): 450 MeV e^-
- DESY: 5.8 Gev e^+

Scan of main parameters ➔ ~ 200 settings

7-plane telescope based on pALPIDE-1 chip



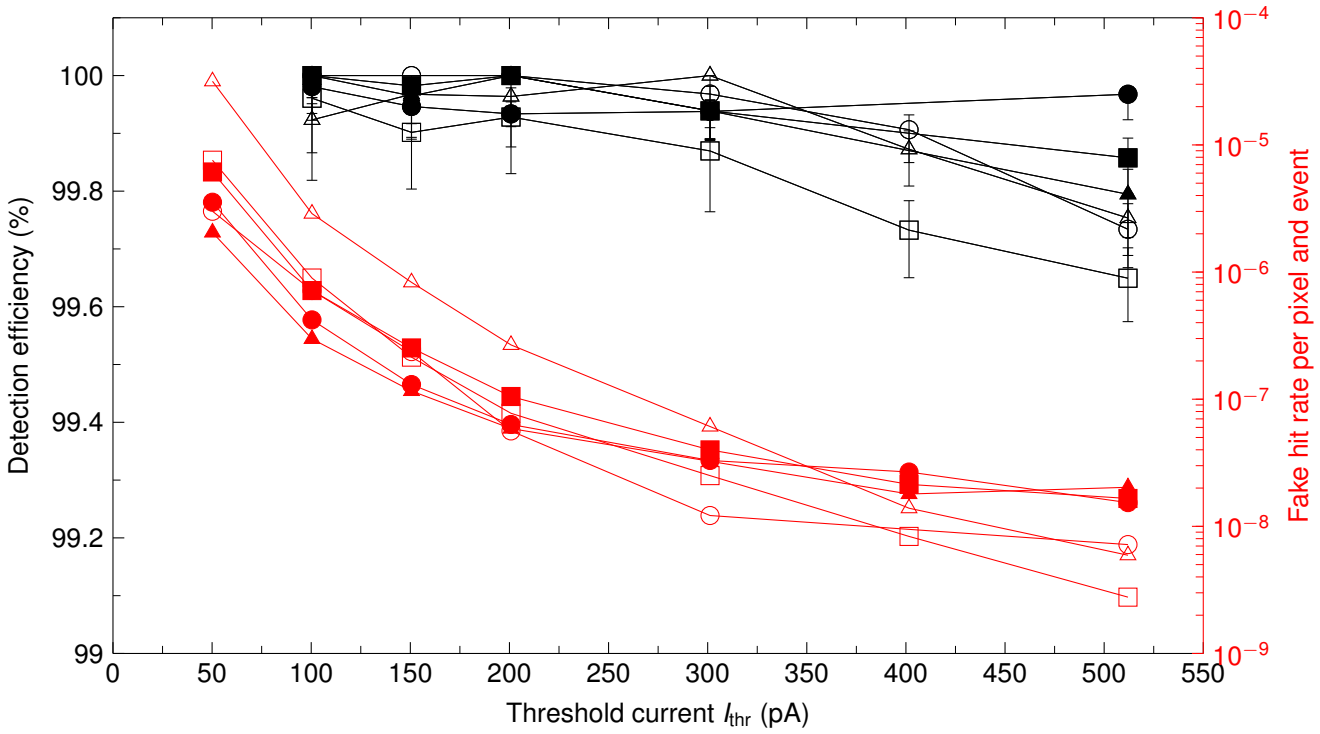




hit map

pALPIDE-1 – PS test beam (Sep 2014)

Efficiency and fake hit rate



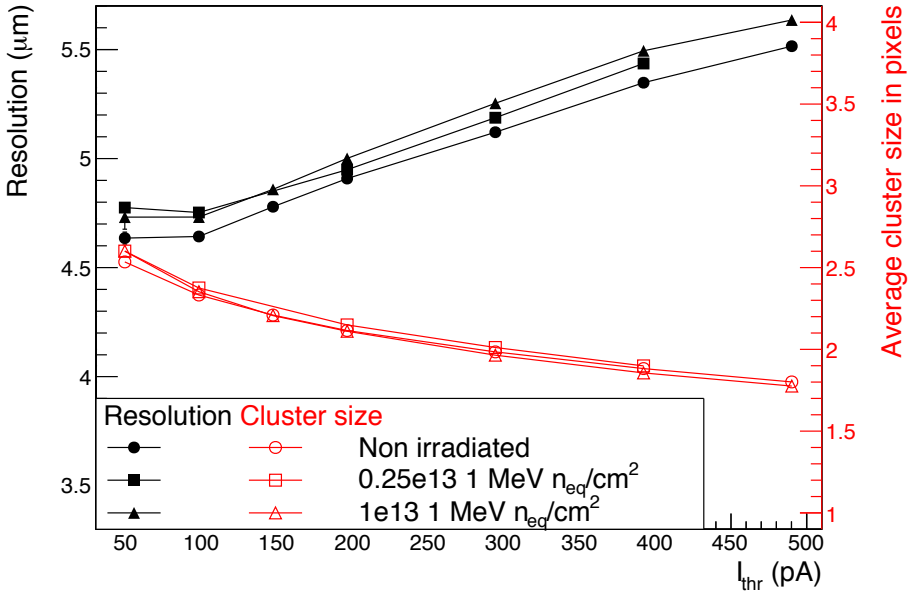
50 pA ➔ ~80 e
500 pA ➔ ~180 e

$\lambda_{fake} << 10^{-5}$ / event/pixel @ $\varepsilon_{det} > 99\%$ ➡ very large margin over design requirements

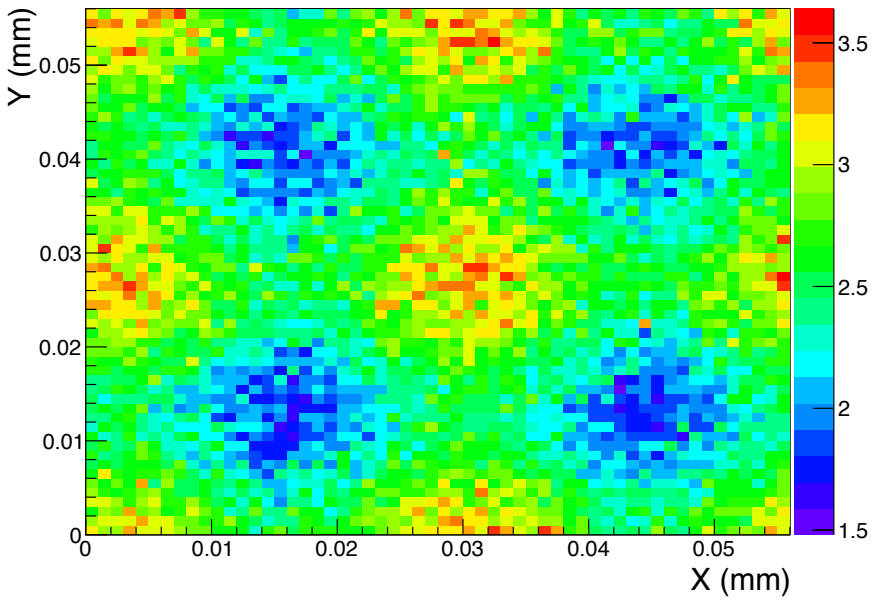
- Measurements at PS: 5 – 7 GeV π^- December 2014
- Results refer to 50 μm thick chips: 3 non irradiated and 3 irradiated with neutrons at 10^{13} 1MeV n_{eq} / cm^2

pALPIDE-1 – PS test beam (Sep 2014)

Spatial resolution



Cluster size vs. position within pixel



$\sigma_{det} < 5\ \mu m$ is achieved with sufficient margin of operation

- Measurements at PS: 5 – 7 GeV π^- September 2014
- Results refer to 50 μm thick chips: non irradiated and irradiated with neutrons 0.25 x 10^{13} and 10^{13} 1MeV n_{eq} / cm^2

Pixel chip – interconnection to flex PCB

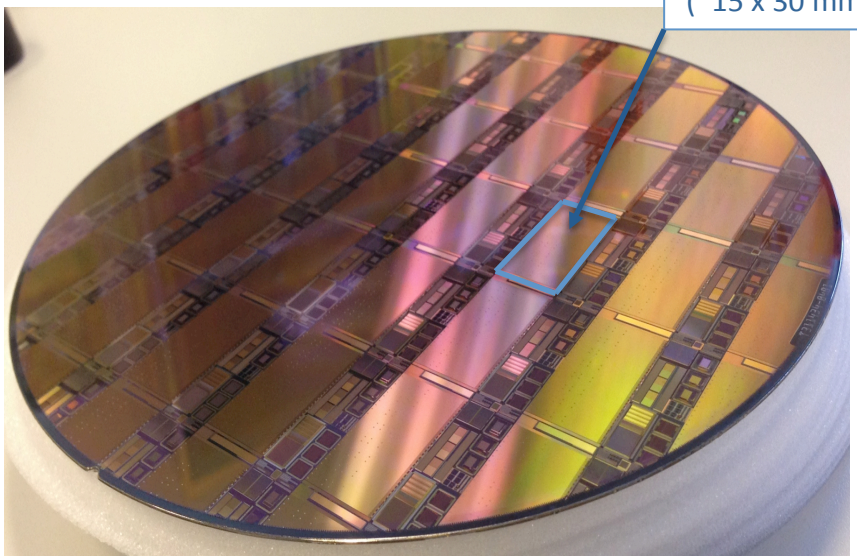
Solder Pads

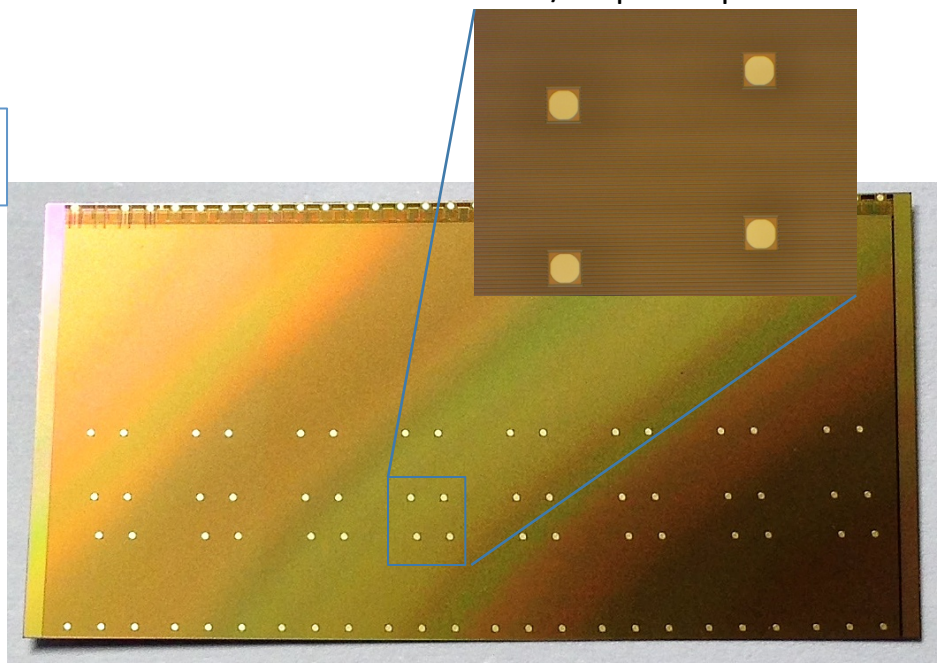
- to solder the chip on the FPC, Al pads need Ni-Au plating (wet-able surface)
- plating is done on wafer using electroless Ni-Au plating, prior to thinning and dicing
- R&D experience 2012-now: plating of about 50 wafers (pad wafers and CMOS wafers)

Status

Market survey concluded

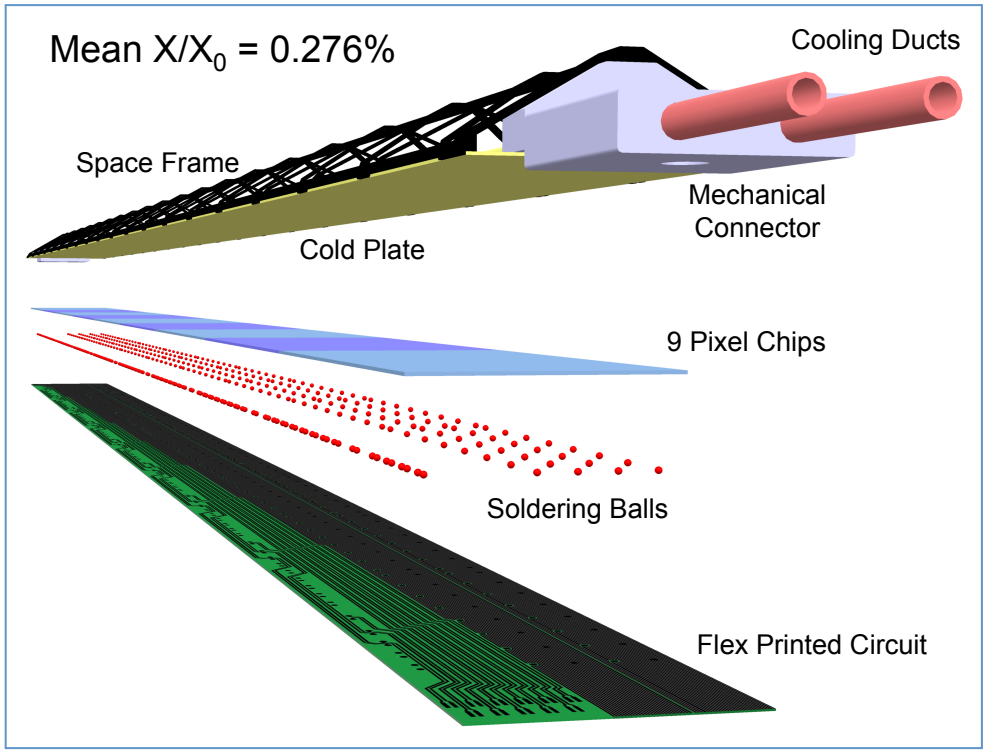
Tendering starting now

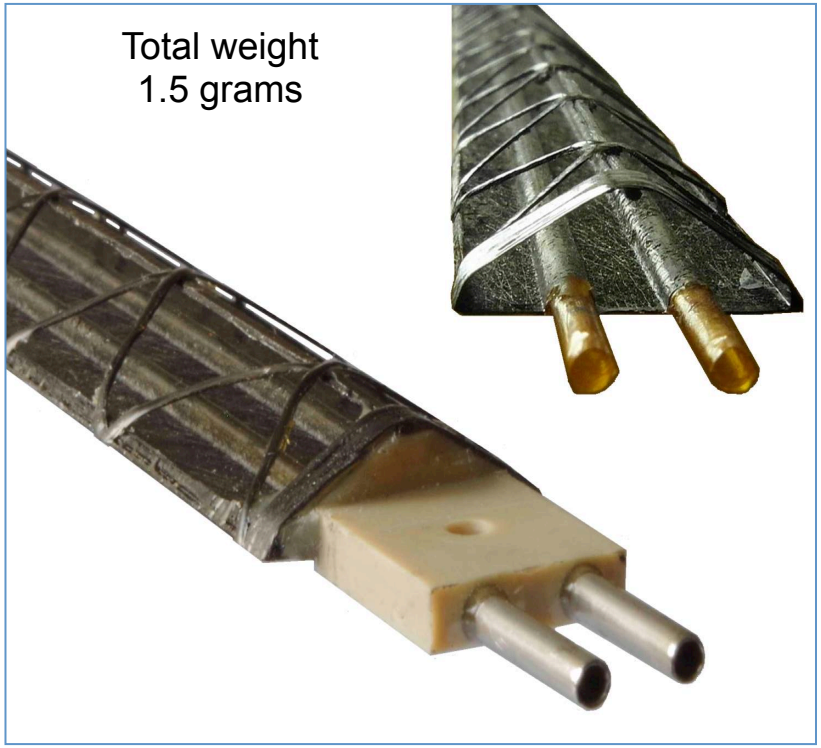




Contact pads are distributed over the matrix (custom designed)

Inner Barrel Stave





<Radius> (mm): 23,31,39

Length in z (mm): 290

Nr. of staves: 12, 16, 20

Nr. of chips/stave: 9

Nr. of chips/layer: 108, 144, 180

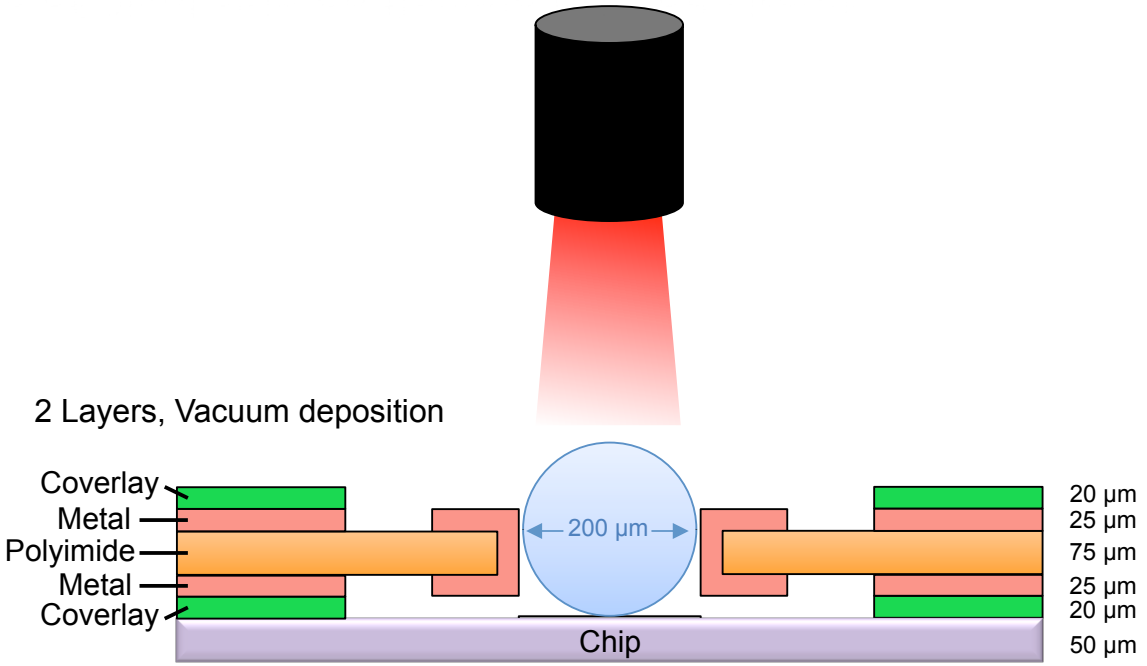
Material thickness: ~ 0.3% X_0

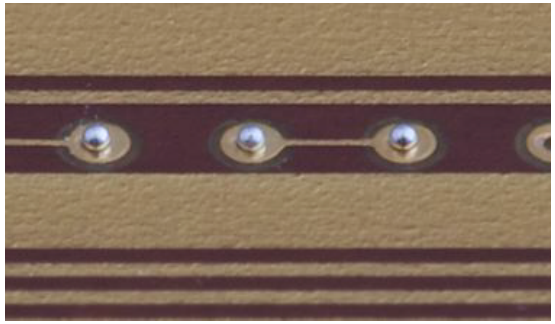
Power density: < 100 mW/cm^2

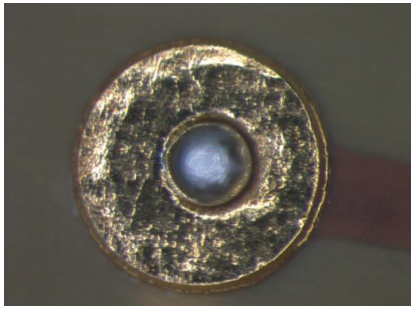
Throughput (@100kHz): < 80 Mb/s × cm^{-2}

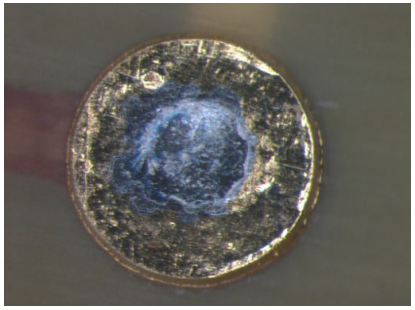
Interconnection of pixel chip to flex PCB

Laser soldering: Interconnection of Pixel chip on flexible printed circuit





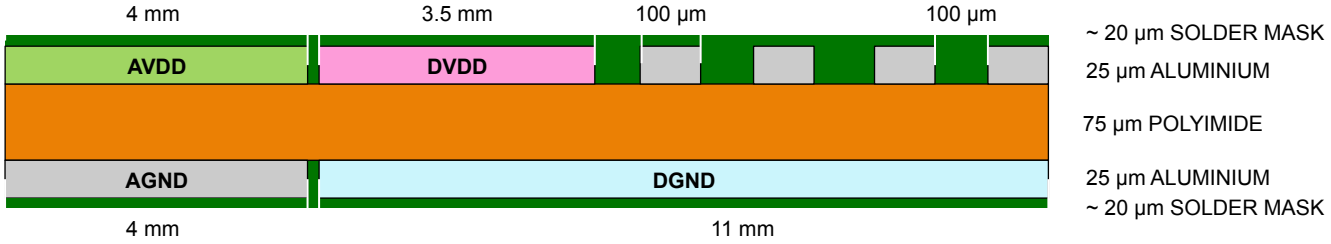




Inner Barrel Stave – flexible printed circuit

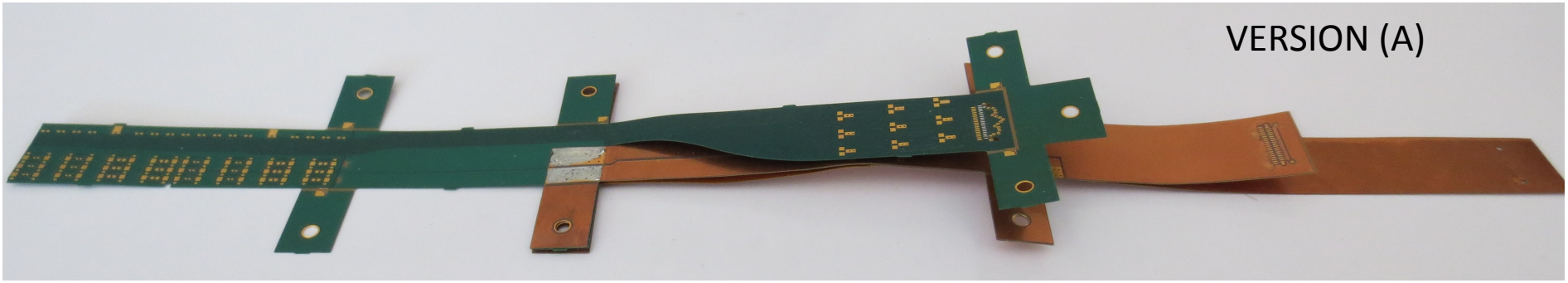
IB Flexible Printed Circuit prototypes (Al power planes and signal tracks)

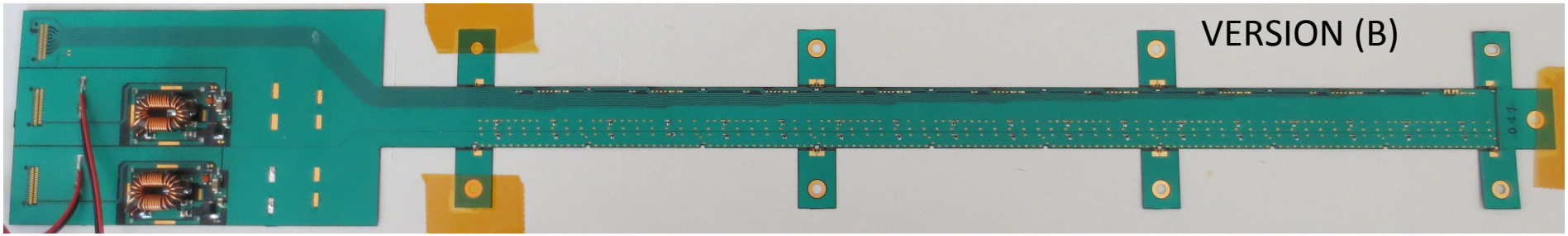
Metallised vias of 220μm diameter



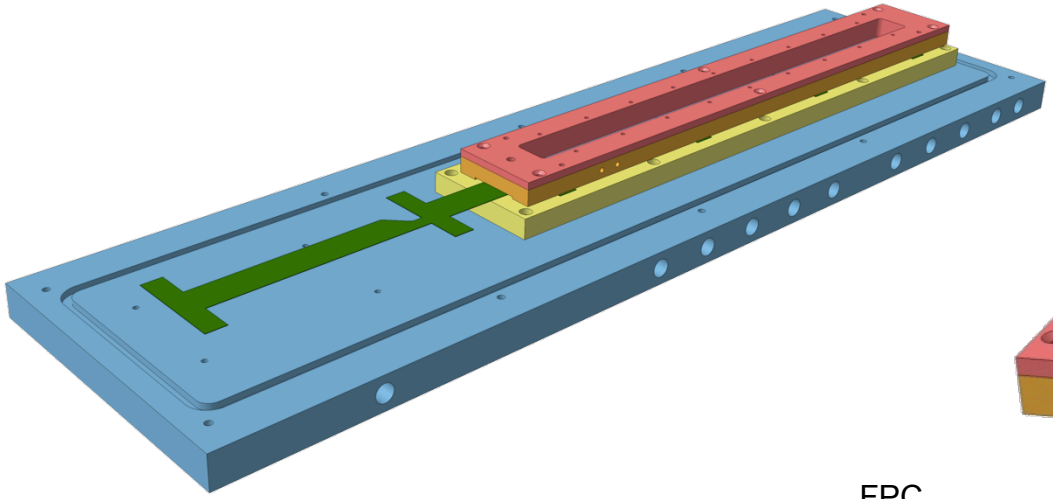
Status

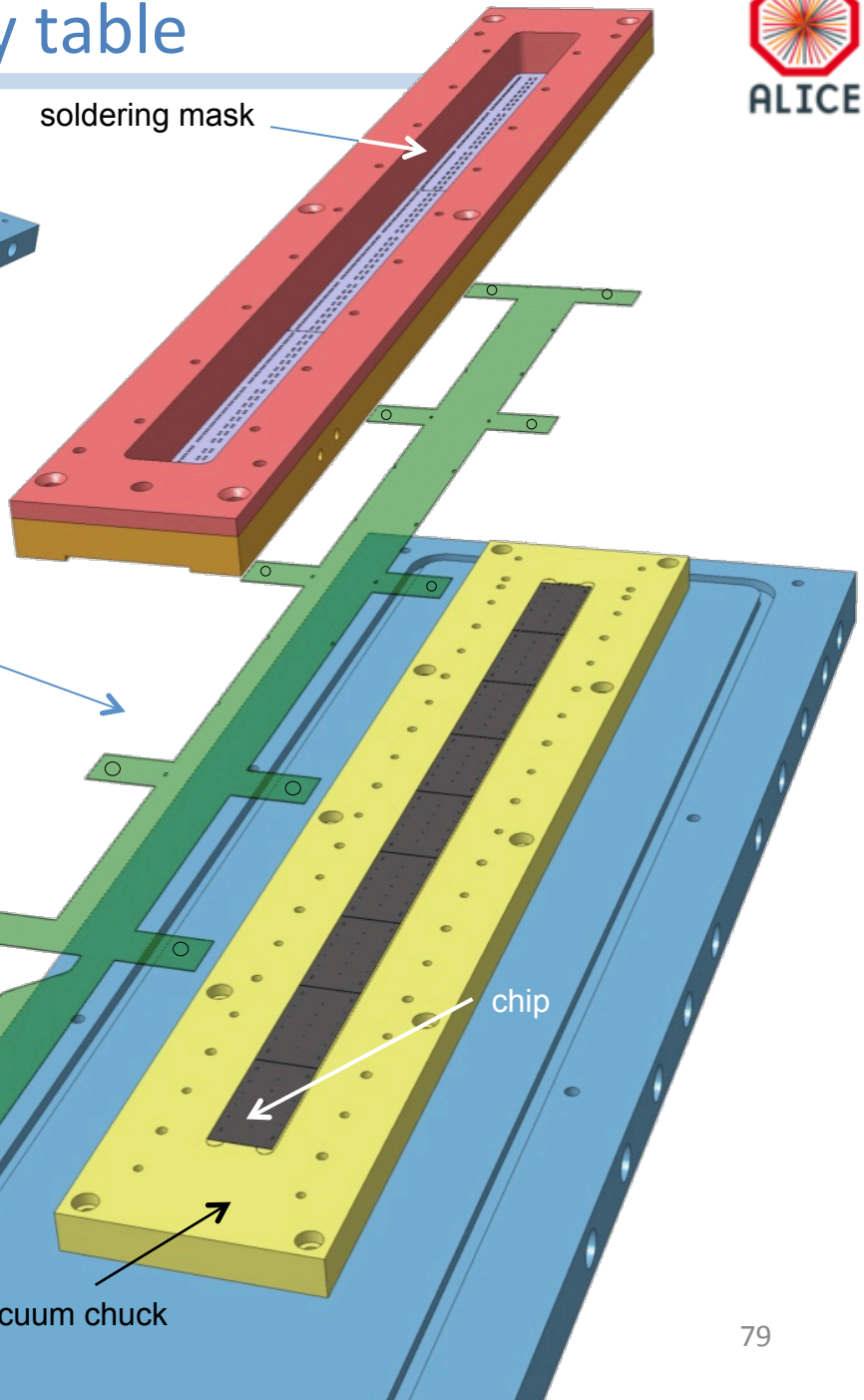
Two FPC versions (differ for the location of DC-DC converters) ready to be tested with ALPIDE-2

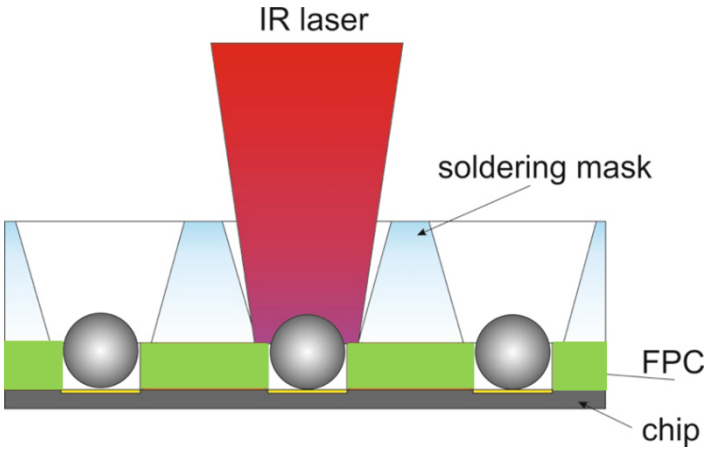




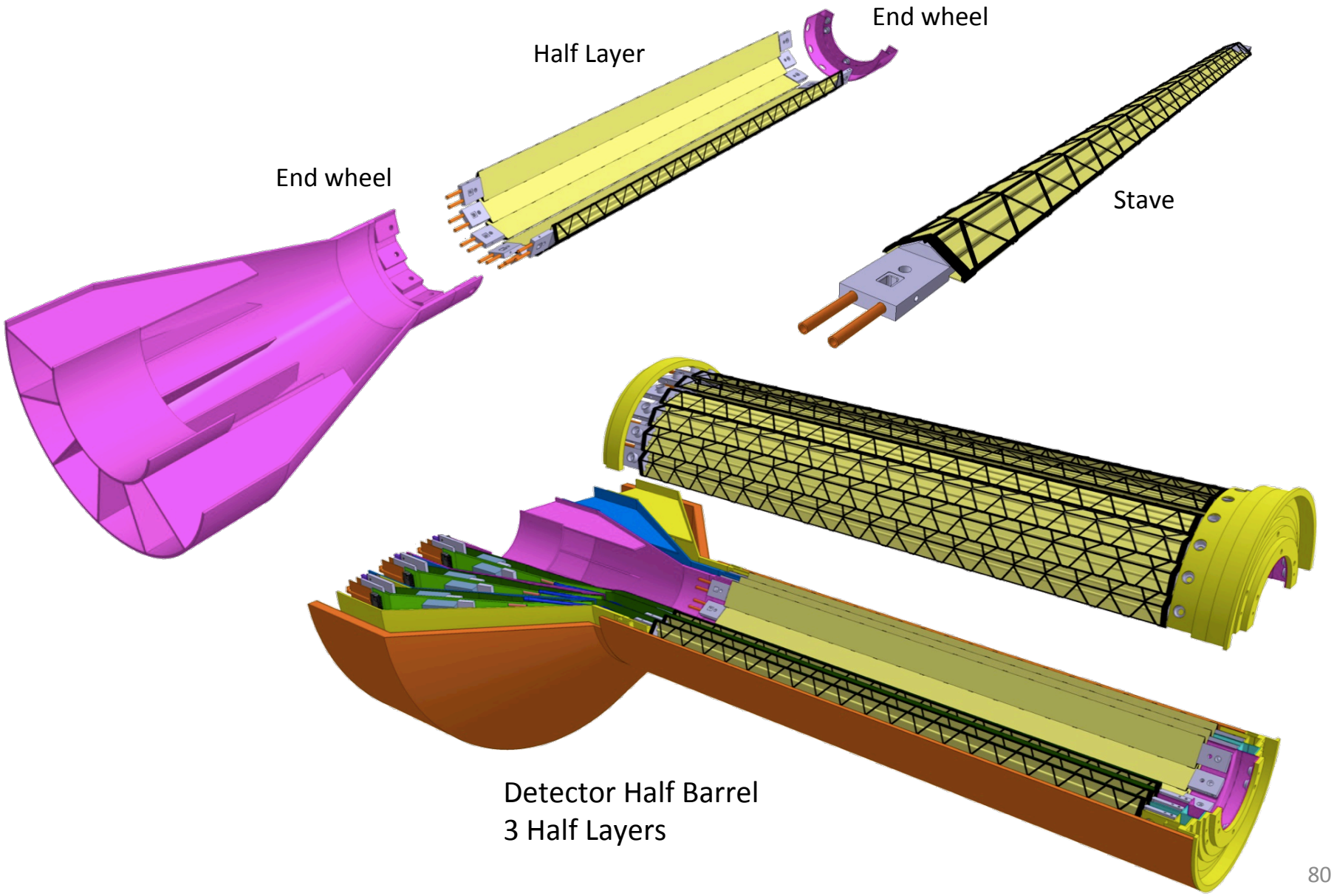
Inner Barrel Stave – HIC assembly table





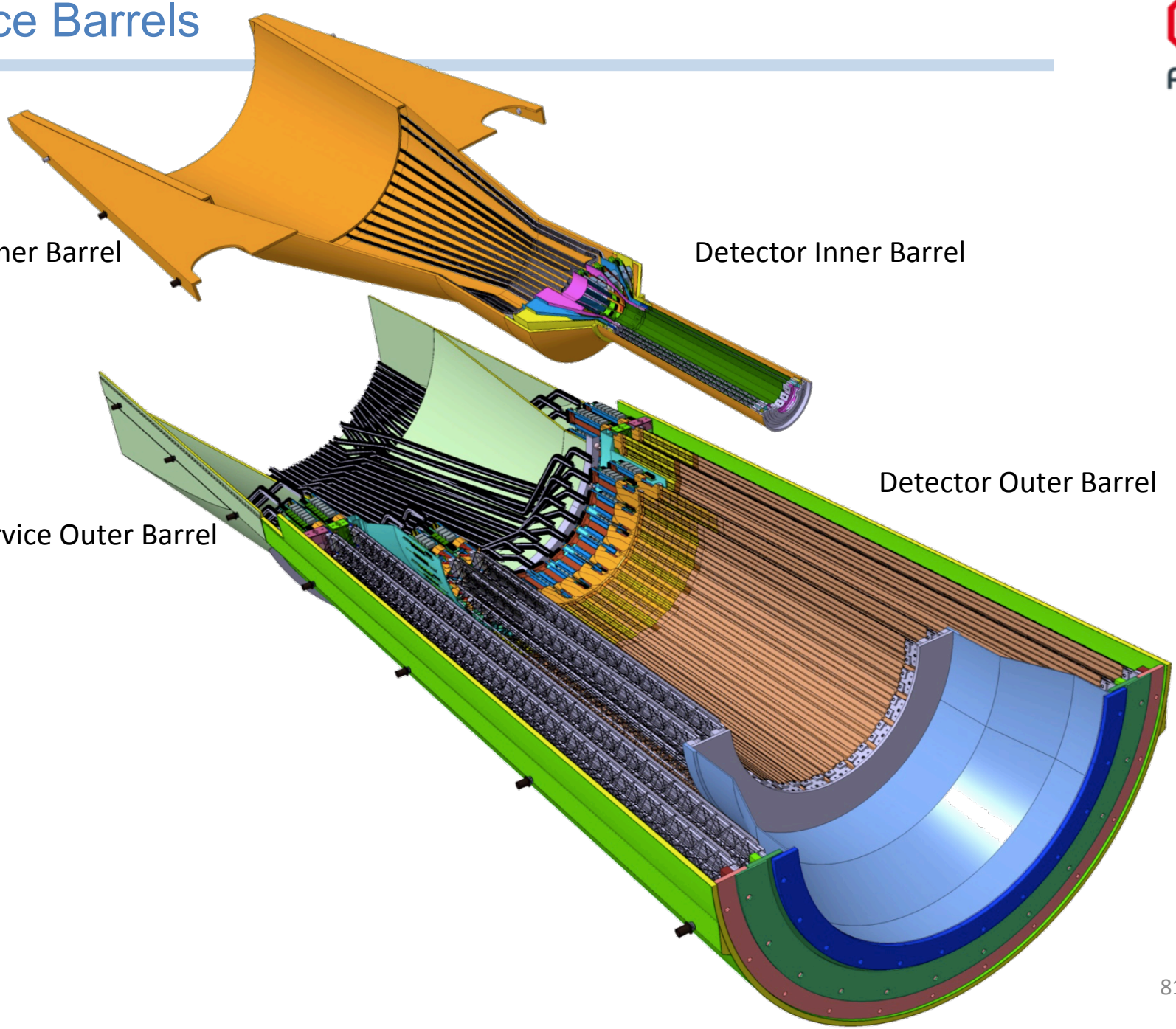


Inner Barrel



Detector Half Barrel
3 Half Layers

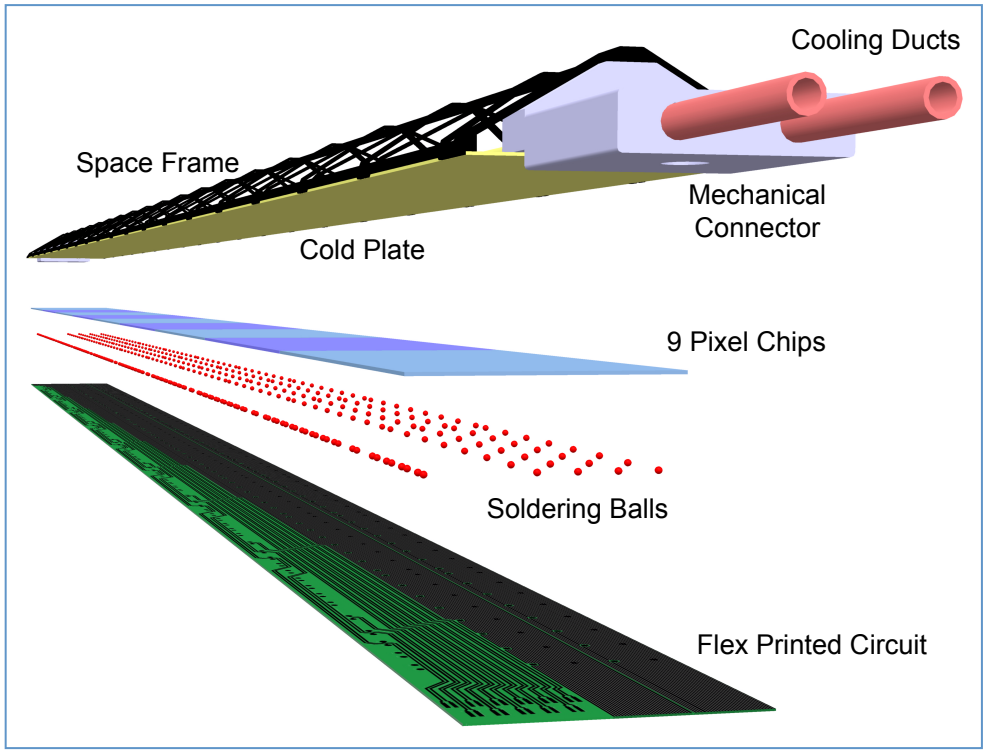
Service Barrels



What’s next ?

Ultra-light vertex detectors

Ultra-light pixel detector



How to further reduce material thickness?

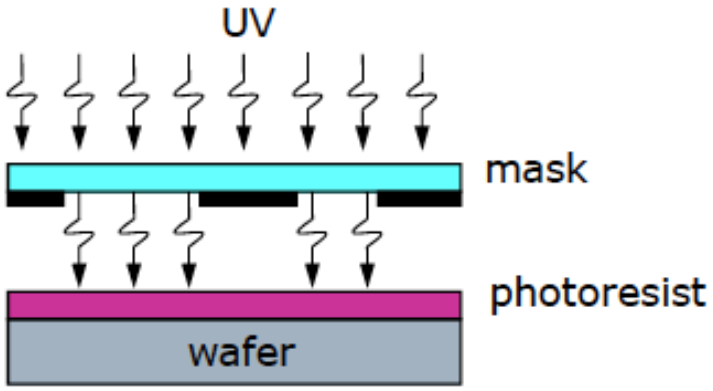
- Eliminate active cooling
  - ➔ For a 30cm long stave possible for power densities below 20mW/cm^2
- Eliminate electrical substrate
  - ➔ Possible if the (monolithic) sensor covers the full stave length

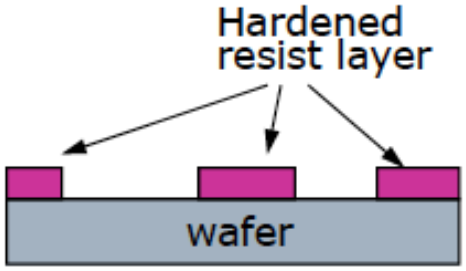
ALPIDE Chip (ALICE ITS upgrade):

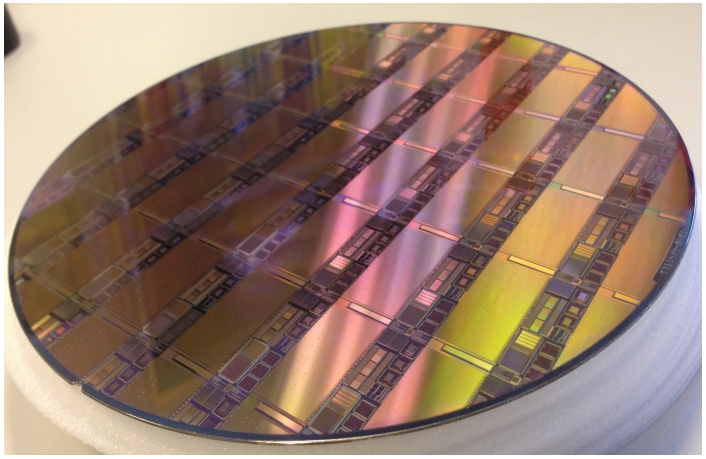
- pixel matrix power density **~7mW/cm^2**

What limits the dimensions of a CMOS chip?

Transferring a mask to silicon surface



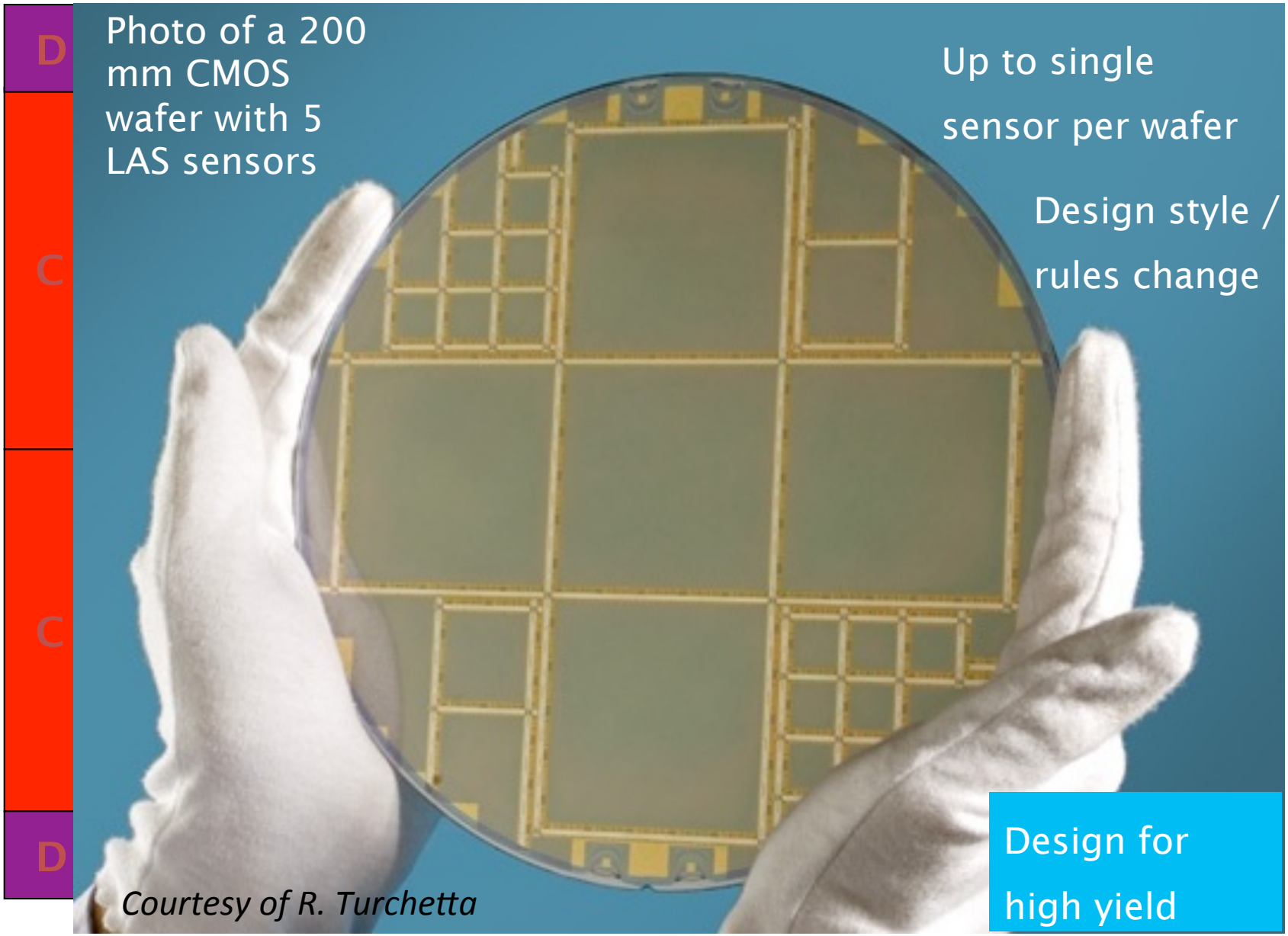




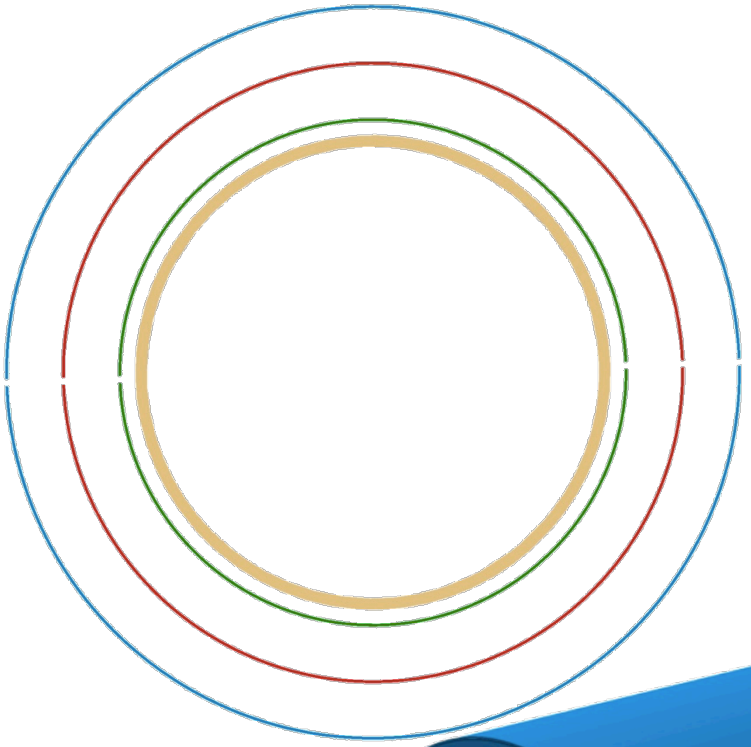
Reticle masks are typically of the order of 2 x 2 cm^2

IC industry demands small size dies for fabrication yield and to facilitate system integration

Stitching technology for CMOS processing

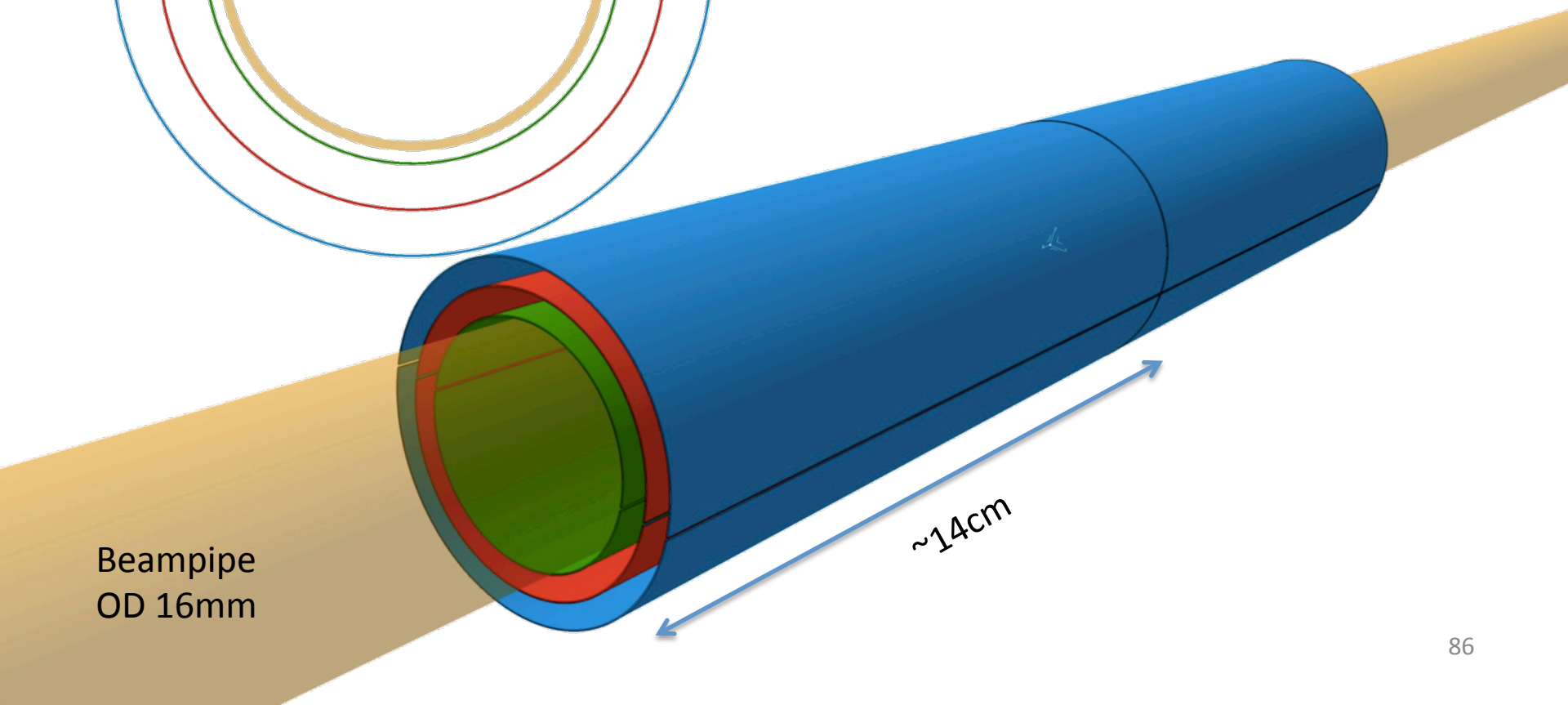


“silicon only” vertex detector



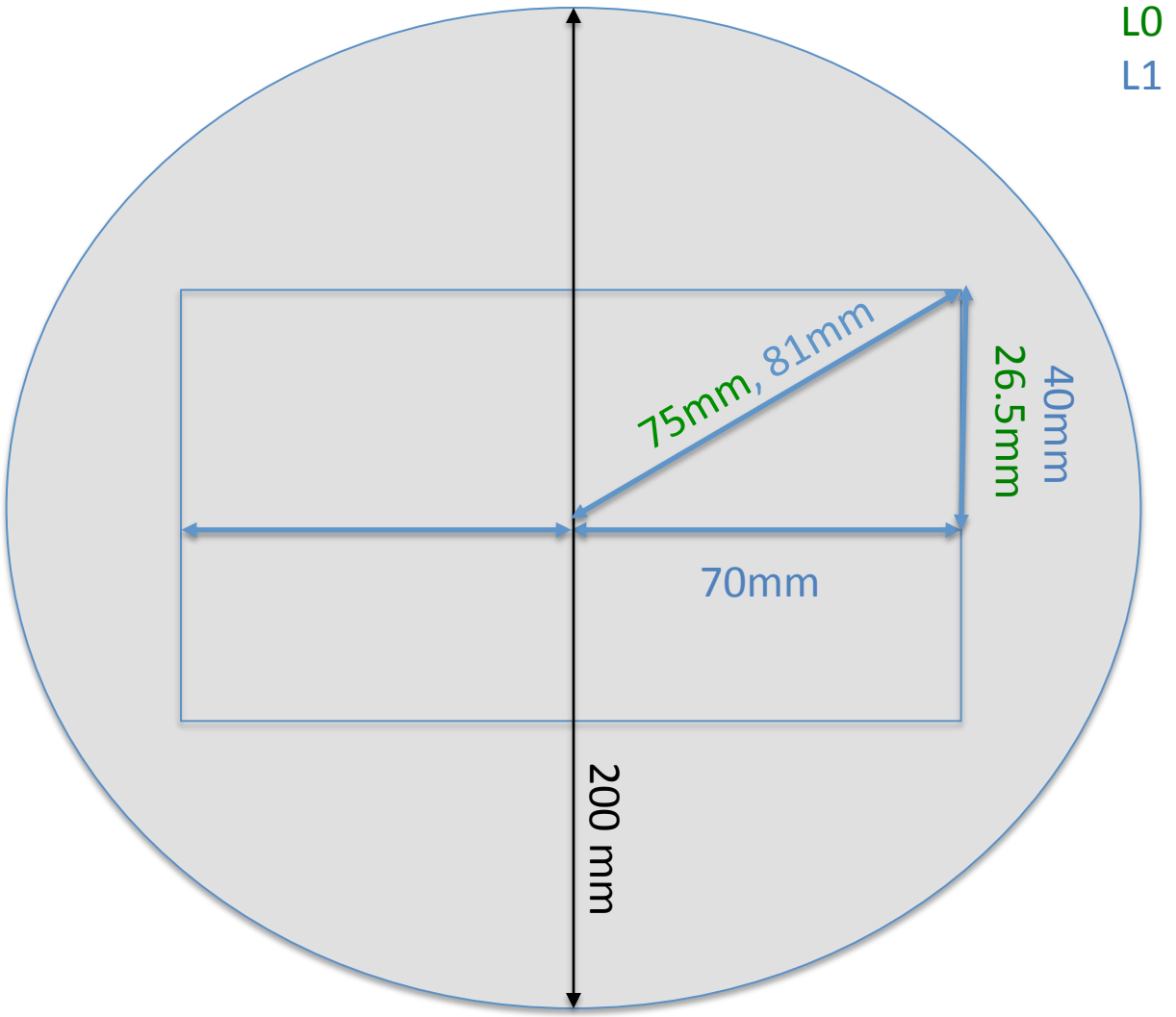
Layer 0, 1, 2

Circumference
L0: 106 mm
L2: 160 mm

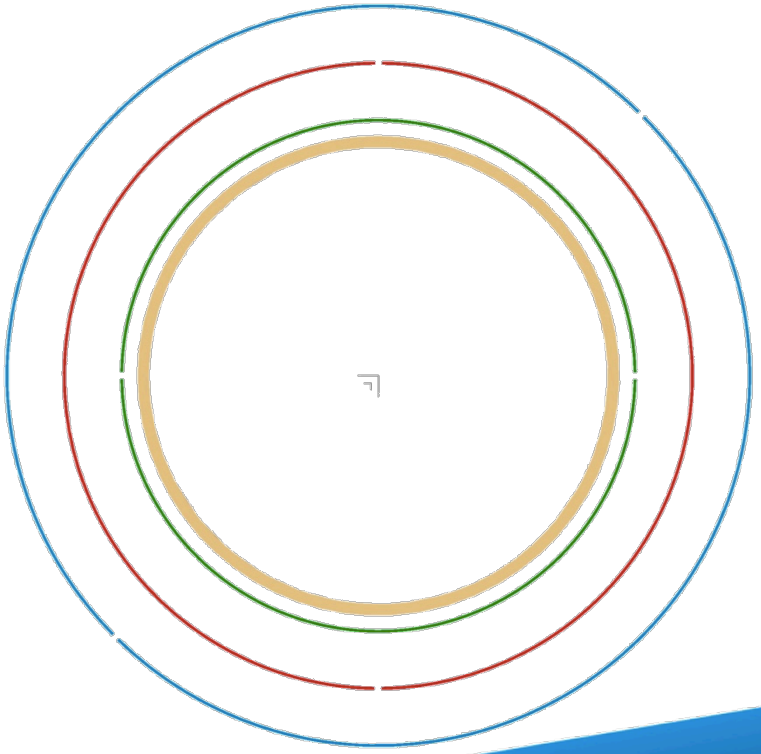


Beampipe
OD 16mm

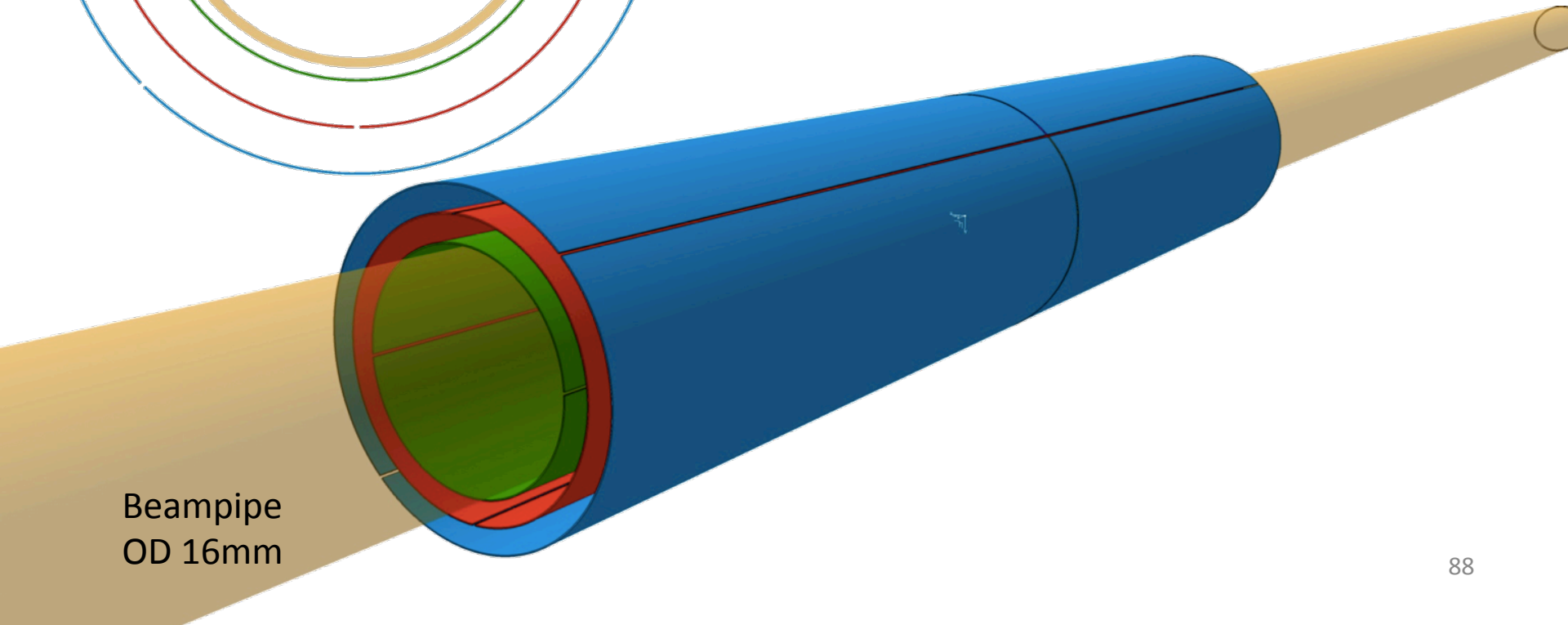
“silicon only” vertex detector



“silicon only” vertex detector

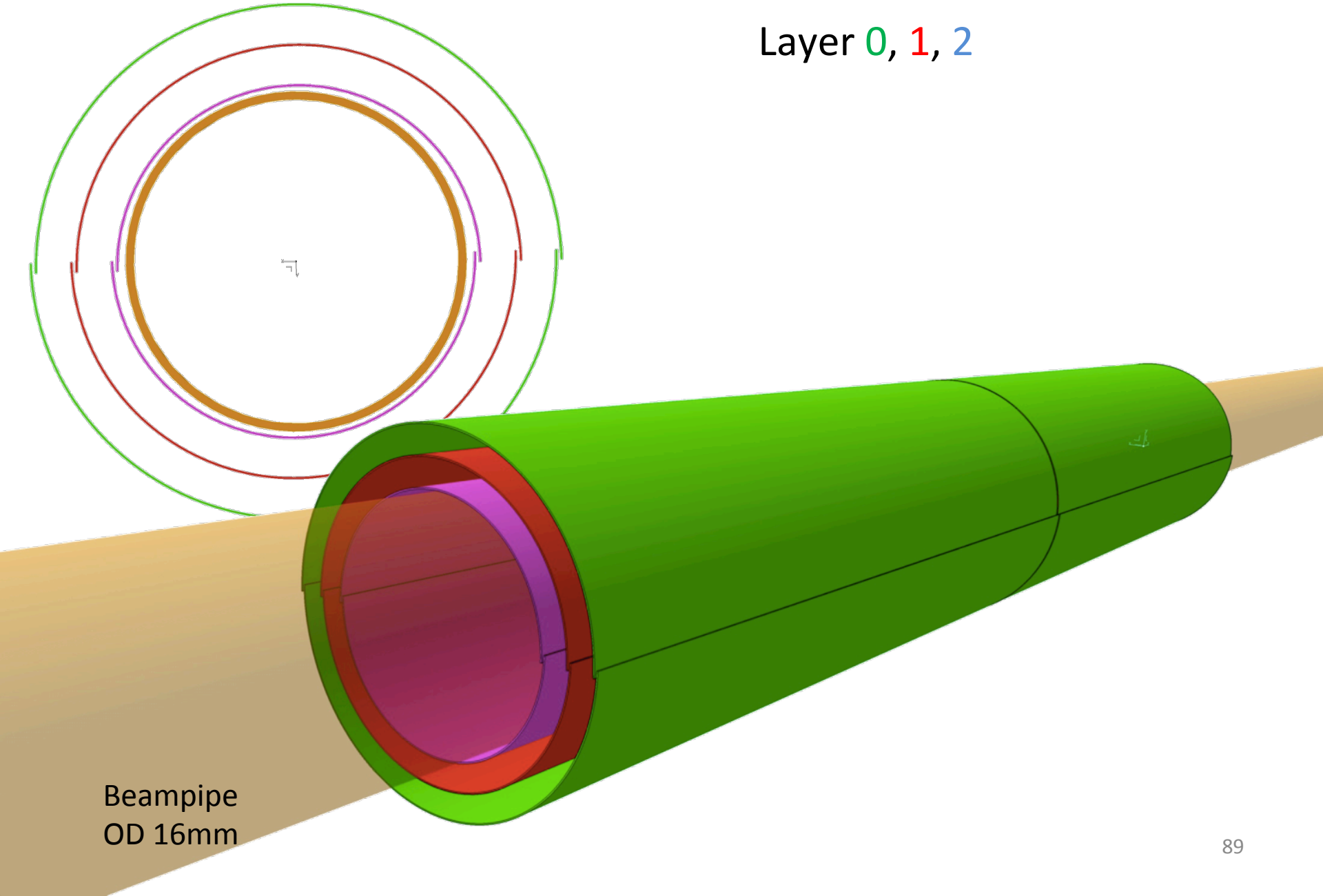


Layer 0, 1, 2

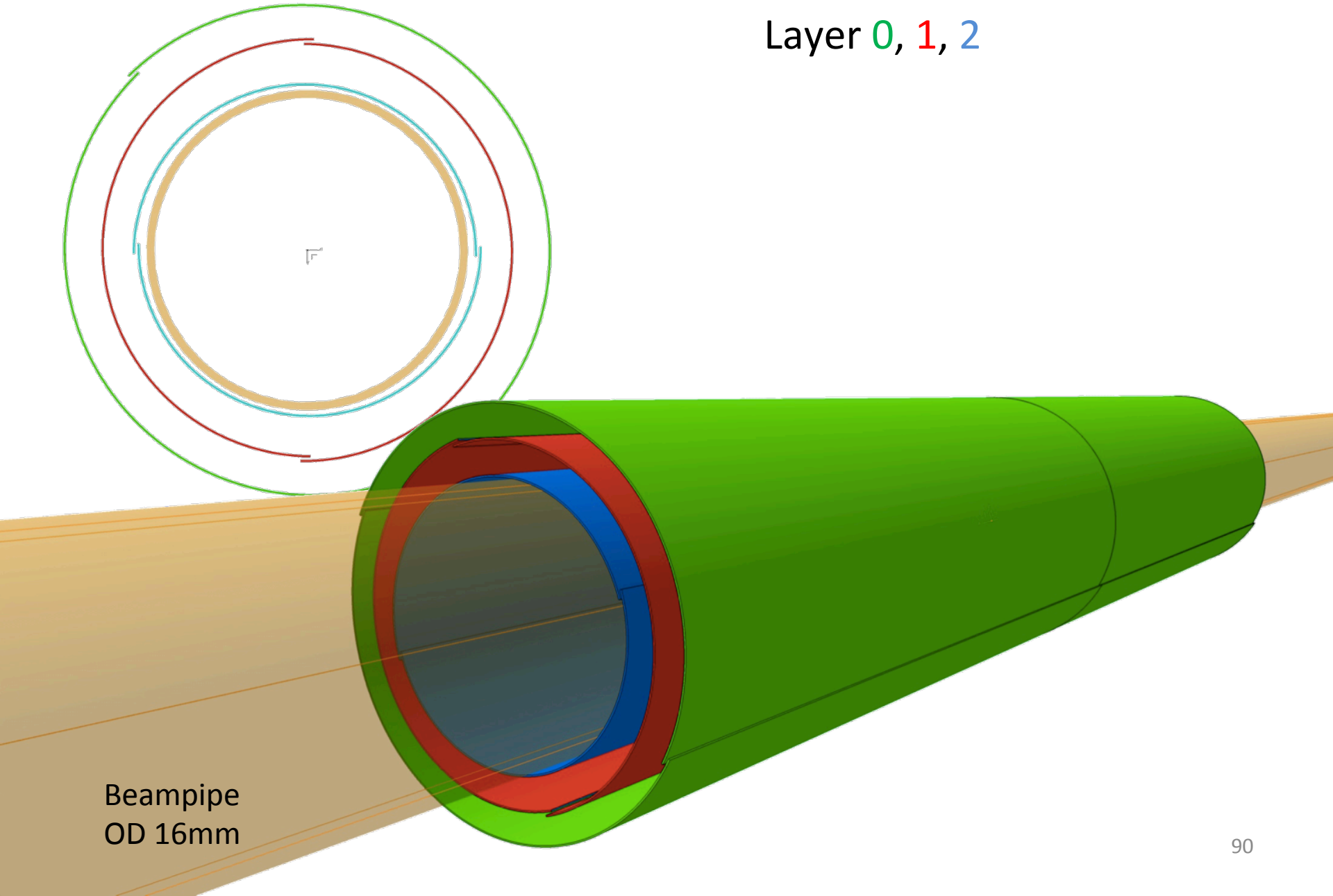


Beampipe
OD 16mm

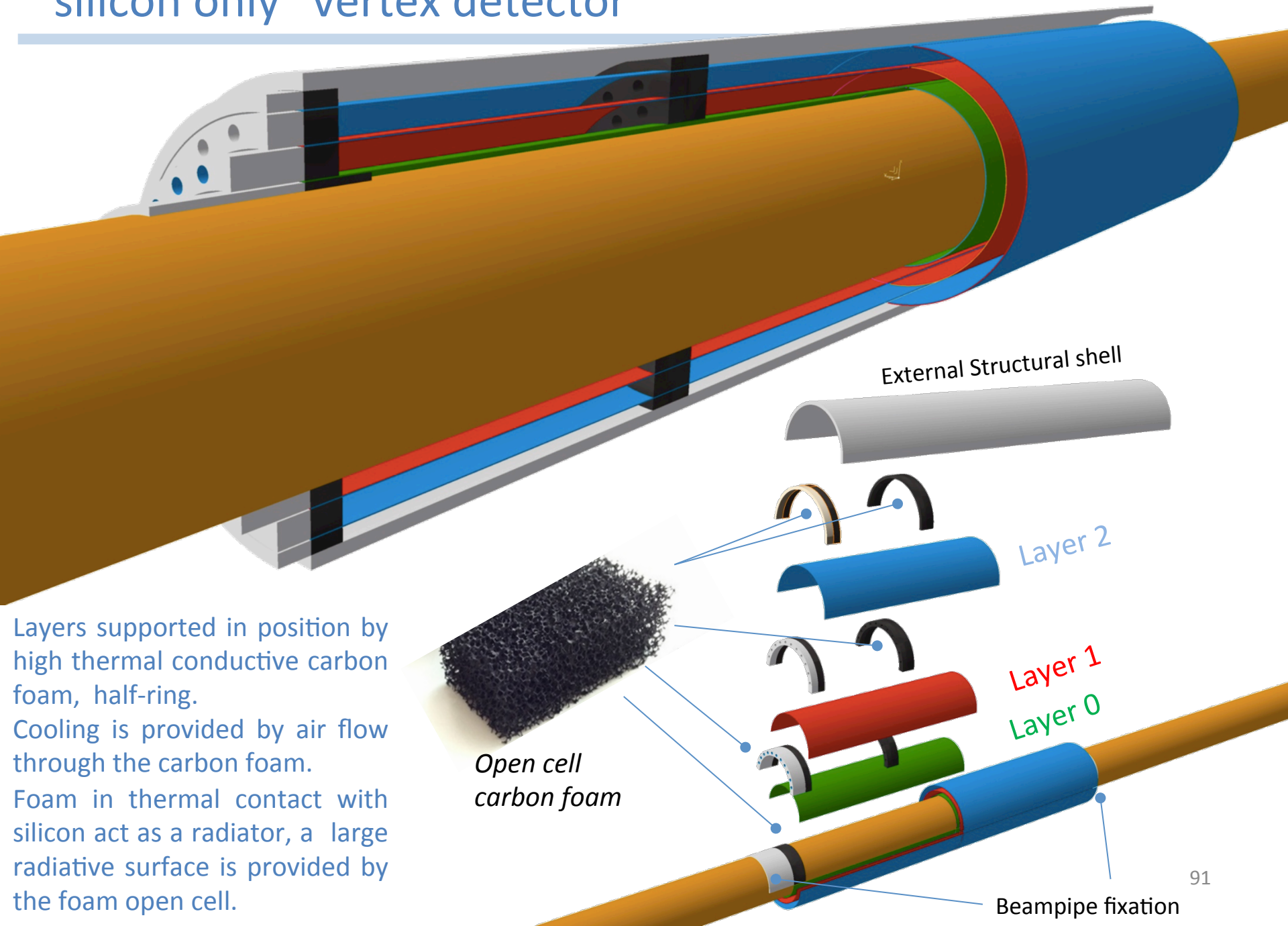
“silicon only” vertex detector



“silicon only” vertex detector



“silicon only” vertex detector



Layers supported in position by high thermal conductive carbon foam, half-ring.

Cooling is provided by air flow through the carbon foam.

Foam in thermal contact with silicon act as a radiator, a large radiative surface is provided by the foam open cell.

Thank you