EIC Readout and DAQ – CD-1 Perspective

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1. **CD-1 as a critical milestone**
2. **Timeline**
3. **EIC Streaming Readout Architecture**
4. **Development Flow**
5. **Other Items** *(Power, Grounding, etc.)*
6. **Summary**

Updated 10 Aug 2020:
a) Slide 5: nomenclature (FE to FEB), data rates, cabling.

1 CD-1

1. **Critical Decision 1.**

2. **DOE Review.**

3. "…baseline CD-1 project must be based on a simple, but day-0 feasible solution, to show to DOE that the EIC detector can be built in a way that is compatible with the EIC science goal." A. Celentano, 30 June 2020.

4. **March 2021.**

5. **All documentation must be completed by December 2020.**
   We need to deliver the project package before completion of YR, with focus on one defendable design.

6. **Upon approval, funds will be available for EIC detector design.**

7. **Various DOE reviews will occur during project execution.**

2 Timeline (tentative)

CD-1: Design
April 2021 – September 2025 (4.5 Years).

CD-3: Construction & Installation
September 2023 – September 2030 (7 Years).

CD-4a: Operations
September 2030 - …

- **Note that parts of CD-1 and CD-3 overlap:**
  Detectors will require readout and DAQ for testing, validation and software development (data, controls, etc.) before CD-3.

- **CD-1 will result in resource-loaded schedules:**
  Project costs and schedules are closely followed by DOE.

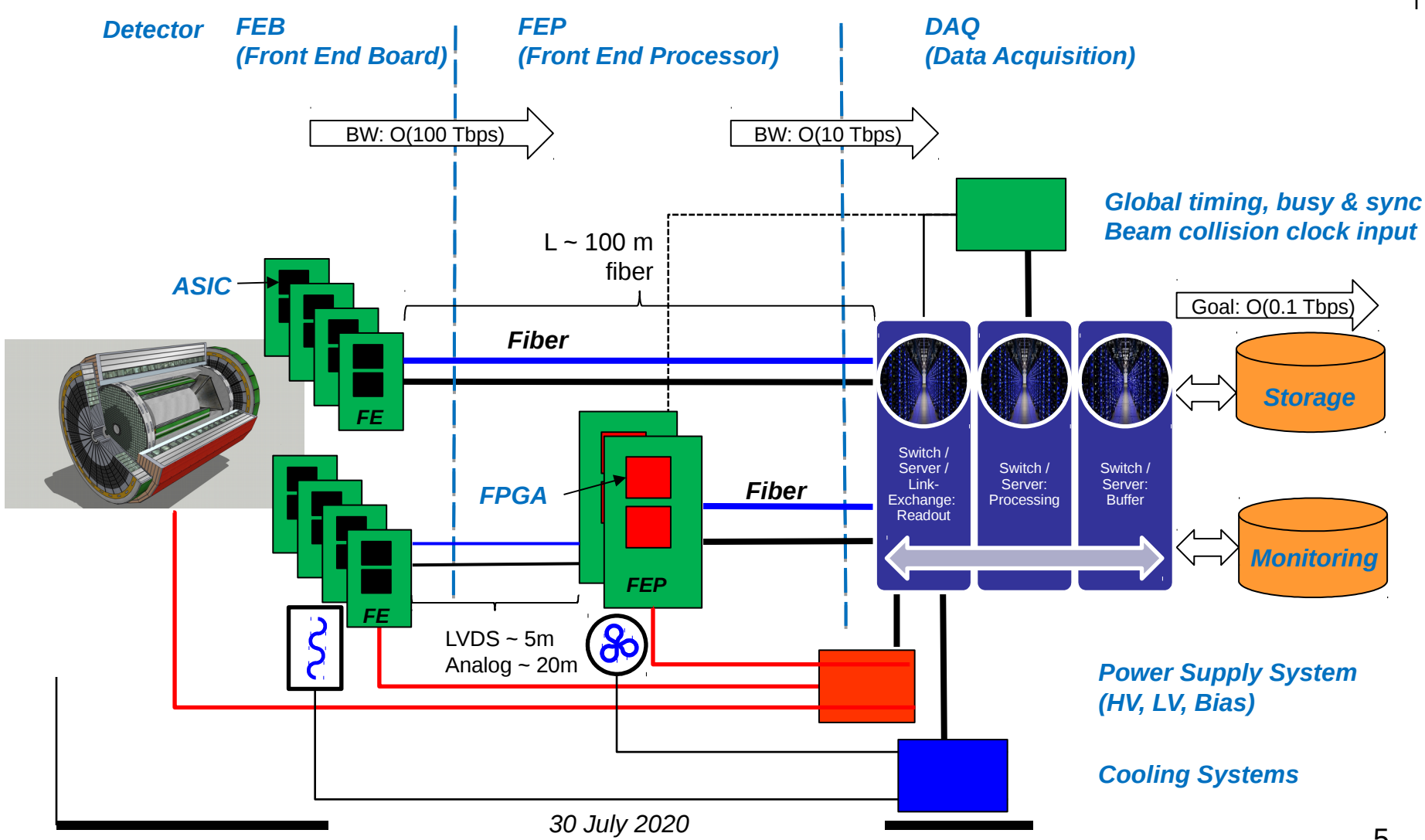
3 EIC Streaming Readout Architecture

- EIC collision data rate is relatively low
  - Comparing to hadron collider, lowered by α_{EM}^2
  - O(100) Gbps [see also 2020 User meeting YR DAQ talk by Andrea/Damien]

- Background and noise likely to drive the design requirement
  - Systematic control of EIC physics calls for low noise detectors and low background experiment at EIC
  - However, noise and background rate cannot be accurately determined at this early stage
  - One of main uncertainty is synchrotron background:
    rate calculation range from manageable to extreme high rate for various tunings of the EIC IR optics and shielding designs. Narrowing the range prior to CD-1

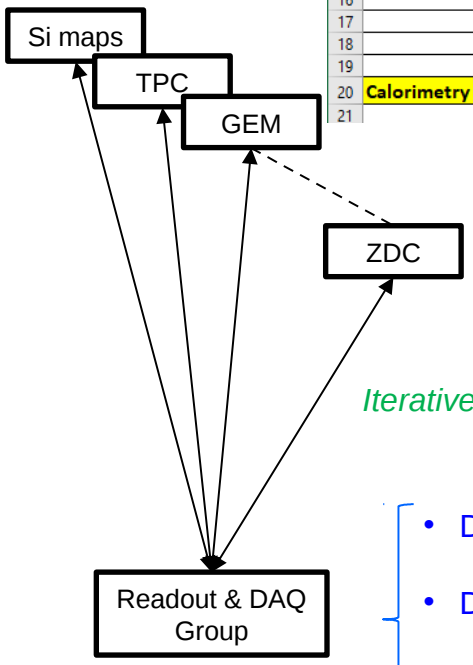
    → Readout architecture considerations
  - Streaming readout front-end (FE) supporting high speed data transmission off the detector
  - Aim to archive all raw data, after data reductions with minimal physics loss
    - Typical techniques include zero-suppression and loss-less compression
  - Mitigation of high backgrounds: further data reductions :
    - Calorimeter-based trigger signals that throttles the data stream :
      Well established technology at possible loss of physics
    - Feature extraction and noise-hit filtering, e.g. clustering, tracklet building :
      Calibration and systematics control is critical
  - A reliable DAQ: global timing synchronization with low-jitter beam collision clock; low and deterministic data loss with busy handling
  - Active data monitoring: server farm reconstruct fraction of data, anomaly detection, online calibration

EIC Streaming Readout Architecture



4 Development Flow

Specifications from detector groups



	Detector	Sub-system	Type	Sub-type	Channels	Detector Gain	Typical Charge	Signal Range	Noise	Capacitance	Single Channel Rate Maximum	Re
10	**Tracking**											
11		Silicon maps	Si	Pixel	200M							x,
12		TPC	GEM	Pads	160K							st
13		GEM	GEM	Strips	217K							st
14		uRWELL	GEM	Strips/Pads								st
15		Cylindrical Micromegas	GEM	Strips								st
16		Drift Chambers	DWC	Wires								st
17		sTGC	GEM	Pad, Strip, Wire								st
18		Straw Tubes	Straw	Wires								Fl
19												
20	**Calorimetry**											
21		e-EMCal	Cal	Pl								

	Readout Attributes	Preamp Gain	ADC Resolution	TDC Resolution	Discriminators (Y/N)	Scalers (Y/N)	AS
	x,y coordinate, Charge integral or Amplitude						
	strip number, Charge Integral or Amplitude						
	strip number, Charge Integral or Amplitude						
	strip number, Charge Integral						
	strip number, Charge Integral						
	strip number, Charge Integral						
	FlashADCs						
	Charge Integral or Amplitude +						

ers /)	ASIC	Number of Channels per ASIC	Number of ASICs	Power per ASIC	ASIC Power Supplies	Data Signals Type	Control Signals Type	Cooling (Y/N)	Type

Iterative Processes

- Develop FE specifications
  (ASIC, PCBs, Interconnects, etc.)
- Develop FEP specifications
  (FPGA, PCBs, Interconnects, etc.)
- Develop System specifications
  (Data Format, Configuration, Control, Interface, etc.)

FEB

- "Coalesce" specifications to minimize the number of ASIC part numbers, e.g., one ASIC type for all GEM-type detectors.

- Power is now nominally 1 W ± 0.25 W per ASIC (64 ch, 32 ch). Detector groups need to consider that cooling will be needed and make provisions for installation. Liquid cooling is efficient and low cost.

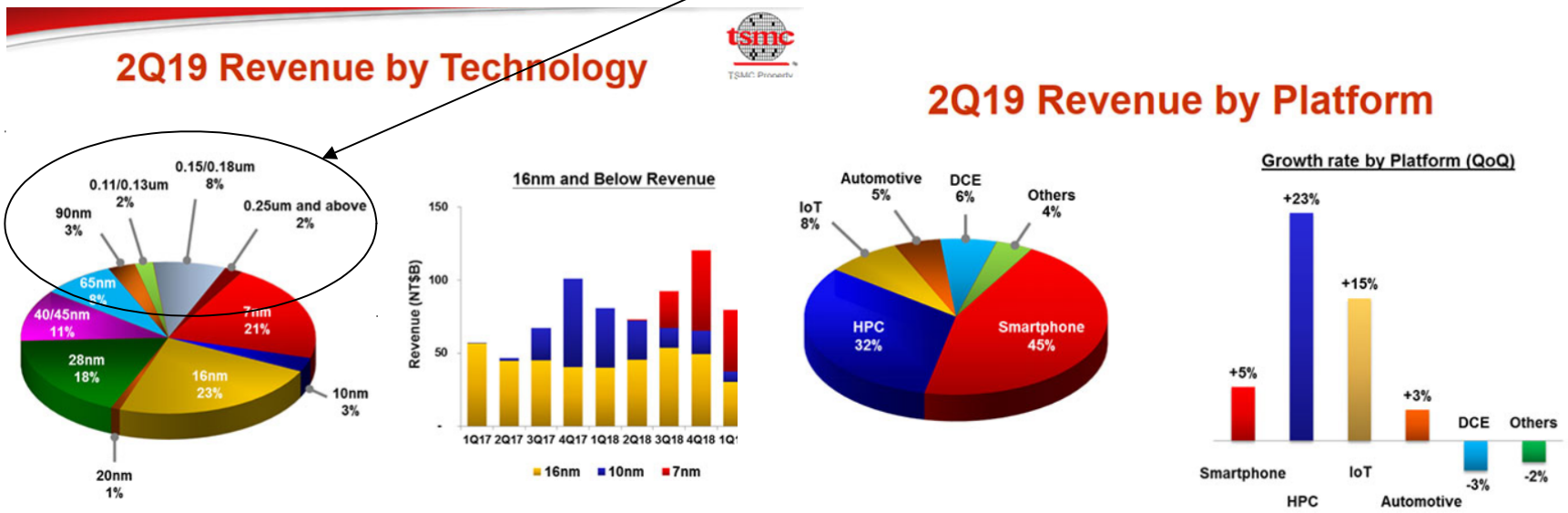
- Consider serviceability as a design criteria.

- ASIC Development (specifications, simulation, design, layout, verification, prototype fabrication and packaging) > 2 years. Must consider re-spin or > 1 year. Therefore, consider an **ASIC design cycle of > 3 years**.
  - Testing is a big effort, especially with a detector for validation.
  - Production (i.e., engineering run) ~ 1 year.
  - And then, a lot more testing.
  - PCB designs must occur concurrently, more testing.

- What if an existent ASIC already meets all the specifications and can be used *as is*?
  - Will the technology node still be available in a few years?
  - Are the fab masks still maintained and available for fabrication?

ASIC Technology Nodes

- Looking at TSMC, as an example, our niche is not that large.



- Presently, the most popular node at MOSIS for TSMC is 180 nm.
- For comparison, the 250 nm node, popular in our community for a number of years, is still supported by TSMC and MOSIS.
- The 250 nm technology node debuted in 1995.
- It is likely that any present robust technology in use by our community will still be supported in 10 years.

ASICs Survey

- A survey is being carried out for existing ASICs in the NP & HEP field for different types of sub-detectors.
- Pixel sensor with MAPS architecture is preferred considering the material budget. The next-generation ALPIDE in 65nm CMOS process, and HV/HR-CMOS designs with small electrode collection are possible technique solutions.
- ASICs for calorimeter, various gaseous detector, silicon timing detector, to support energy (with amplitude measurement, full pulse high speed digitization in Gsps level, or continuous digitization) and timing measurement with resolution in 10ps level. The detailed specification for different sub-detector is not finalized yet, so the survey covers examples with different dynamic range, peaking time, buffer depth and sampling rate.
- High speed data transmission: FESoC with embedded serializer; independent serializer and deserializer for data aggregation; and versatile optical links for radiation environment on front-end with limited space.
- Most of the surveyed designs are with 250nm, 130nm and 65nm technologies.

FEP

- "Coalesce" specifications to minimize the number of FPGA/PCB part numbers.
- Standardization of data format (header, timestamp, etc.) at the system design level is very desirable. However, standardization of inputs from the FE is not easy at an early stage. Output of the FE may be specific to the ASIC design. Aim for FEP reformatting into standardized format for downstream processing.
- Hardware development is not as constrained as for the ASICs – FPGAs are commercially available off-the-shelf (COTS) products.
- Firmware development requires specialized expertise in close connection with the detector development.
- Power demands can be high. But for the FEPs that are outside of the detector volume, it is easier to manage cooling and other infrastructure needs.
- Consider serviceability as a design criteria.
- Testing and integration takes considerable time and resources.
- Allocating a minimum of 3 years for development (and overlapping co-design with the FE) is sensible.

5 Other Items

- Power Supply & Cooling Systems
  - Use COTS units – Wiener, CAEN, …

- Grounding & Shielding
  - We have a plan based on recent projects: floating supplies referenced to ground at the detector grounding mesh/grid for low noise and good signal integrity.

Environment	21 °C ± 2 °C, RH < 50%.
Grounding	Ground Mesh in Detector Interaction Region Area. Bonding of Segregated Loads.
Cabling	NEC 2011 NFPA 70, UL CL2 or better.
Cable Routing	NECA/NEMA 105-2007. Open cable tray systems.
EMI & RFI	FCC part 15 Class B, CISPR 11/ EN 55011 Class B, CISPR 22/ EN 55022 Class B and EN 61000-6-3.
Power Supplies	Floating and referenced to the ground mesh at the detector.
Racks	Open frame, COTS (i.e. Hammond C4F247736) with horizontal and vertical cable managers.

6 Summary

- We are working on one defendable streaming DAQ design for the CD-1 project following an aggressive schedule. Expected to deliver prior completion of YR
  - Building upon on-going YR work. Inputs and suggestions will be appreciated

- Need to finalize specifications:
  - From detectors
  - For ASICs, FEB and FEP
  - For DAQ, system.

- Is it possible to design a series of ASICs, FEBs, FEPs (possibly one per each detector type) with the same, or a sub-set of, I/O interface specifications?
  - Data, control, configuration formats (channel, timestamp, etc.)
  - Zero suppression, timing, synchronization, etc.

- CD-3
  - ~3 years away and overlaps CD-1.
  - The large number of items will require considerable resources for procurements.
  - Large procurements will likely take ~1 year per each contract award.
  - Schedules will be challenging but doable.