ALPHACORE

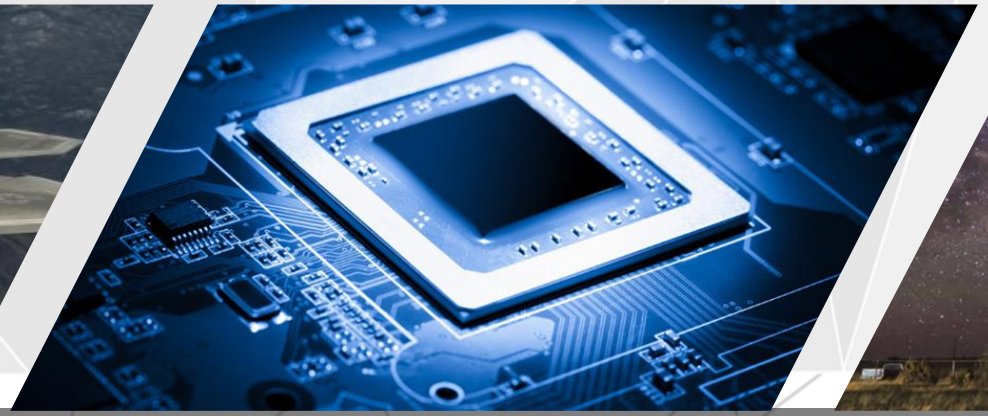
ROBUST HIGH-PERFORMANCE MICROELECTRONICS

Update on Alphacore's Readout ICs

Presented by : Esko Mikkola

Streaming Readout Meeting

November 16, 2020



Outline

- Alphacore's 90nm - 180nm CMOS preamplifiers and ADCs status.
- Alphacore's 22nm – 28nm CMOS ADCs status.
- Future plans

Alphacore's Goals

- Alphacore is completing two DOE Phase II programs:
  - STTR Phase II, "**Multi-Channel Readout IC for Nuclear Physics Experiments**"; PoP ended May 2020
  - SBIR Phase II, "**Picosecond Digitizer**"; PoP ended August 2020
- Key goal of this work has been to develop versatile detector readout solutions, both IP and ICs.
- The IP blocks can be used to relatively quickly build the exact, compact readout ASICs configurations most suitable for a target application when the need arises. Alphacore can build the exact ASIC for a customer in need using the tested IP.
- Alphacore is wrapping up both DOE Phase II programs and seeking further funding/collaboration opportunities.

Summary of Recent Readout Circuit Designs

	90nm - 180nm CMOS readout ckts	22nm – 28nm CMOS readout circuits
Main funding source	DOE NP STTR Ph2 (until May 2020)	DOE HEP SBIR Ph2 (until August 2020)
Evaluated Design #1	180nm programmable preamplifiers	28nm, 10b, 300MS/s, 0.8mW ADC
Evaluated Design #2	180nm 10b, 50MS/s, 7mW ADC (1-ch, 6-ch)	28nm 10b, 500MS/s, 1.2mW ADC
Evaluated Design #3	180nm 12b, 100MS/s, 64mW ADC (1-ch, 6-ch)	28nm, 9b, 1GS/s, 2mW ADC
Evaluated Design #4	180nm serializer interface with PLL	28nm, 10b, 2.4GS/s, 6mW ADC
Evaluated Design #5	90nm 14b, 50MS/s, 62mW ADC	22nm, 10b, 5GS/s, 19mW ADC (recently taped out)
Deliverables now	Preamplifier and ADC single channel test boards, multichannel bare die	Test boards for all ADCs (the output interface is not suitable for actual detector readout experiments)
Deliverables with small amount of additional funding	Packaged multi-channel 180nm test chips	ADC chips and test boards with FIFO output interfaces suitable for detector readout experiments
Deliverables of potential follow-on program	Multi-channel 90nm chips, FPGA based evaluation boards, improved specifications, more channels per chip	Multichannel chips, FPGA based evaluation boards, improved specifications

Charge Sensitive Amplifiers (CSA) Tapeout

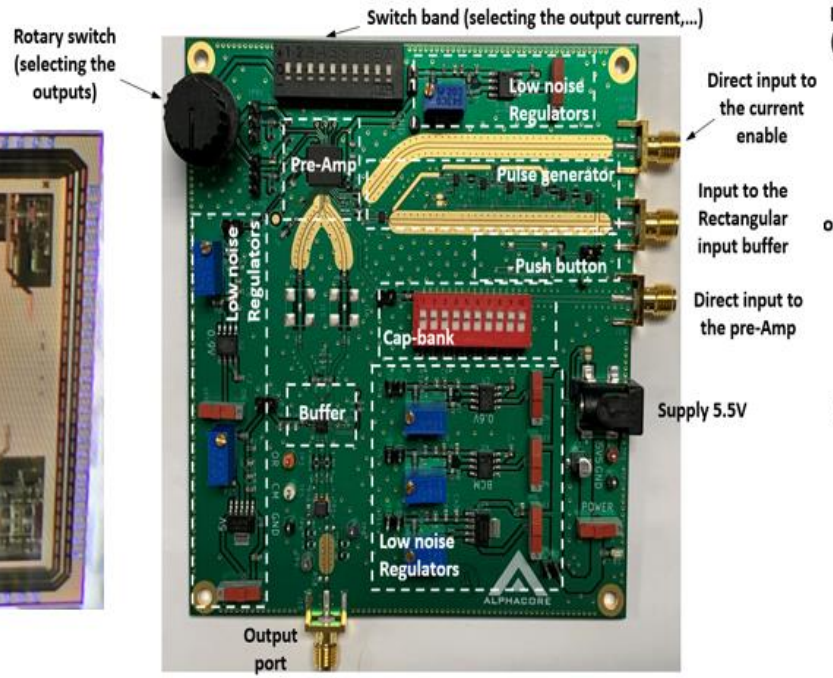
Test chip for CSAs die micrograph

# Simulated specifications	CSA1 with programmability	CSA2	CSA3
Equivalent Noise Charge(ENC) worst case (electrons)	556	1.8K	480
ENC increase rate (electrons/pF)	22.25	negligible	22.25
Rise Time typical (ns)	92	208	20
Gain (mV/fC)	30.45	29.8	2.3
Rise time programmability (ns)	50n-200	NA	NA
Gain Programmability (mV/fC)	15-60	NA	NA
Fully Differential Output	Yes	Yes	Yes
Common Mode of Full Differential Output	0.8-1	0.8-1	0.8-1
Shaper Circuit	Yes	Yes	No

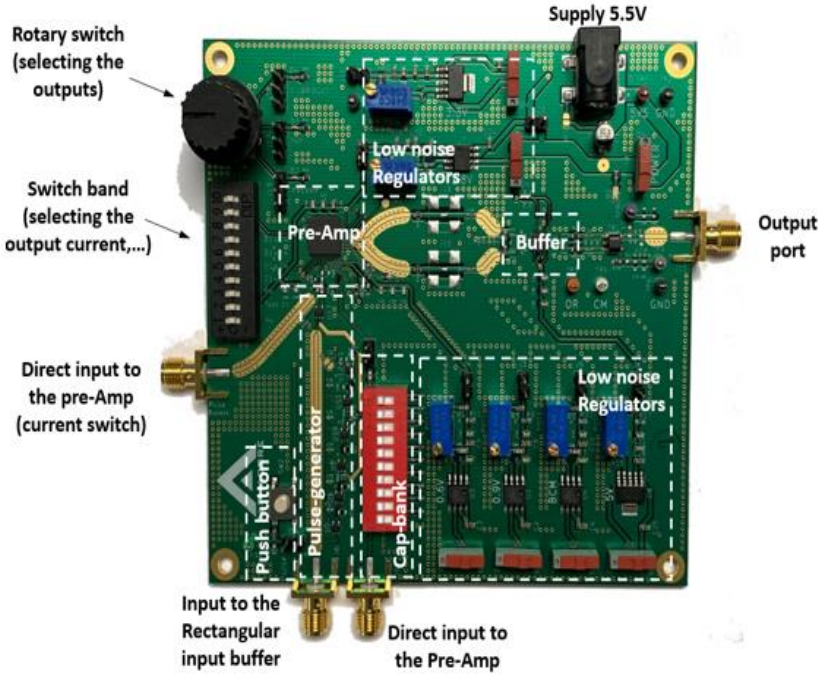
CSA Micrograph and Evaluation Boards

CSA evaluation boards and/or packaged chips are available for customers. 16-ch preamplifiers are available as bare die.

Die micrograph

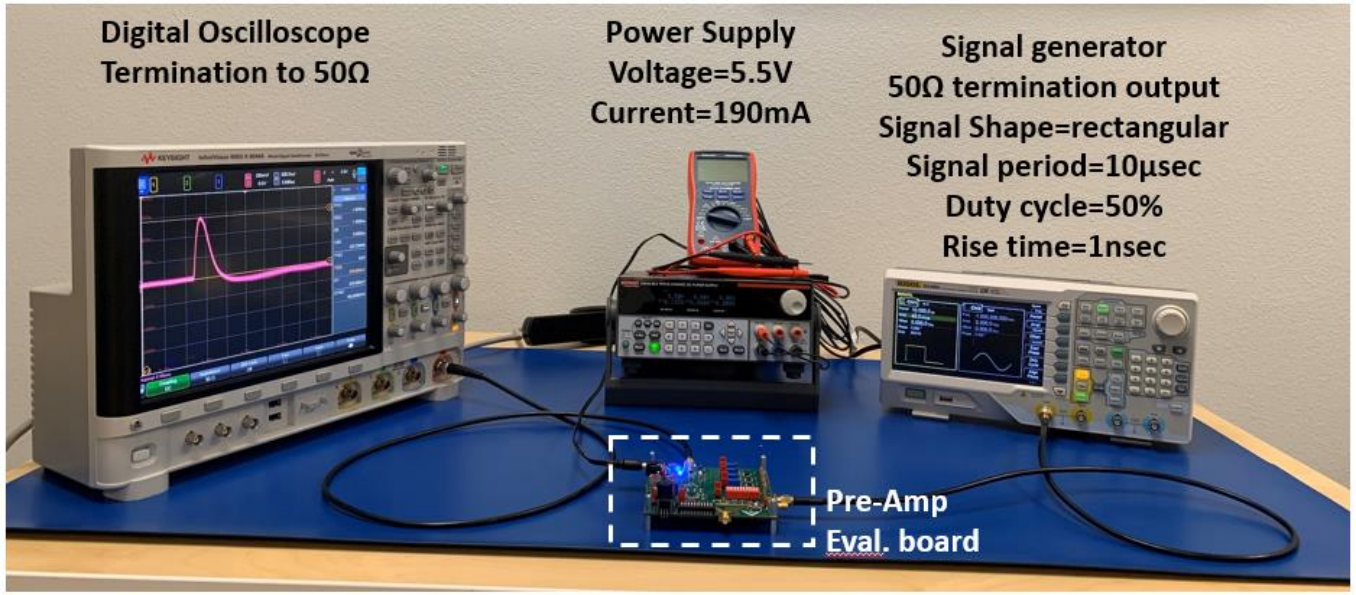


CSA evaluation board 1

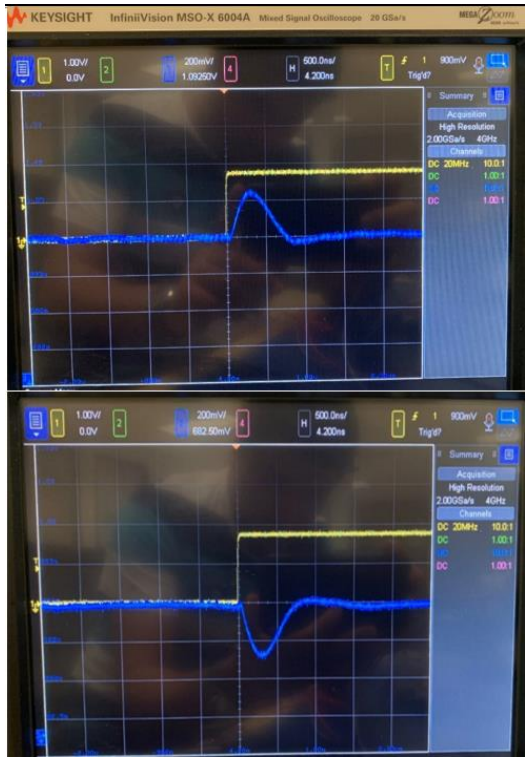


CSA evaluation board 2

CSA measurement setup



CSA measurement test setup

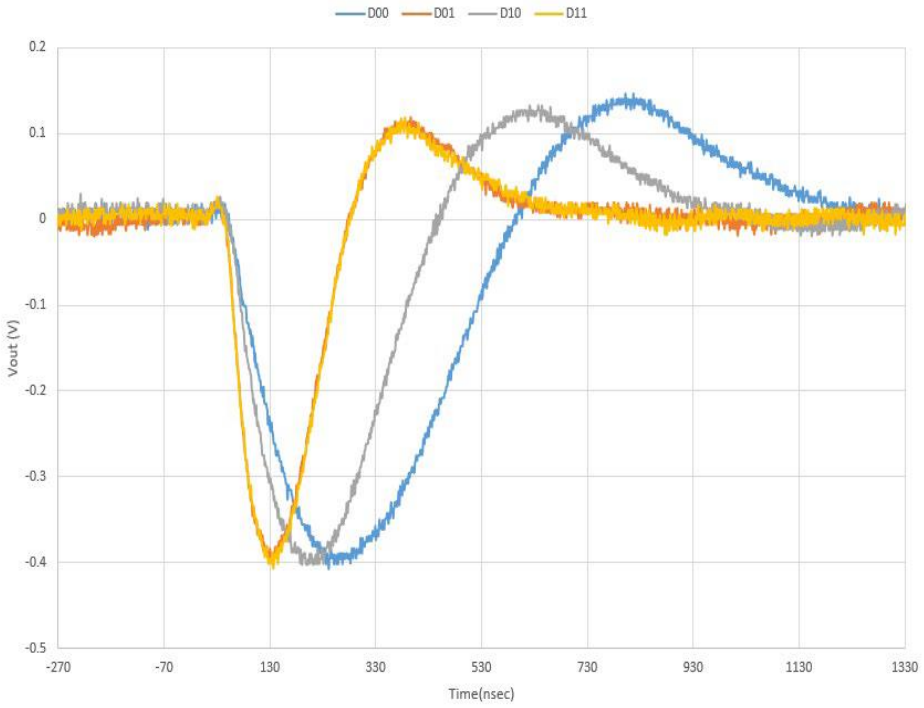


Measured pulse waveforms on an oscilloscope

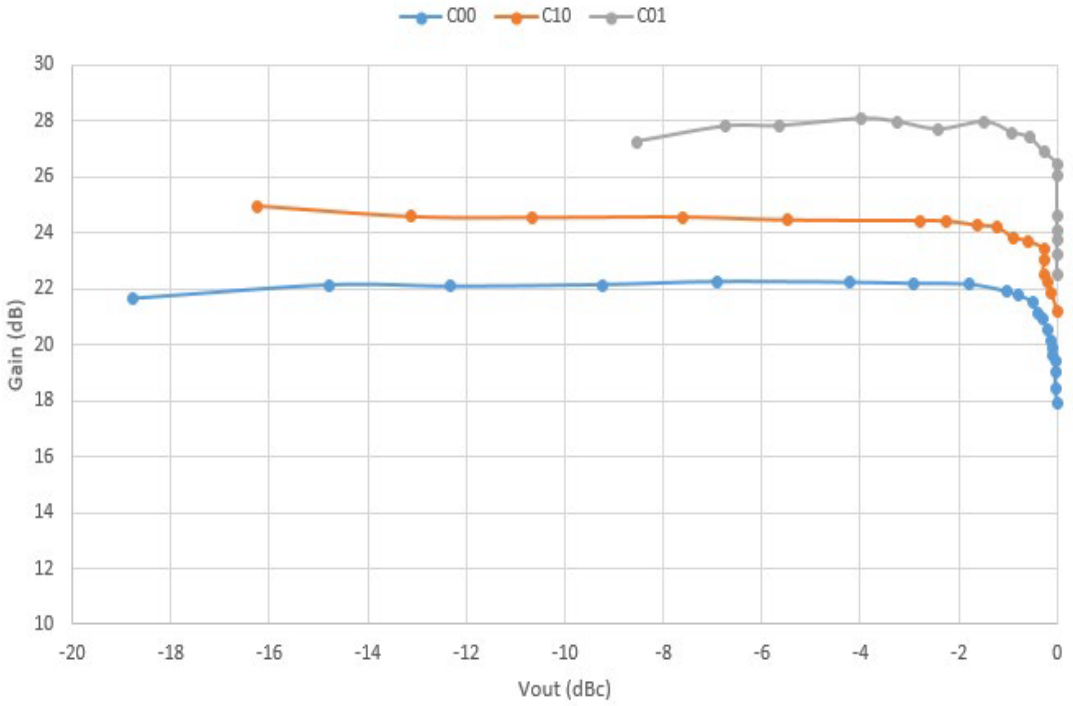
Noise measurement with logic analyzer

CSA1 Test Results

Noise was measured as 430 electrons for 50pF detector capacitance

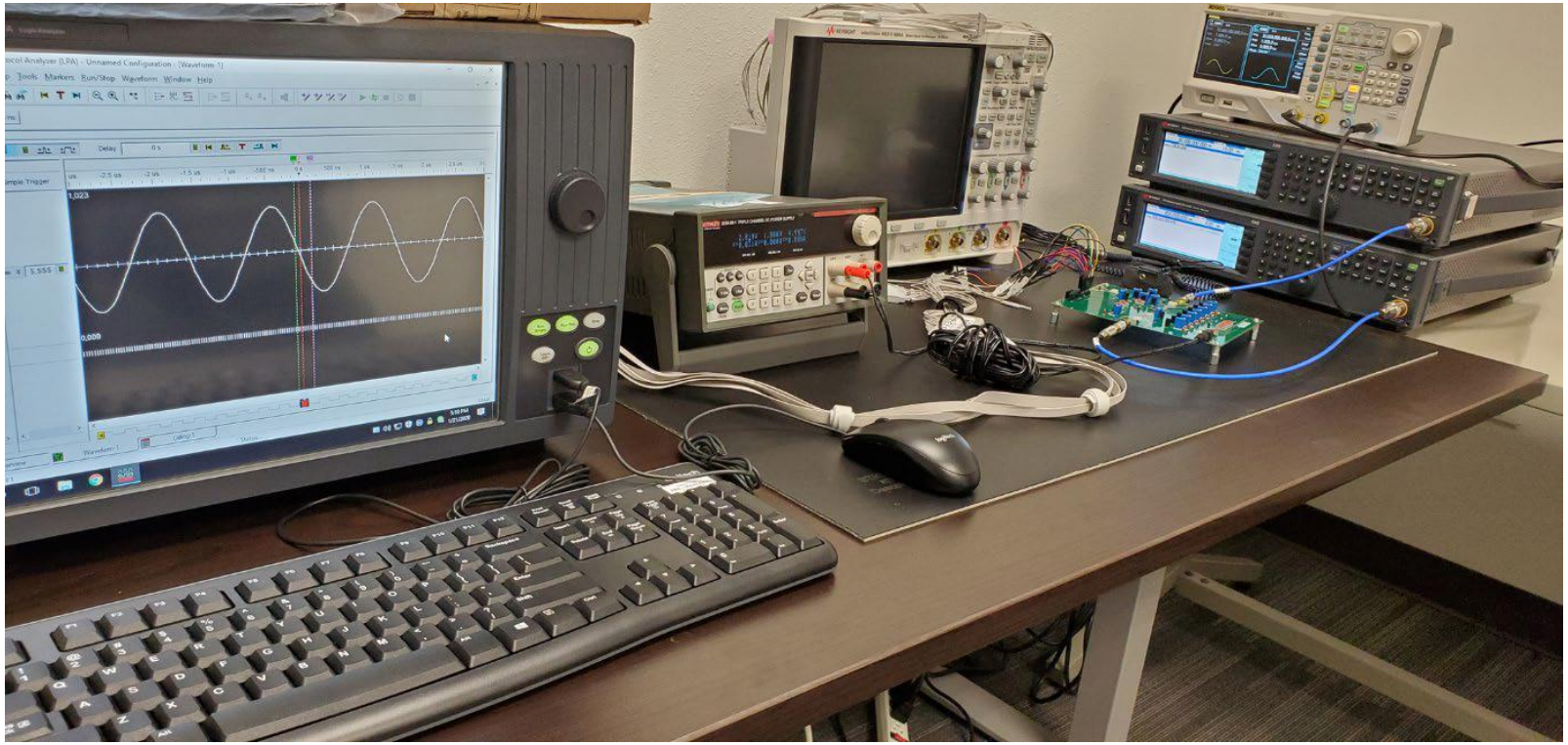


Shaping time programmability measurements



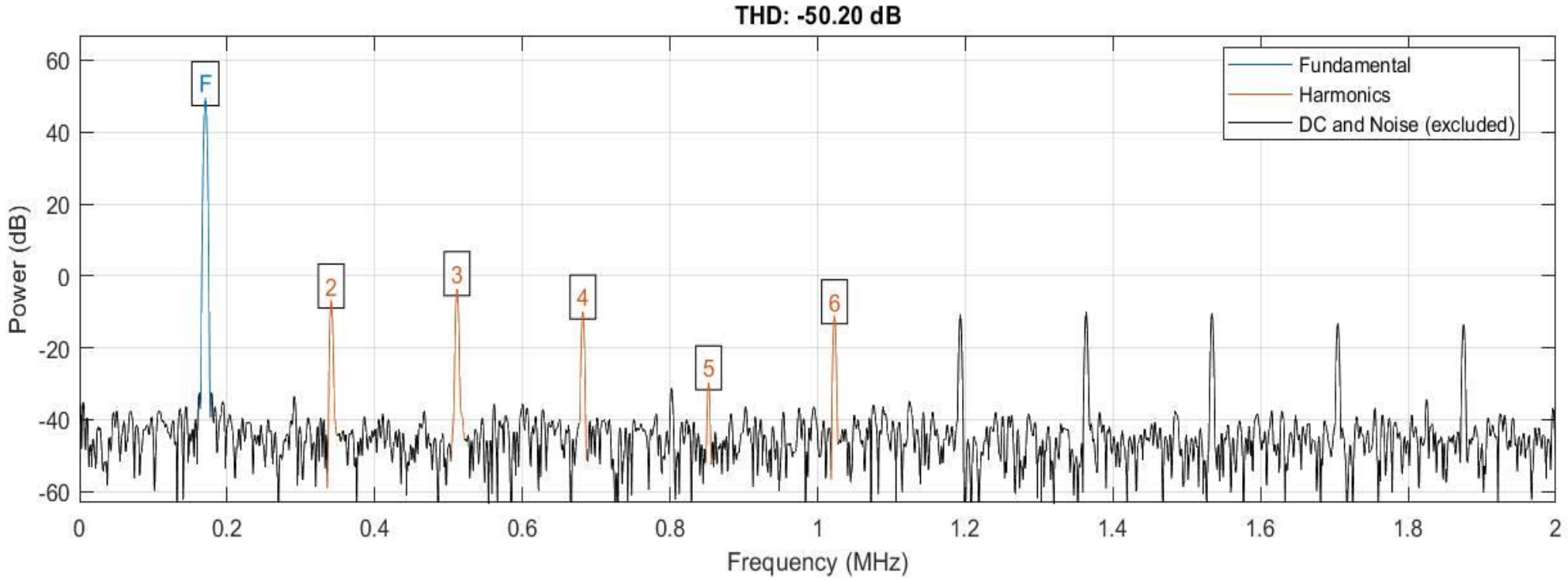
Gain programmability measurements

Analog to Digital Converters Test Results



ADC Test Setup

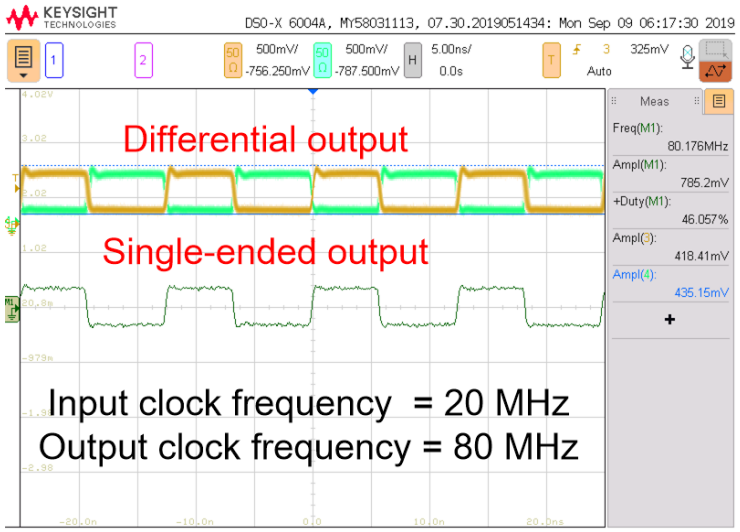
180nm, 10-bit, 50MS/s, 7mW ADC Test Results

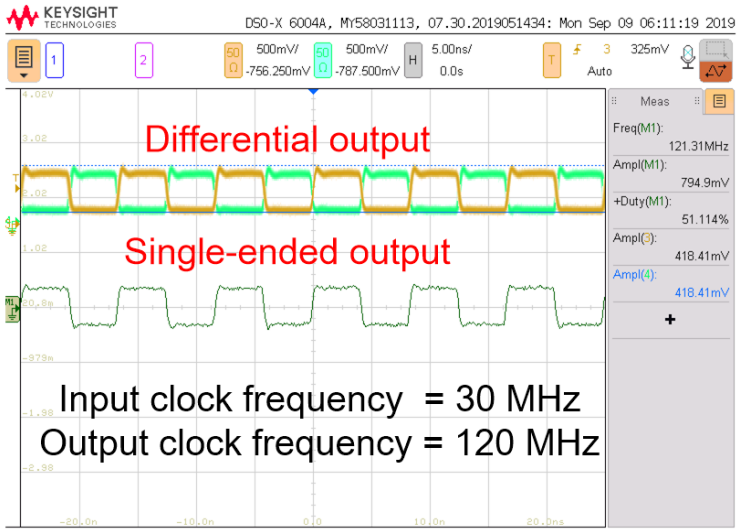


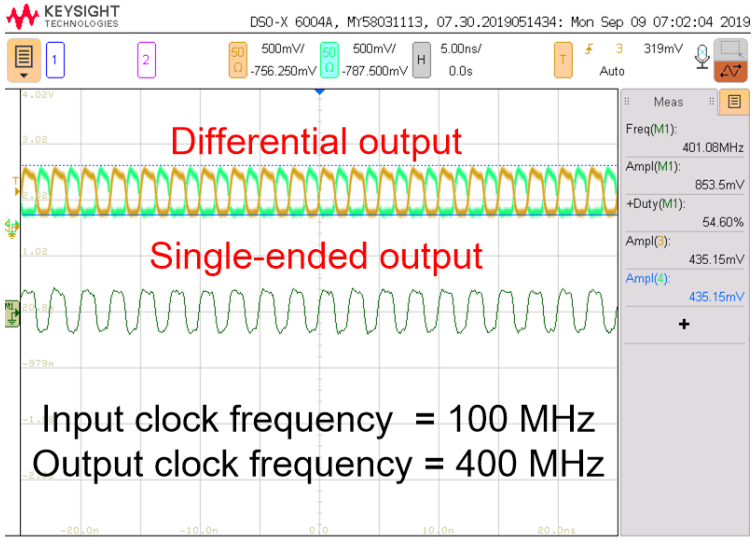
SINAD = 44.04 dB
SNR = 45.24 dB
SFDR = 52.83 dB
THD = -50.20 dB
ENOB = 7.31 Bits

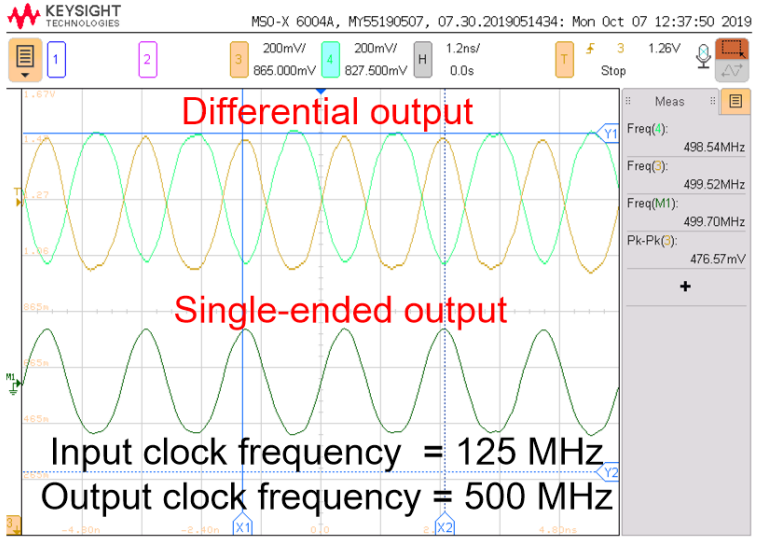
ADC test boards and/or packaged chips are available for customers. 6-ch ADCs are available as bare die.

180nm Low-power High-Bandwidth I/O Interface Test Results





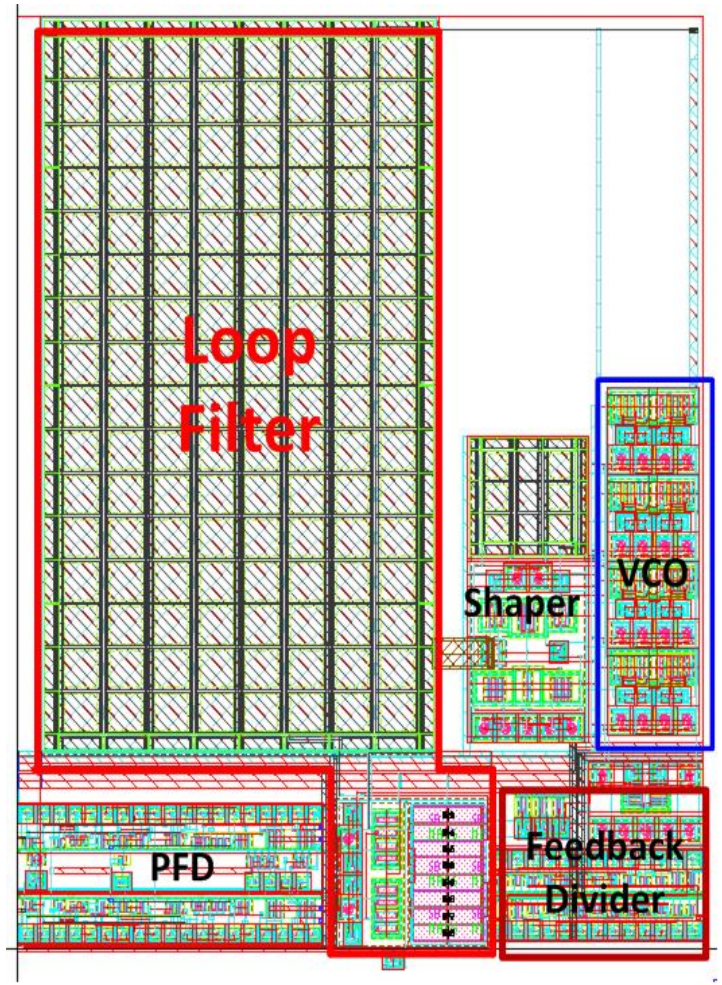




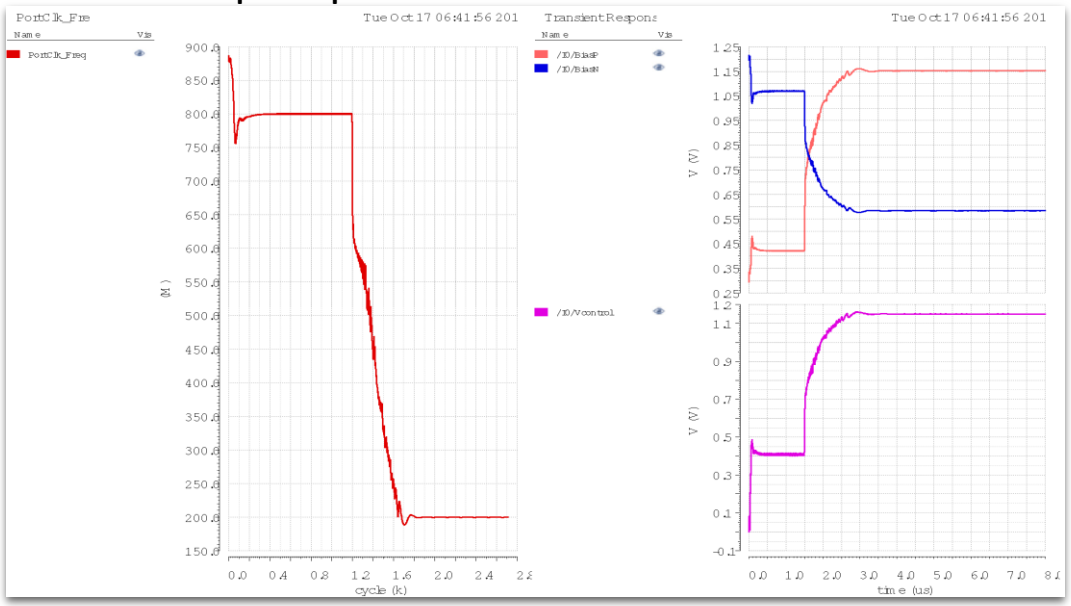
180nm General Purpose PLL for Serializer, Test Results

Alphacore's PLL

- Output freq. range: 80 to 800 MHz
- Power at $1.8\ V$ supply: $3.69\ mW$



Step response from 200MHz to 800MHz



A performance summary of Alphacore's PLL

Input Freq. (MHz)	Output Freq. (MHz)	Lock time	Phase noise	RMS jitter (ps)	Peak-to-peak Jitter(ps)
50	200	2.3us	-144.16dBc/Hz @10MHz	0.339	2.09502
75	300	1.5us	-141.688dBc/Hz @10MHz	0.304	1.87872
100	400	1.2us	-144.4679dBc/Hz @10MHz	0.178	1.10004
125	500	980ns	-145.7717dBc/Hz @10MHz	0.134	0.82812
150	600	880ns	-145.8564dBc/Hz @10MHz	0.119	0.73542
200	800	420ns	-144.3804dBc/Hz @10MHz	0.113	0.69834
Assume the Bit error ratio is 10^{-3}					

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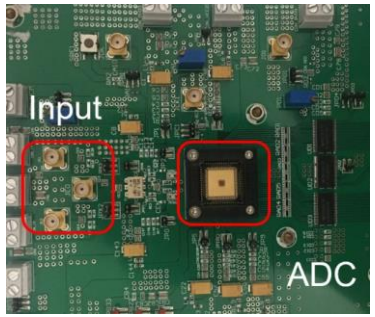
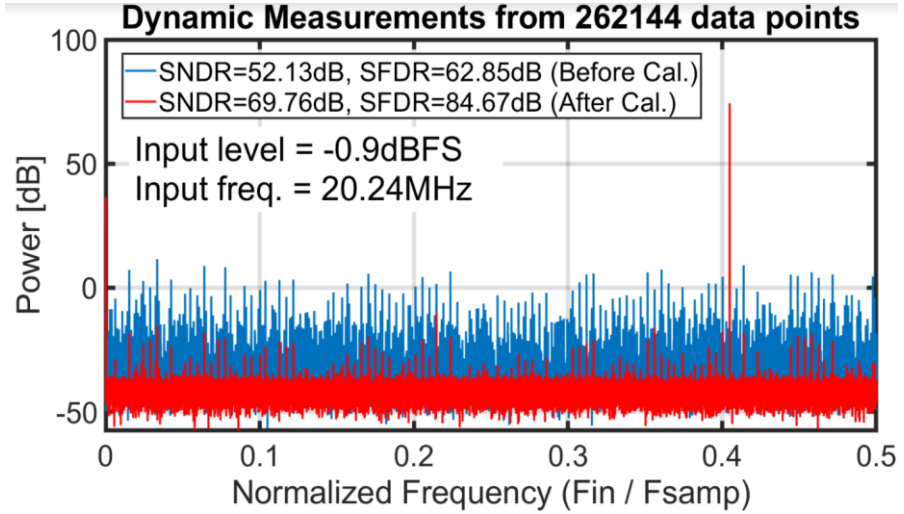
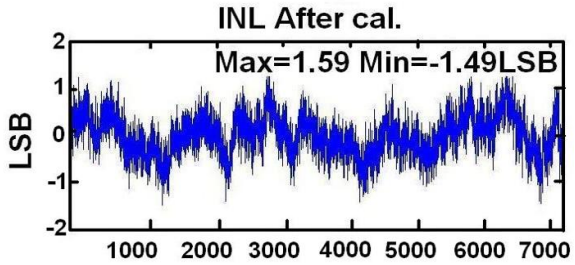
90nm 14-bit, 50MS/s, 62mW ADC (2-channel)



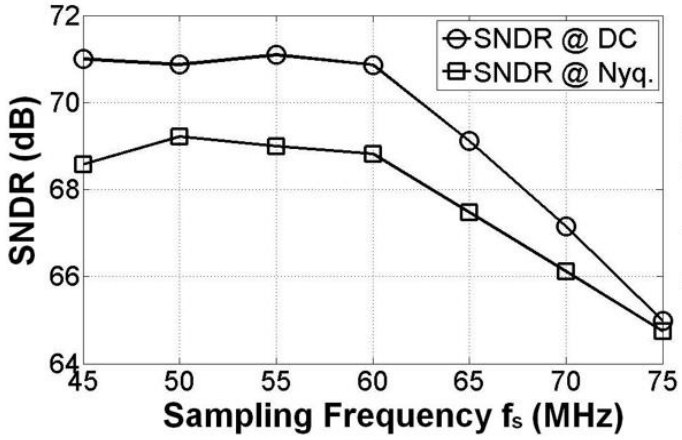
Packaged die and test board



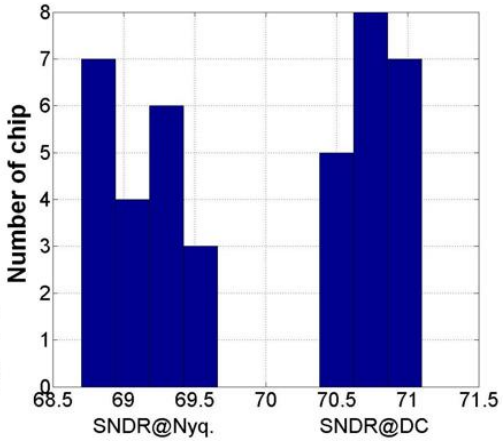
Test results, FFT



Test results, INL



SNDR vs. Sampling f

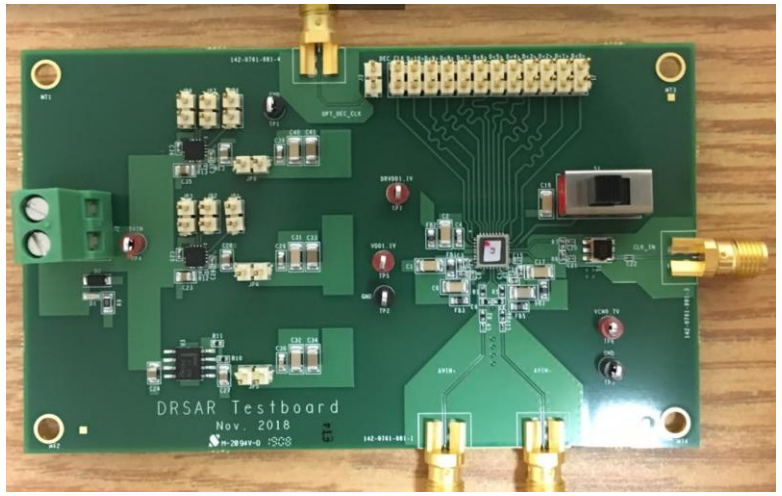


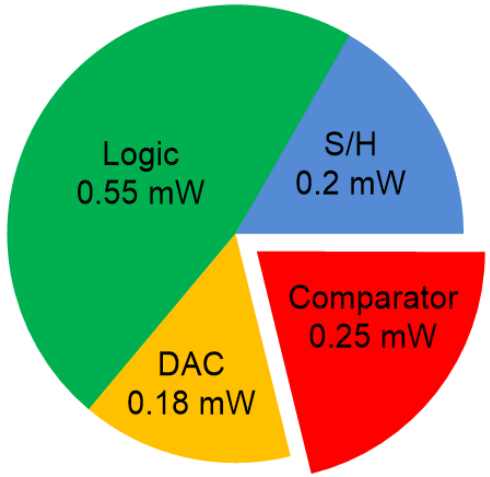
Die Yield

IP Library of 22nm and 28nm CMOS High-Performance Low-Power ADCs

- The library contains more than five 300MS/s – 20GS/s ADCs.
- They are radiation tolerant designs and available for NP/HEP experiments.
- The ADCs can be delivered with “full raw data stream output interface” and/or with “digital waveform sampling buffer” FIFO output interface. The much simpler FIFO interface is enough for most nuclear physics experiments and it enables very low power dissipation and simpler board design.
- Next slides show examples of the library elements.
- **Please contact Alphacore for more details (test results, channel quantity, test boards, pricing...)**

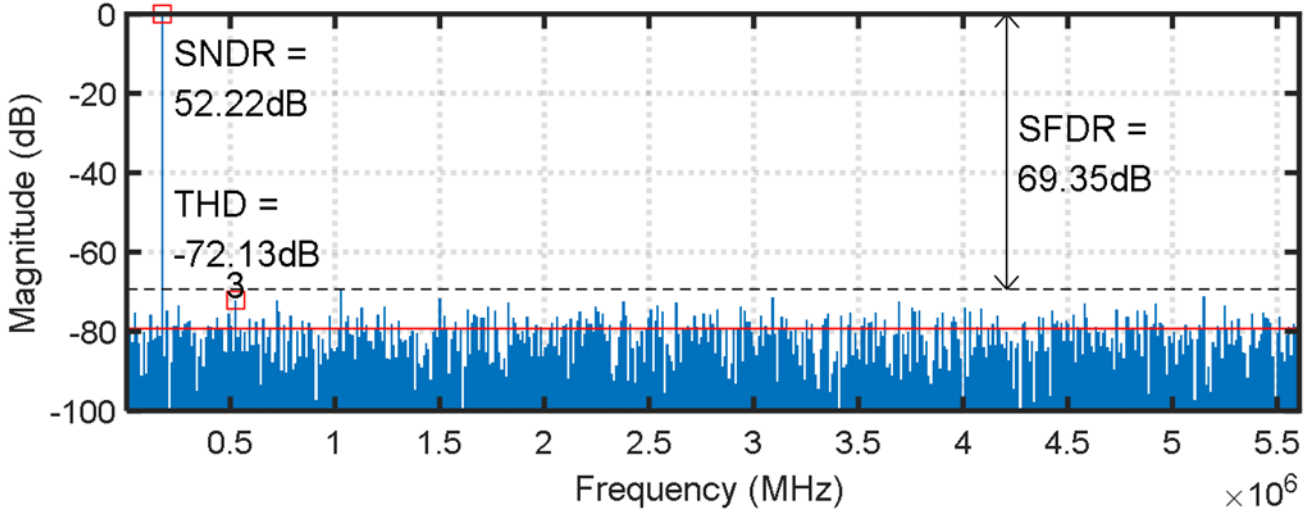
A10B500M, 10bit, 500MS/s, Ultra Low Power ADC

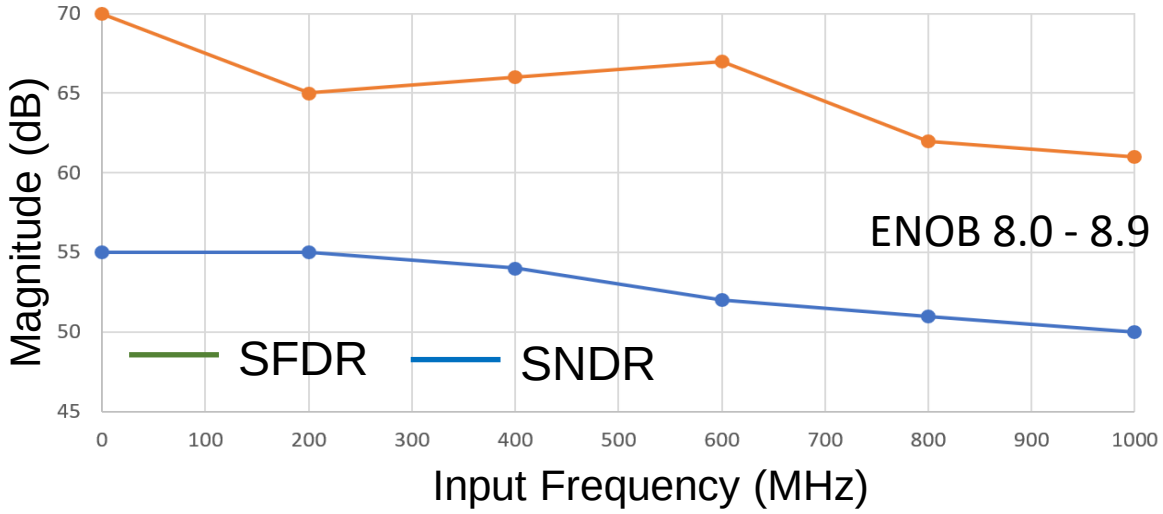




- Single channel ADC with wide input bandwidth (beyond 4th Nyquist zone)
- ENOB 8.0 - 8.9 over four Nyquist bands
- Ultra Low Power <1.18 mW (FOM <6.0fJ/conv.)
- **Can be used as the unit channel in a 10-bit, time-interleaved ADC with sample rate of tens of GS/s**

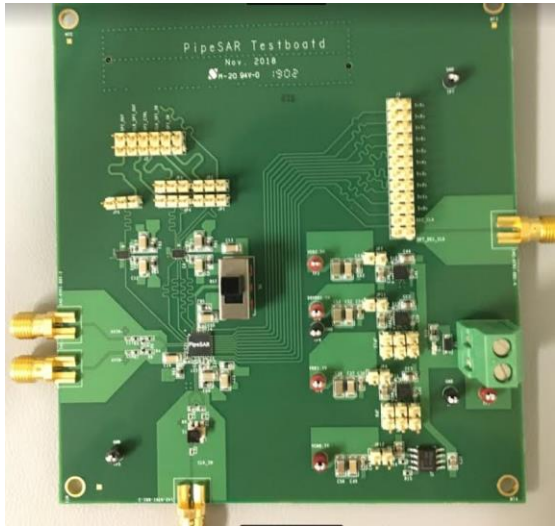
A10B500M, 10bit, 500MS/s, Ultra Low Power ADC





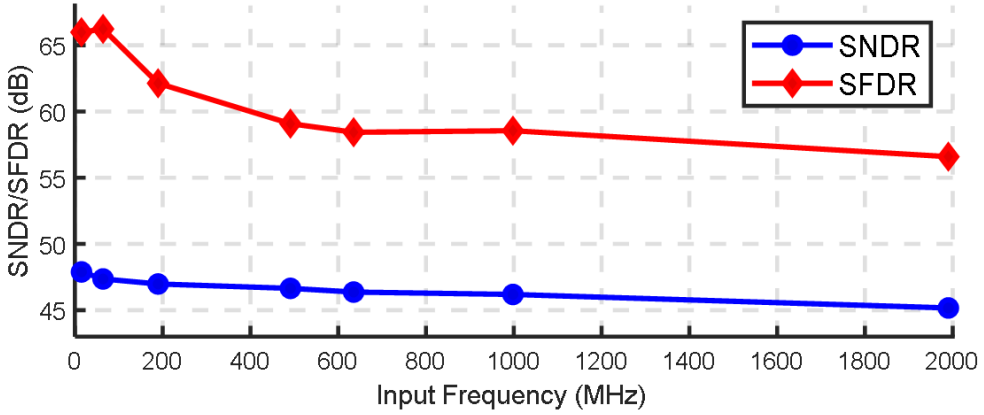
- Single channel ADC with wide input bandwidth (beyond 4th Nyquist zone)
- ENOB 8.0 - 8.9 over four Nyquist bands
- Ultra Low Power <1.18 mW (FOM <6.0fJ/conv.)
- **Can be used as the unit channel in a 10-bit, time-interleaved ADC with sample rate of tens of GS/s**

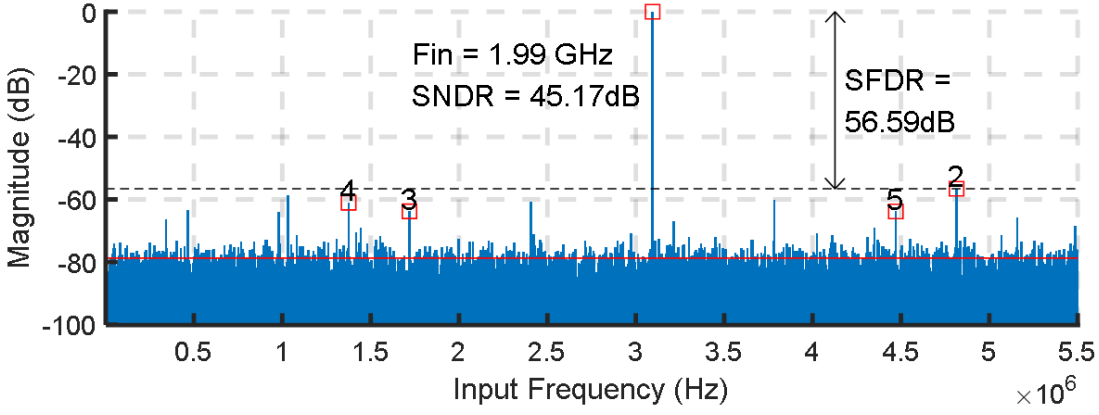
A9B1G, Wide Input BW, 9-bit, 1GS/s ADC



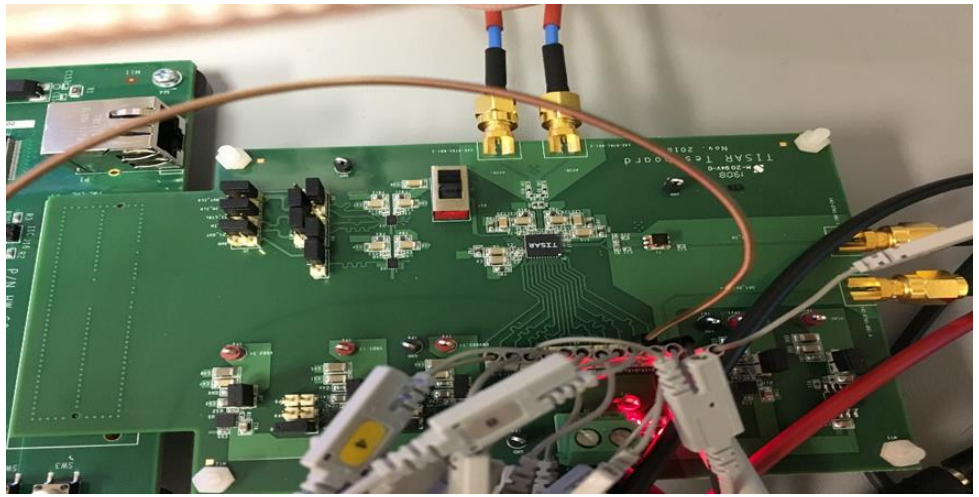
- Single channel with wide input bandwidth (beyond 4th Nyquist zone)
- ENOB stays within 7.2-7.7 over the first four Nyquist bands
- Power <2.1mW (FOM = 10fJ/conv)
- Can be used as the unit channel in a 10-bit, time-interleaved ADC with sample rate of tens of GS/s

Output decimated by a factor of 91 in this test set-up

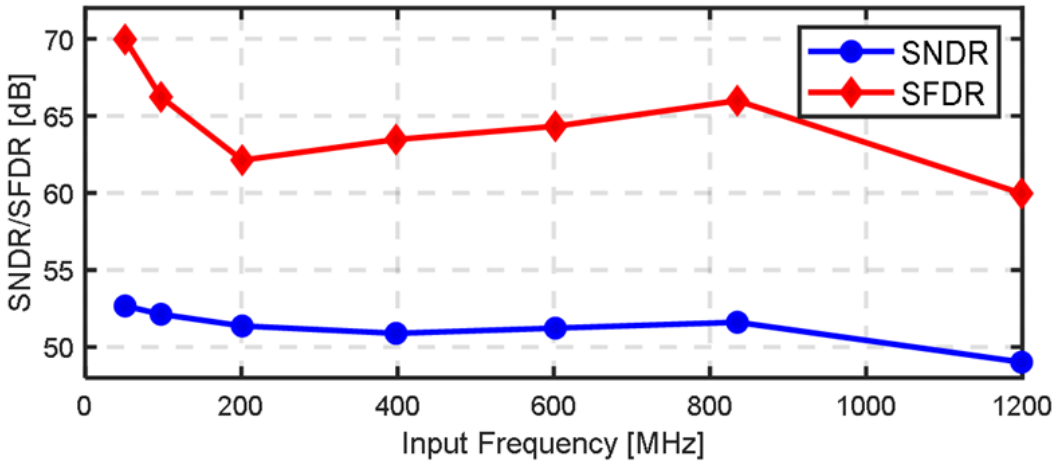


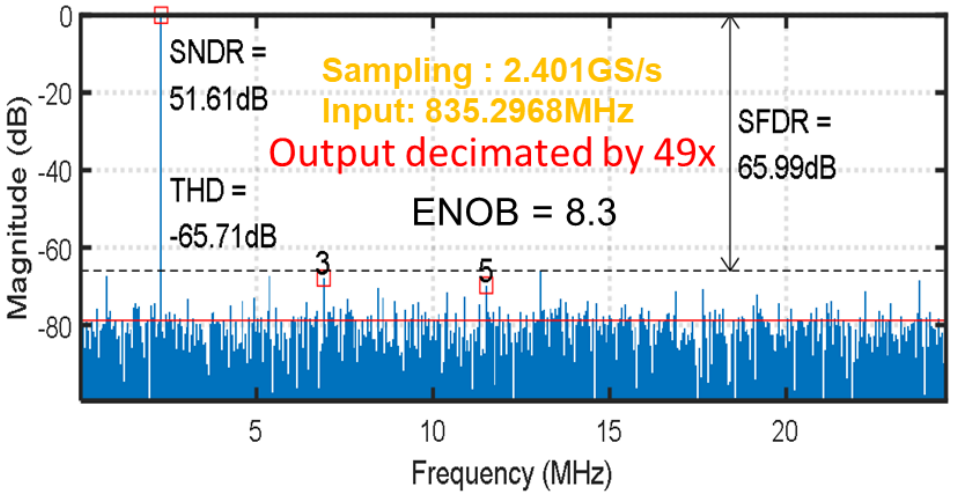


A10B2G, 10 bit, 2.4GS/s, Ultra Low Power ADC

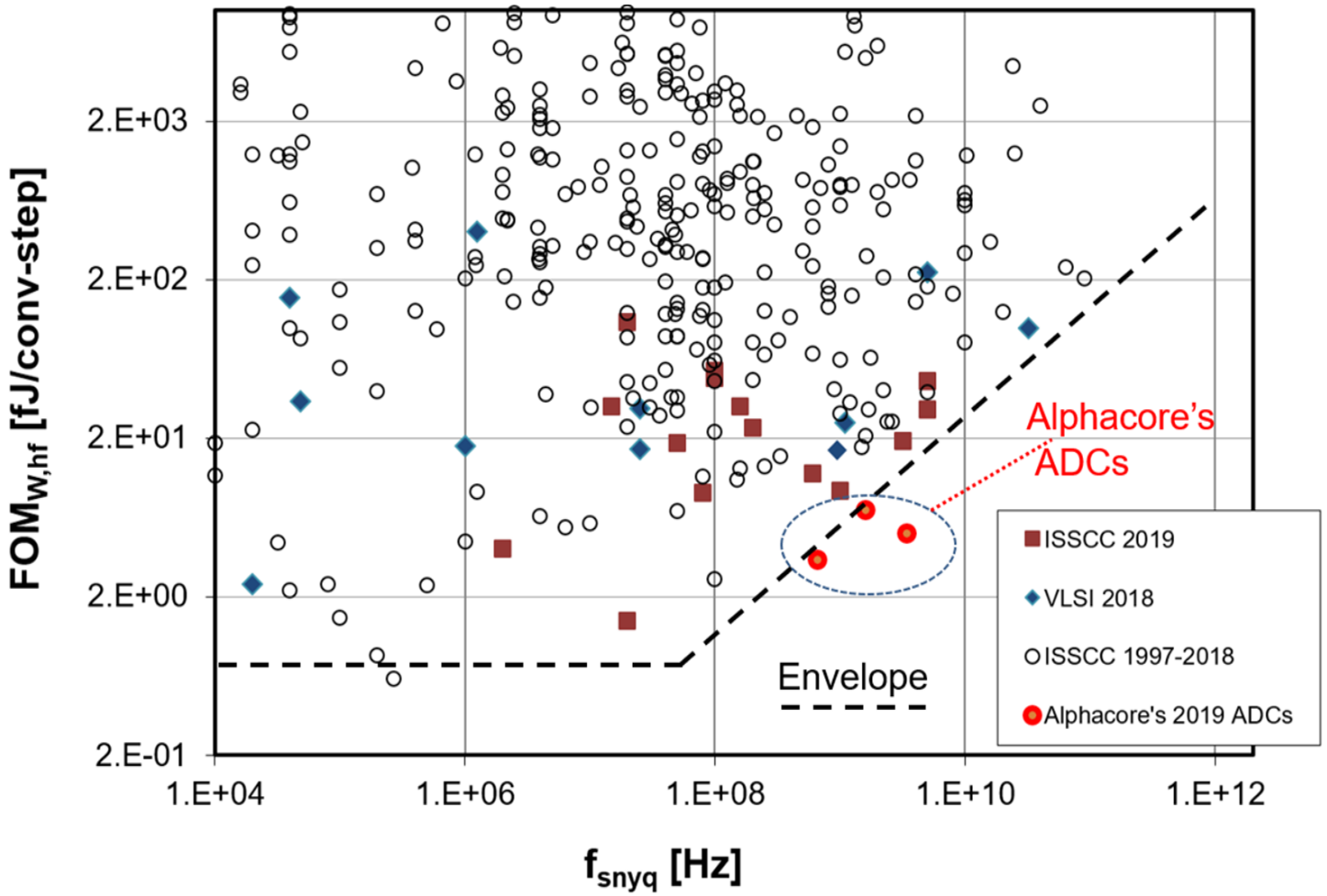


- The ADC has a 8-way interleaved architecture, with combined sampling rate of 2.4GS/s. The sampling rate is limited by on-chip clock buffers. Optimized buffers would deliver up to 3.2GS/s with 6mW of additional power.
- We can interleave 16-way(on-chip) to achieve 6.4GS/s for continuous digitization with no dead time
- The developed calibration algorithm has been shown to be very effective for the calibration of interleaving spurs, in this case yielding SFDR of 60-70 dB and ENOB that varies from 7.9 bits to 8.5 bits in the first Nyquist band.
- Power = 6 mW (FOM = 6.9fJ/conv)

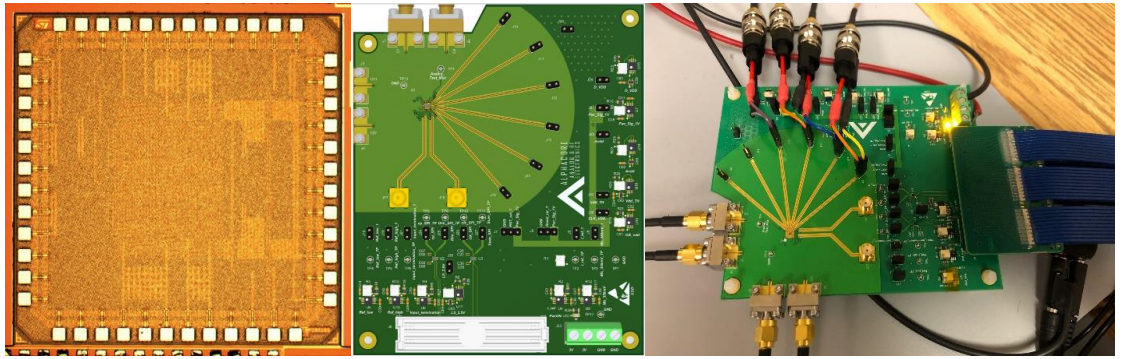




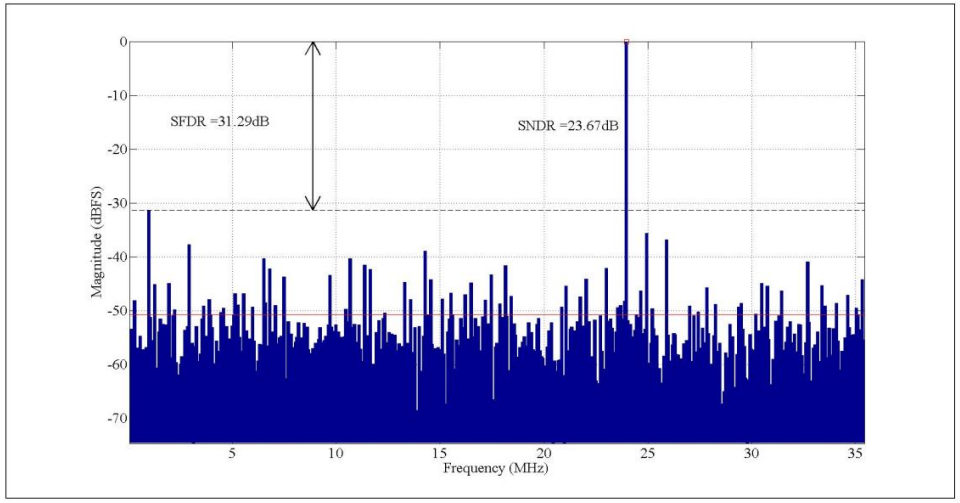
Alphacore's Ultra Low Power ADCs Walden Chart comparison: FOM vs Speed



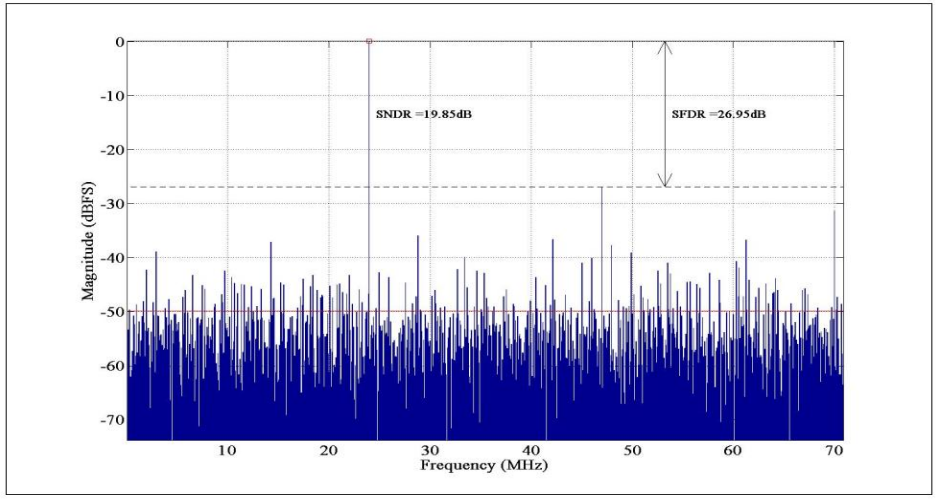
20GS/s 20GHz 6bit ADC



- IP functionality testing completed with a COB package.
- Development of a high-speed custom package with the lowest possible parasitics has been planned. The expected performance with a proper package is >4.5 ENOB, >20GS/s, >20GHz and <300mW.
- The COB package and our current test setup allows testing the ADC at 16GS/s and 8GHz.
- The goal is to be able to test beyond 20GS/s sample rate and 20GHz input bandwidth



ENOB is 3.7 when tested at 9GS/s and 8GHz input bandwidth



Measurements achieved for sampling frequencies up to 17.2GS/s with ENOB up to 3.0 – 3.2 bits

Summary

- This presentation introduced Alphacore's silicon evaluated ADCs and other IP relevant to Nuclear Physics and High Energy Physics researchers.
- Alphacore encourages the researchers to contact us for IP and ICs availability.
- Alphacore is currently looking for opportunities to optimize these readout solutions for actual needs

Acknowledgement

Work on these programs were primarily part funded by DoE/ Nuclear Physics, Grant #DE-SC00017074, and DoE/High Energy Physics, Grant #DE-SC001787.

We especially appreciate the guidance by Drs. Manouchehr Farkhondeh, Michelle Shinn, and Helmut Marsiske.

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Questions?