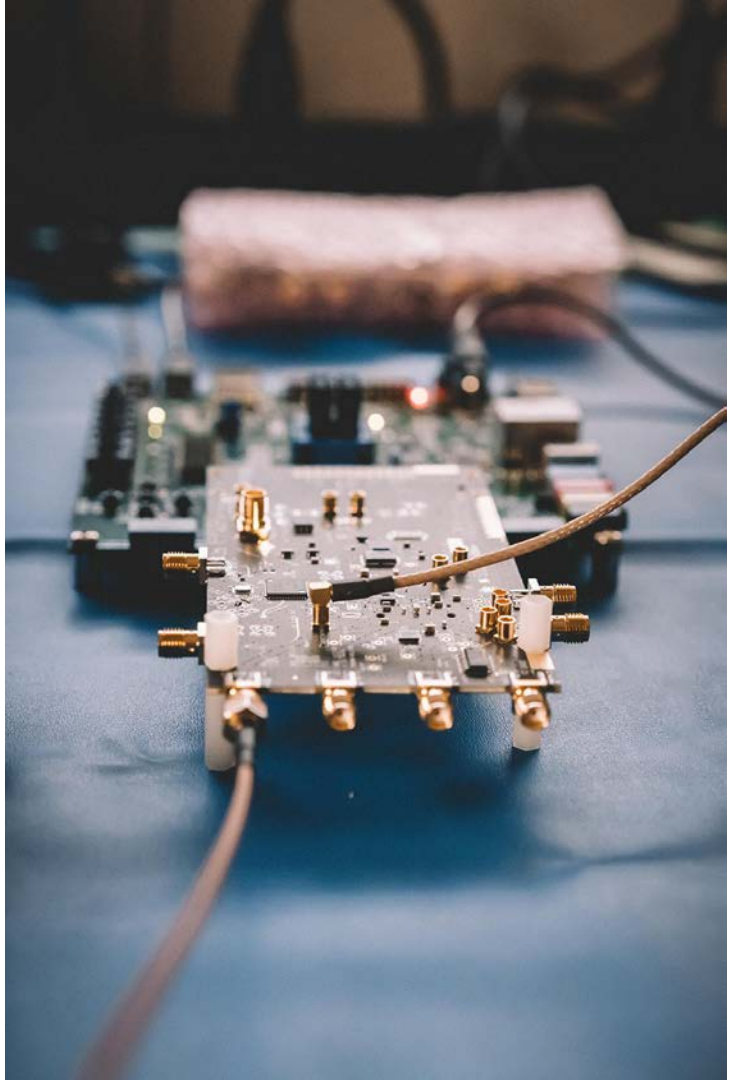

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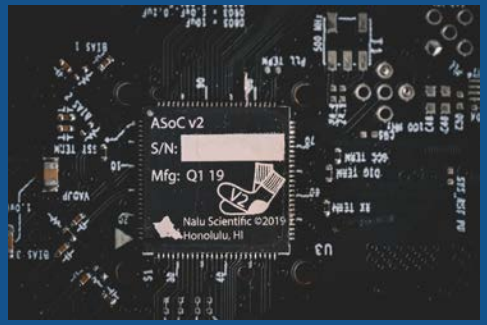
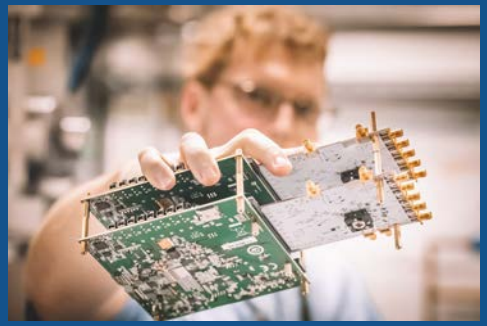
Frontend microelectronics for fast signal acquisition and feature extraction for particle detection and tracking

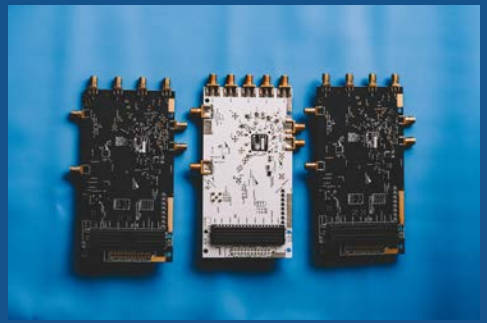
Nov 16, 2020
Isar Mostafanezhad, Ph.D.
Founder and CEO at Nalu Scientific LLC

Work partially funded by US DOE SBIR Grants:

DE-SC0015231, DE-SC0017833, DE-SC0020457







ABOUT NALU SCIENTIFIC

Fast Growing Startup in Honolulu, Hawai'i
- Located at the Manoa Innovation Center
- Over $10M in committed funding, 15 staff members
- Access to advanced design tools
- Rapid prototyping and testing lab

Scientific Expertise
- HEP/NP particle detection and tracking
- Radiation detection
- Readout electronics for Particle Physics

Technical Expertise
- Analog + digital System-on-Chip (SoC)
- Field Programmable Gate Arrays (FPGA)
- Complex multi-layer Printed Circuit Board (PCBs)

NALU SCIENTIFIC
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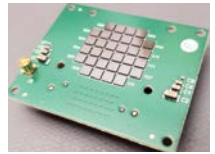
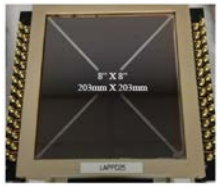
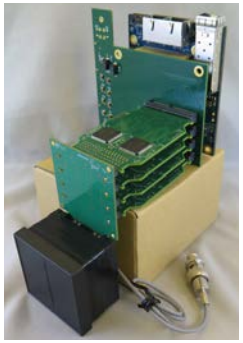
WAVEFORM DIGITIZER SoCs
FOR PRECISE TIME OF FLIGHT ESTIMATION







1. Front-end Chips:

- Event based digitizer+DSP
- 4-32 channel scope on chip
- 1-15 Gsa/s, 12 bit res.
- Low SWaP-C
- User friendly: FW/SW tools

2. Integration:

- SiPM
- PMT
- LAPPD
- Detector arrays

3a. Main application:

- NP/HEP experiments
- Astro particle physics

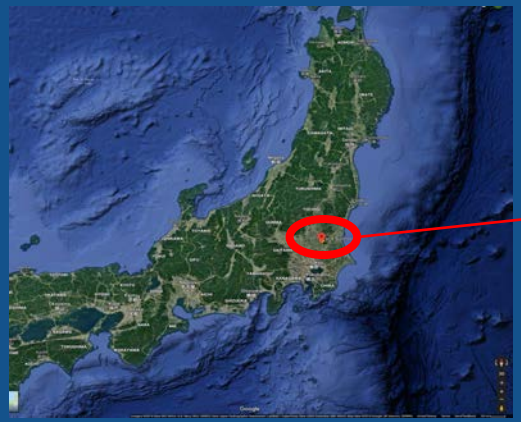
3b. Other applications:

- Beam Diagnostics
- Plasma/fusion diagnostics
- Lidar
- PET imaging

Streaming DAQ workshop, Nov 2020. LAPPD photo courtesy of Incom.

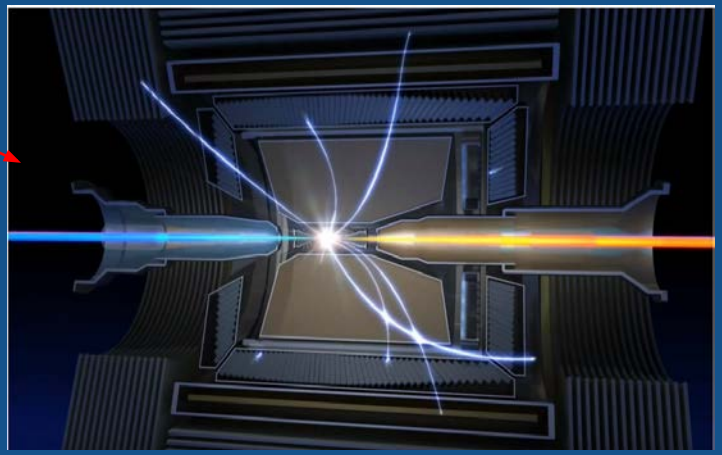
WHERE WE STARTED

A Search for New Physics – The Belle II Experiment



Tsubuka City
Located 60 mi north of Tokyo

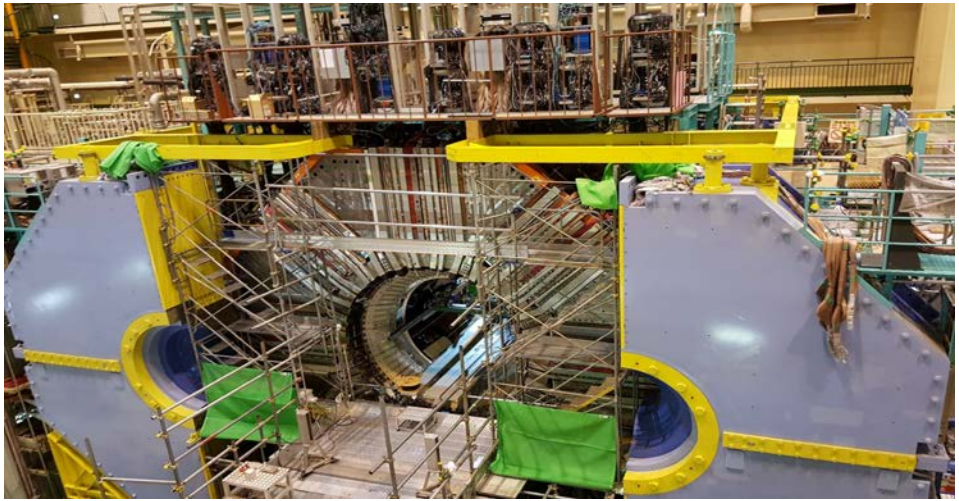
High Energy Accelerator Research Facility (KEK)
in Tsukuba



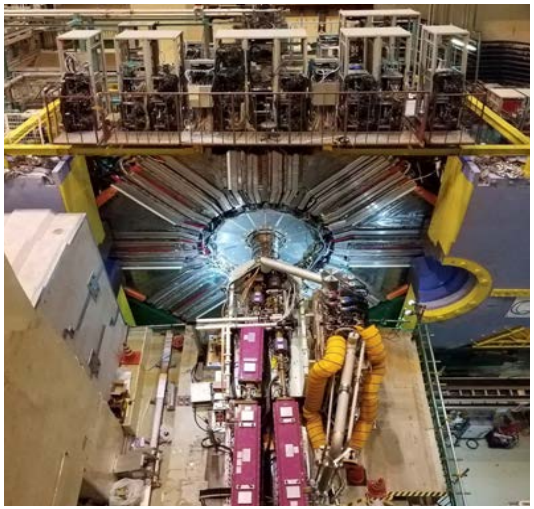
Interaction point inside the electron/positron collider

HISTORY - BELLE II

Belle II Upgrade is a 26+ Country, 900 Member Collaboration



2015



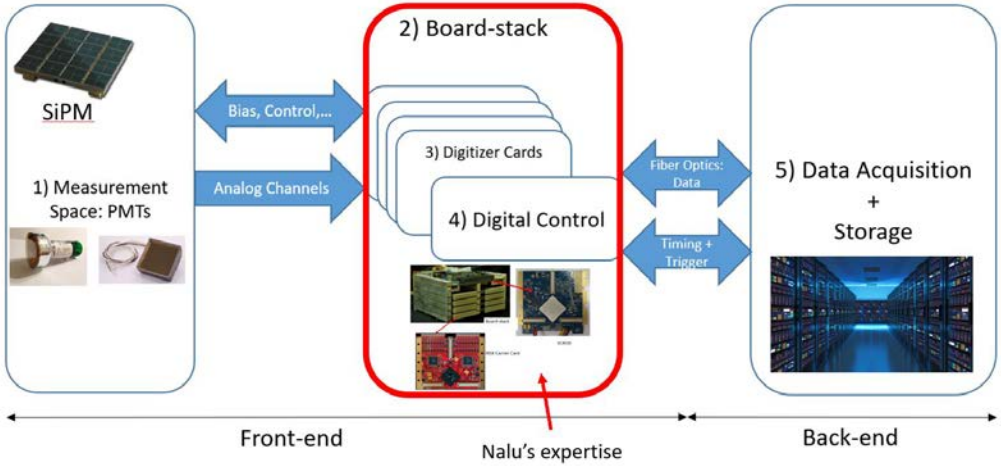
2018

Nalu Staff designed and implemented front-end electronics and FW for KLM (muon system) and iTOP (Cerenkov-based PID) sub-detectors.

Belle II: e+ e- experiment at 40x luminosity of Belle -> Detector needs to operate at severe beam background

HOW DOES NP/HEP EXPERIMENT WORK?

LESSON ONE



LESSON TWO

Next gen Particle Physics electronics need to be:

- Radiation hard
- High performance
- Accommodate long trigger delay
- Low cost, low power
- User friendly

Solution: New System-on-Chip Integrated Circuit

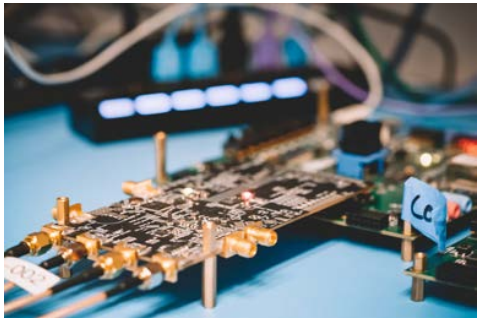
Opportunity: Not many commercial options available

Proposed Solution:
Chip level integration of switched capacitor array (analog) with digital processing.

Current SoC-ASIC Projects

Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Available Date
ASoC	3-5	0.8	16k	4	35	Rev 3 avail
HDSoC	1-3	0.6	4k	64	80-120	Feb'21
AARDVARC	8-14	2.5	32k	4	4	Rev 3 avail
AODS	1-2	1	8k	1-4	100-200	Rev 1 avail

- **ASoC**: Analog to digital converter System-on-Chip
- **HDSoC**: SiPM specialized readout chip with bias and control
- **AARDVARC**: Variable rate readout chip for fast timing and low deadtime
- **AODS:** Low density digitizer with High Dynamic Range (HDR) option



ASoC V3 DESIGN DETAILS

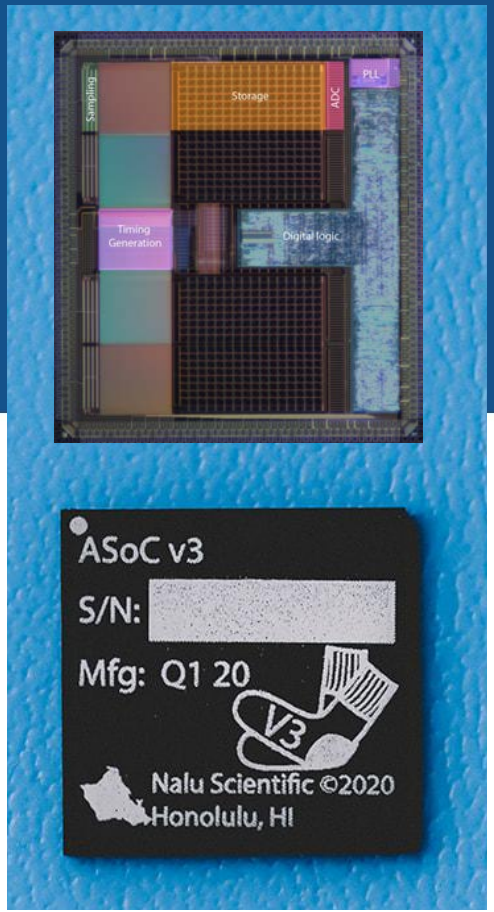
Compact, high performance waveform digitizer

- High performance digitizer: 3+ Gsa/s
- Highly integrated
- Commercially available, low cost, patented design
- 5mm x 5mm die size

Parameter	Spec
Sample rate	2.4-3.6GSa/s
Number of Channels	4
Sampling Depth	16kSa/channel
Signal Range	0-2.5V
Number of ADC bits	12 bits
Supply Voltage	2.5V
RMS noise	~1.5 mV
Digital Clock frequency	25MHz
Timing resolution	<25ps (see below for details)
Power	120mW/channel
Analog Bandwidth	850MHz
Serial interface	Up to 500 Mb/s***

- Calibration memory access
- PLL on chip
- Isolated analog/digital voltage rings
- Serial interface
- Self triggering
- Completed DOE Phase II SBIR
  - Eval cards avail
  - Custom boards under dev

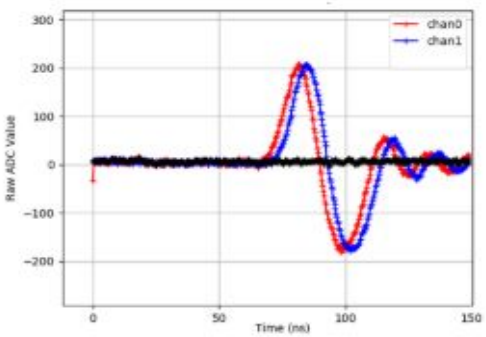
IEEE NSS 2020



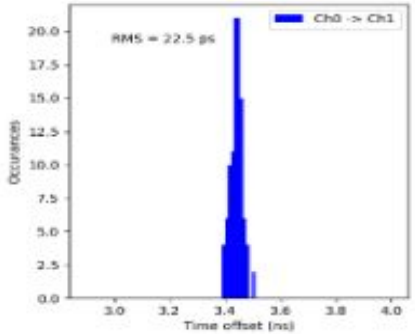
ASoC V2* MEASUREMENTS

*V3 under test

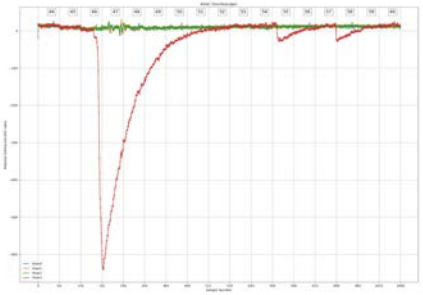
Live demo at IEEE NSS-MIC 2019



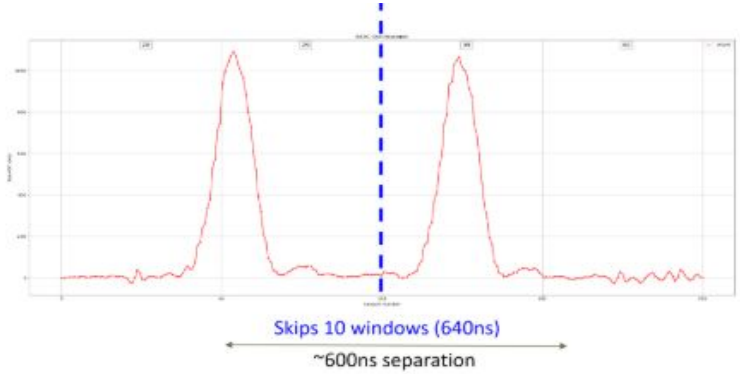
Timing resolution: 22ps

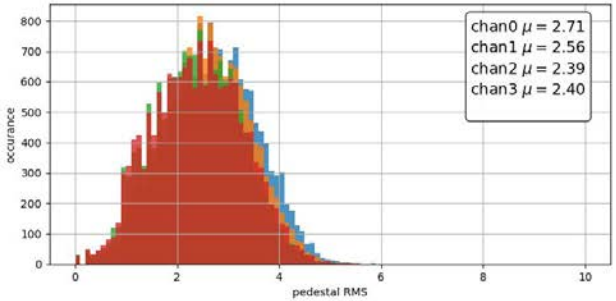


SiPM waveform readout



ROI Readout

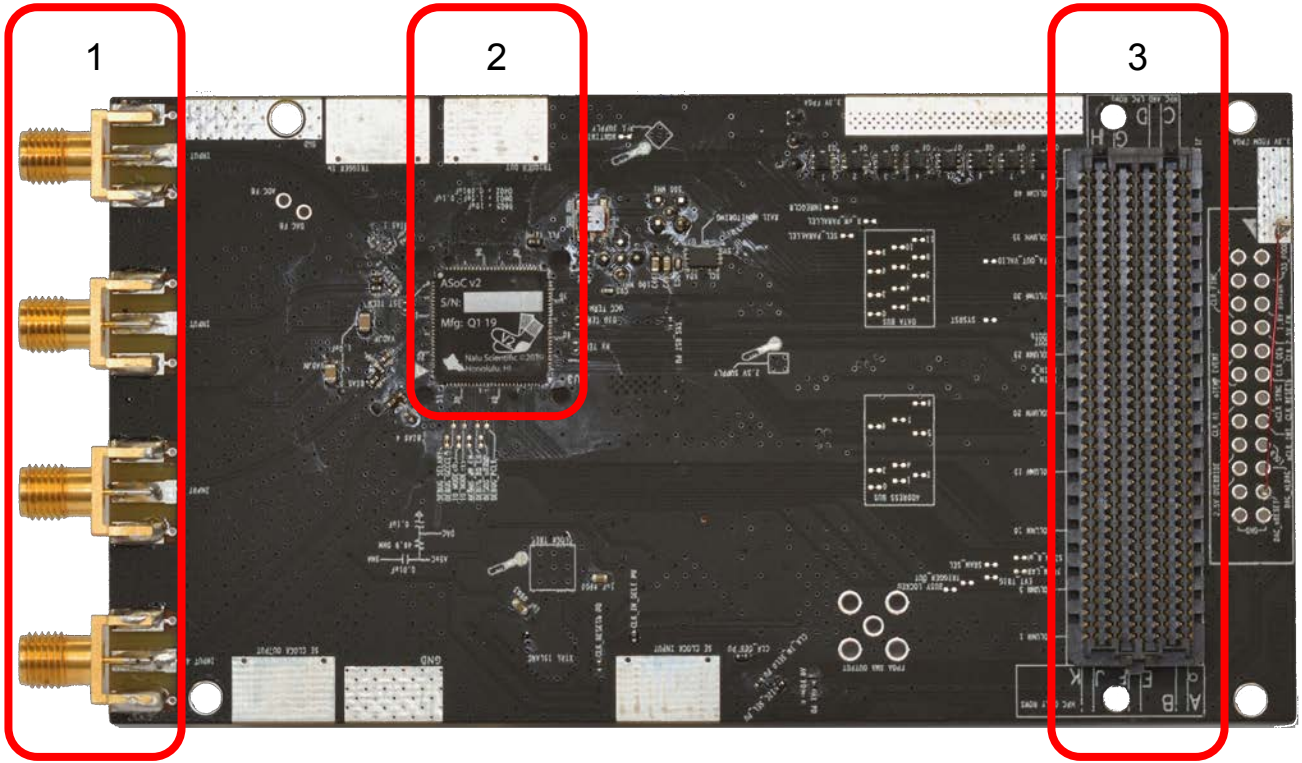


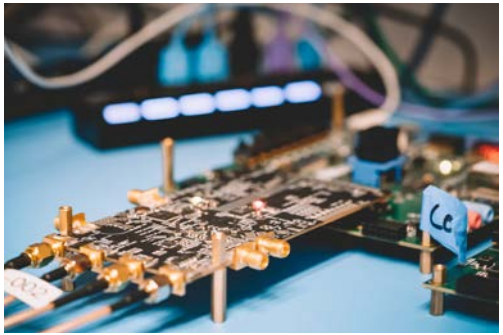


Noise residuals after pedestal subtraction - typical ~2.5 counts = 1.0mV

ASoC Eval Card

1. SMA inputs
2. ASoC chip
3. FMC for FPGA card





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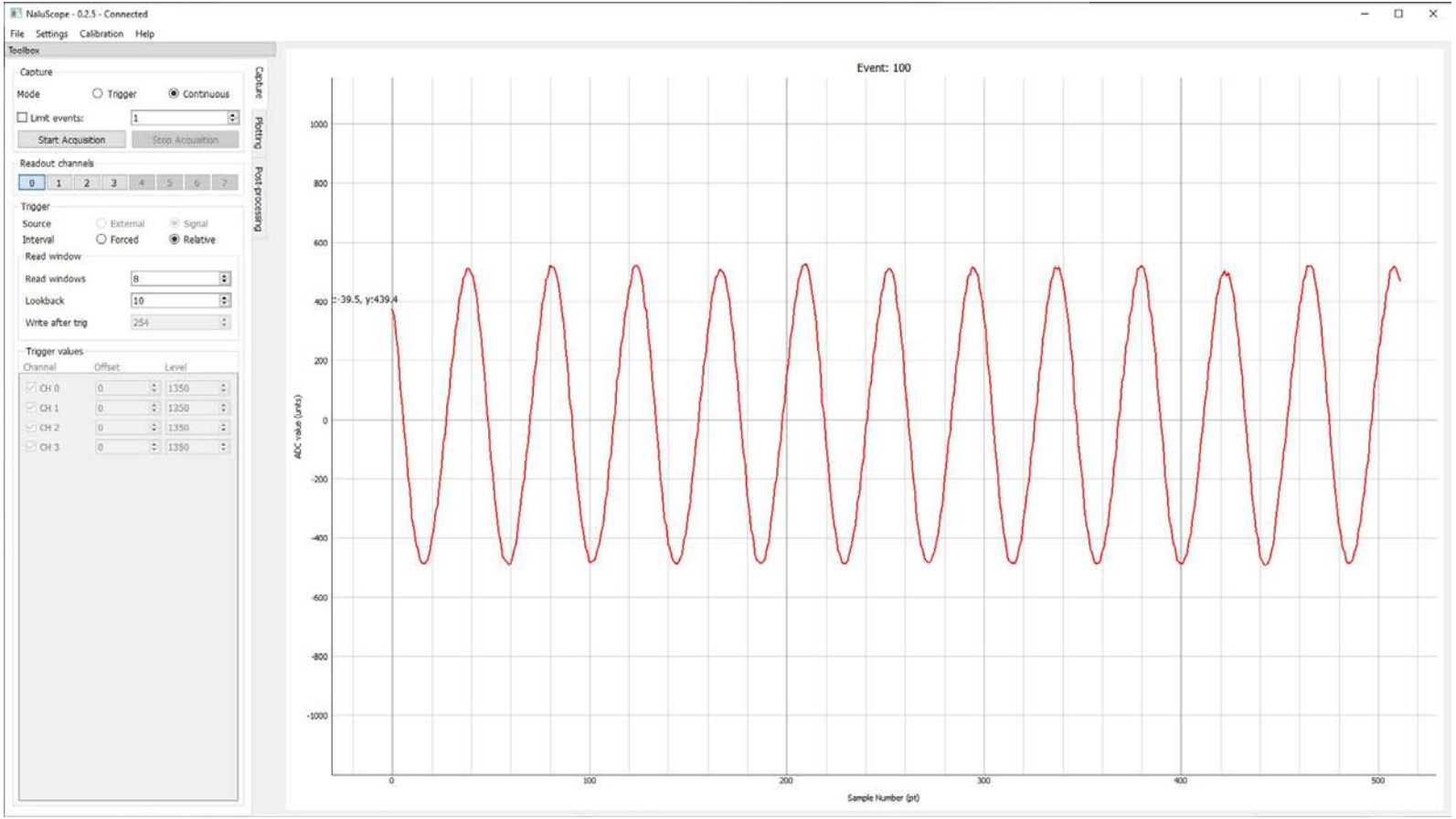
NaluScope Common Software and GUI

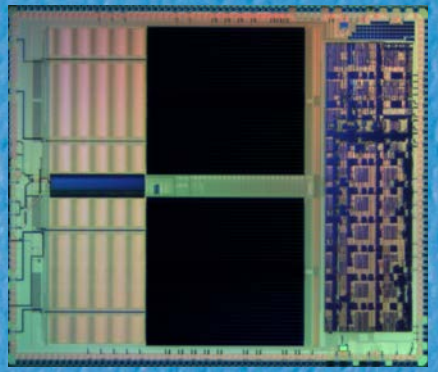


NALU SCIENTIFIC
ENABLING INNOVATION

AARDVARC V3 DESIGN DETAILS

Compact, high performance waveform digitizer

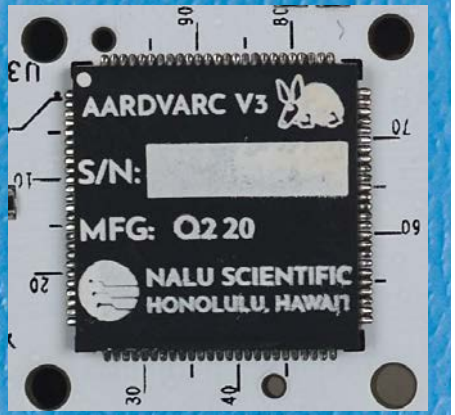
- High performance digitizer: 10+ Gsa/s
- Highly integrated
- Commercially available, low cost, patented design
- 5mm x 5mm die size



Parameter	Spec
Sampling Rate	10-14 GSa/s
ABW	> 1GHz
Depth	32k Sa
Trigger Buffer	~3 us*
Deadtime	0**
Channels	4
Supply/Range	1.2V/0.3-0.9V
ADC bits	12
Timing accuracy	<5ps (@13 GSa/s)
Technology	130 nm CMOS
Power	80mW/ch

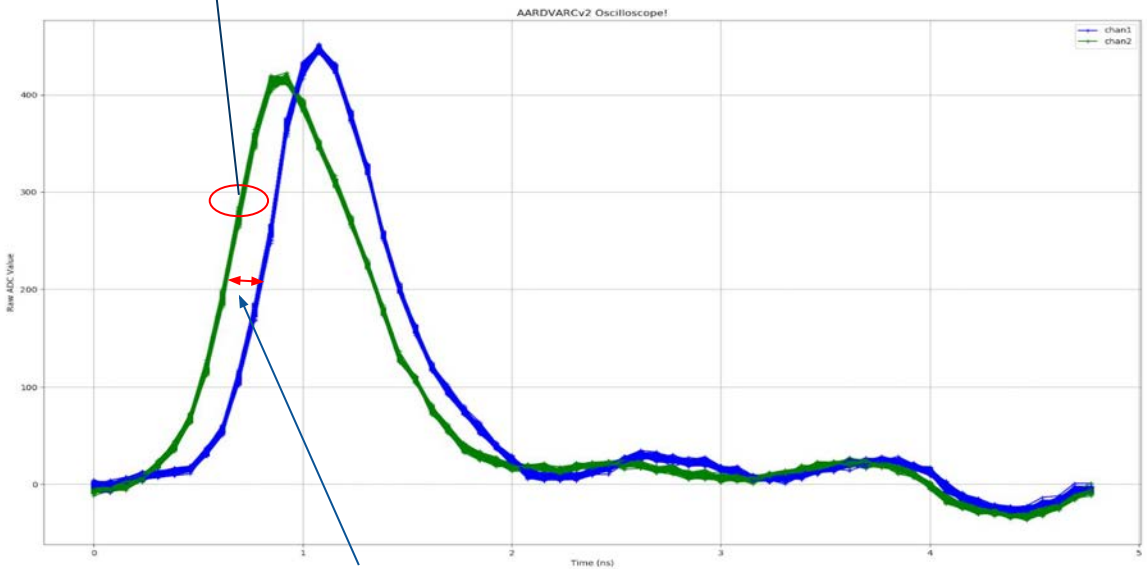
- On chip calibration
- On chip PLL
- On chip feature extraction
- Isolated analog/digital voltage rings
- Serial interface
- Funded DOE Phase IIA SBIR

IEEE NSS 2020



AARDVARC V2*

Overlayed 250 events showing very small timing jitter

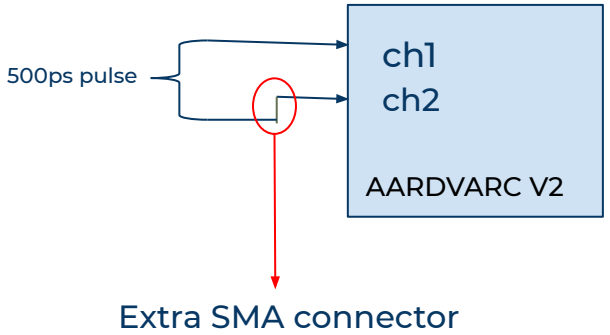


Delay caused by an extra SMA connector ~ 140ps (1-2 Samples at 13 GSa/s)
Jitter measured at ~1-2ps

Two pulses in two channels in 250 events

Pulses created by shunting Si5341 square wave output

Difference in timing created by adding a right angle connector to cable



Note: the pulse gen is synced with ASIC sampling clock.

*V3 is under test with expected similar performance

HDSoC V1 DESIGN DETAILS

High density waveform digitizer with dead-timeless readout

- High Density: 64 channels
- Highly integrated, SiPM gain + bias
- Commercially available, low cost CMOS

Parameter	Spec
Sampling Rate	1-2 GSa/s
ABW	> 600MHz
Depth	2k Sa
Trigger Buffer	~3 us*
Deadtime	0**
Channels	64
Supply/Range	2.5
ADC bits	12
Timing accuracy	80-120ps
Technology	250 nm CMOS
Power	TBD

- On chip calibration
- Serial interface
- On chip Feature extraction
- Virtually dead-timeless
- Phase I SBIR Project

**Up to 240 KHz / ch with single serial link using on-chip self trigger and feature extraction.
Up to 400 kHz / ch with additional serial links.

Dead-timeless operation

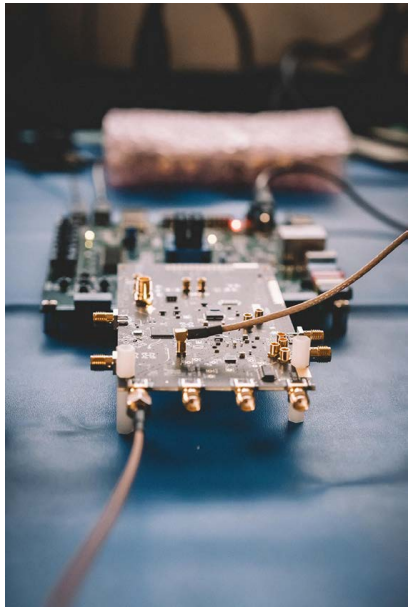
- **Multi-bank switched capacitor array:**
  - Older versions of chips (ASoC, AARDVARC)
  - Long internal analog memory (storage)
  - Capable of self triggering
  - Suitable for long trigger delays (3-5 us)
  - Large die size
  - **ASoC V3 may be able to readout up to ~100 kHz of input rate without deadtime (estimated).**
- **Virtual analog memory:**
  - New lines of chips (HDSoC)
  - Unlimited virtual depth (up to a certain rate)
  - Small die size, lower power
  - Dead-timeless up to a certain rate, designed with self-triggering in mind
  - Suitable for streaming mode readout
  - Feature extraction and on-chip data reduction
  - Estimated 240-400 kHz rate handling

How can Nalu's chips contribute?

Project	Sampling Frequency (GHz)	Buffer Length (Samples)	Number of Channels	Timing Res. (ps)	Rate handling	TRL	Suitable for	Potential EIC Sub Detectors
ASoC	3-5	16k	4	35	~100kHz	High	Low density, precision timing, flexible board integration	
HDSoC	1-3	4k	64	80-120	~240, 400 kHz	rev1	High density SiPM, MA-PMT	mRICH, dRICH
AARDVARC	8-14	32k	4	4	~125kHz	Med	Precision timing, low density	
AODS	1-2	8k	1-4	100-200		Med		

- Significant investment from DOE SBIR program
- All chips designed with commercial grade design tools - can be readily commercialized
- Nalu staff already involved with EIC-PID readout, white papers, etc
- Ongoing discussion with system integrators to connect chips to DAQs
- High levels of integration on chip - clock, calibration, memory - experiment in mind.
- Previous versions of similar technology have been used in experiments (Belle II)

Summary



- Nalu Scientific portfolio of FE/digitizer electronics
  - Specialized for NP/HEP experiment readout
  - High integration (clock, memory, calibration)
  - Packaged chips and eval cards available
  - Additional testing under way including irradiation
- Nalu staff have been involved in:
  - Previous NP/HEP electronics/FW development
  - Advanced mixed signal ASIC design
  - A variety of detector electronics design
- Funding:
  - SBIRs: costly chip development
  - Trade studies: initial assessment
  - Custom design contracts: Implementing new packaging and PCB designs
- Next steps:
  - Continue chip+PCB development
  - Continue engagement with experiments in order to tailor the designs to evolving experiment needs
  - Eval boards available for testing

ACKNOWLEDGEMENTS

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