A free running DAQ for COMPASS++/AMBER

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Federal Ministry
of Education
and Research

COMPASS++ / AMBER Collaboration

Work on physics program of possible COMPASS successor was started ≈10 years ago:

EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

CERN-SPSC-2019–022
SPSC-P-360
September 30, 2019

51 institutions, ~260 authors,
19 new institutions with respect to COMPASS (Majority from USA, also Germany, Italy, Russia etc.)

Proposal for Measurements at the M2 beam line of the CERN SPS

– Phase-1 –

COMPASS++*/AMBER†

B. Adams[14,13], C.A. Aidala[1], G.D. Alexeev[15], M.G. Alexeev[42,43], A. Amoroso[42,43], V. Andrieux[45,20],

http://cds.cern.ch/record/2676885

COMPASS++ / AMBER Physics

Program	Physics Goals	Beam Energy [GeV]	Beam Intensity [s^{-1}]	Trigger Rate [kHz]	Beam Type	Target	Earliest start time, duration	Hardware additions
muon-proton elastic scattering	Precision proton-radius measurement	100	$4 \cdot 10^6$	100	$\mu^\pm$	high-pressure H2	2022 1 year	active TPC, SciFi trigger, silicon veto,
Hard exclusive reactions	GPD E	160	$2 \cdot 10^7$	10	$\mu^\pm$	$NH_3^\uparrow$	2022 2 years	recoil silicon, modified polarised target magnet
Input for Dark Matter Search	$\overline{p}$ production cross section	20-280	$5 \cdot 10^5$	25	p	LH2, LHe	2022 1 month	liquid helium target
$\overline{p}$-induced spectroscopy	Heavy quark exotics	12, 20	$5 \cdot 10^7$	25	$\overline{p}$	LH2	2022 2 years	target spectrometer: tracking, calorimetry
Drell-Yan	Pion PDFs	190	$7 \cdot 10^7$	25	$\pi^\pm$	C/W	2022 1-2 years	
Drell-Yan (RF)	Kaon PDFs & Nucleon TMDs	~100	10^8	25-50	$K^\pm, \overline{p}$	$NH_3^\uparrow$, C/W	2026 2-3 years	"active absorber", vertex detector
Primakoff (RF)	Kaon polarisa-bility & pion life time	~100	$5 \cdot 10^6$	> 10	K^-	Ni	non-exclusive 2026 1 year	
Prompt Photons (RF)	Meson gluon PDFs	≥ 100	$5 \cdot 10^6$	10-100	$K^\pm$ $\pi^\pm$	LH2, Ni	non-exclusive 2026 1-2 years	hodoscope
K-induced Spectroscopy (RF)	High-precision strange-meson spectrum	50-100	$5 \cdot 10^6$	25	K^-	LH2	2026 1 year	recoil TOF, forward PID
Vector mesons (RF)	Spin Density Matrix Elements	50-100	$5 \cdot 10^6$	10-100	$K^\pm, \pi^\pm$	from H to Pb	2026 1 year	

Table 2: Requirements for future programmes at the M2 beam line after 2021. Muon beams are in blue, conventional hadron beams in green, and RF-separated hadron beams in red.

PHASE-1

Conventional hadron and muon beams

2022 - 2025 and beyond

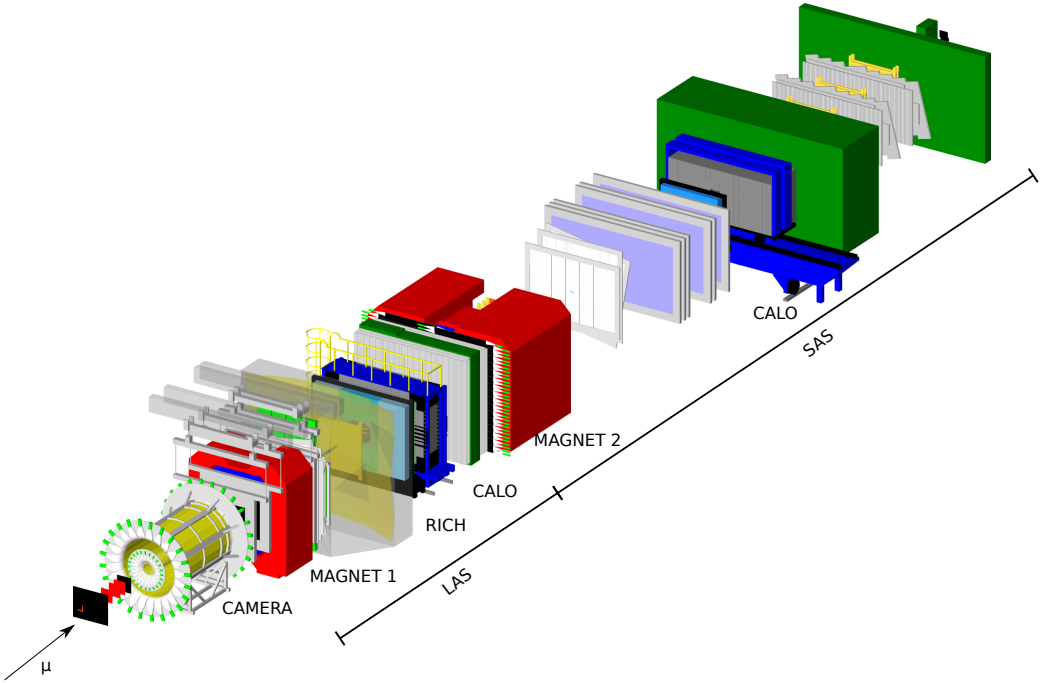
PHASE-2

Conventional and RF-separated Hadron/Hadron and muon beam

2026 and beyond

Phase-1 was recommended to the CERN research committee during last SPSC meeting!

Spectrometer



2016/17 GPD Setup

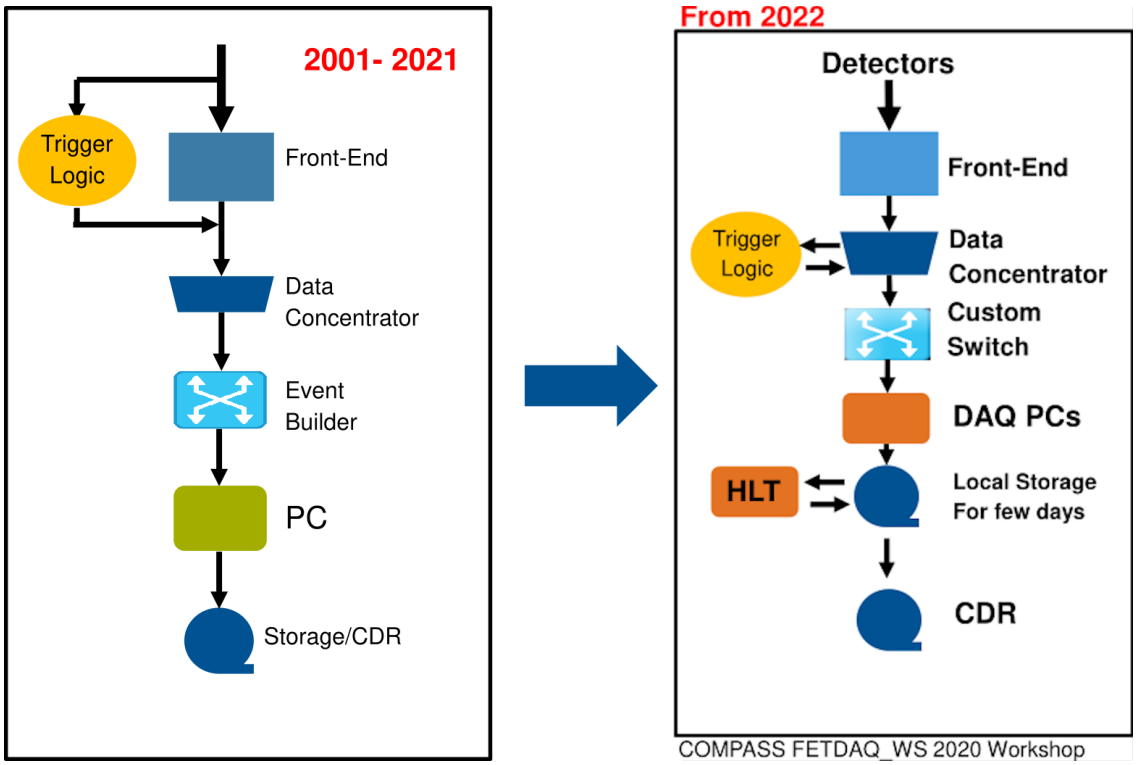
- Located at the M2 Beam-line
  - Momentum Range: 20-250 Gev
  - Muon Mode: $5 \cdot 10^7 \frac{muons}{s}$
  - Hadron Mode: $10^8 \frac{hadrons}{s}$
  - Future RF separated beam
- Variable Target Region
- Two-stage forward spectrometer
  - **Calometry:** ECAL/HCALs
  - **PID:** RICH/CEDARs
  - **Tracker:**

    Silicons, SciFis, GEM, PixelMM, DriftChambers, Straws, MWPCs, Hodoscopes

$\approx$ 400 k Channels to be equipped with new streaming enabled FE

(+new detector developments for the different physic programs)

Evolution of DAQ Architecture

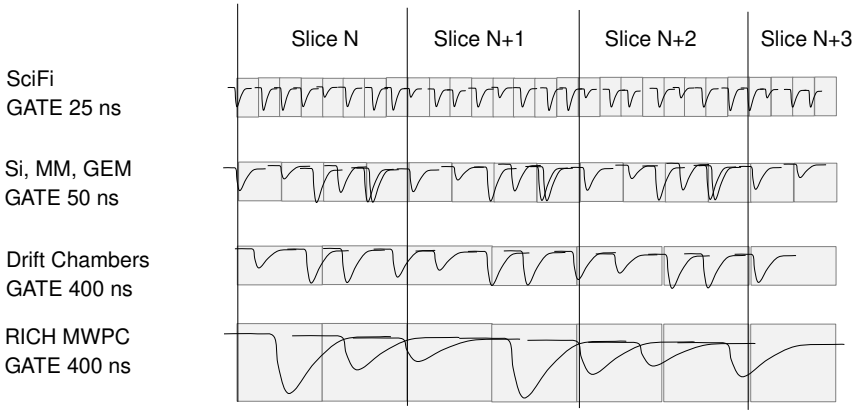


- **Free Running Mode:** complete data stream from the detectors is saved to tape.
  (Pre-filtering/selection of data has to be done in physics reconstruction stage.)
- **Filtered Mode:** Online information from trigger processors / HLT is used to reduce data size before it is written to tape.

Time Slices and Images instead of Events

Time Slices are generated by a synchronous signal which is distributed to all front-ends.

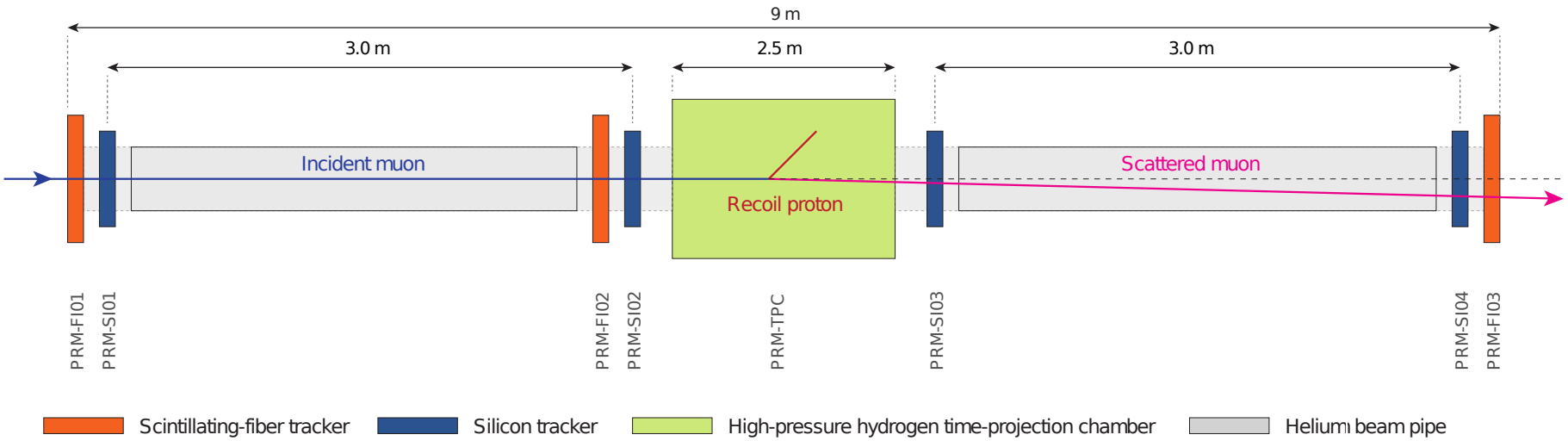
Additional partition in **images** according to detector resolution and rates.



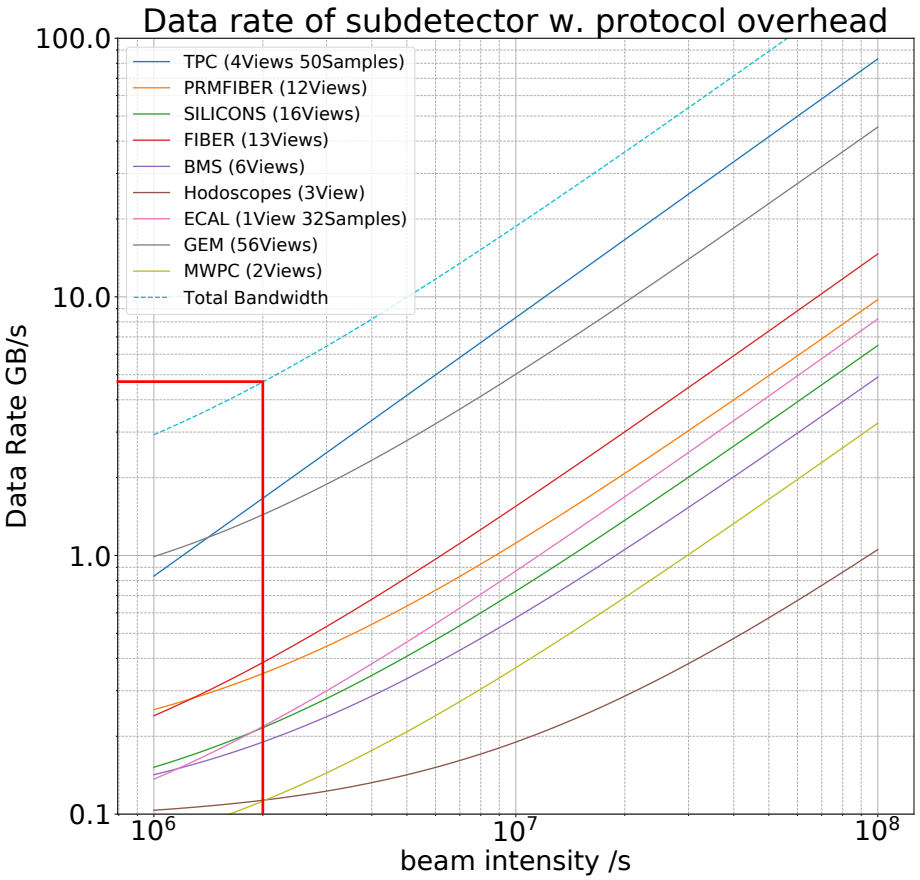
First Measurement: Proton Charge Radius

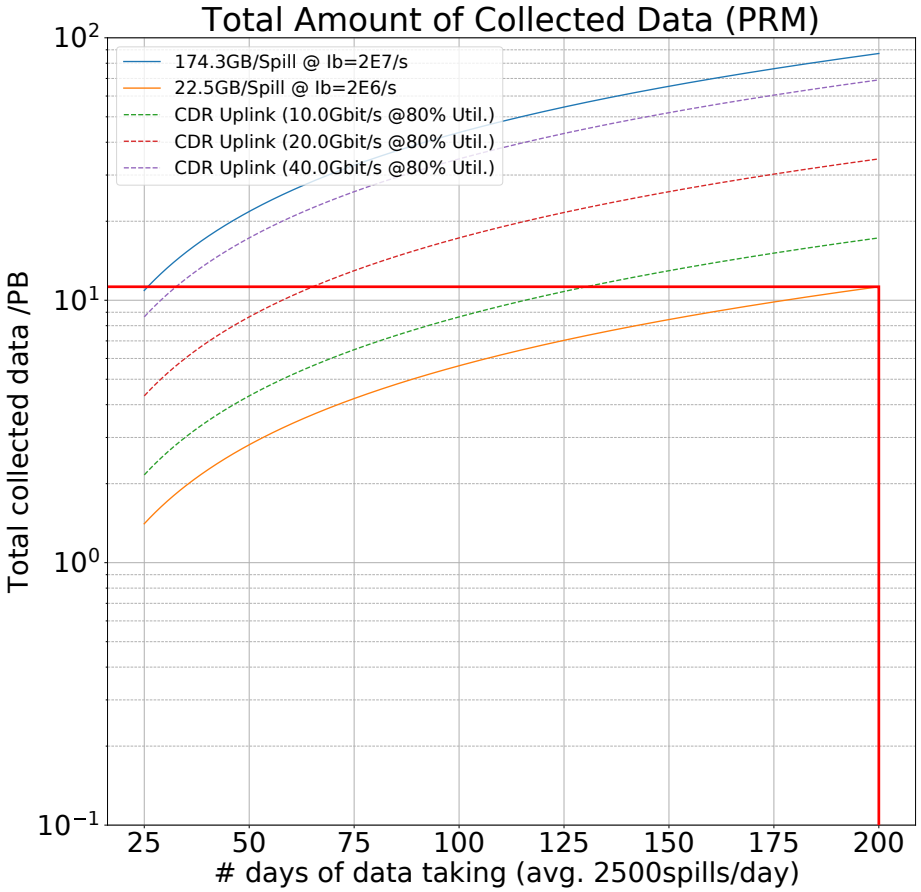
Measurement of low-Q2 elastic-scattering via detection of low-energetic recoil-protons and scattered muons with small scattering-angle.

- TPC as an active target with the ability to measure the low-energetic recoil-proton
- Silicon trackers along large leaver-arm to measure small scattering-angles
- Fiber tracker → timing
- BMS for momentum measurement
- ECAL for radiative effects
- Small trackers (SciFi,GEM) for measuring the scattered muon



Expected Data Rates

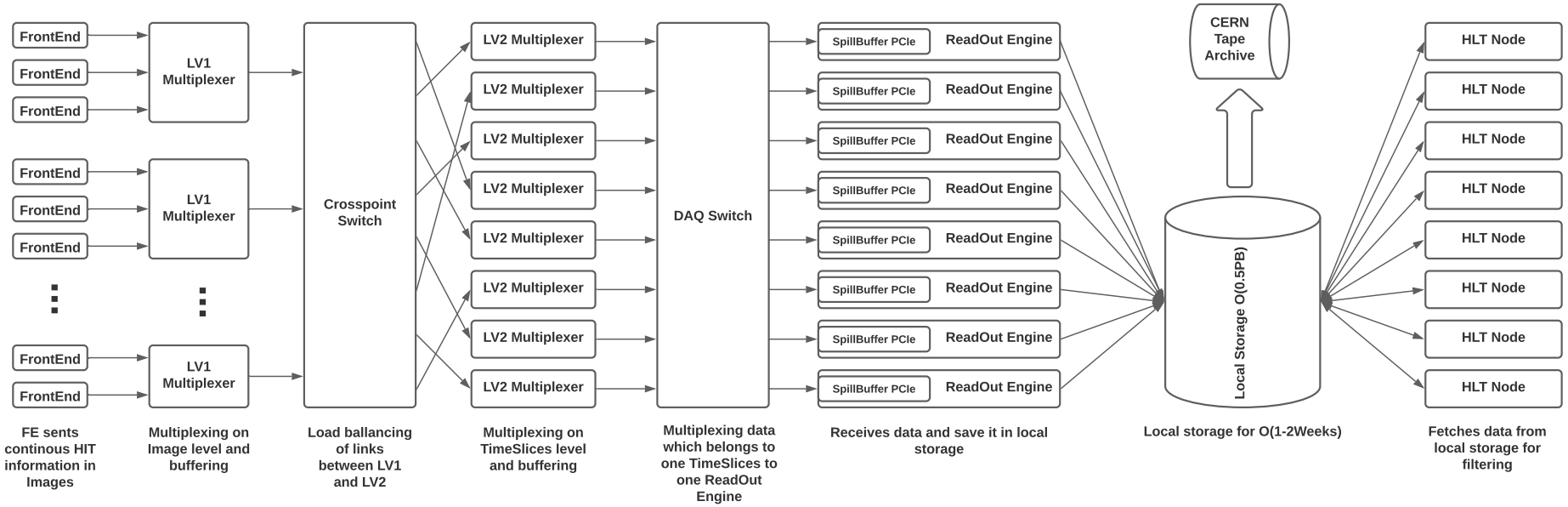




For a beam intensity of 2E6 muons/s $\approx$ 5 GB/s (on spill) $\rightarrow$ 1.5 GB/s (sustained)

Total amount of collected data $\approx$ 10 PB in 200days

DAQ Structure



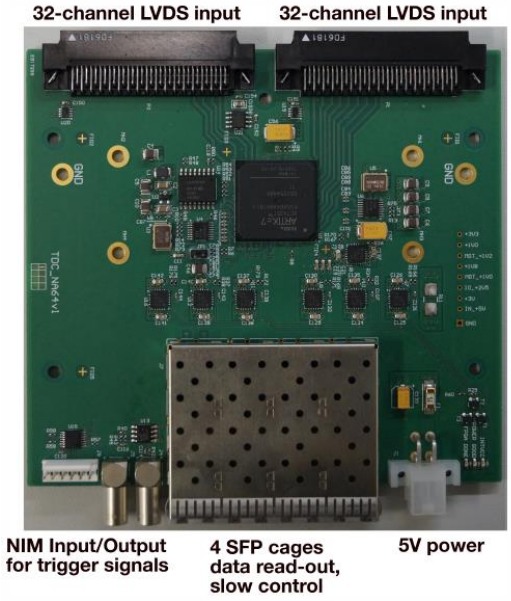
- UCF as low level protocol to encapsulate different user protocols (IPBus, TCS, Data) over one physical link.
- Data protocol is 32 bit aligned similar to previous s-link
- Each level adds header/footer frames to carry information of the source of data
- Data consistensy check (protocol & checksum) on each level

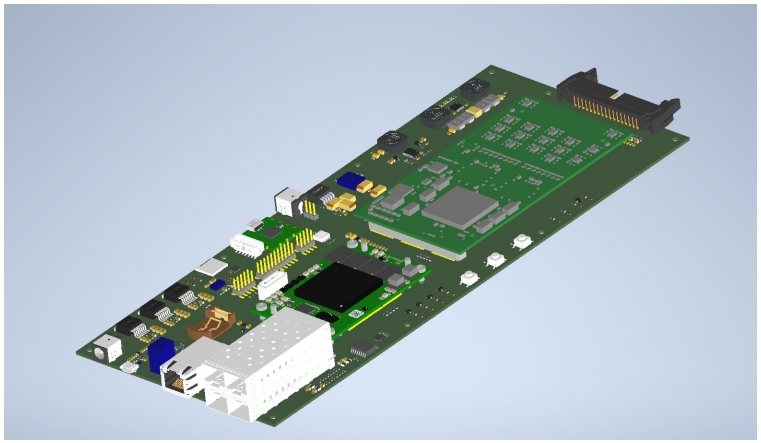
Hardware & Firmware Developments

Frontends

A FPGA based ifTDC:

- ARTIX-7 FPGA XC7A-35
- 64 channels (LVDS) & 2x LEMO
- Bin Size: 400 ps, 200 ps, 100 ps
- Differential nonlinearity : 10%, 20%, 40%
- Low price point $\leq$ 10 Euro/channel





Feature extracting ADC:

- Carrier Board for MSADC card
  (12 bit 32 ch@40 MS/s 16 ch@80 MS/s)
- Xilinx Zynq Ultrascale+ MPSoC
  (Trenz UltraSoM+ Modules TE808 or TE803)
- 4x SFP+ connectors (16.3 Gb/s max)

Cross Point Switch

Crosspoint Switch Components

- **interfaces:**
  - 12 x 12 channel CXP transceiver (MPO fiber connectors)
  - Ethernet for IPbus
  - JTAG
  - TCS (Trigger Control System) receiver
- **Switching and Control:**
  - **Vitesse VSC3144-02** – fully configurable 144x144, asynchronous, 6.5 Gbps crosspoint switch
  - **Xilinx Artix-7 FPGA** for switch control and monitoring

- **Interface FPGA – Crosswitch:**
  - 90 MHz, 11-bit parallel data bus
  - Multiple program assignments can be queued and issued simultaneously ⇒ fast programming (<< 1us)

Developing in the future uses MACOM M21605G-12 switch ICs

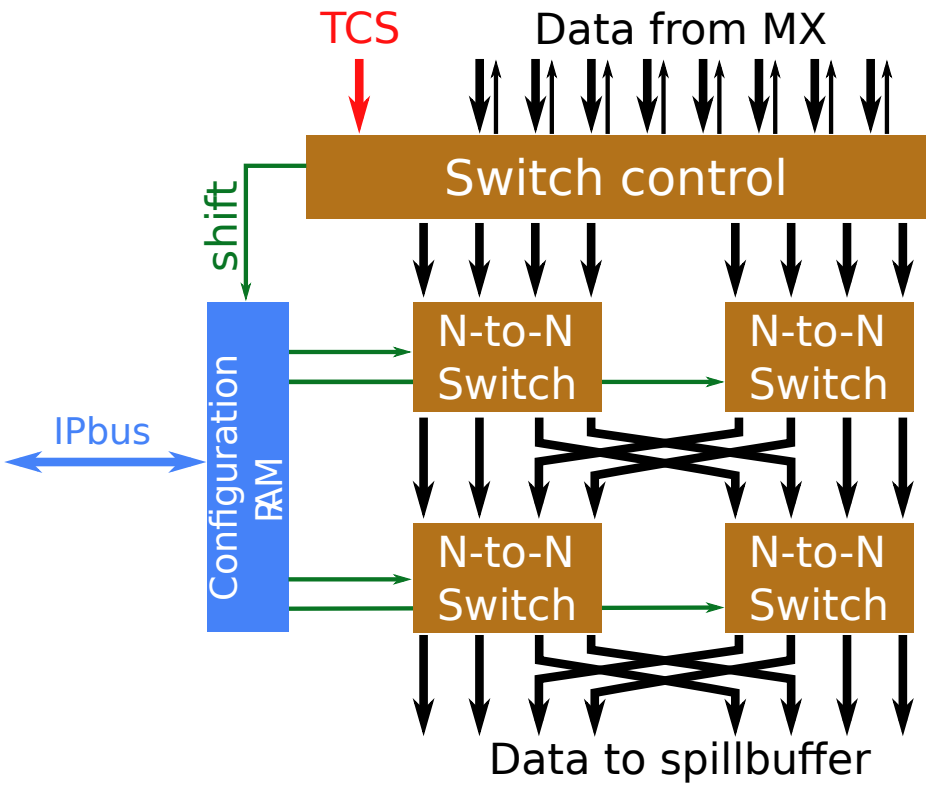
(Non-blocking, asynchronous 12.5 Gbps 160x160 switch)

DHmx/DHsw

Backbone module of DAQ

- Xilinx Virtex-6 VLX30T
  - Custom board in AMC form factor
  - 16x 6.25 Gb/s links
  - 4 GB DDR3 Memory
  - VME carrier board
  - ATCA carrier board (under development)
- Firmware versions:
  - LV1 Multiplexer with UCF links
  - LV2 Multiplexer with UCF links
  - Full Bandwidth DAQ Switch

Switch Architecture



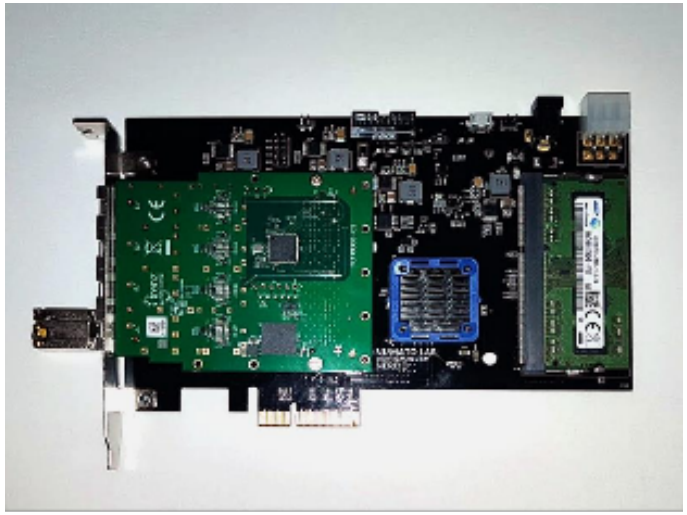
- Switch control
  - change of the switch mapping when frame transmission for a given time slice is complete
- 4-to-4 switch
  - routes frames from an input to a specific output
  - input-output mapping is changed according to configuration in BRAM
- Slow control over IPbus

Allows full bandwidth switching of incoming time slices to SpillBuffer.

SpillBuffer Card

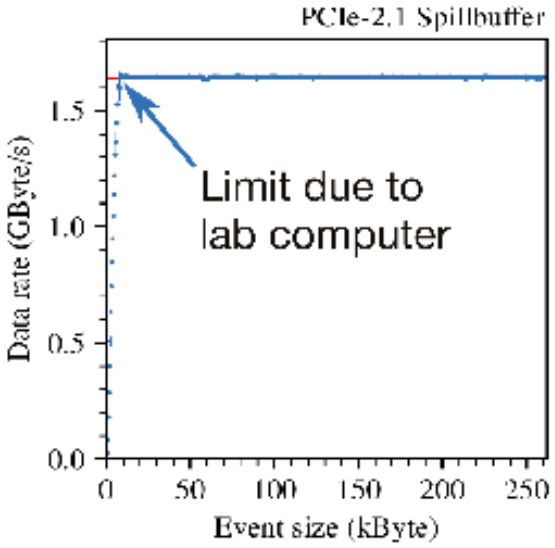
Hardware:

- Kintex 7 XC7K160T FBG676
- Based on commercial hardware
  - Nereid Kintex-7 PCI Express
  - Trenz FMC – SFP adapter
- PCIe-Gen2 x4 interface
- 4x SFP Connection
- 4 GB DDR3 memory



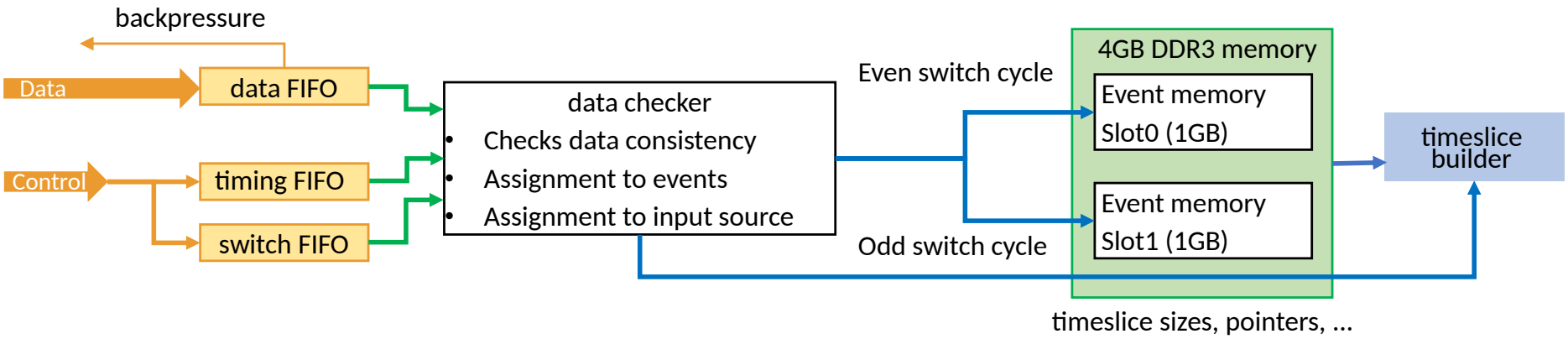
Performance Test:

- Local data generator
- Scan of time slice sizes
- Stable PCIe data rate of $\gtrsim 1.6\,\mathrm{GB/s}$



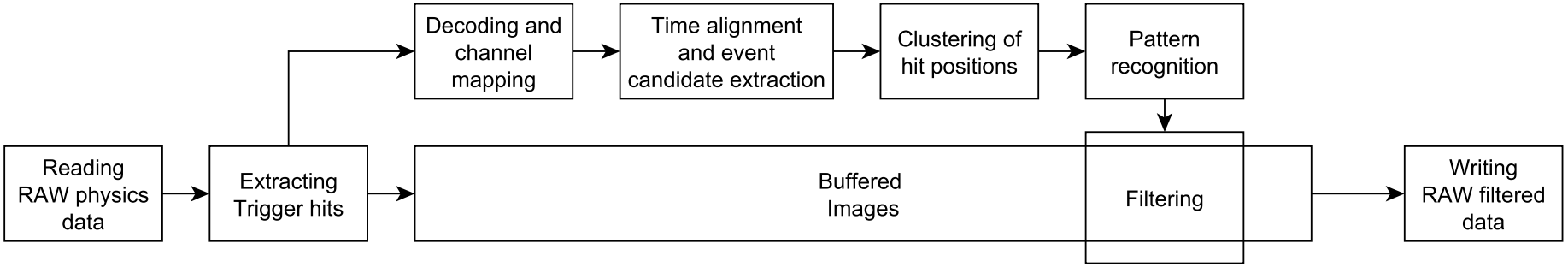
Time Slice Builder Algorithm in SpillBuffer Card

- Single 6.25 Gb/s Aurora interface
  - Data
  - Timing information
  - Switch configuration
- Time slices stored in DDR3 memory
- Combination of time slices according to
  - time slice number
  - switch configuration
- Build time slices push to PCIe
- Internal bandwidth 3 GB/s



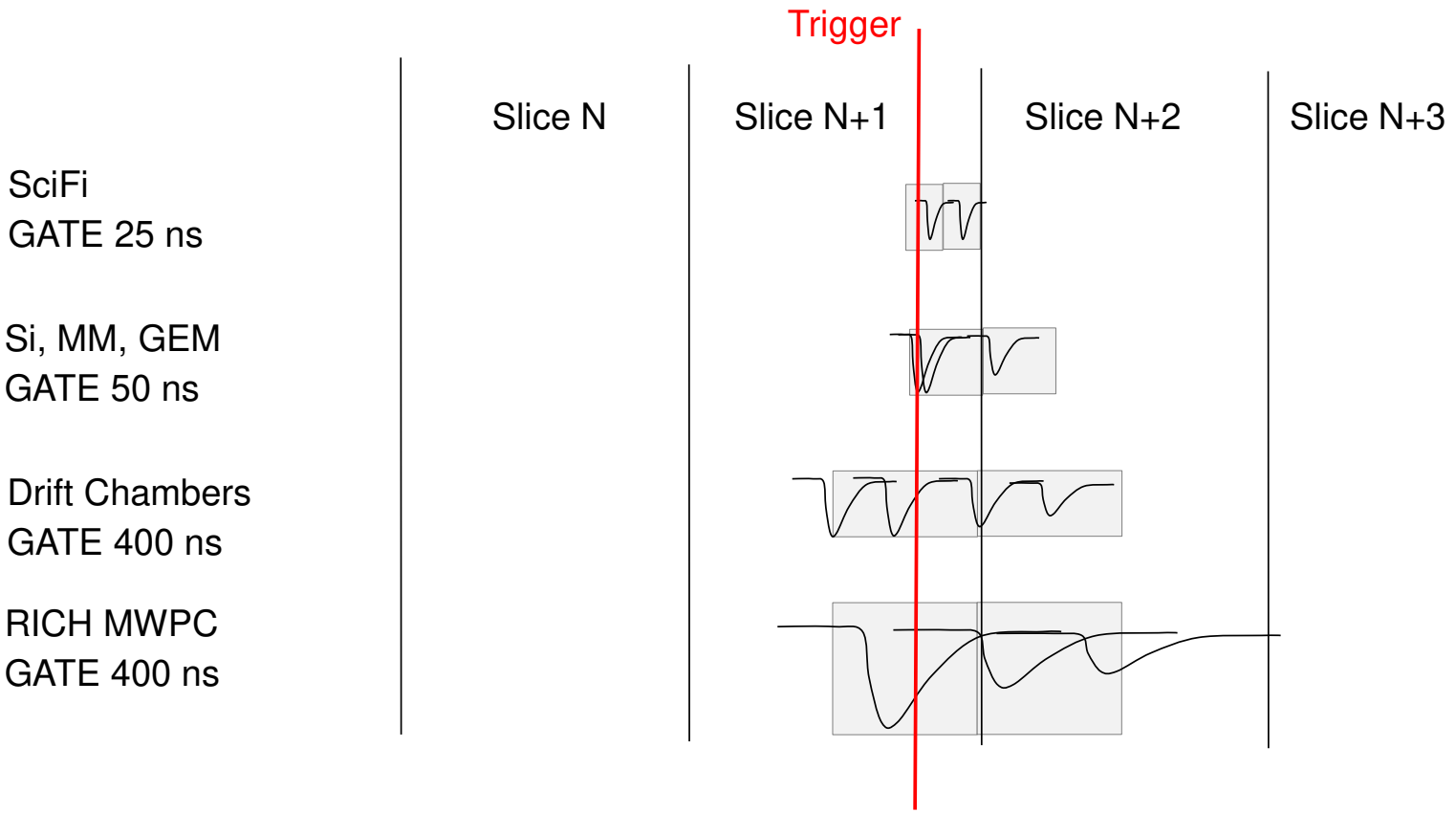
High Level Trigger Implementation

- CPU based implementation on AMD RYZEN EPYC architecture
- HLT access data from local storage server via 25 Gbit/s network
- Piplined approached runs asynchronous to DAQ data taking



Framework allows implementation of different filter algorithm by the users!

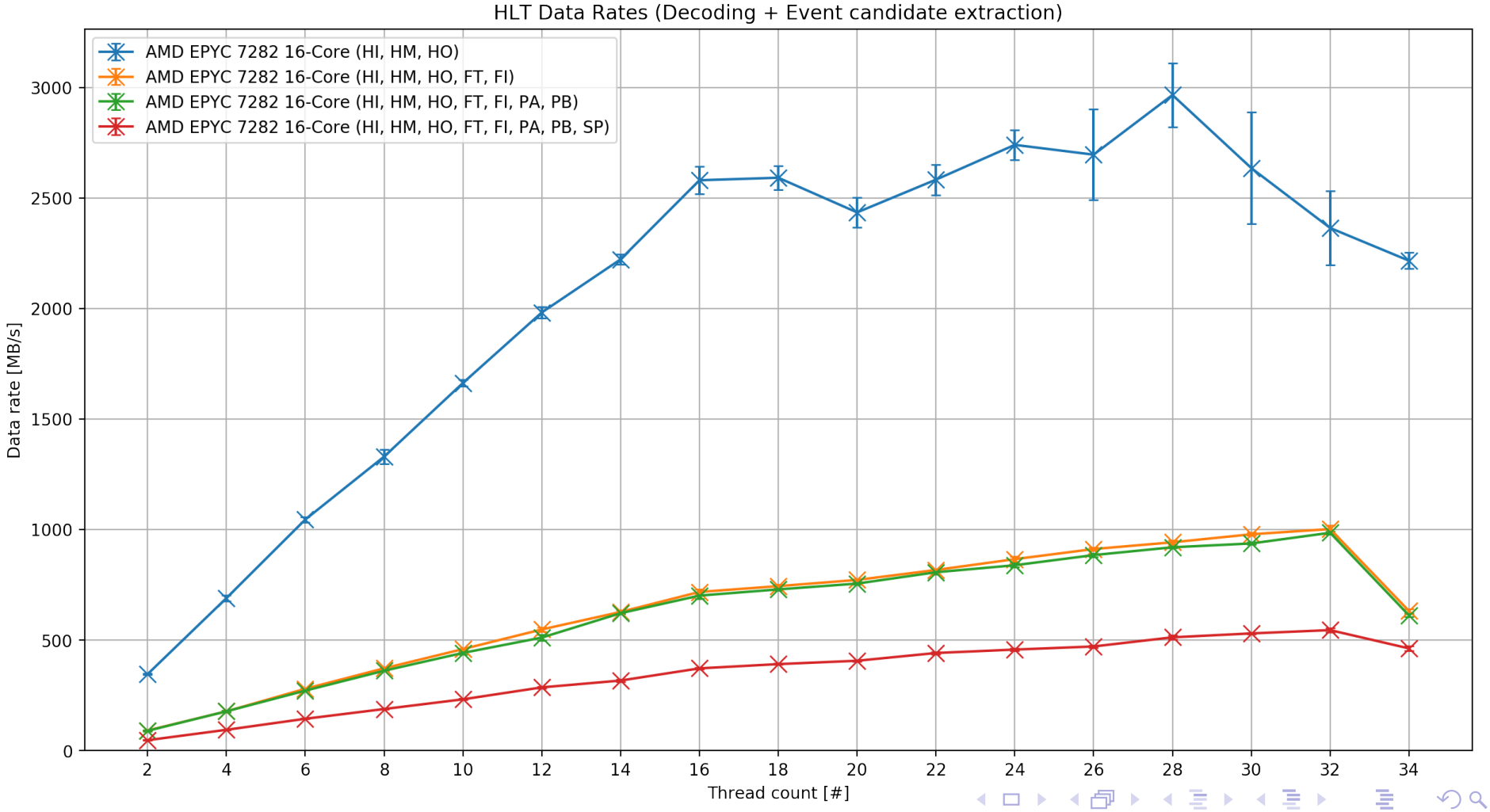
Data Reduction after filter decision



After filter decision two consecutive images from DAQ data stream are saved.

High Level Trigger Performance

Test is performed with generated MC data for PRM setup and different sets of detector information:



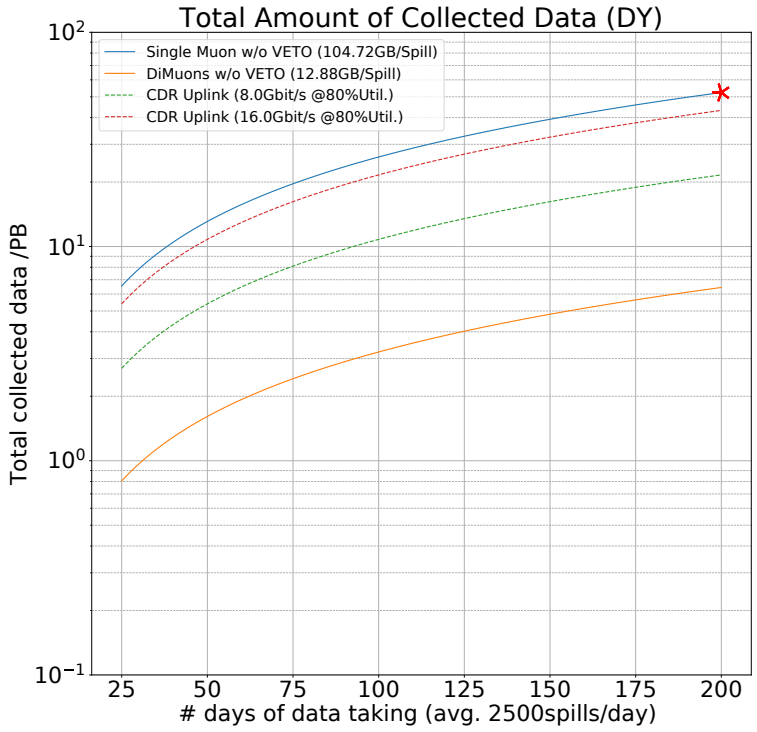
Conclusions

Developments fulfill the requirements we need for the first PRM measurement!

But whats about the other measurements?

Increasing Data Rates for other Physic Programs (DY)

Drell-Yan requires the read-out of the whole spectrometer!



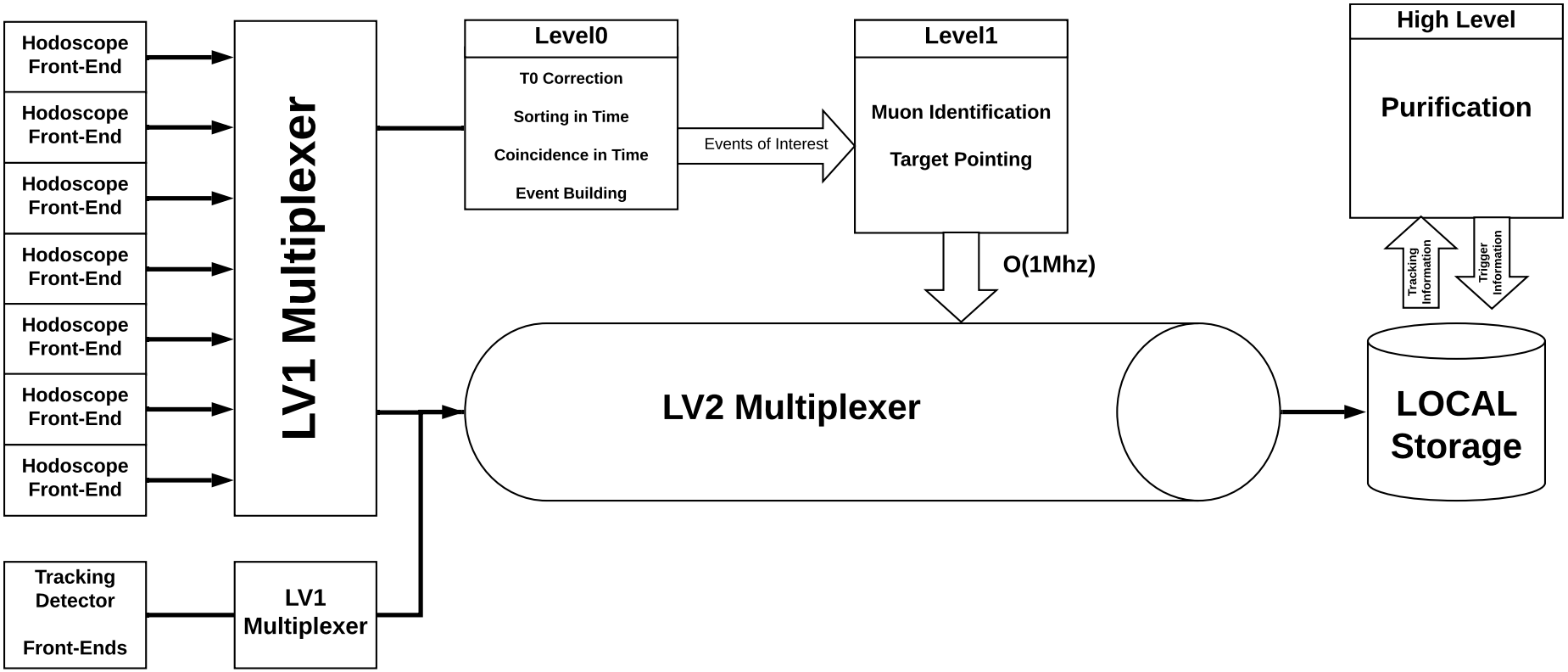
Even after simple online filtering (target pointing) we expect $\approx 20\,\mathrm{GB/s}$ (on spill)

$\rightarrow$ Increase in overall bandwidth needed!

Multi Stage Filtering

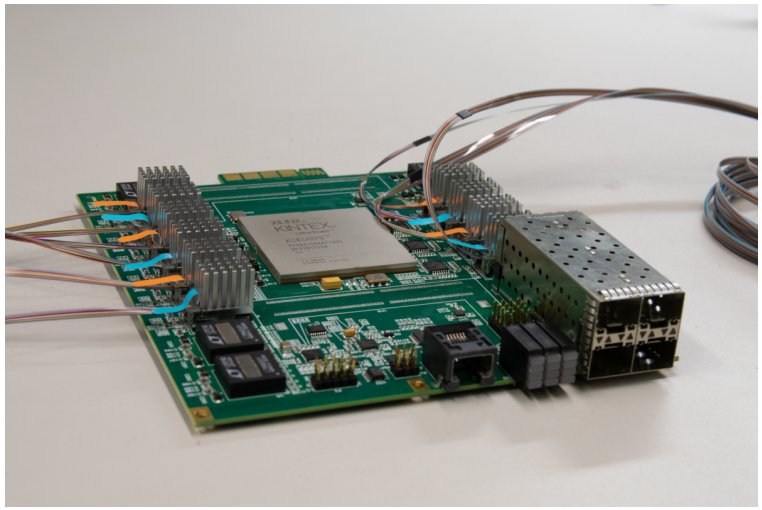
Online Filtering via FPGA to reduce data before ReadOut engines.

→ Stream of an **subset** of detectors is sent to Filter-Logic.
→ Full stream buffered in LV2 Mux for DAQ.



iFDAQ XCKU095 Card

Increasing link speed on multiplexer and 30x30 DAQ-switch:

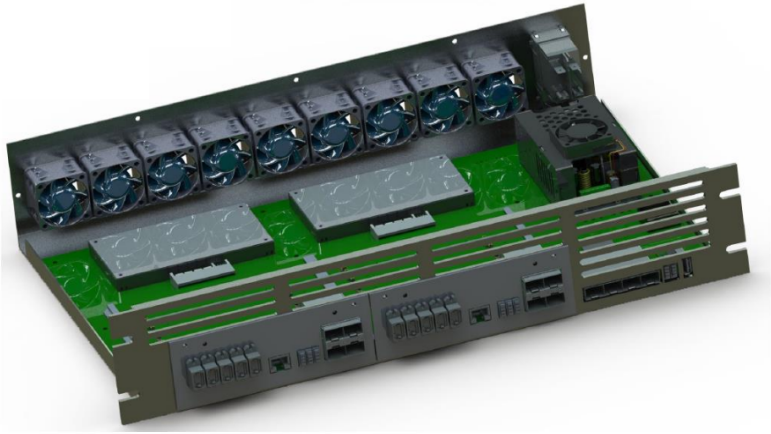


Specifications:

- Xilinx Kintex UltraScale XCKU095.
- Up to 16 GB DDR4 memory.
- 64 optical links (up to 16 Gb/s):
  - 60 via MPO connectors.
  - 4 via SFP+ connector.

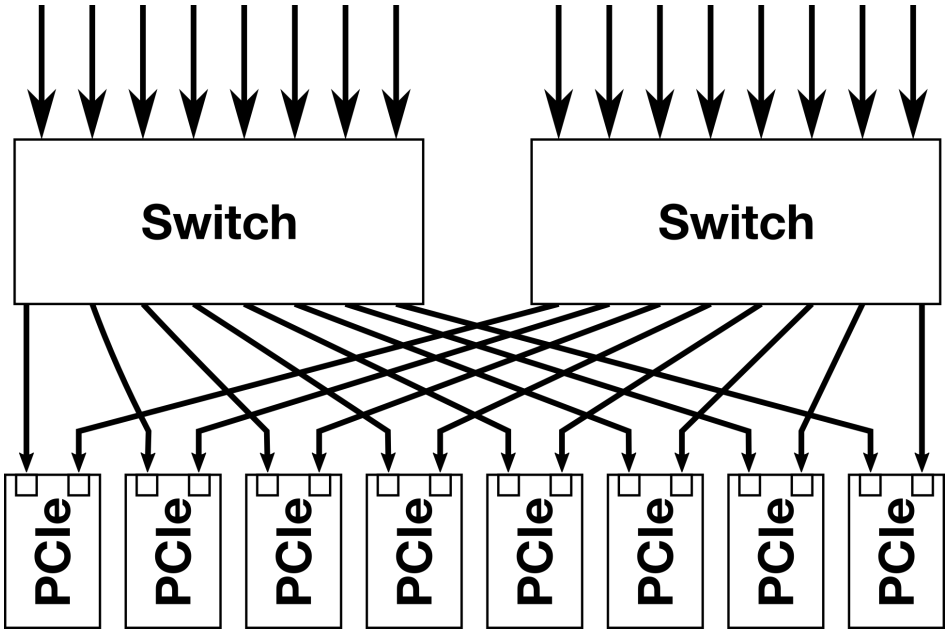
Form factor:

- Custom Form factor with 2U 19 Inch crate for two cards.
- Holds carrier + cooling + PSU



Better usage of PCIe Bandwidth

Using Multiple DAQ Switches (or a 30x30 XCKU095 Switch) for better use of PCIe bandwidth of Spillbuffer cards:



Thank You!

Questions ?