Prototype DAQ system for CBM





HELMHOLTZ RESEARCH FOR GRAND CHALLENGES **David Emschermann** Streaming Readout Wokshop VII – BNL/Zoom – 17.Nov.2020



> The FAIR facility and construction site

Location of CBM at FAIR and mCBM at GSI

> The CBM data challenge

The mCBM µTCA readout chain (2020)

> The mCBM CRI readout chain (2021)



The FAIR accelerator facility

Primary Beams

- 10¹²/s; 1.5 GeV/u; ²³⁸U²⁸⁺
- 10^{10} /s 238 U⁹²⁺ up to 11 (35) GeV/u
- 3x10¹³/s 30 (90) GeV protons

Technical Challenges

- cooled beams
- rapid cycling superconducting magnets
- dynamical vacuum

Secondary Beams

- radioactive beams up to
 1.5 2 GeV/u; up to factor 10000
 higher in intensity than presently
- antiprotons 3 30 GeV

Storage and Cooler Rings

- radioactive beams
- 10¹¹ antiprotons 1.5 15 GeV/c,

stored and cooled





FAIR construction site – October 2020



GSI and completed FAIR campus in 2025



https://fair-center.eu



CBM related sites on the GSI and FAIR campus



Green IT Cube data center (2016) mCBM test facility (2018) CBM experiment (2025)



CBM cave construction – October 2020



Construction of CBM cave



The CBM experiment at FAIR

- Heavy-Ion fixed target experiment
- To be built on a beamline of the SIS100 synchrotron at the new FAIR facility in Darmstadt, Germany
- Physics program: investigate rare probes and potential phase transitions in the region of high baryon-densities
- > Up to 10 AGeV Au
- > Up to 30 GeV p
- > Acceptance: $2^{\circ} < \theta_{Lab} < 25^{\circ}$
- "High precision High statistics"



1st beam in 2025



The CBM data challenge

- > Very high interaction rate environment:
 - $10^{5} 10^{7}$ /s (A+A), up to 10^{9} /s (p+A)
- Non-trivial criteria for event selection
- Fast detectors with radiation tolerant freestreaming readout electronics
- > High-speed Data AQuisition (DAQ) system
- FPGA based readout chains
- > About 1-2 TByte/s bandwidth to the High Performance computing farm, where the First Level Event Selector (FLES) is located
- State of the art computing infrastructure allowing for online event reconstruction
- Online event selection to reduce data by a factor 100-1000 for archiving at ~1 GByte/s



The CBM data flow



FAIR phase 0 activities





CBM streaming readout protoype setup - eTOF

eTOF at STAR

presented at:

Streaming Readout Workshop VI



Run20 (Dec2019 – Sep2020) successfully completed



Run-by-Run <u>online</u> QA of eTOF Run20 data

Important step towards CBM control concept





CBM streaming readout protoype setup – mCBM @ SIS18



mCBM at GSI presented today: Streaming Readout Workshop VII

G-PAC of GSI/FAIR, 10th June, 2020 \rightarrow fully granted !



F(AIR

mCBM as test bench



mCBM@SIS18

CBM full system test setup for high rate A-A collisions at the SIS18 facility

10⁸ beam particles/s

10% gold target

=> 10⁷ interactions/s





The mCBM experiment and readout chain in 2021

established 2018: 1st commissioning with beam Dec 2018 / Mar 2019 2nd campaign Nov 2019 / May 2020 3rd campaign – Λ study Feb 2021 / May 2021

> mCBM: a fixed target, high interaction rate, heavy ion physics experiment and test-site for CBM technology



CBM cave construction – October 2020



The mCBM readout and control architecture (DPB)



DPB board configuration



3 2 1 0 FMC channel number

GBTx ROB #1 - links FLIM – link #1 GBTx ROB #2 - links FLIM – link #2

- AFCK board (Creotech, Poland)
- Xilinx Kintex 7 FPGA (325T FFG900)
- Receives several GT links at 4.8 Gbps (multimode fiber, 50 m)
- Indexes data in timeslices
- Allows for data pre-rpocessing
- Sends one single FLIM link at 10 Gbps (singlemode fiber, 300 m)



mCBM readout chain 2020



Acronyms used in the mCBM readout



FPGA : Field Programmable Gate Array

Acronyms

- **DPB** : Data Processing Board
- **TFC** : Timing and Fast Control Syst.
- FLES : First Level Event Selector
- **GBTx** : CERN rad.-hard interface ASIC

µSlice (µS) : Self contained data block for a subset of the experiment, minimal size depends on degree of data time sorting.

Timeslice : Collection of µS, self contained data block for the full experiment and a given time interval, includes overlap to avoid edge losses.



The mCBM data path



mCBM commissioning with beam, first results



March 27 - May 24, 2020 campaign:

- max. collision rate: 4 MHz
- max. total data rate: 3 GB/s
- 20 TB data taken

David Emschermann | Streaming Read



mCBM commissioning with beam, first results

Pairs []



mCBM commissioning with beam, first results



DPB, FLIB and CRI



Xilinx Kintex-7 XC7K325T

Xilinx Kintex-7 XC7K325T

BNL-712 as CRI



Xilinx Kintex Ultrascale XCKU115





Common Readout Interface card 1.0

- Joint production of BNL-712 cards with sPHENIX/BNL
- > This is the Common Readout Interface card (CRI-1.0)



> Every subsystem in mCBM will use this card from 2021 to transfer data to the FLES

> The CRI card is also the core element of the TFC system

David Emschermann | Streaming Readout Workshop VII | BNL + Zoom | 17.Nov.2020 | Page 27



CBM will have

36 CRI by 2022

DAQ chain evolution at mCBM



The CBM readout and control architecture (CRI)





TFC Concept

- The Timing and Fast Control system (TFC) is meant to synchronise data processing electronics experiment-wide over optical fibres
- > Organised as a hierarchical network for scalability
- Based on CRI cards
- Distributes timing information to endpoints (CRI)







The CBM readout chain in 2021



- > next step: FDR extension of readout chain to the GSI IT cluster
- > for more powerful online monitoring and online event selection and direct storage access to Lustre



The CRI DAQ rack prototype



- > This is the CBM DAQ prototype rack (est. September 2020)
- > all data from mCBM subsystems will transit here (replicate 24x at SIS100)
- the rack is it hosts the TFC system and FLES Entry Nodes fitted with CRI

mcbmcri - JTAG server

cbmin00x - 2x TFC-CRI

cbmin007 - 1x CRI

cbmin006 - 1x CRI

cbmin005 - 1x CRI

cbmin004 - 1x CRI

cbmin003 - 2x CRI

cbmin002 - 2x FLIB

2 CRI cards and 1 HDR HCA are installed in each Entry Node

→ CBM



Milestones towards realization of full readout system for CBM

2020 build a demonstrator rack for mCBM move entry nodes from GC to the mCBM take 300m long EDR InfiniBand link into operation install CRI boards in entry nodes introduce TFC system upgrade processing node cluster (Kronos nodes) 2021 control DAQ from ECS prepare for data taking with beam identify and procure final CRI+ board 2023 identify and procure final entry node server scale up to SIS100 system size 2024 introduce throttling to TFC 1st data taking with beam 2025



Summary

CBM

- Validate detector and DAQ concept with mCBM up to highest collision rates
 - upgrade to final DAQ hardware (CRI + TFC)
 - prepare for commissioning of new readout chain in Q1/2021
 - commission benchmark Λ baryon measurement in Q2/2021









The end



Thank you for your attention



Bonus slides



DAQ chain evolution at mCBM



Timeslices and Microslices

- Definitions and concepts in the CBM readout chain
- MicroSlice (µS) = self-contained data container from a single CRI and for a fixed period of time
 - Output of the CRI in CBM => generated in FW
 - Constant length in experiment time
 - Typical period of time: 10's of µs to ms
- TimeSlice (TS) = container collecting the µS of all CRI cards in the setup and for a given number of µS
 - Assembled by FLESNET (CBM DAQ prototype) => generated in SW
 - Typical number of µS: 10-1000 => time range: ms to s
 - Includes an overlap µS
 - One TS for the full setup for each time interval





CBM streaming readout protoype setup - mCBM

mCBM@SIS18 The CBM Collaboration **Compressed Baryonic Matter Experiment** June 2020

1st results from mCBM Run20 streaming readout setup with μ TCA DAQ system











David Emschermann | Streaming Readout Workshop VII | BNL + Zoom | 17.Nov.2020 | Page 40

mCBM at GSI

presented today:

Streaming Readout Workshop VII

Common Readout Interface card for CBM



- > BNL-712 card was developed for ATLAS
- > also known as FLX-712 or FELIX
- > CBM name: Common Readout Interface (CRI)
- > core of CBM readout chain from 2021

- Xilinx Kintex UltraScale XCKU115 FPGA
- > 48 optical links (MiniPODs)
- > PCIe Gen3 x16 (2x8 with switch)
- Separate TFC input via TMC



Fiber mapping on cave patch panel for 2021







14.09.2020 - 12:30 # # MTP cave patch panel т0 STS MUCH TRD-I TRD-O TOF RICH PSD 1 - 1 - 1 - 1 - 1 -1 - 1 - 11 -1 1 -1 -1 -1 -Rx Rx Rx Τx Rx Τx Rx Rx Rx Rx Rx Rx Rx Tx Rx Tx Τx Τx Τx Τx Τx Τx Τx Τx



Entry Node configuration - CRI data path



- > 8x CRI boards are already installed
- > 8x CRI boards to come in December 2020
- > 18x CRI boards ordered for 2022

basic configuration of CRI entry nodes for 2021:

- > 2x CRI max 235 Gbps (in)
- > 1x HDR HCA max 120 Gbps (out)



The CRI DAQ rack prototype

ASUS ESC8000 TFC This is the CBM DAQ prototype rack G4 links 1x Timing and Fast Control (TFC) server > **cbmin00x** - 2x BNL-712 St Entry Nodes (EN) G3 **cbmin007** - 1x BNL-712 mcbmcri G3 HUB JTAG **cbmin006** - 1x BNL-712 USB G3 **cbmin005** - 1x BNL-712 Deell G3 **cbmin004** - 1x BNL-712 G3 **cbmin003** - 2x BNL-712 > 1x JTAG server G3 cbmin002 - 2x FLIB 8x CRI card (= BNL-712)

The Processing Node cluster









Commissioning of mCBM



1st data campaign: Nov./Dec. 2018 & March 2019

2nd data campaign: Nov. 2019 & May 2020







Diamond T0 counter





Commissioning of mCBM

March 2019 : 10^8 Ag ions/s (1.58 AGeV) + Au (2.5mm) \rightarrow 10 MHz collision rate





Commissioning of mCBM





Trunk cables linking HTD cave to the DAQ container and to the Green Cube



2x 50 m long OM4 cable for HTD-DAQ



300 m long OS2 cable for DAQ-GC

144x core trunk fibers for mCBM

max bandwidth of MM connection with 4.8 Gbps GBT links: 144 * 4.8 Gbps = 691.2 Gbps

max bandwidth of SM connection with 100 Gbps (EDR) links: 72 * 100.0 Gbps = 7200.0 Gbps



The end

