Readout & DAQ

Fernando Barbosa
Kai Chen
Jin Huang

Streaming VII Workshop
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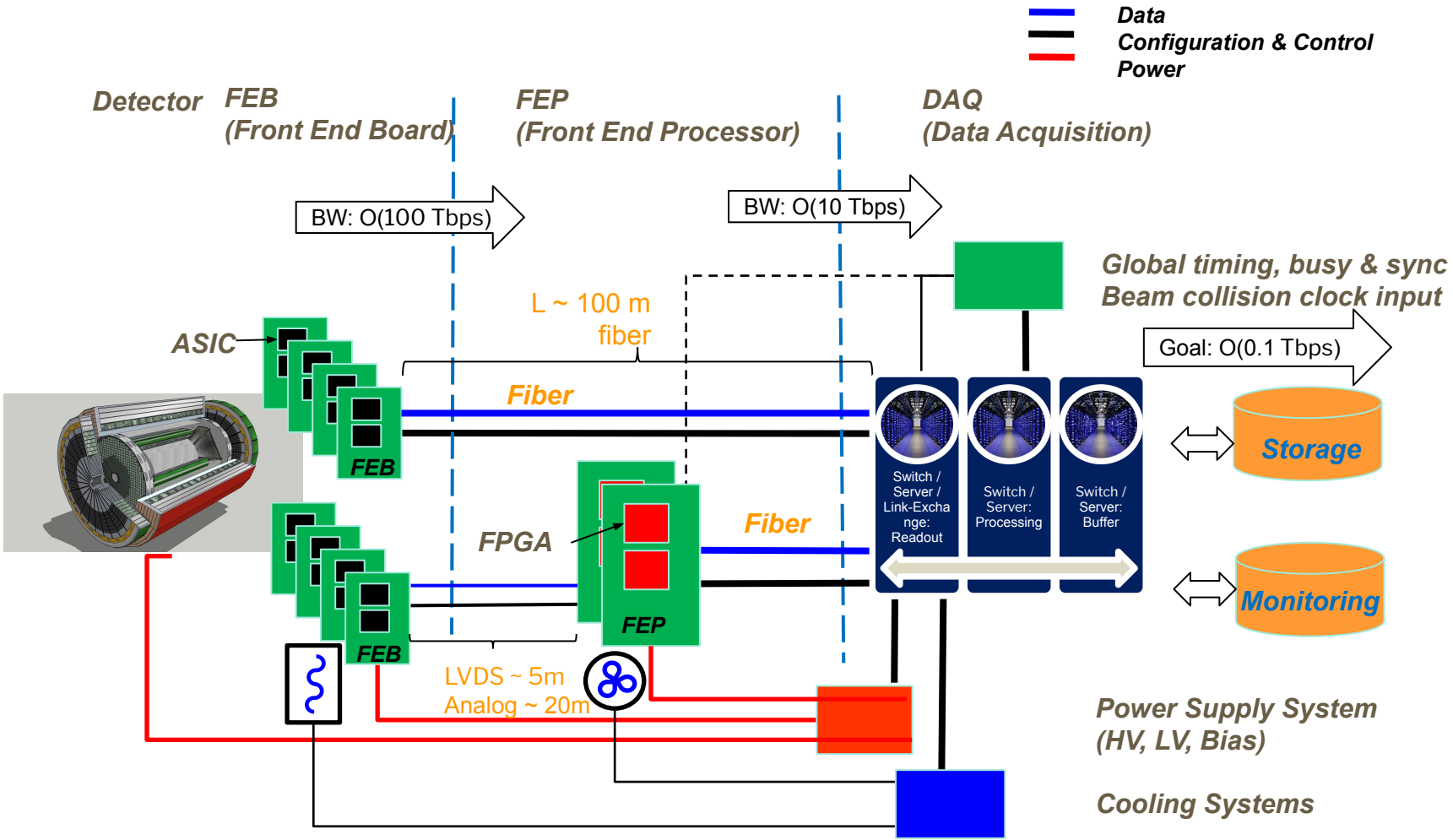
Outline

- EIC streaming readout architecture
- Potential general purpose R&D
- FELIX-based DAQ in the ATLAS (HL-LHC) & DUNE experiments

EIC Streaming Readout Architecture



FEBs & FEPs Development

- "Coalesce" specifications to minimize the number of ASIC/FPGA/PCB part numbers
- Power is now nominally 1 W ± 0.25 W per ASIC (64 ch, 32 ch). Cooling systems will be an integral part of the detector design
- Serviceability as a design criteria
- ASIC Development timeline is critical
    - From "scratch" is a big undertaking
    - Look to existing designs and possible updates
- Standardization of data format (header, timestamp, etc.) at the system design level
- PCB board design and assembly should meet standards like IPC
- Firmware development requires specialized expertise in close connection with both the detector development and the DAQ systems
- Power demands for the FEPs, which are outside of the detector volume, can be high: cooling and other infrastructure needs are easier to manage
- Testing and integration (w/ detectors/prototypes) takes considerable time and resources

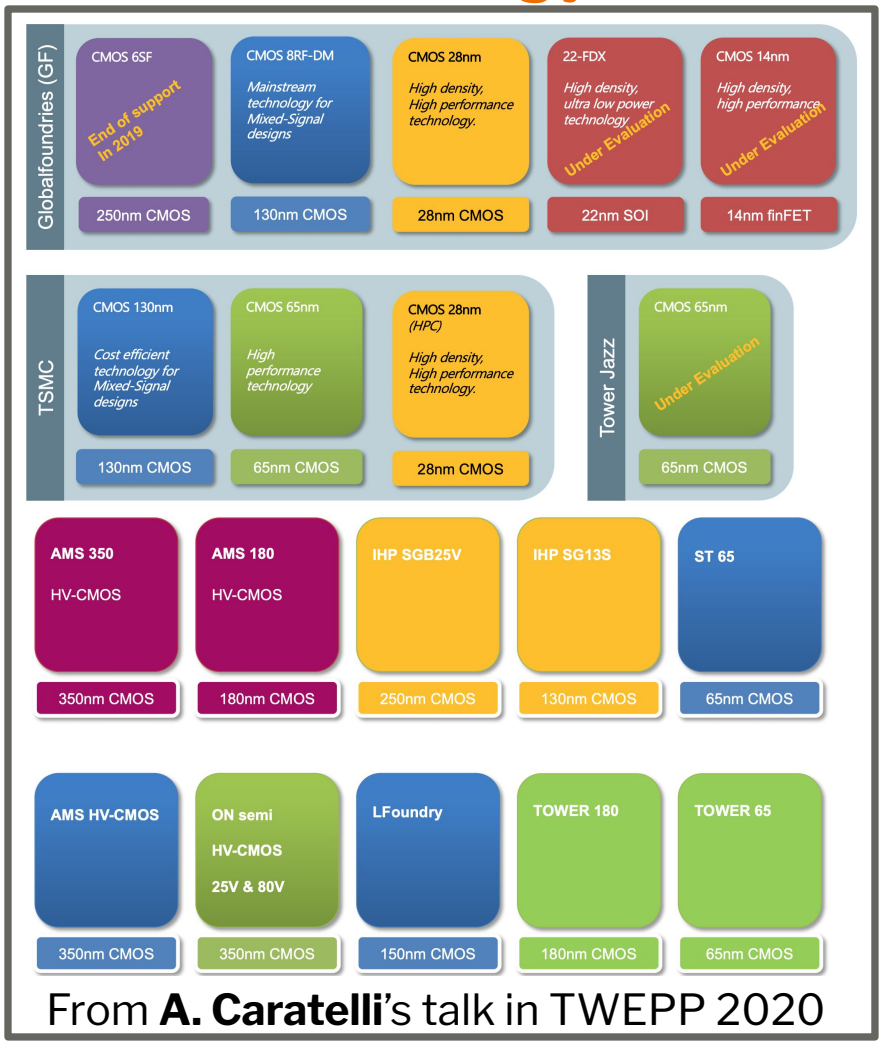
Readout Channels

Detector	Sub-system	Type	Sub-type	Channels
Tracking				
	Silicon Vertex Tracker	Si	Pixel	200M
	TPC	GEM	Pads	160K
	GEM	GEM	Strips	217K
	uRWELL	GEM	Strips/Pads	
	Cylindrical Micromegas	GEM	Strips	
	Drift Chambers	DWC	Wires	
	sTGC	GEM	Pad, Strip, Wire	
	Straw Tubes	Straw	Wires	
Calorimetry				
	e-EMCal	Cal	PMT/SiPM	5k
	C-EMCal	Cal	PMT/SiPM	24k
	h-EMCal	Cal	PMT/SiPM	26k
	h-Hcal	Cal	PMT/SiPM	3k
	c-Hcals	Cal	PMT/SiPM	2.8k

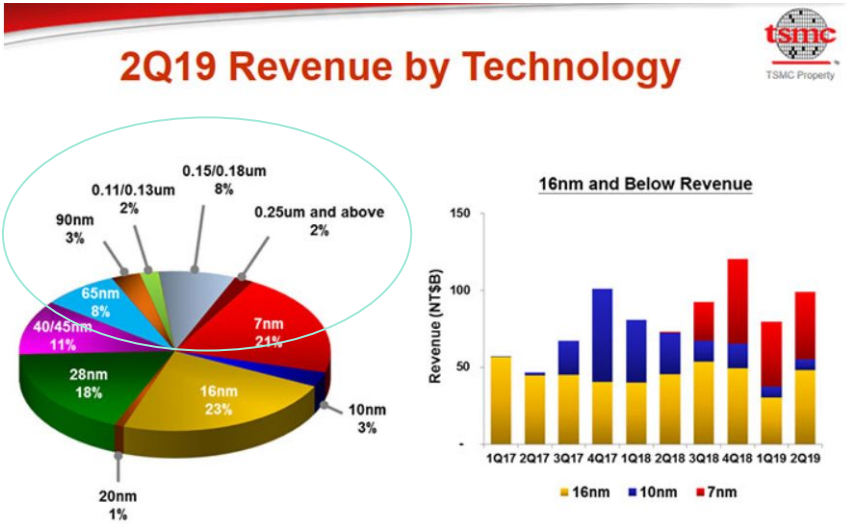
Detector	Sub-system	Type	Sub-type	Channels
PID				
	mRICH @ e-endcap	RICH	PMT/SiPM	
	dRICH @ h-endcap	RICH	PMT/SiPM	300k
	GEM RICH	GEM	Strips	220k
	hpDIRC @barrel	DIRC	PMT/SiPM	100k
	psTOF @barrel	TOF	PMT/SiPM	
	LGAD TOF	TOF	PMT/SiPM	
	LAPPD/MCP-PMT TOF	TOF	PMT/SiPM	
Far Forward Detectors				
	ZDC		PMT/SiPM	
	Low Q2 tagger		PMT/SiPM	
	Luminositymonitors		PMT/SiPM	
	Roman Pots	Si Strips	Si	
	Proton Spectrometer		PMT/SiPM	
	Lepton Polarimeter		PMT/SiPM	
	Hadron Polarimeter		PMT/SiPM	

Readout Variant	Channels (actual)	Channels w/+10% Spares	Type
V1	200M	220M	Si
V2	220k+	242k+	Straw/GEM - fADC
V3	377k+	415k+	GEM
V4	461k+	507k+	PMT/SiPM

ASIC Technology Nodes



From **A. Caratelli**'s talk in TWEPP 2020



- Presently, the most popular node at MOSIS for TSMC is 180 nm
- For comparison, the 250 nm node, popular in our community for a number of years, is still supported by TSMC and MOSIS. The 250 nm technology node debuted in 1995
- It is likely that any present robust technology in use by our community will still be supported in 10 years
- CERN evaluates and qualifies silicon technology processes, provides support to HEP community for selected technologies, releases mixed signal PDKs with rad-hard IP blocks for the different design nodes

ASIC Surveys

- ASICs for calorimeter, various gaseous detector, silicon timing detector, to support energy (with amplitude measurement, full pulse high speed digitization in Gsps level, or continuous digitization) and timing measurement with resolution as good as 10ps level.
- Support various of dynamic range, peaking time, gain, buffer depth and sampling rate
- Data rate reduction
  - Self-triggering
  - Zero-suppression and loss-less compression in digital domain
- Data Stream from front-end ASIC can be collected by Data Aggregator ASIC like the GBT series chips

APV25	PA+SH+Analog memory
SAMPA	PA+SH+ADC+DSP
DREAM	PA+SH+SCA (+ external ADC)
AFTER	PA+SH+SCA (+ external ADC)
VMM3	PA+SH+Timing+Amplitude
TIGER	PA+SH+Timing+Amplitude
GEMROC1	PA+SH+Discriminator+Timing
MAROC3A	PA+SH+Discriminator+ADC+Timing
ALFE	PA+SH
ALTIROC for LGAD	PA+Discriminator+Timing
ETROC for LGAD	PA+Discriminator+Timing
HGCROC	PA+SH+ADC+Timing
TOFPET2	PA+Discriminator+ADC+TDC
PASTTREC	PA+SH+Discriminator
COLUTA	8-ch ADC: 40Msps, rad-hard, 14 bit dynamic range
NEVIS ADC	4-ch ADC: 40Msps, rad-hard, 11.7 bit dynamic range
WASA	50Msps ADC
SAMPIC	SCA+ADC +Timing
DRS series	SCA w/o digitizer
TARGETX	SAC w/ digitizer
Waveform digitizers from NALU: ASOC, AARDVARC,...	
Few 5G/10Gbps serializer, or transceiver: lpGBT/GBT series, LOCx2,...	

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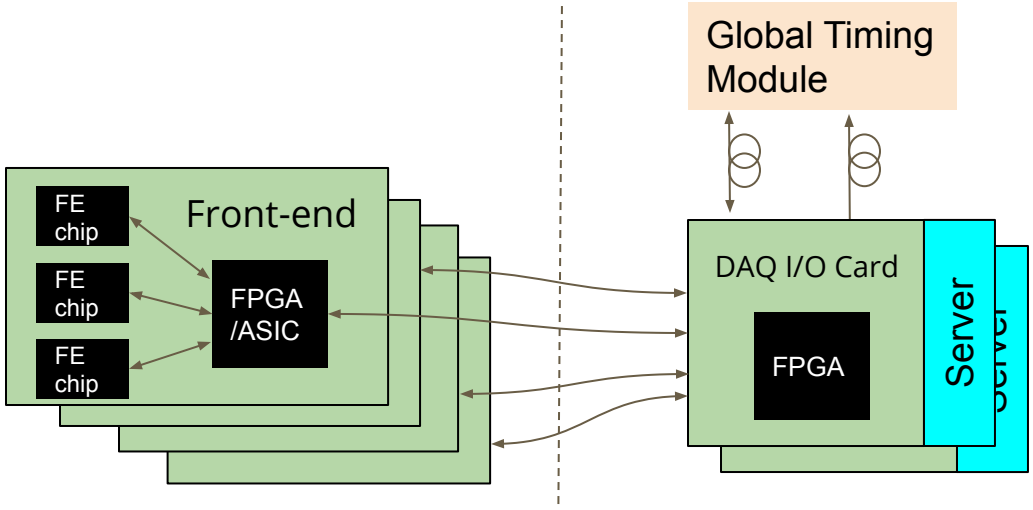
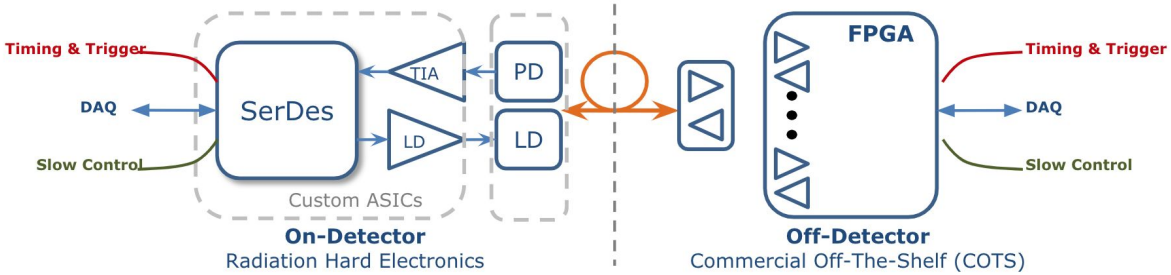
High Precision Timing Distribution (HPTD)

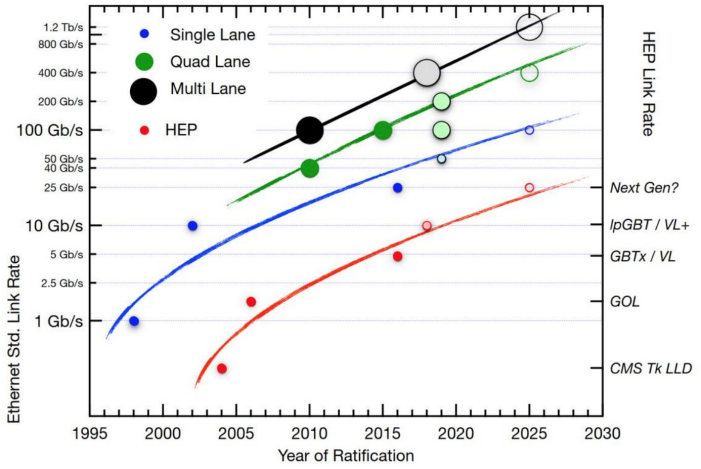


Fix-latency (power cycling)
Phase adjustment in BE (and FE when w/ FPGA)
Phase compensation (temperature drift)
Phase measurement in BE

- With Xilinx FPGA:
  - **Resolution** for phase adjustment is about ***(Unit Interval)/64***, e.g. **~1.5ps** for 10G link
  - **Precision** for phase measurement can also reach **~1ps**
- CERN HPTD group is working on the R&D for HL-LHC experiments
  - tx_phase_aligner project for fix-latency
  - TCLink project for phase compensation
  - https://ep-ese.web.cern.ch/project/high-precision-timing
- R&D will be needed to aim at the machine parameters of EIC

High Speed Links Development @ CERN

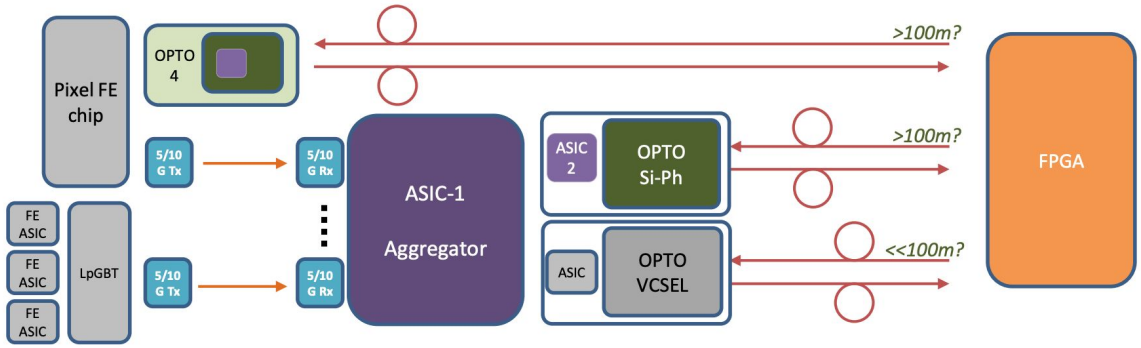




GOL: Gigabit Optical Link
GBT: GigaBit Transceiver
LpGBT: Low-Power GBT

	CMOS	**Power Consumption**	**Link Speed**	**TID**
GOL for LHC (e.g. ALICE)	250 nm	400 mW/chip	Uplink: 1.6Gb/s	~10Mrad
GBT for LHC Run-3	130 nm (1.5V)	980 mW/chip	Bidirectional: 4.8Gb/s	~100Mrad
LpGBT for HL-LHC Run-4	65 nm (1.2V)	500 mW (5.12 Gbps) 750 mW (10.24 Gbps)	Uplink: 5.12/10.24 Gb/s Downlink: 2.56 Gb/s	~200Mrad

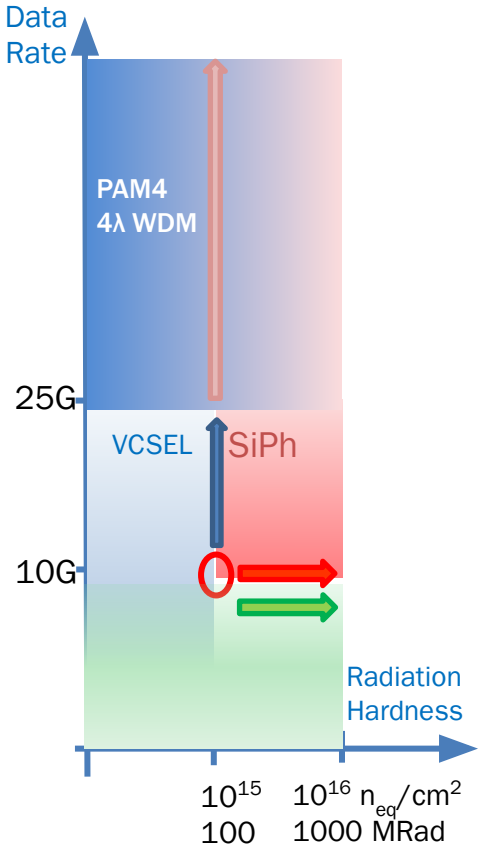
High Speed Links Development @ CERN



Activity	Task	Description
ASICs	ASIC-1	Very high data rate aggregator/transmitter
	ASIC-2	Optoelectronics drivers
	ASIC-3	Low-mass electrical cable transmission (active cable)
FPGA	FPGA-1	FPGA-based system testing and emulation
OPTO	OPTO-1 & 2	Silicon Photonics System & Chip Design
		Silicon Photonics Radiation Hardness
	OPTO-3	Next-generation VCSEL-based optical link
	OPTO-4	Silicon Photonics packaging

"Down scaled" Activity

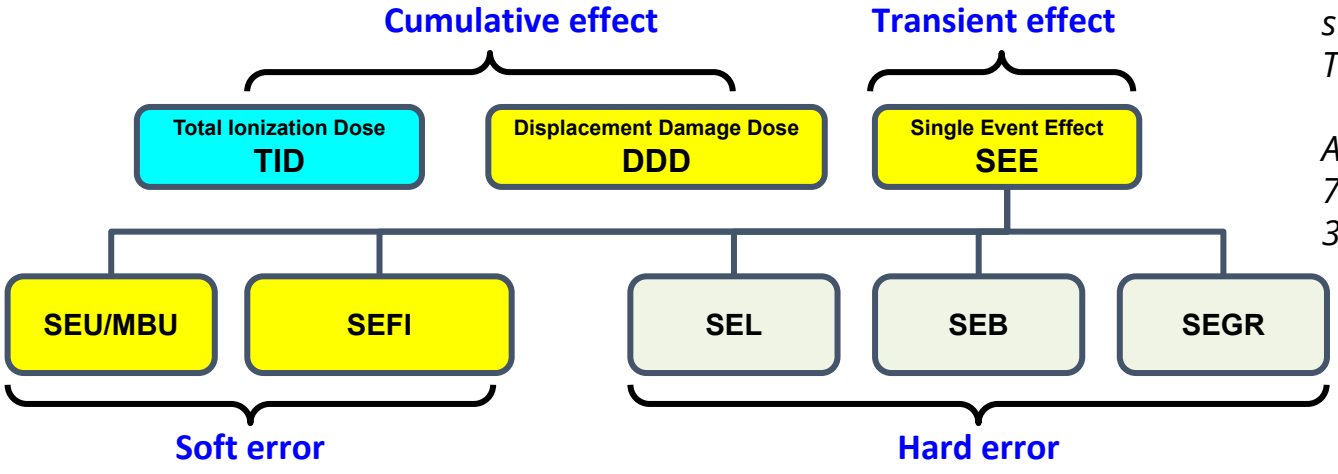
"Dropped" Activities



Sources from **CERN EP Department**

28Gbps NRZ / 56Gbps PAM4 Transmitter with **28nm** CMOS **Si-Photonics**: integration of optoelectronic devices in a "Photonic Si chip", by using WDM: 40Gbps NRZ is possible. **Mach-Zehnder Modulator** is also insensitive to NIEL.

COTS Devices in Radiation Environment



Examples:
sPHENIX TPC FEE: 100 krad TID for 5 years

ATLAS LAr front-end: 75 krad TID for 10 years, 300 krad if COTS

FPGA:

- *SRAM-based or Flash-based*
- *TMR (Triple Modular Redundancy) for user logic*
- *Scrubbing for FPGA configuration*
- *Data coding with error detection and correction*
- *Remote reconfiguration*

TID and SEE R&D for other general-purpose COTS chips:

- *ADC for digitization*
- *Amplifiers*
- *Voltage regulator*
- *COTS transceiver*
- *Clock chips*

Many relative R&D for devices in existing experiments.
Need the requirements (with safety factors) for different sub-detectors.

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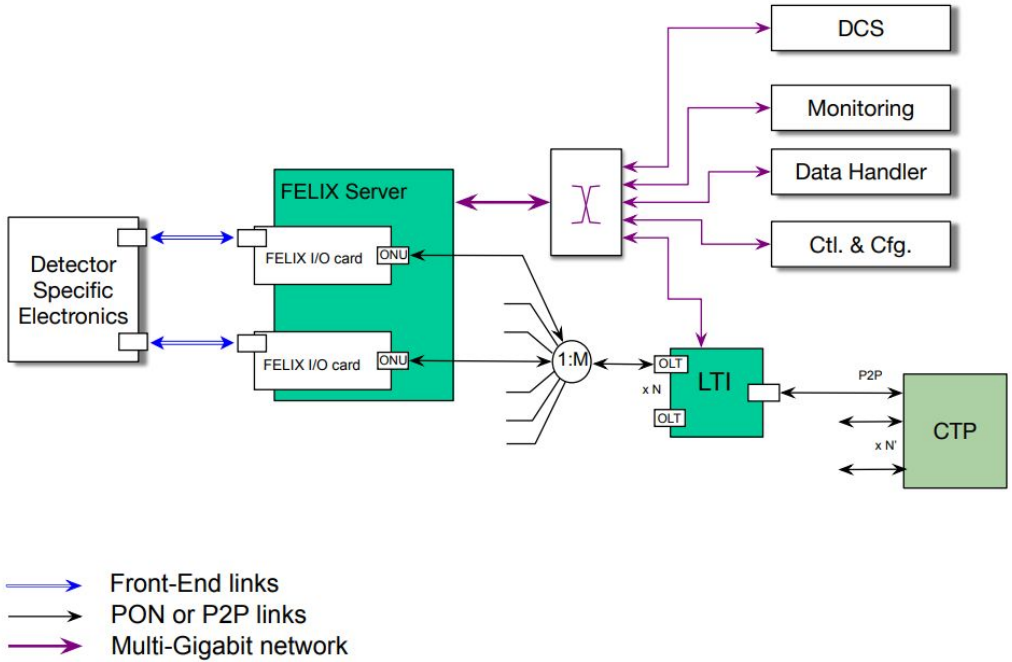
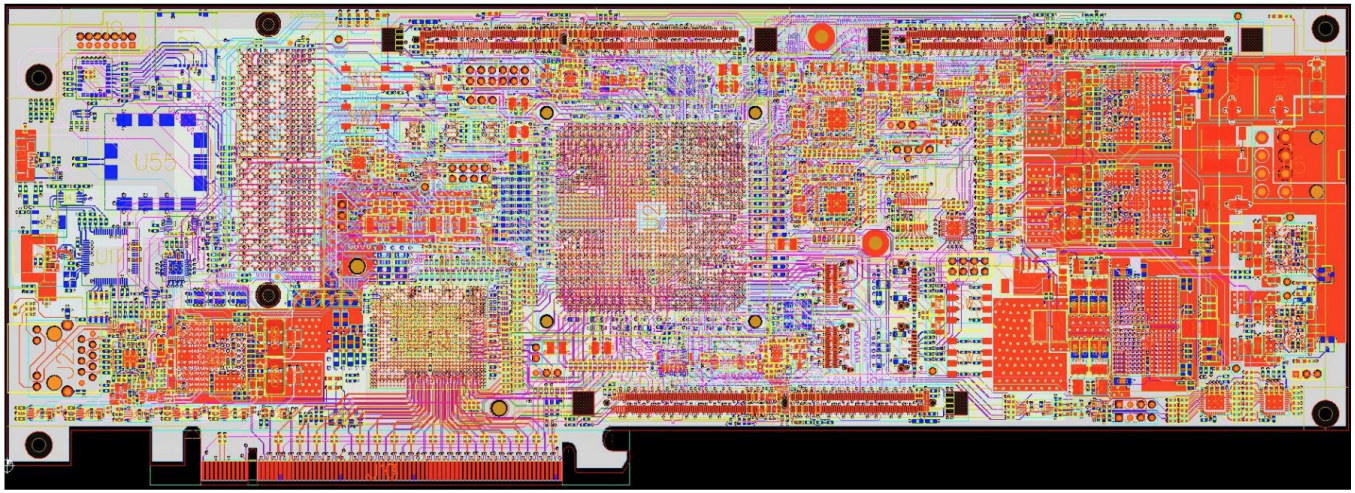
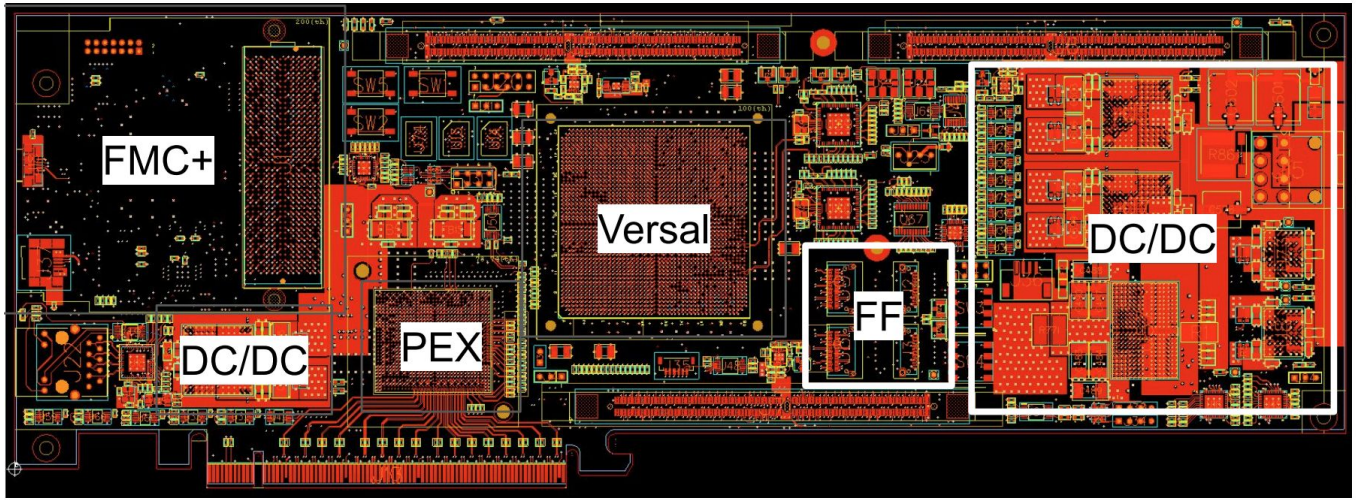


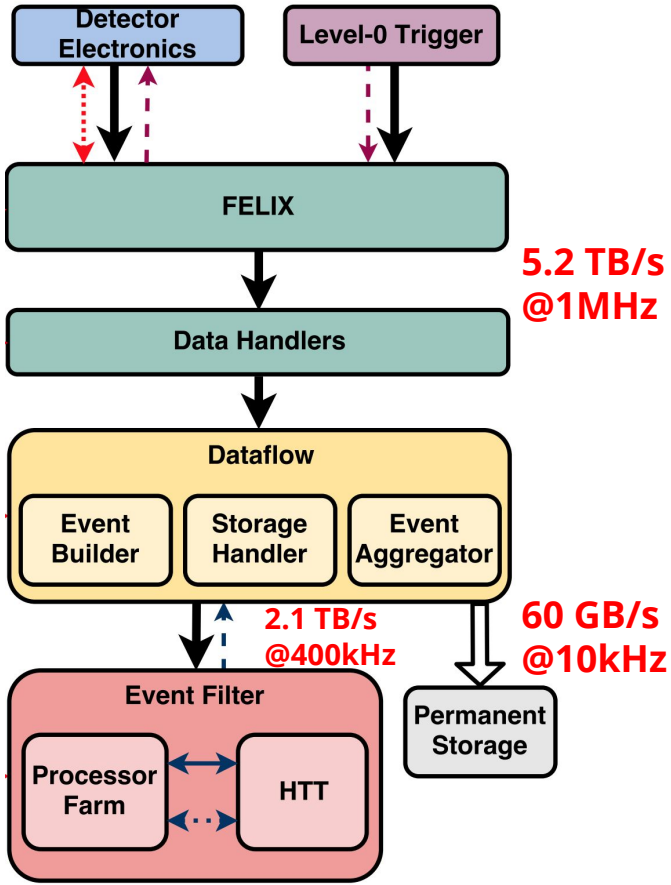
PCIe Card Prototype for ATLAS HL-LHC and DUNE





- *Submitted for fabrication in November*
- *PCIe Gen-4 for prototype; May be upgraded to Gen-5 for future version*
- *Optical links up to 28Gbps*

ATLAS in HL-LHC (from 2027)



- Trigger rate: 1MHz
- ~200 interactions per bunch-crossing
- Data rate: 5.2 TB/s
- ~20,000 fibers with detector

FELIX:

- Distribute trigger & command signals to the Front-Ends
- Transmits the full detector data up to the Data Handlers

Data Handlers:

- Receives the data from FELIX servers over the network at 1 MHz
- Performs data formatting and send data fragments to the Dataflow system

Dataflow:

- ***Event Builder*** builds event records and manages the storage volume of the Storage Handler system
- ***Storage Handler*** buffers event data before and during processing by the Event Filter
- ***Event Aggregator*** collects, formats and transfers the output to CERN permanent storage

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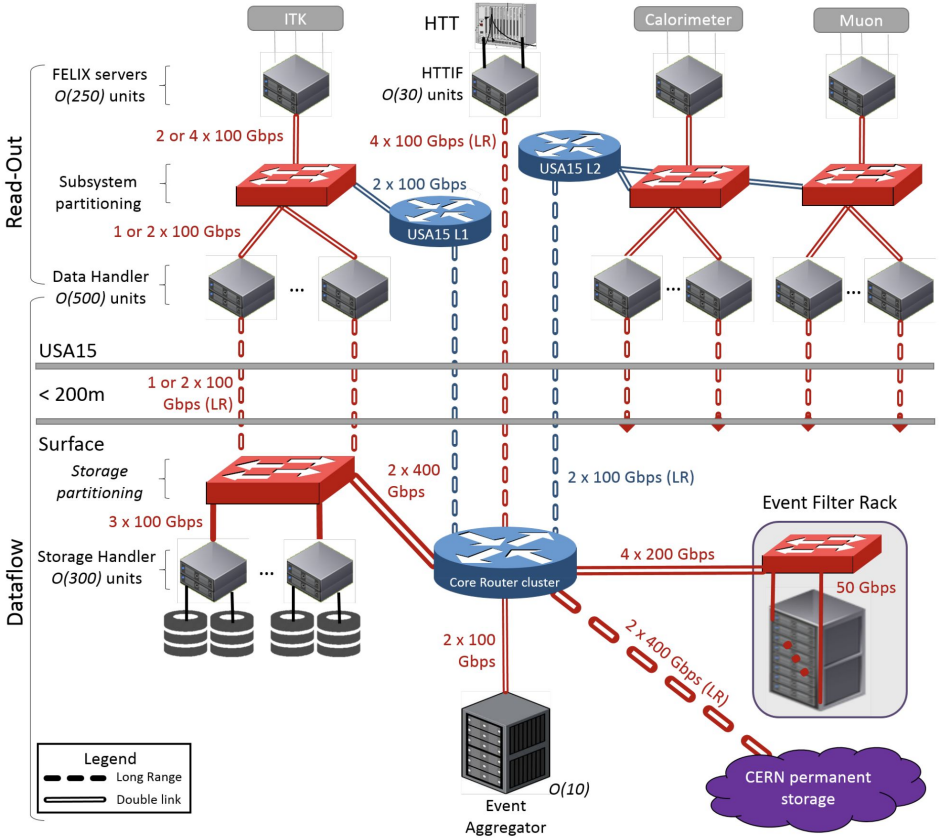

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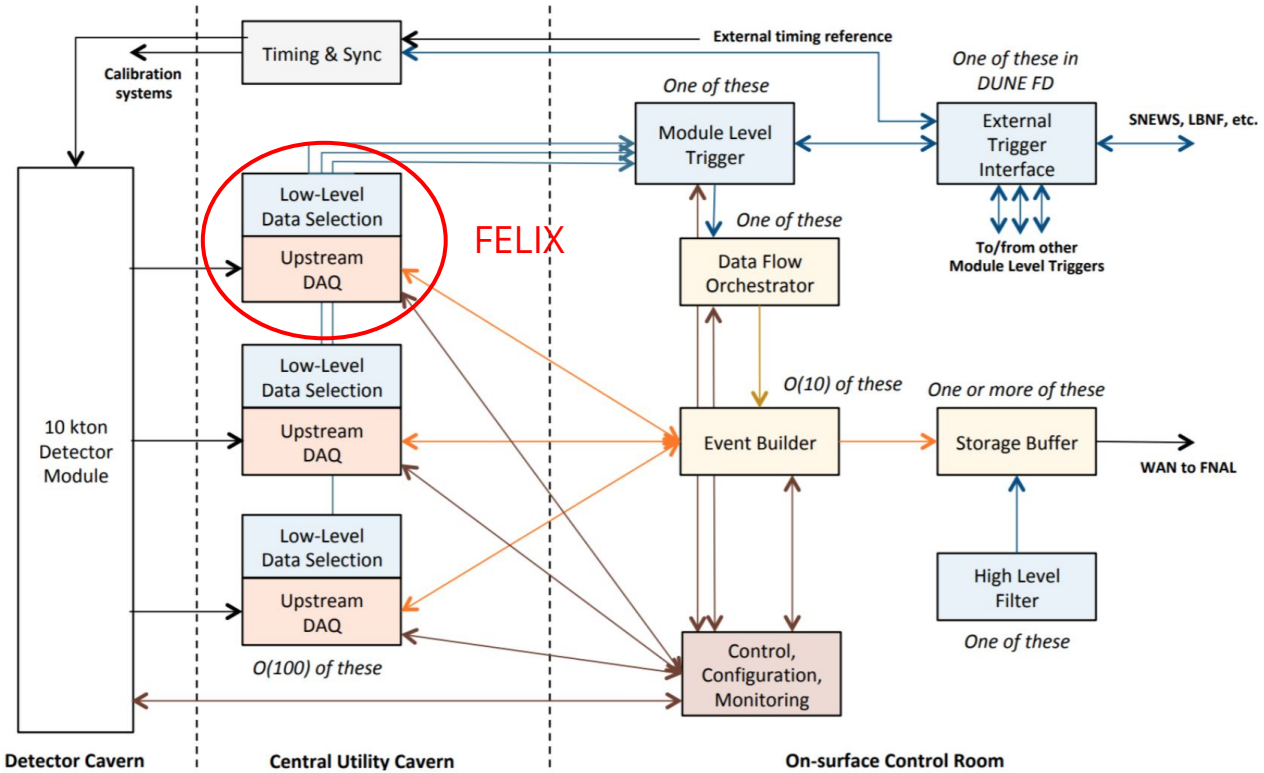
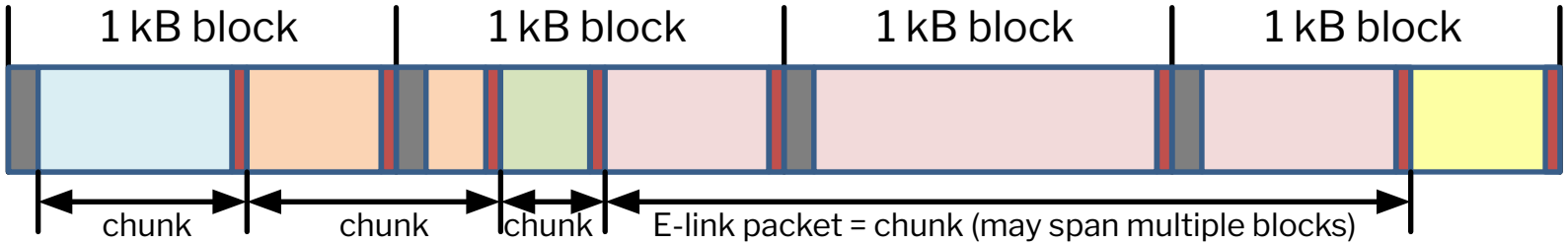
DUNE SP Far Detector (from 2027)



- Streaming readout
- ~11.3Tb/s data streaming via 1,500 fibers per 10kton SP module (384k ADC channels)
- ~100 seconds buffer for the full Supernova Neutrino Burst (SNB) data: ~150TB
- ~10 seconds transient buffer for SNB triggering

Data format (for ATLAS in Run3 and ProtoDUNE SP)



- Fixed block size of 1 kB (larger for SP-ProtoDUNE)
- The DMA runs continuously, thereby eliminating DMA setup overheads and achieving high throughput (about 12 GB/s for the Gen-3 16-lane interface of the FLX-711).

32 bits block header: E-link ID, Block sequence, Start of block symbol

16-bits trailer: Fragment type (first, last, both, middle, null); Flags (error, truncation, timeout, CRC error); Fragment length (10 bits)

Mode	chunk size	Rate/link	Links/server	chunks rate/server	data rate /server
GBT	40 bytes	100 kHz	384 (2 cards)	38.4 MHz	15 Gbps
FULL	4800 bytes	100 kHz	12 (1 card)	1.2 MHz	46 Gbps
ProtoDUNE	~480 bytes	2 MHz	10 (1 card)	20 MHz	74 Gbps

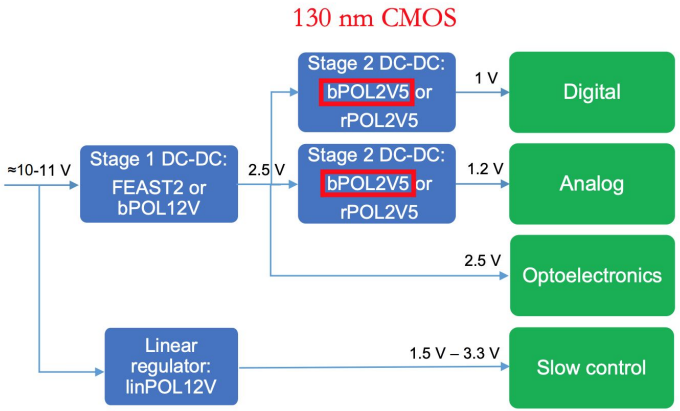
ATLAS: stable operation up to 150 kHz/ 200 kHz for GBT/FULL mode,
For FELIX + SW ROD performance and evaluation of 1MHz trigger rate: Carlo's talk in NSS2020

Summary

- Streaming readout:
  - Streaming readout front-end supporting high speed data transmission off the detector
  - Aim to archive all raw data, after data reduction techniques with minimal physics loss:
    - Zero-suppression and loss-less compression
    - Self-triggering in ASIC design
  - Mitigation of high backgrounds: further data reductions :
    - Calorimeter-based trigger signals that throttles the data stream
    - Feature extraction and noise filtering
  - A reliable DAQ:
    - Global timing synchronization with low-jitter beam collision clock
    - Low and deterministic data loss with busy handling
- Potential general purpose R&D:
  - High precision timing distribution over large system
  - COTS chips in radiation environment: FPGA/ADC/Amplifier/Clock/Power
  - 5/10G level Opto-electronics (transceiver and optical module) aimed on EIC requirements
  - Power distribution to sub-detectors, rad-hard power regulators
  - Machine learning in DAQ firmware for noise/background reduction

Extra Information...

Power for Chips

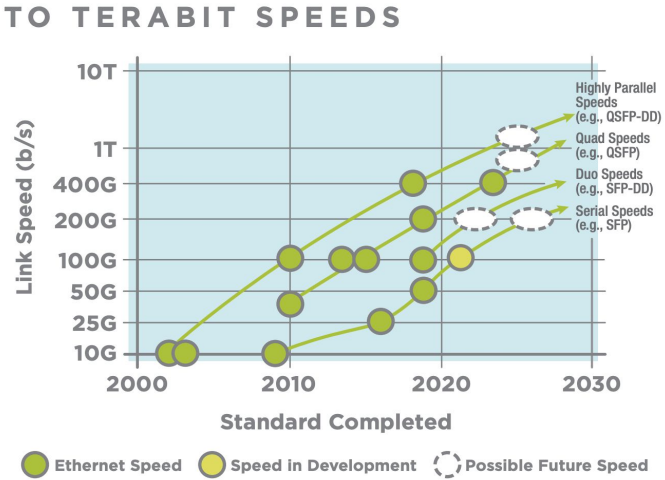


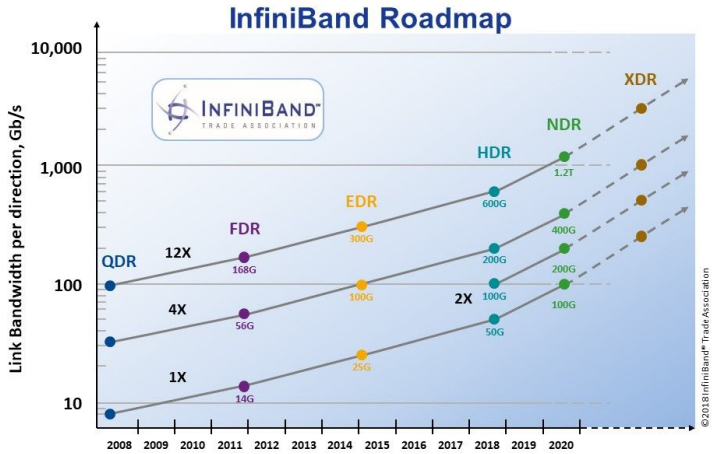
	Name	Type	Vin max	Iout max	Technology	Radiation specs	Package	Availability
Stage1	**FEAST2**	DCDC buck	12V	4 A	350nm CMOS with High Voltage extension at 80V	150Mrad 5e14 n/cm^2 SEE "immune"	QFN32	✓ (End of life! Last order in June 2021)
Stage1	**bPOL12V**	DCDC buck	10-11V (current version), ongoing effort to reach 12 V	4 A	350nm CMOS with High Voltage extension at 25V	150Mrad 2e15 n/cm^2 SEE "immune"	QFN32	In development (see planning slide 20)
Stage2	**bPOL2V5**	DCDC buck	2.5V	3 A	130nm CMOS	150Mrad 7e15 n/cm^2 SEE "immune"	Naked chip with bumps for flip-chip	In development (see planning slide 20)
Stage2	**rPOL2V5**	DCDC resonant switched capacitor	2.5V	3 A	130nm CMOS	150Mrad 7e15 n/cm^2 SEE "immune"	Naked chip with bumps for flip-chip	In development
Linear	**linPOL12V**	Linear regulator	12V	80 mA	350nm CMOS with High Voltage extension at 25V	150Mrad 2e15 n/cm^2 SEE "immune"	DFN8	✓

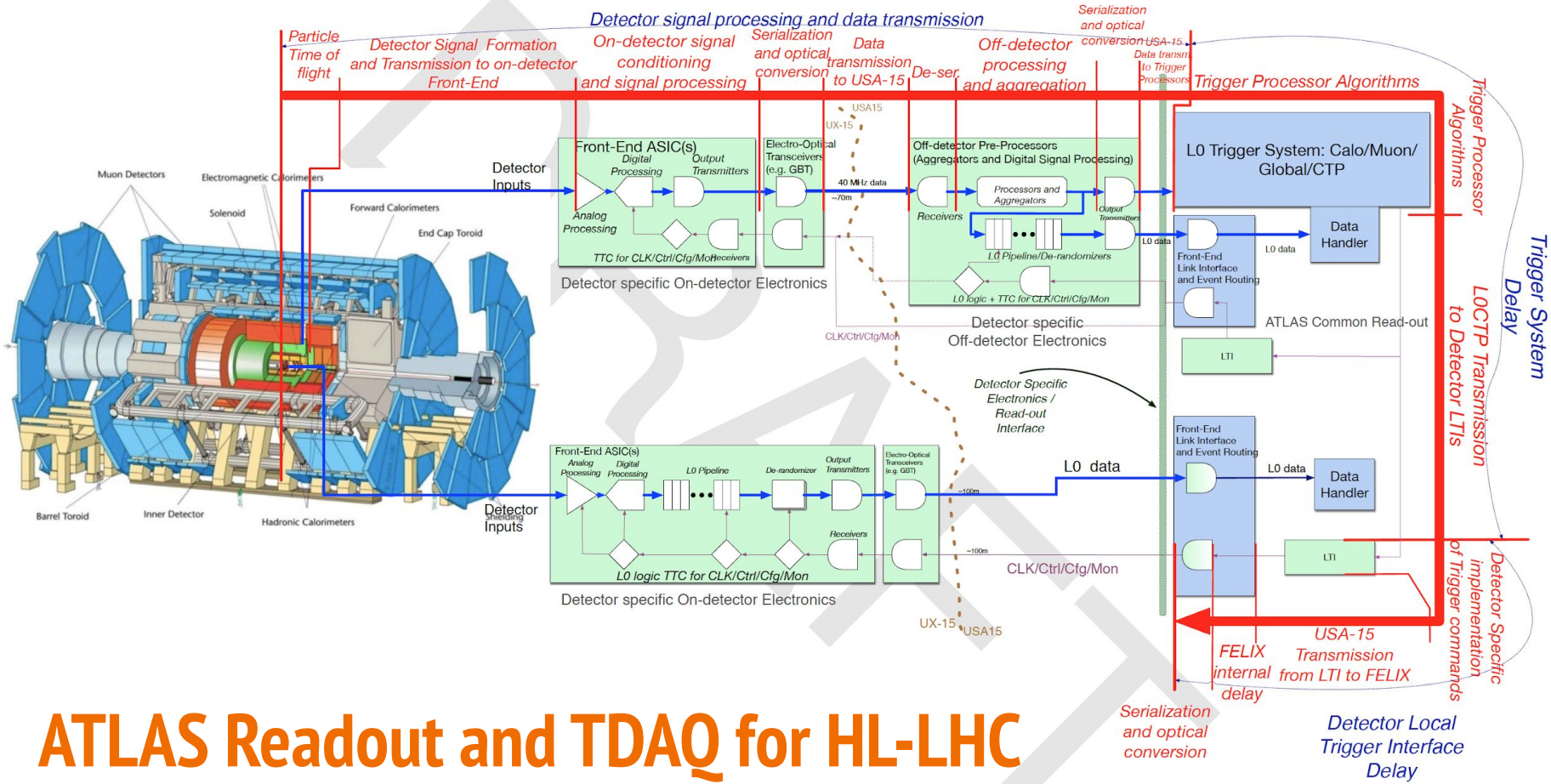
- See ***G. Ripamonti***'s slides in TWEPP 2020
- http://project-dcdc.web.cern.ch/project-DCDC

High Bandwidth COTS Solutions for Back-End

- Xilinx: **112Gb/s PAM4** SERDES will be supported by Versal devices; Intel has also demonstrated 112Gb/s PAM-4 Transceiver I/O
- 200G/400G will be available for single lane with **coherent optical transmission**
- **Terabit Ethernet**: 800 Gbit/s and 1.6 Tbit/s may become IEEE standard in 2025
- **PCIe Gen 6** with PAM4: 128GB/s per 16 lanes (specification to land in 2021); Extended PCIe like CCIX >200GB/s is possible.







ATLAS Readout and TDAQ for HL-LHC