32 Channel ASICs for Detector Signal Digitizing and Processing

SBIR Awards: **DE-SC0017213**
DE-SC0018566

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Presentation Outline

Pacific MicroCHIP Corp.

- The Company, Its Specialization/Expertise
- ASIC Development Motivation
- Relevance to the NP Program
- Project Goals
- ASIC #1 - 12-bit 32 Ch 500MS/s ADC
- Chip Specifications and Architecture
- Comparison to ADCs Available on the Market
- Chip Carrier and Packaging
- Testing Results
- Future Plans
- ASIC #2 – Event Driven Backen with 12-bit 32 Ch 200MS/s ADC
- Chip Specifications and Architecture
- Digital Backend Implementation
- Chip and Its Packaging
- Testing Results
- Future Plans

The Company

- **Pacific MicroCHIP Corp. was incorporated in 2006.**
- **It is headquartered in Culver City, California.**
- **Main focus of the Company – providing IC/ASIC design services and turnkey solutions.**

Office in Culver City, CA

Our Offerings

Pacific MicroCHIP Corp.

IC/ASIC Design Services:

- **Circuit Design (analog, RF/mixed, digital)**
- **Simulation**
- **Physical Design**
- **Chip Assembly**

Turnkey Solutions:

- **ASIC Design**
- **Chip Fabrication Logistics**
- **Package Development (involving a 3rd party)**
- **Chip Packaging (involving a 3rd party)**
- **PCB Development for Testing/Eval. (involving a 3rd party)**
- **Testing/Characterization (an in-house lab)**
- **Delivery of Chips, Parts and Board Level Solutions**

SBIR Funded Development of ASICs for Detector Signal Processing

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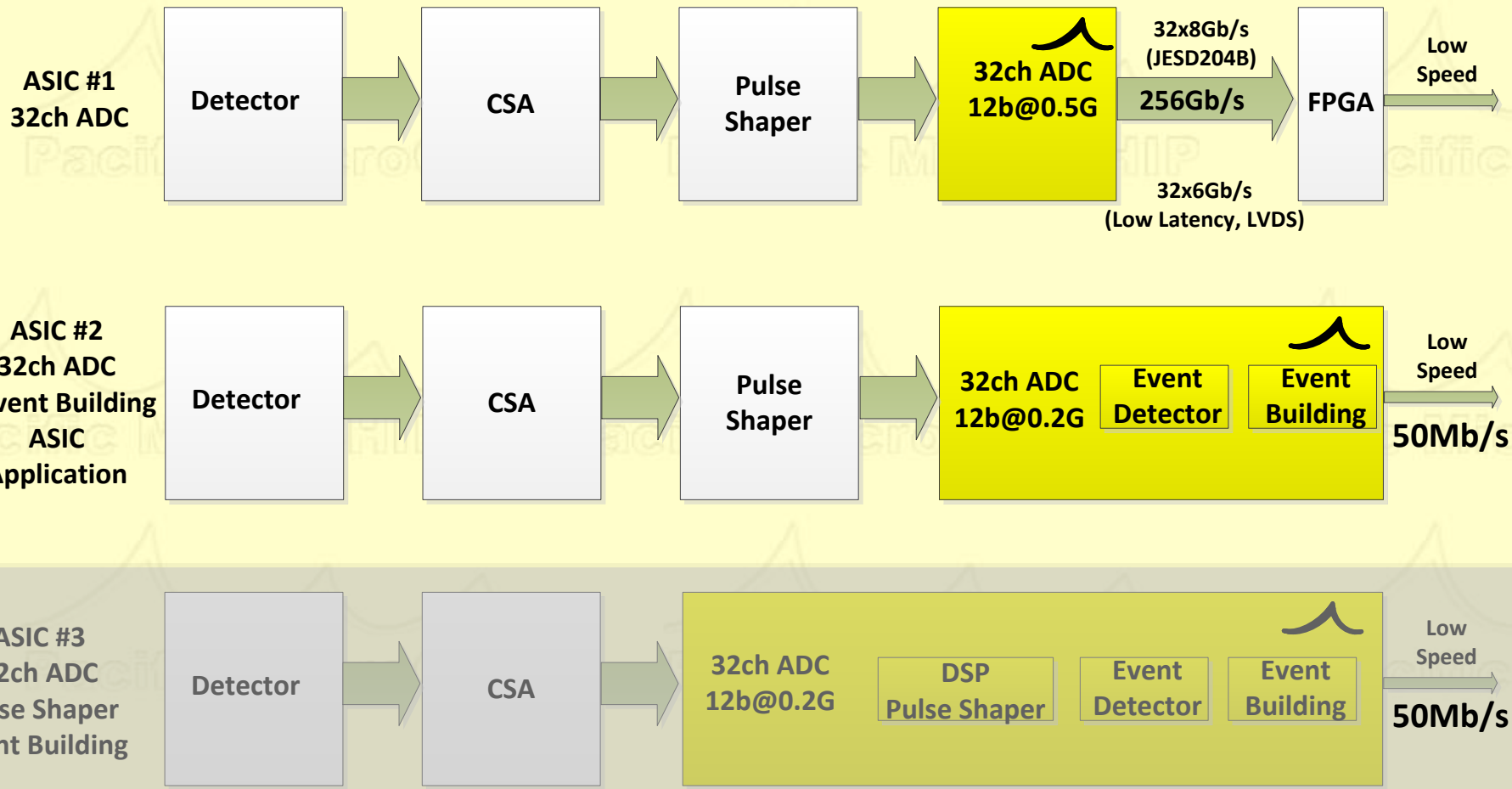
ASIC #1: 32 Ch 12-bit 0.5GS/s ADC

ASIC #2: 32 Ch 12-bit 0.2GS/s ADC + Event Driven Back-end

Where the ASICs Fit



DoE SBIR proposal rejected at administrative screening as *"state-of-the-art is not being advanced"* ☹

Relevance to the NP Needs

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Modern detectors include thousands of signal processing channels

Need for digitizing channels to:

- **Shrink in size – our ASICs combine 32 independent ADCs per chip.**
- **Reduce power consumption – 25mW (ASIC #1), 6mW (ASIC #2) per channel.**
- **Reduce wire congestion:**
  - **. ASIC #1 and ASIC #2 – a serial interface can be shared between 2, 4 or 8 ADCs.**
  - **. ASIC #2 – Event Driven Back-end greatly reduce interface data rate.**

Other requirements:

- **Digitizing accuracy - our ADC features 12-bit resolution.**
- **Adequate sampling speed - our ADC features up to 0.5GS/s (ASIC #1).**
- **Low conversion latency - we offer down to 8ns (ASIC #1).**

ASIC Development Project Goals

- To design chips.
- To fabricate the chips.
- To develop a special chip carrier.
- To package the chips.
- To develop a test PCB and a DUT socket.
- To develop a GUI and a test bench.
- To test and characterize ASICs.

ASIC #1
12-bit 32 Channel 500MSps Low Latency ADC

ASIC #1
12-bit 32 Channel 500MSps Low Latency ADC

Pacific MicroCHIP Corp.

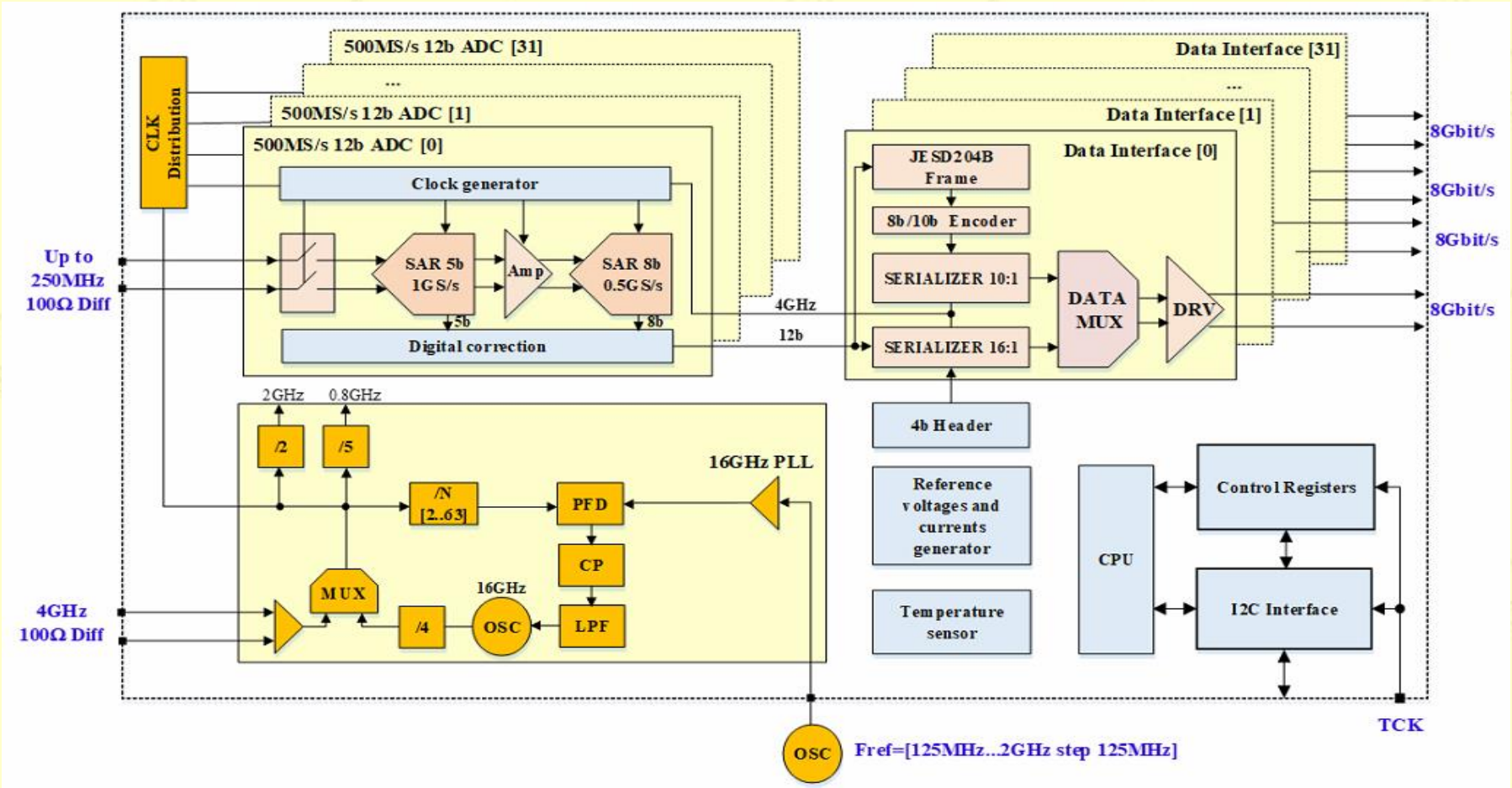
Specifications (expected performance):

- 32 independently operated ADC channels
- 500 MS/s sampling rate
- 0.6Vpp differential input swing
- 10-bit ENOB
- 250MHz input signal bandwidth
- -40C..+125C temperature range
- 25mW/channel power consumption (with an interface)
- JESD204B output data interface
- 8ns latency (direct ADC data output mode)
- 32x8Gb/s output data rate
- I2C interface for ASIC control
- 7.7mm^2 ASIC layout footprint
- A solder bumped die in a BGA package
- 28nm CMOS technology

12-bit 32 Channel 500MSps Low Latency ADC

Pacific MicroCHIP Corp.

ASIC Block Diagram

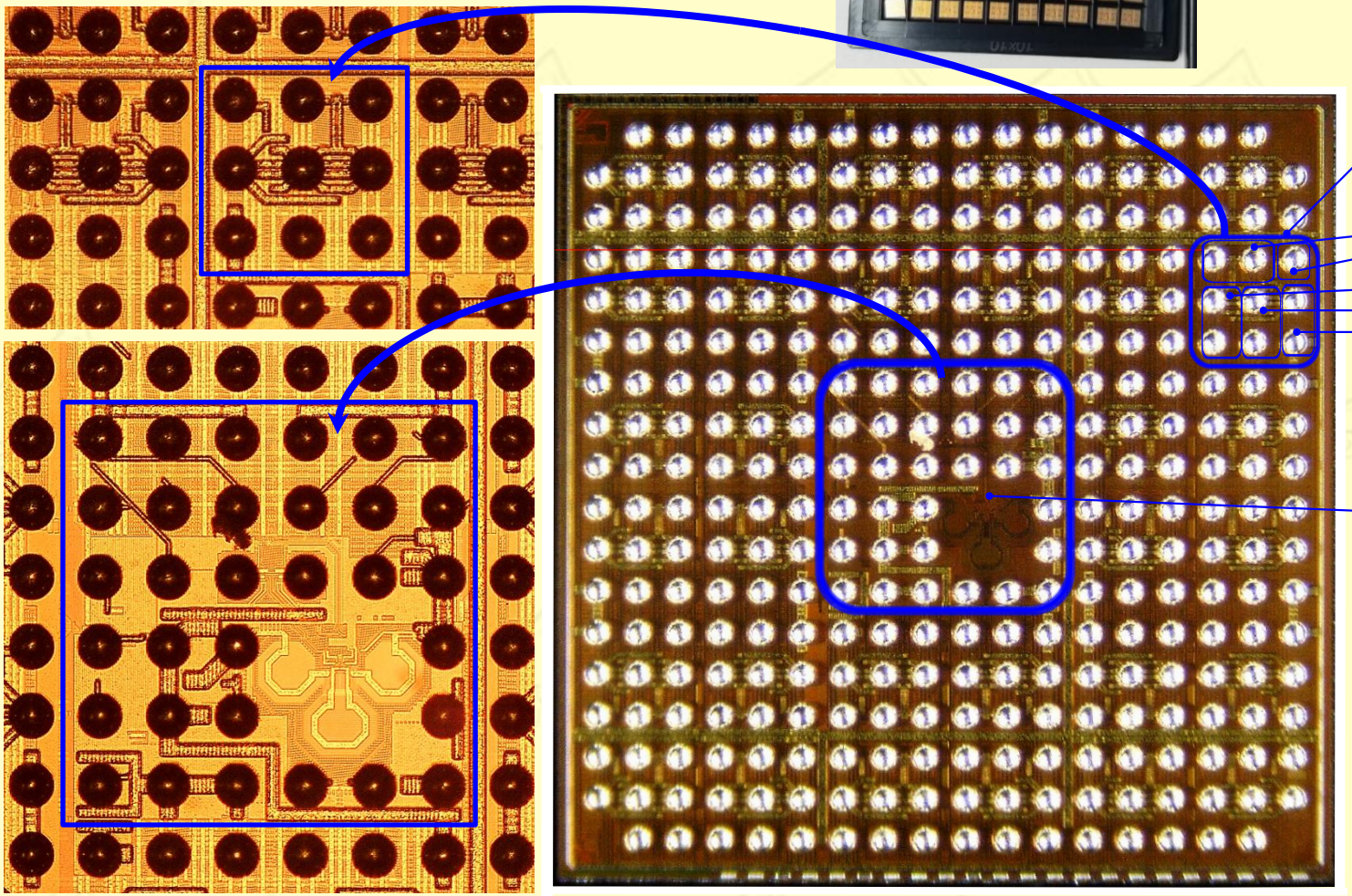


Comparison to ADCs Available on the Market

#	Vendor	# of Channels	Sample Rate, MS/s	Power Cons. per Channel	Architecture & Latency
1.	TI 12-bit ADS52J90	32	40	41mW	Pipeline 2.5us
2.	TI 12-bit ADS5403IZAYR	1	500	1W	Pipeline 240ns
3.	TI 12-bit ADS54T04IZAYR	2	500	1.15W	Pipeline 240ns
4.	ADI 12-bit AD9234BCPZRL7	2	500	1.5W	Pipeline 240ns
5.	Pacific Microchip Corp. 12-bit*	32	500	25mW	SAR/Pipeline 8ns

* Expected performance

Fabricated Chips



Chip Packaging

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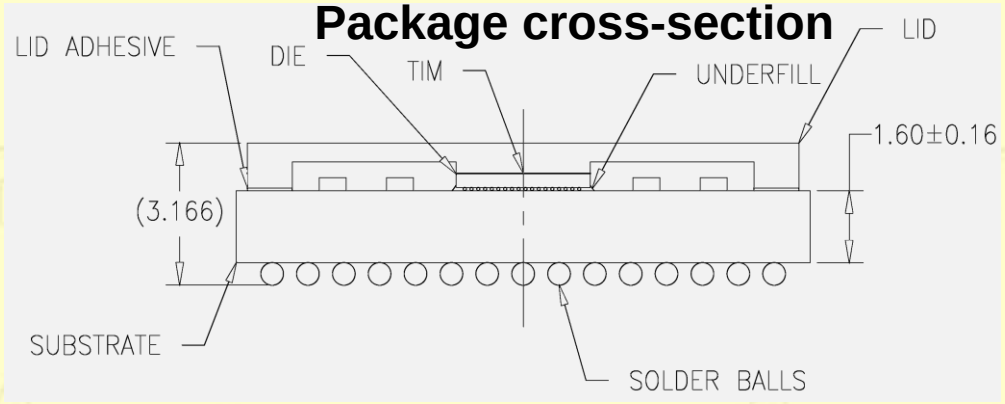
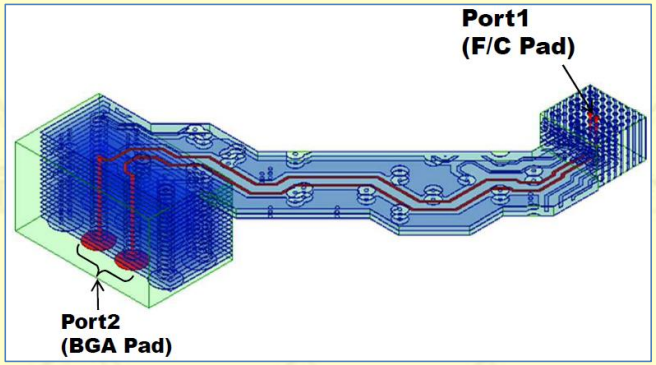
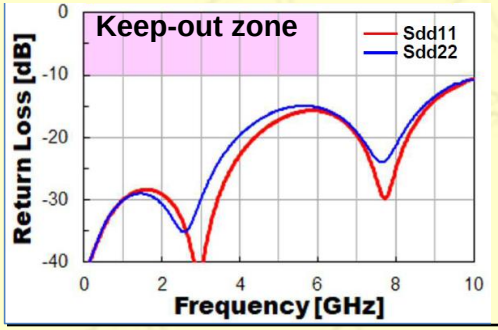
BGA 15.2 x 15.2 mm, 18 x 18 balls, 0.8mm ball pitch

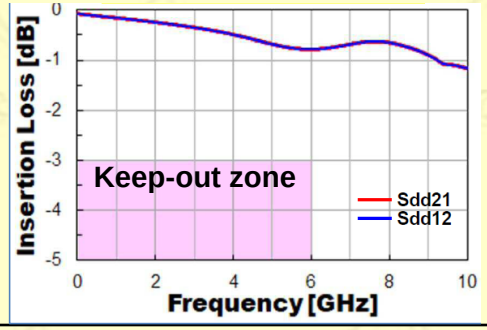
Package Design

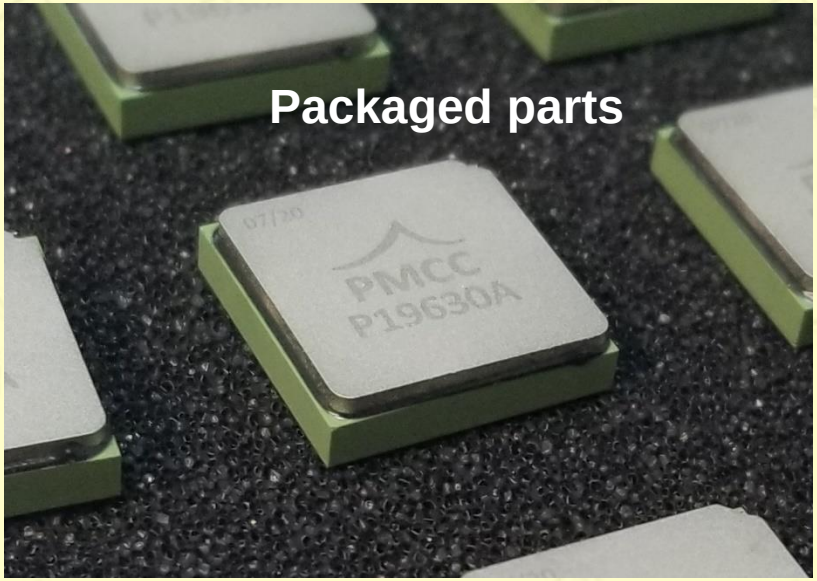
S-parameter simulation results for longest I/O wires:
S11 < -10dB up to 10GHz
S21 > -1dB up to 9GHz











Testing Setup

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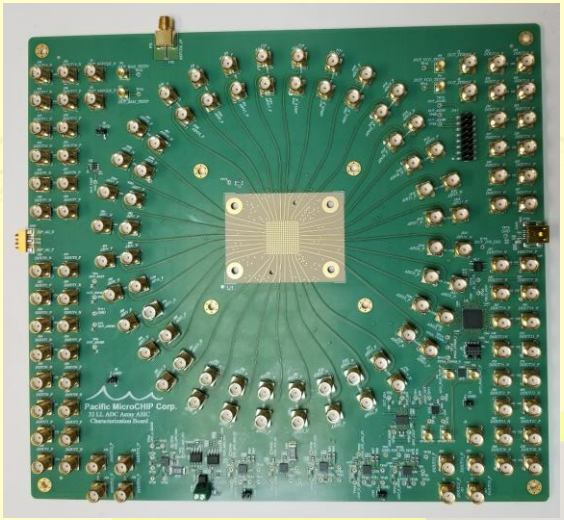
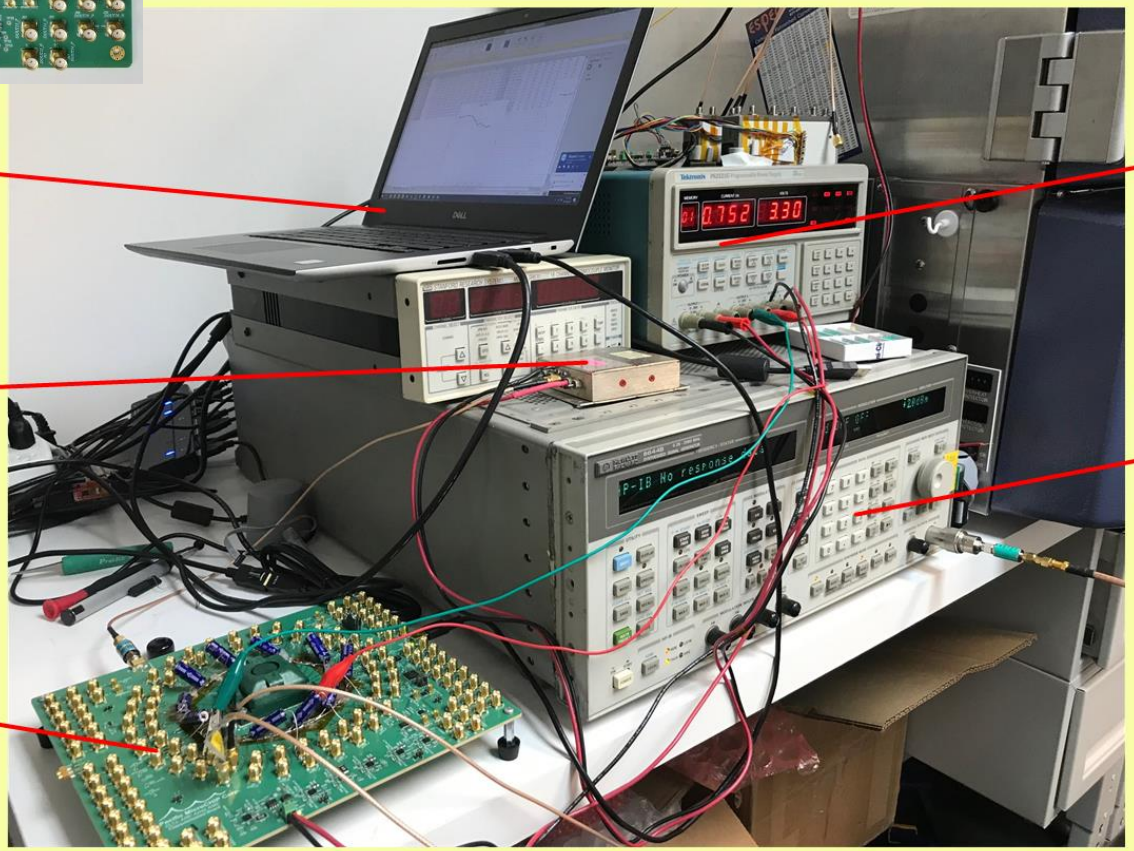


← Test Board

- Exposed area in the center for DUT socket
- 32 differential inputs in a circle for delay equalization
- 32 differential outputs at the PCB's edge (less critical to PCB losses)



Preliminary Testing Results

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Power Consumption

Supply	V [Volts]	I [mA]	P [mW]
VDDD	0.9	445	400.5
VDD18	1.8	9	16.2
VDDA	0.9	88	79.2
VDD12	1.2	564	676.8
PLL	0.9	60	54.0
Total:			1226.7
Per Channel:			**38.3**

Notes: Power of the JESD204B interface is included. An input signal is applied only to a single ADC out of 32. The VDDD consumption is expected to increase when a signal is applied.

Preliminary Testing Results

PLL Performance

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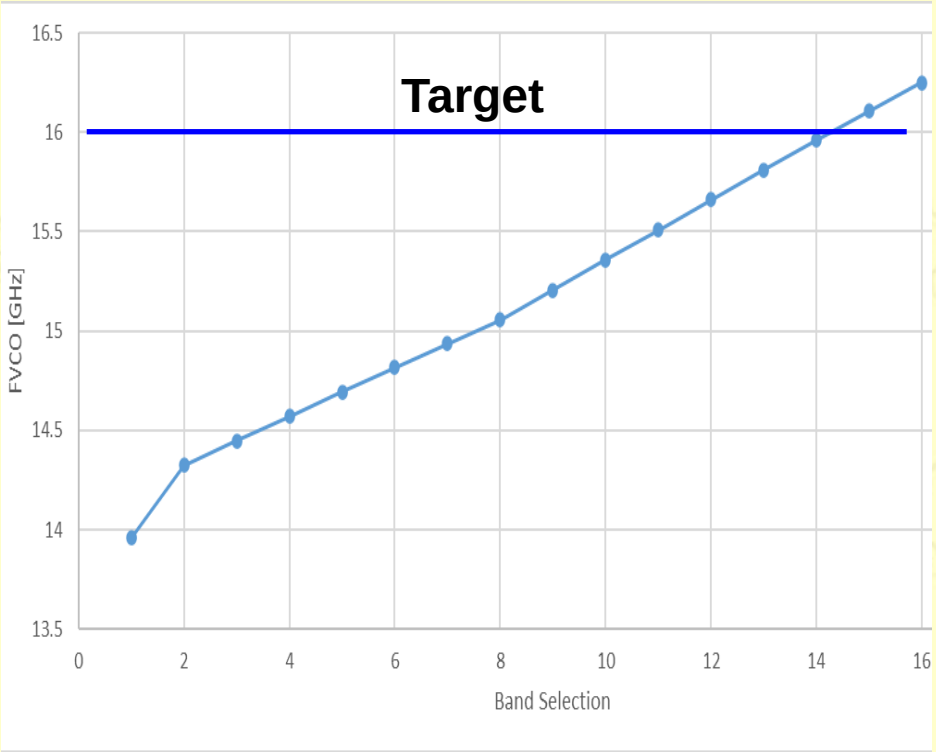
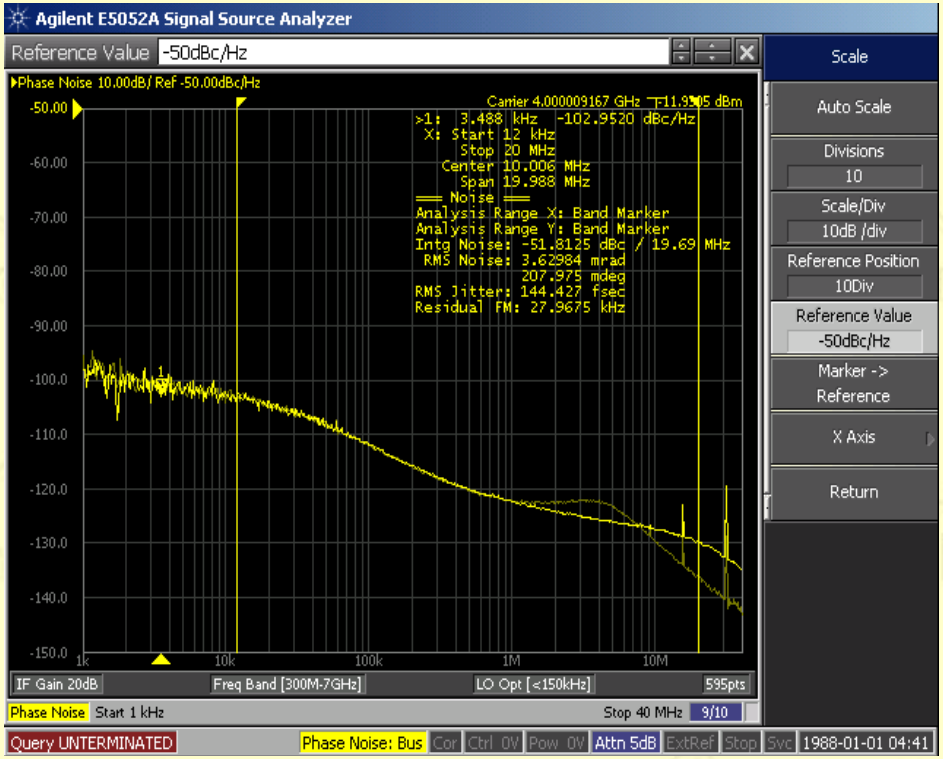
Targeted frequency achieved on the 14th band. It will be tuned up in the 2nd prototype.

Phase noise tested at 16GHz/4. 144fs RMS jitter (12K-20MHz range). Jitter does not depend significantly on PLL BW.

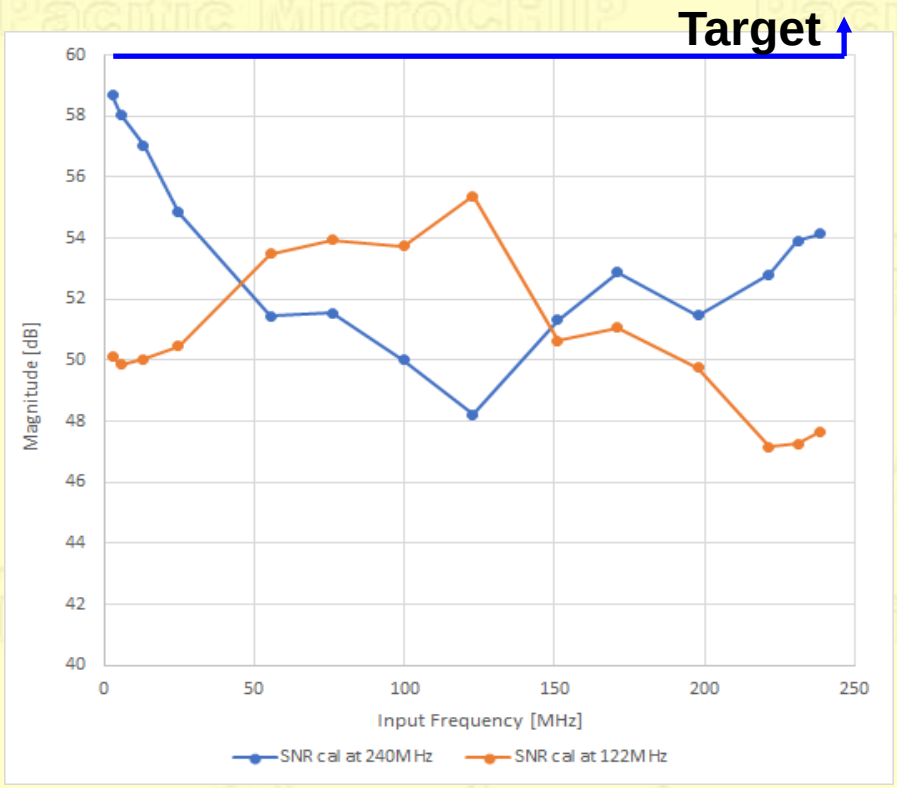


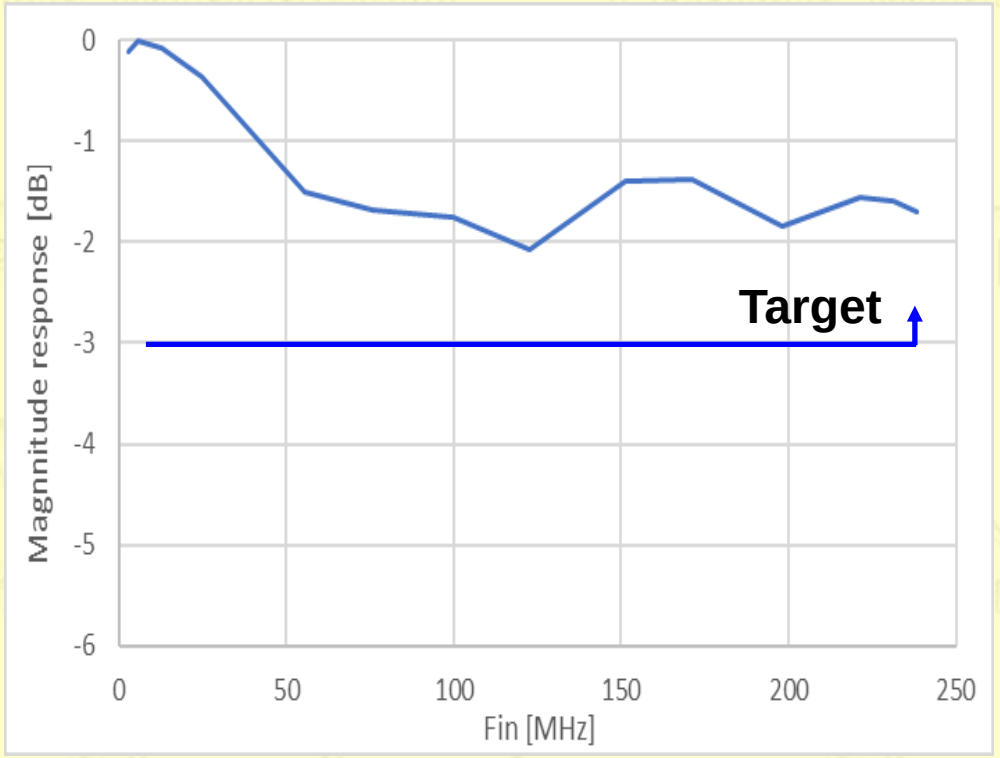


Preliminary Testing Results

Pacific MicroCHIP Corp.

ADC Performance





ENOB vs. Input signal frequency.

When the ADC is calibrated at 240MHz:

9.5 ENOB @ 5MHz

8.6 ENOB @ 250MHz (Nyquist)

When the ADC is calibrated at 122MHz:

8.8 ENOB @ 122MHz

Future Plans for ASIC #1

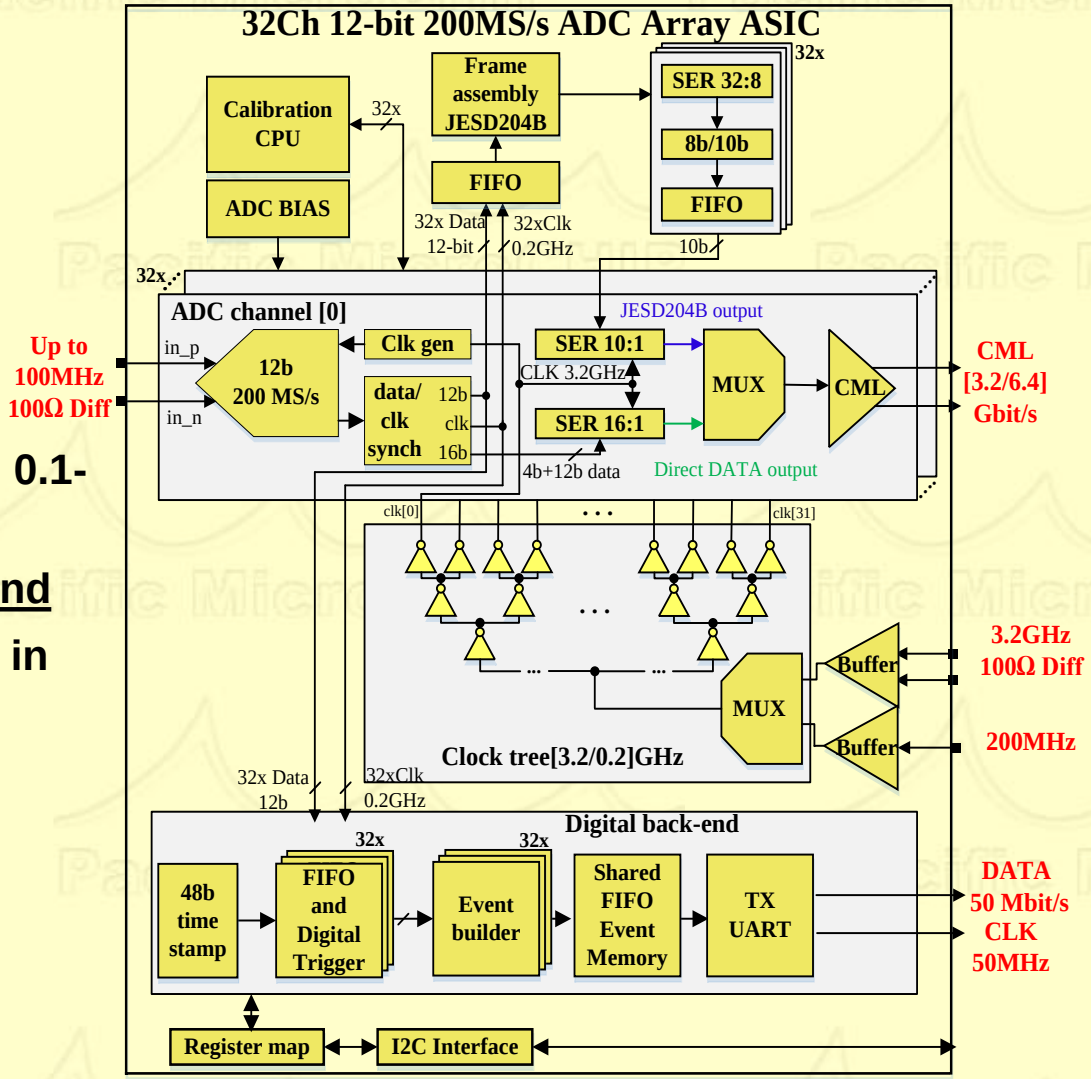
Pacific MicroCHIP Corp.

- **To finish testing the chip's 1st prototype (End of Ph II).**
- **Transition to Phase IIB – to redesign the chip, increase its performance, fix issues identified during testing.**
- **To fabricate the final chip.**
- **To test/evaluate it.**
- **To prepare the chip description and datasheets.**
- **To organize the ADC ASIC design as an IP block and advertise it.**
- **To provide the chip to the DoE community and commercial customers.**

ASIC #2
12-bit 32 Channel 200MSps ADC With Event Driven Back-end
(Digital part developed in collaboration with the LBNL)

ASIC #2 Specifications/Features

- 32 independent ADC channels
- Programmable sampling rate of 200/100/50 MS/s
- Synchronous clock/reset for 32 ADC channels
- ENOB > 10-bit
- 1Vpp differential input signal
- Programmable input signal bandwidth 0.1-0.3 GHz
- Integrated Event Driven Digital Back-end
- JESD204B output data interface (used in the ADC mode)
- Low power consumption
  5 mW / channel (w/o interface)
- I2C interface for ASIC control
- Integrated CPU for ADC calibration
- Integrated temperature sensor



Raw ADC Data Output

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Mode	JESD 204B lanes	ADC per lane	Lane data rate	ADC data rate
Full speed	16	2	6.4Gbps	200MS/s
Half speed	8	4	6.4Gbps	100MS/s
Quarter speed	4	8	6.4Gbps	50MS/s

- Programmable ADC sampling rate of 200/100/50 MS/s
- Constant JESD204B output data rate of 6.4Gbps
- Shared JESD204B output data interface between 2/4/8 ADCs reduces the number of interface lines, allowing high system integration density

ADC Power Consumption

Pacific MicroCHIP Corp.

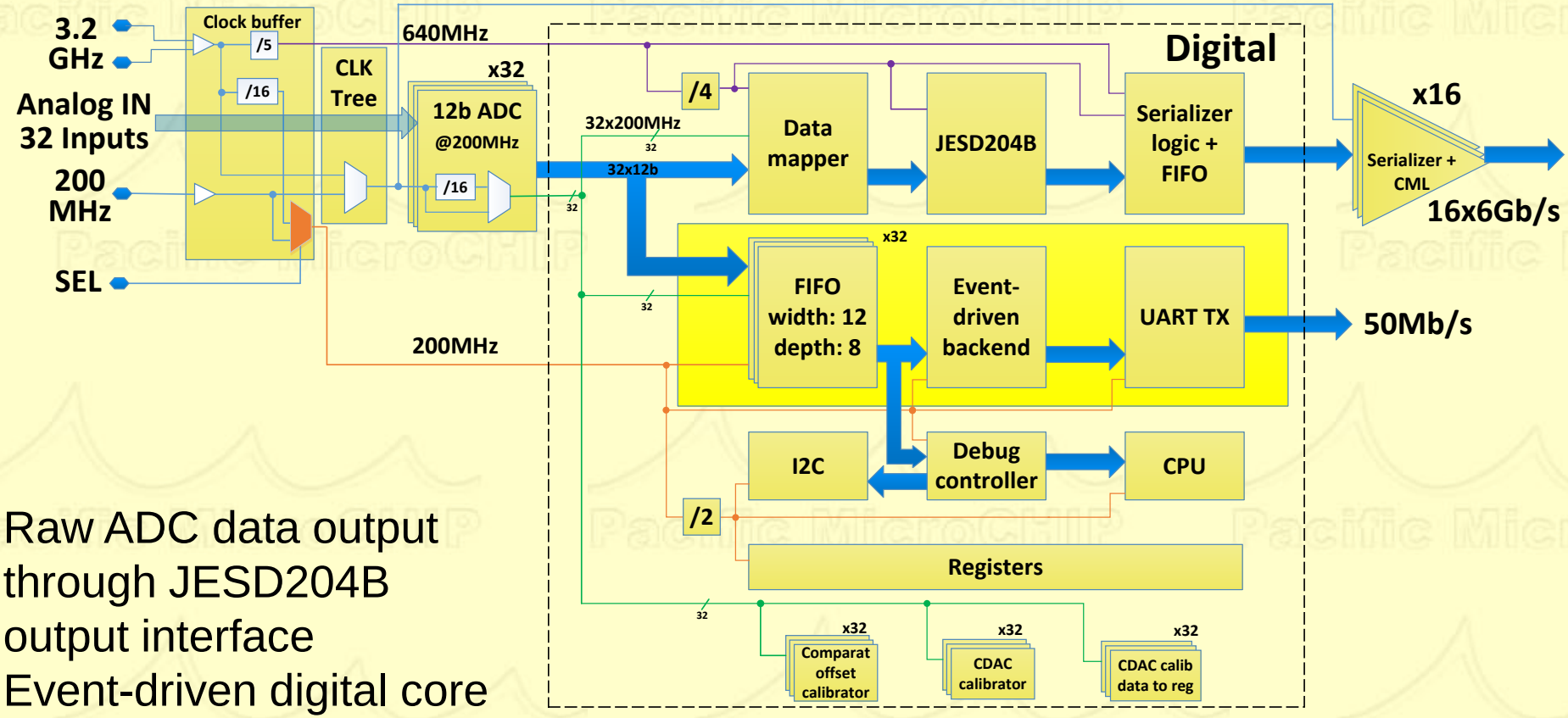
Block	Analog supply current, mA @ 0.9V	Digital supply current, mA @ 0.9V	I/O supply current, mA @ 1.2V	Ground, mA @ 0V
ADC CHANNEL	1.65	7.82	14.88	25.03
ADC CORE 12b@200Msps	1.46	1.62	N/A	3.73
JESD204B PHY	N/A	4.58	14.88	19.48

Typical power consumption of ADC w/o DATA interface: **5mW / ch**

Typical power consumption of ADC with DATA interface: **15.7mW / ch**

(*One JESD204B output data lane used per 2 ADCs operates at 200Msps*)

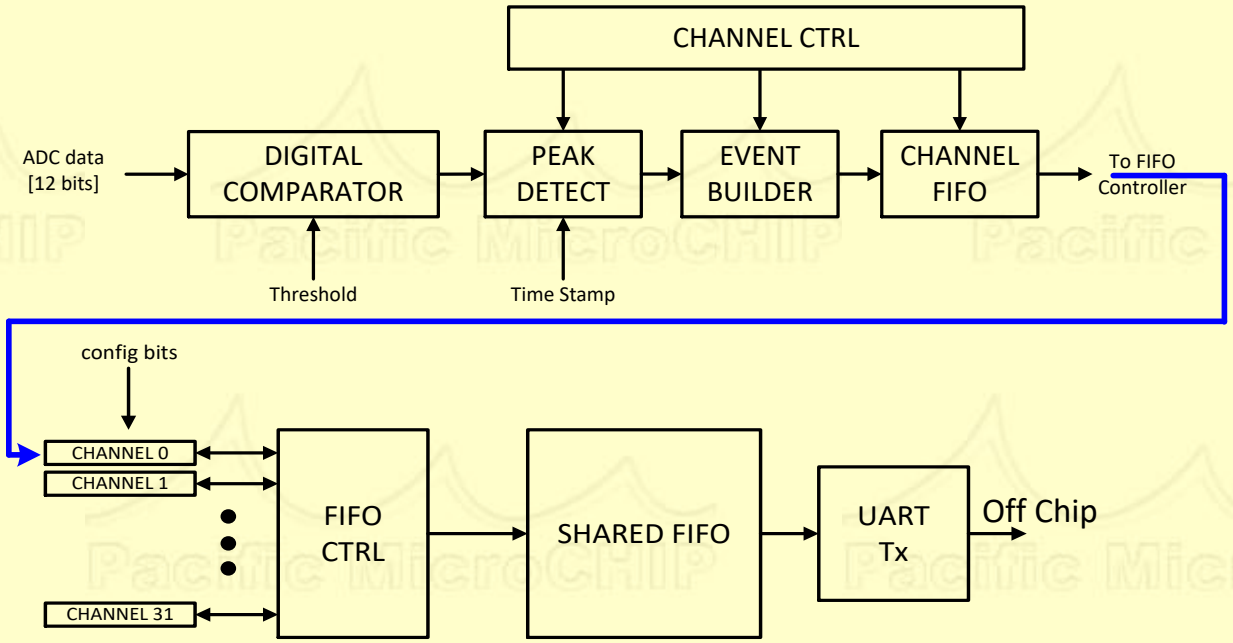
Digital Part



- Raw ADC data output through JESD204B output interface
- Event-driven digital core output through UART interface
- I2C interface for ASIC control registers programming
- Built-in calibration FSM / CPU for calibration purposes

Event–Driven Digital Back-end

- This ADC output is monitored by a digital comparator with a programmable threshold
- When the ADC input exceeds threshold, a timestamp is assigned, and the peak value of the incoming ADC data is recorded.

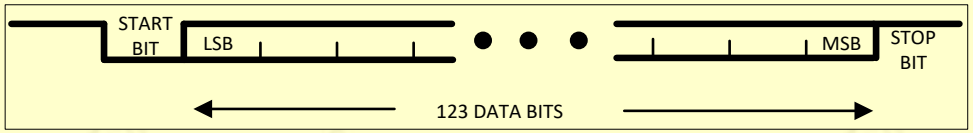


Event-driven digital back-end was built in collaboration with the LBNL. We want to thank Dr. Carl Grace for his efforts.

- When the event is completed, the relevant information is assembled into a packet at the block's back-end. When the shared FIFO is ready, events stored in the channel FIFO are read out.

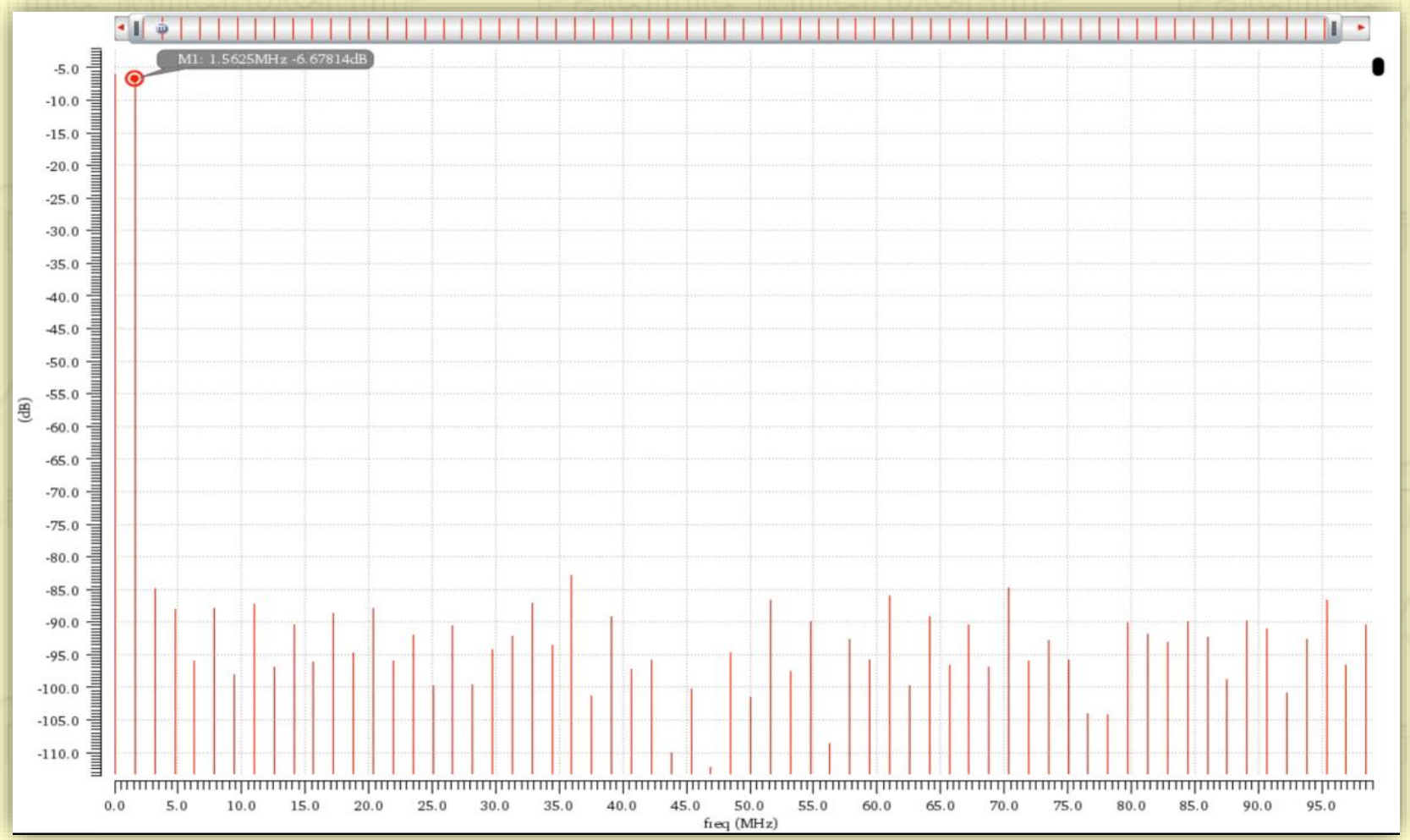
Output Data Frame

Bits	Field Name	Comment
[123]	Parity	Used to monitor integrity of data transmission.
[122]	Event Declaration	0 → test event (see text), 1 → normal
[121:109]	Window Interval	Determines the number of ADC samples to examine looking for a peak.
[108:104]	Channel ID	5-bit unique identifier.
[103:56]	TOA (Time of Arrival)	The timestamp of where the ADC value passed the threshold. Covers ~16 days at a 200 MHz clock rate.
[55:44]	TOP (Time of peak)	Supports shaper peaking times of up to 20 µs at a 200 MHz clock rate.
[43:32]	TOT (Time over Threshold)	Supports shaper pulse widths of up to 40 µs at a 200 MHz clock rate.
[31:20]	Peak Value	12-bit peak value recorded in the event.
[19:8]	Channel Threshold	12-bit threshold value used during this event.
[7:6]	Channel FIFO usage	For diagnostics and debugging.
[5:0]	Shared FIFO usage	For diagnostics and debugging.



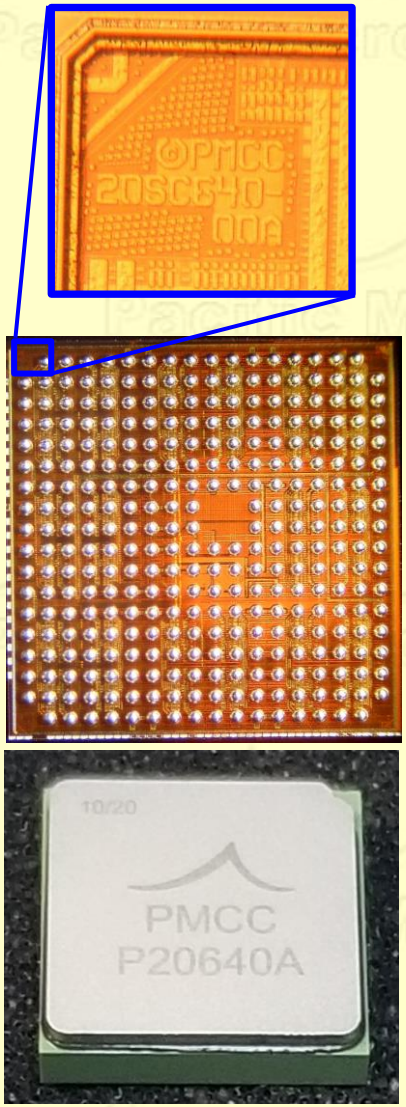
50Mbps / 124bit / 32ch
≈ 12.6k/s events per channel

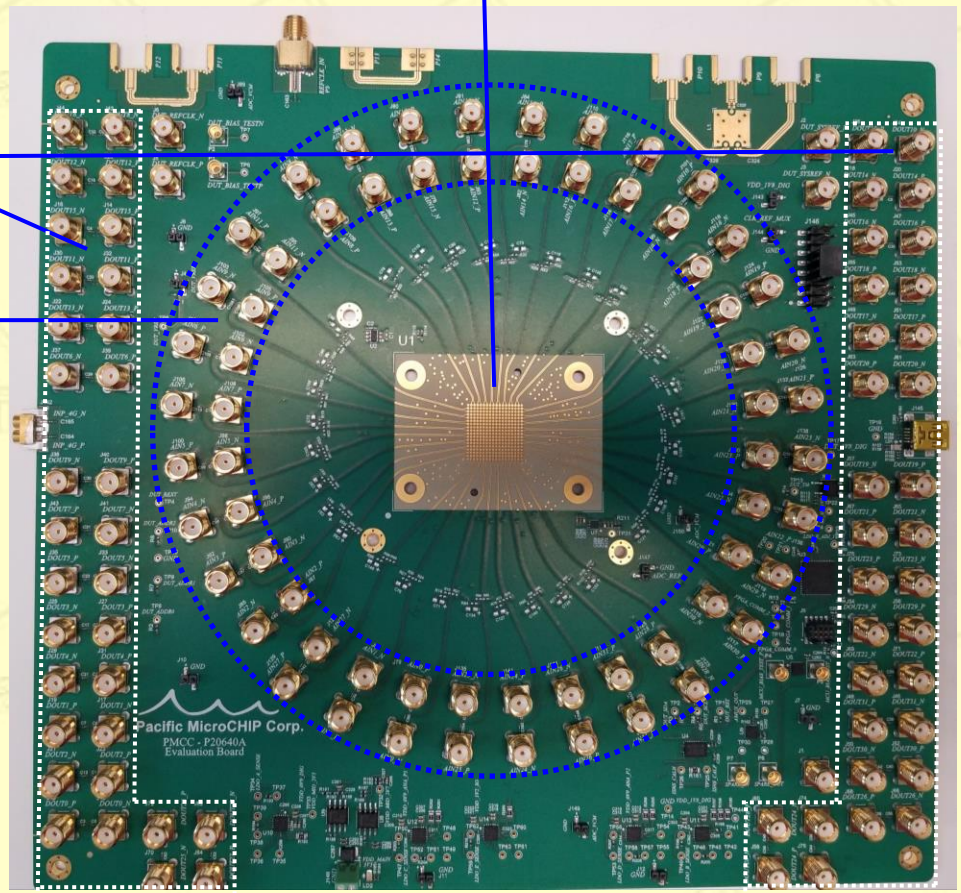
ADC Output Spectrum vs. Input Signal Frequency (Simulated)



Typical performance: **SFDR > 74dB**, **ENOB > 10.4-bit** for Fin<100MHz

Chip, Assembled Part, Test Board

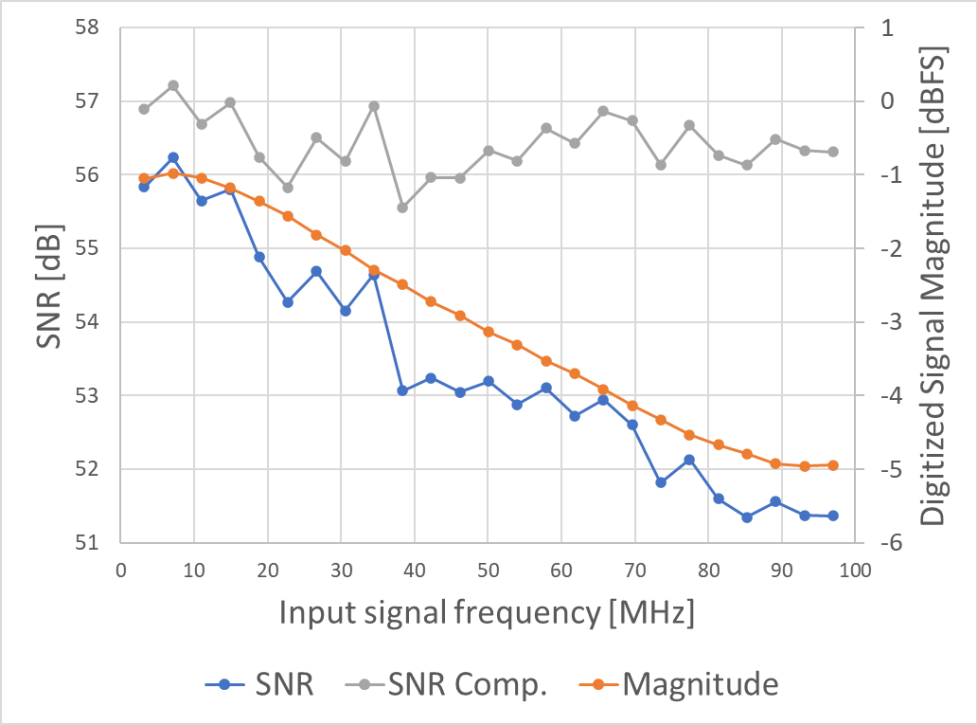


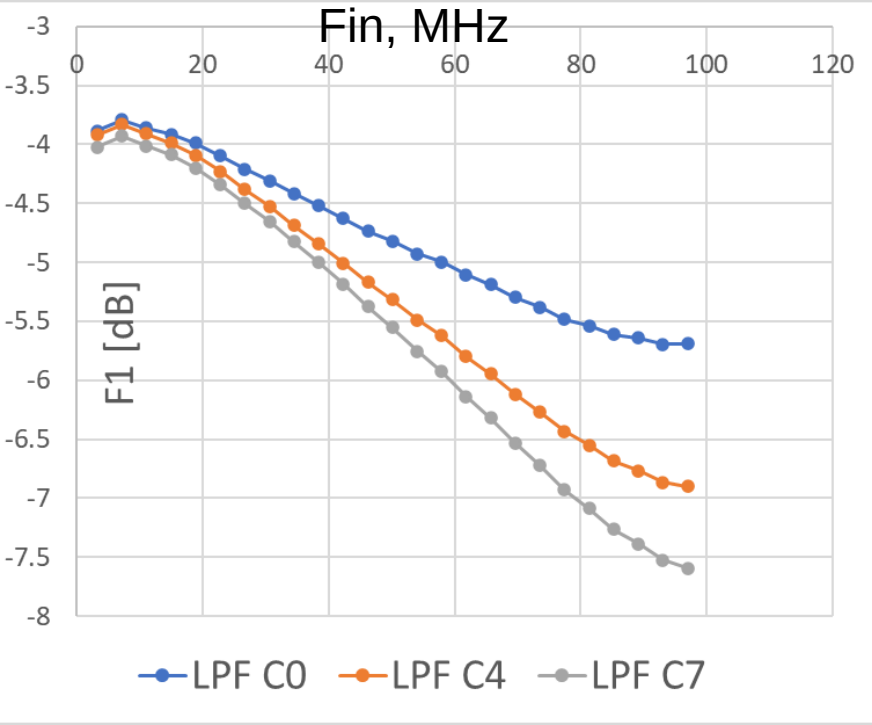


Preliminary Testing Results

SNR within 56dB to 57dB => ~9-bit ENOB
Target is >10-bit ENOB

BW depending on LPF coefficients:
40MHz to 60MHz @ -1dB
80MHz to >100MHz @ -3dB





Future Plans for ASIC #2

Pacific MicroCHIP Corp.

- **To finish testing the chip's 1st prototype (by May'21).**
- **Transition to SBIR Phase IIA or IIB – to redesign the chip, increase its performance, fix issues identified during testing.**
- **To fabricate the final chip.**
- **To test/evaluate it.**
- **To provide the chip to the DoE community and commercial customers.**

THANK YOU !

Application ideas for presented ASICs are appreciated!

Unanswered questions?
Please email: dalius@pacificmicrochip.com