Cold Electronics for Noble Liquid TPCs

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BROOKHAVEN NATIONAL LABORATORY

a passion for discovery

U.S. DEPARTMENT OF ENERGY | Office of Science

Outline

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  - Motivation
  - From JFET to CMOS
- R&D on CMOS Cold Electronics
  - Analog FE ASIC
  - ADC ASIC
  - FPGA
- TPC & Electronics Design in Experiments of SBN & LBN
  - MicroBooNE
  - LBNF 35 Ton
  - LAr1-ND
- Summary

A Brief History of Cold Electronics

Motivation

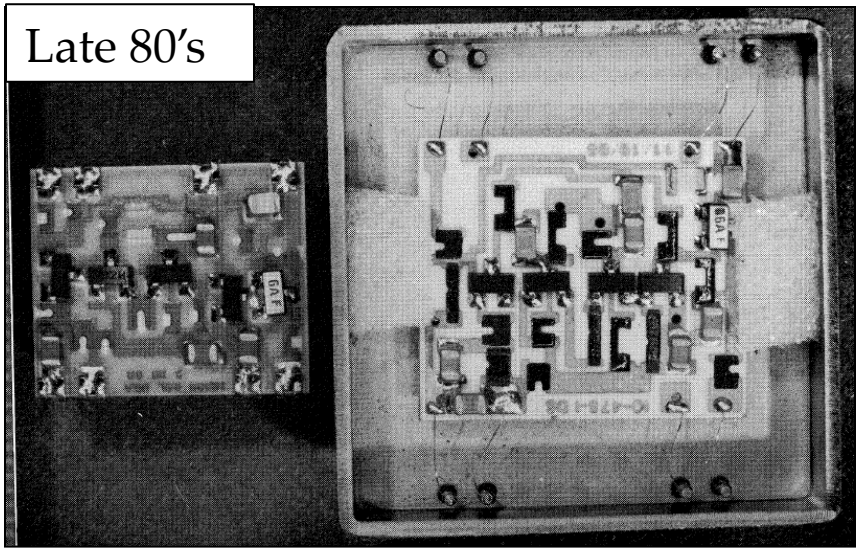
- Readout electronics developed at BNL for low temperatures (77K-300K) is an enabling technology for noble liquid and mixed phase detectors for neutrino and dark matter research
  - Cold electronics decouples the electrode and cryostat design from the readout design. With electronics integral with detector electrodes the noise is independent of the fiducial volume (signal cable lengths), and much lower than with warm electronics
  - Signal multiplexing results in large reduction in the quantity of cables (less outgassing) and the number of feedthroughs/cryostat penetrations
- R&D of CMOS cold electronics started in 2008
  - We had started thinking about LAr TPCs, before the FNAL decision for LAr TPC (and not for Water Cherenkov) for LBNF had been made
  - In 2009 we informed the FNAL director that we were developing cold electronics for future neutrino detectors, and he was supportive
  - MicroBooNE started with plans for JFET's and, the FE ASIC caught up with MicroBooNE delays

Neutrino Experiments using Cold Electronics

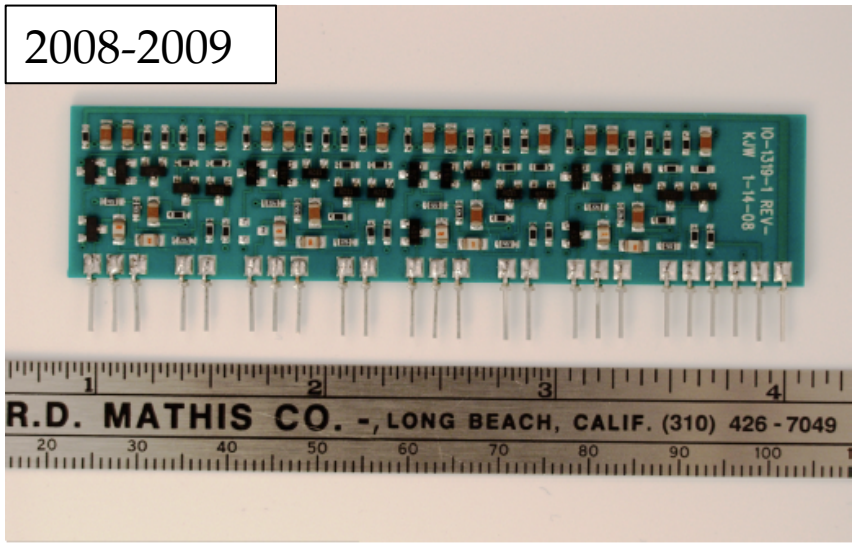
- Projects using, and potentially will be using cold electronics:
  - MicroBooNE
  - ARGONETUBE
  - CAPTAIN
  - LArIAT
  - LBNF 35 Ton
  - LAr1-ND
  - ICARUS, with collaboration of CERN
- ***R&D on cold electronics started before most of these projects were anticipated or in existence***

Cryogenics front-end based on JFET

Late 80's

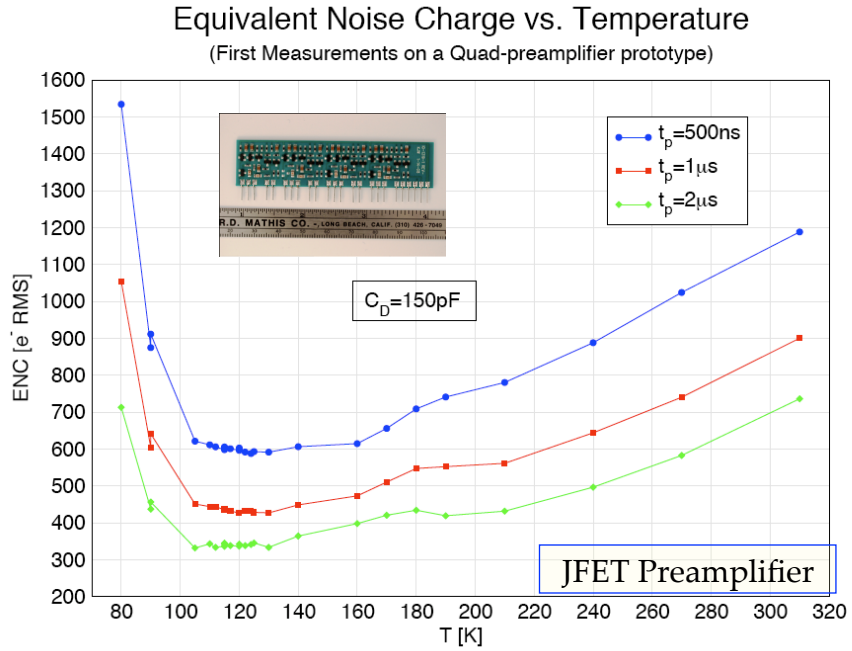


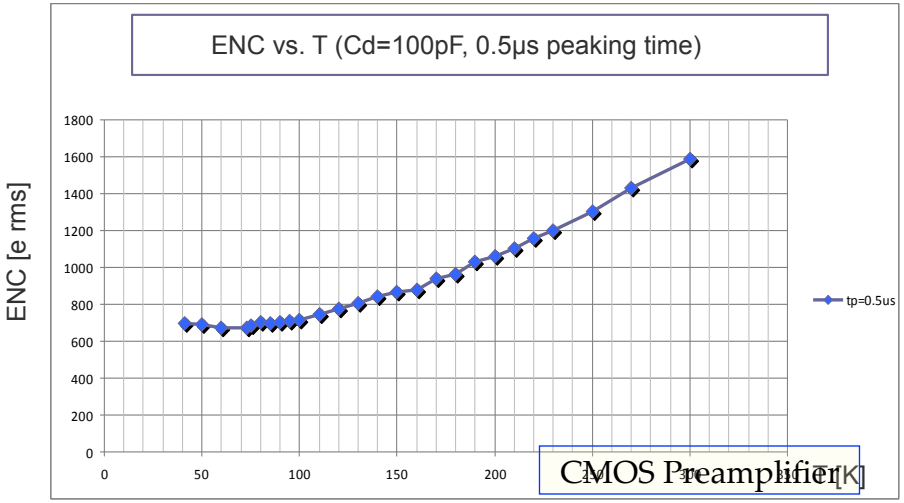
2008-2009



- Helios-NA34
  - Liquid Argon calorimeter
  - 576 preamplifiers
  - Operation: 4 years, multiple cool-downs
- NA48
  - Liquid Krypton calorimeter
  - Preamplifiers in LKr: 13,212 channels
  - Operation: 16 years so far, plan to run until 2015, expected to be in operation for 17 years
- Several years of experience
  - MicroBooNE front-end design started from JFET as well

From JFET to CMOS

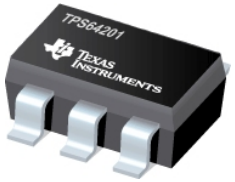




- JFET based preamplifier designed for MicroBooNE
  - Bulk mobility and transconductance increase as temperature decreases, carrier freeze out causes ENC increasing when temperature lower than ~100K
- CMOS technology – test result of an existing ASIC in 0.25 *μm (not designed for LAr)*
  - CMOS in LAr has less than half the noise as that at room temperature, higher mobility and higher transconductance/current ratio
- MicroBooNE has adopted the cryogenic CMOS analog front end ASIC developed for LBNF LAr TPC program

R&D on CMOS Cold Electronics

Cold Electronics

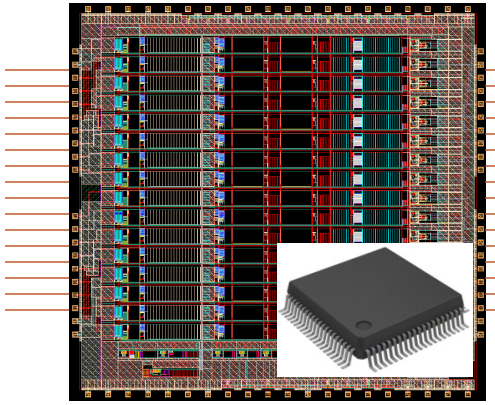


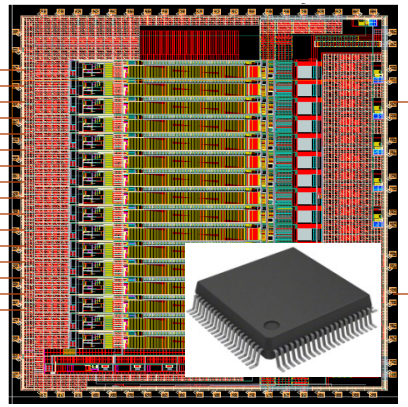
voltage regulation
(COTS)
(< 100mV dropout)

front-end ASIC
~ 5mW/ch.

ADC ASIC
~ 5mW/ch.

FPGA (COTS)
~ 8mW/ch.



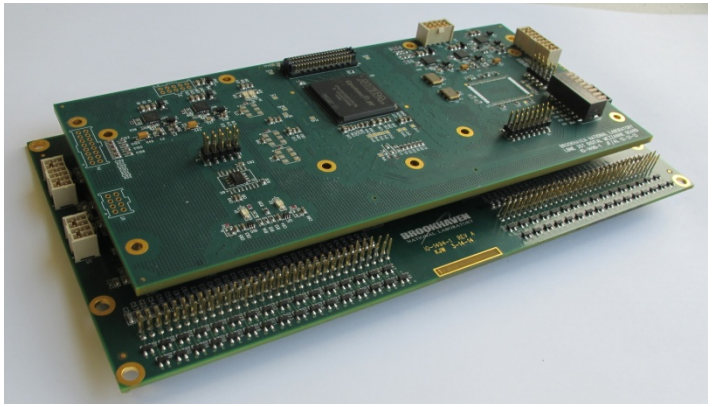


overall 128:2
multiplexing

8 x

1 x

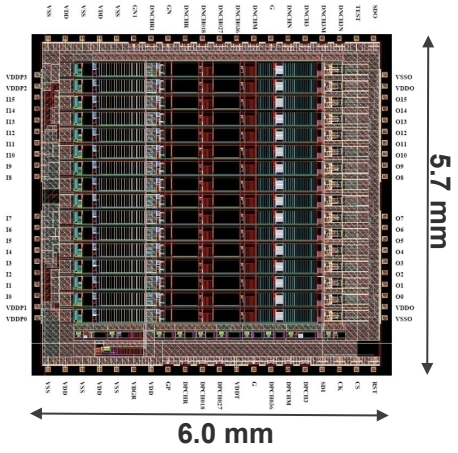
A Complete Front End Readout Chain

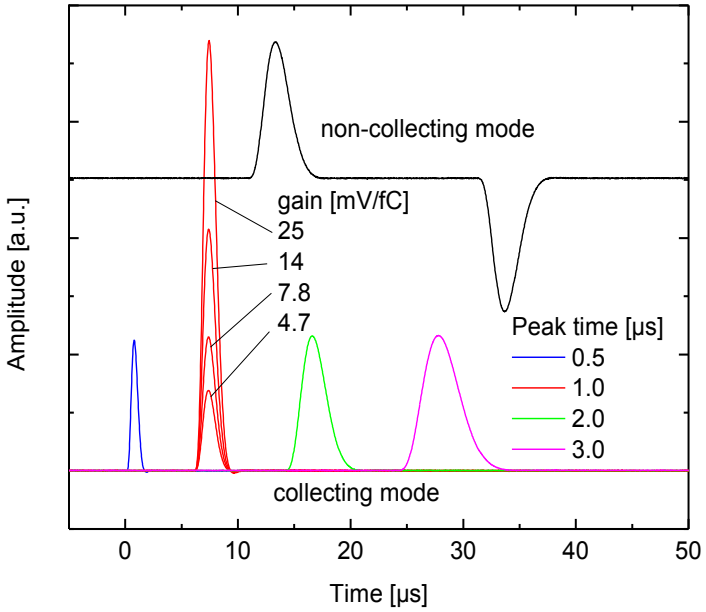


front-end cold
module
serving 128 wires
~ 2.4 W

Analog FE ASIC

Low Noise, Low Power, Long Cryo-Lifetime

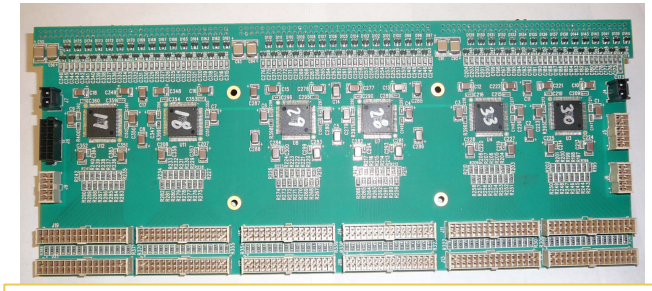




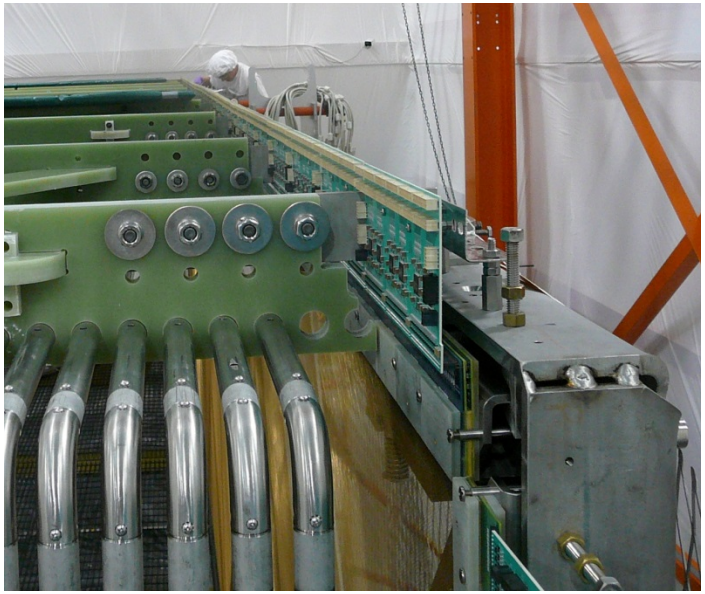
- 16 channels per chip
- Charge amplifier with high-order filter
- Adjustable gain: 4.7, 7.8, 14 and 25 mV/fC (55, 100, 180, 300 fC full dynamic range)
- Adjustable filter time constant (peaking time): 0.5, 1, 2, 3 µs
- Selectable collection/non-collection mode (baseline)
- Selectable DC/AC (100 µs) coupling
- Rail-to-rail analog signal processing
- Band-gap referenced biasing
- Temperature sensor (~3 mV/°C)
- 136 registers with digital interface
- 5.5 mW/channel (input MOSFET 3.6 mW)
- ~15,000 MOSFETs
- Designed for long cryo-lifetime
- Technology CMOS 0.18 um, 1.8 V, 6M, MIM, SBRES

Analog FE ASIC in MicroBooNE

8,256 channels instrumented with FE ASICs

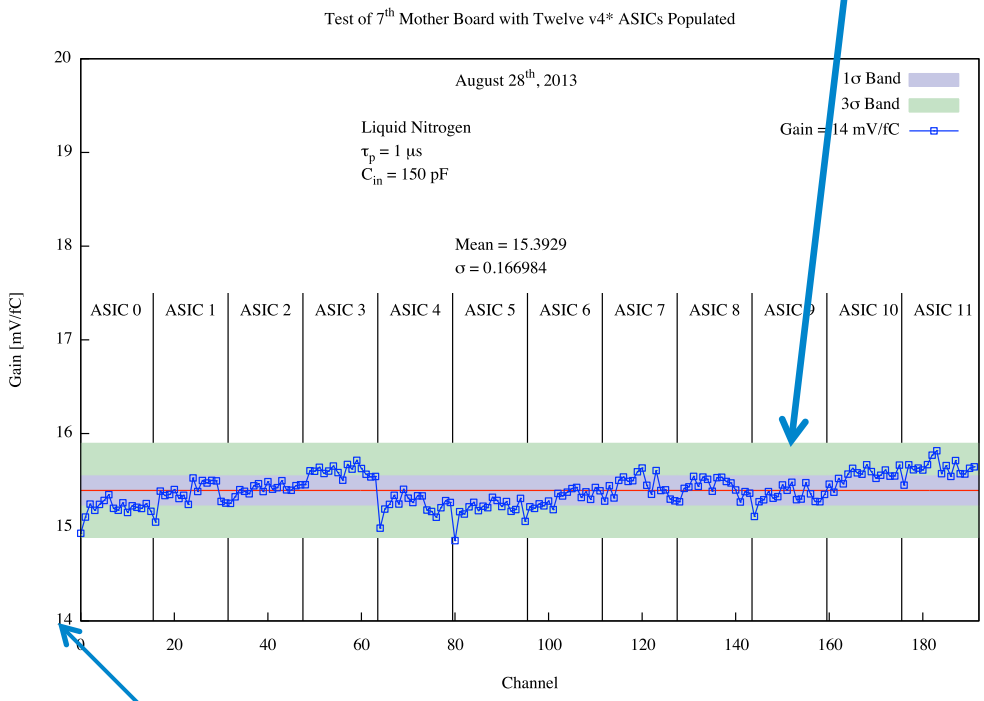


MicroBooNE cold mother board with 12 analog FE ASICs (192 channels)



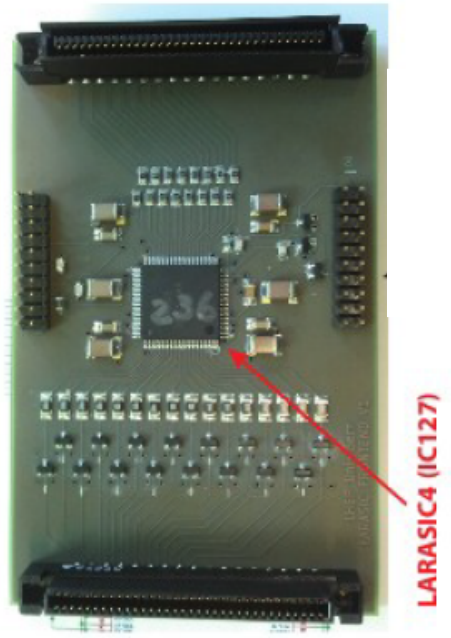
50 cold mother boards (8,256 channels) are installed on MicroBooNE TPC

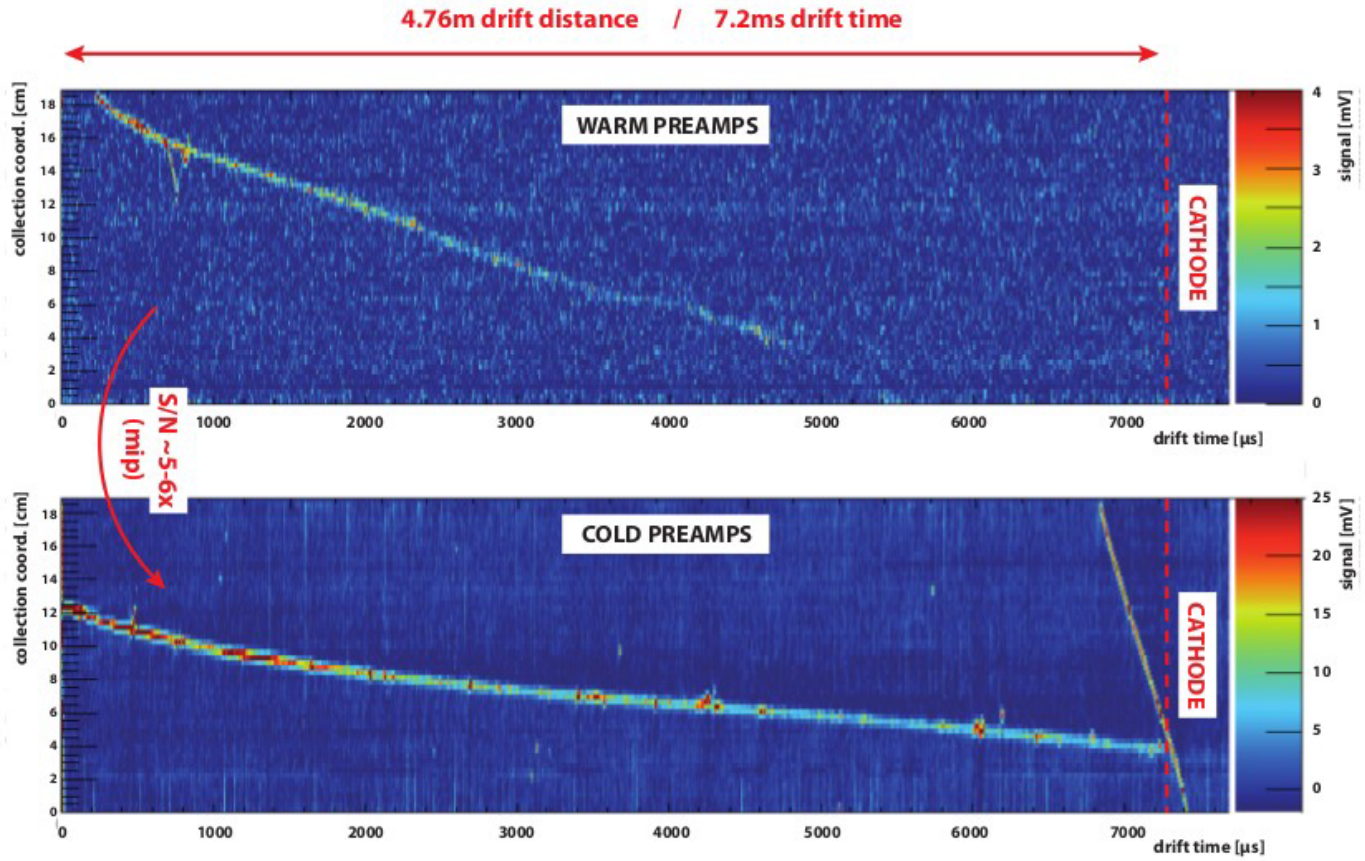
$\sigma_{gain} \approx 1\%$



Note: Offset scale

Analog FE ASIC in ARGONTUBE (Bern)
5-6x Improvement on S/N



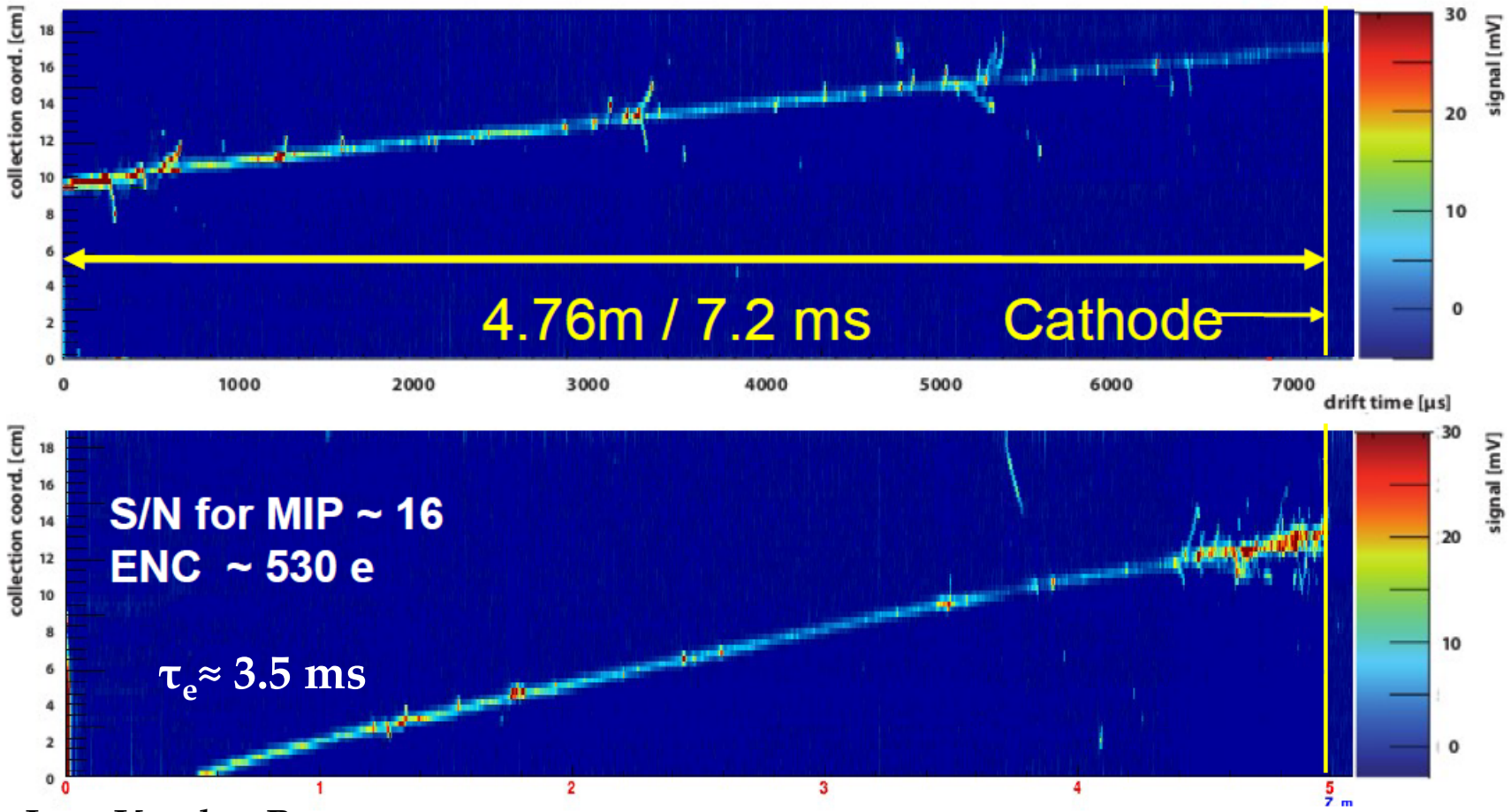


- N.B. different color scale on two plots
- Courtesy of Igor Kreslo @ University of Bern

Testing MicroBooNE cold preamps with ARGONTUBE

~ 5 m long electrons drift in LAR: first time!

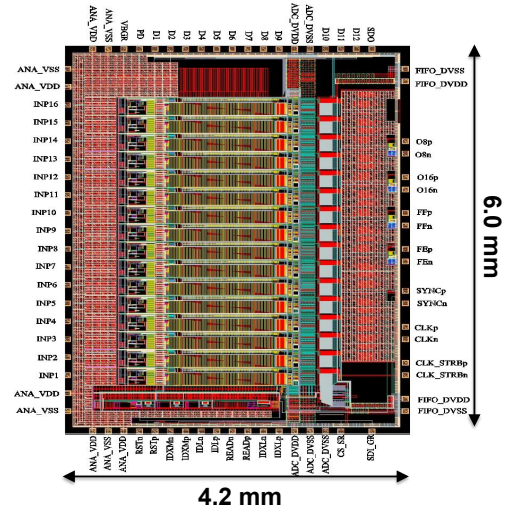
twice MicroBooNE drift lentgh, < ½ E-field

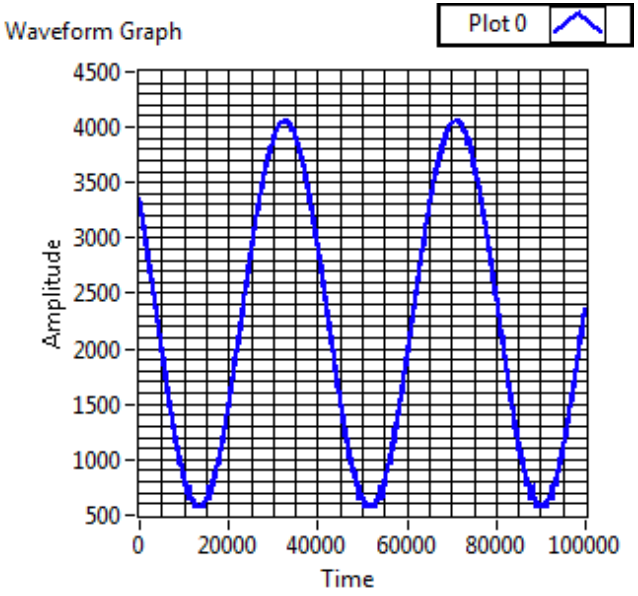


From: Igor Kreslo, Bern

ADC ASIC

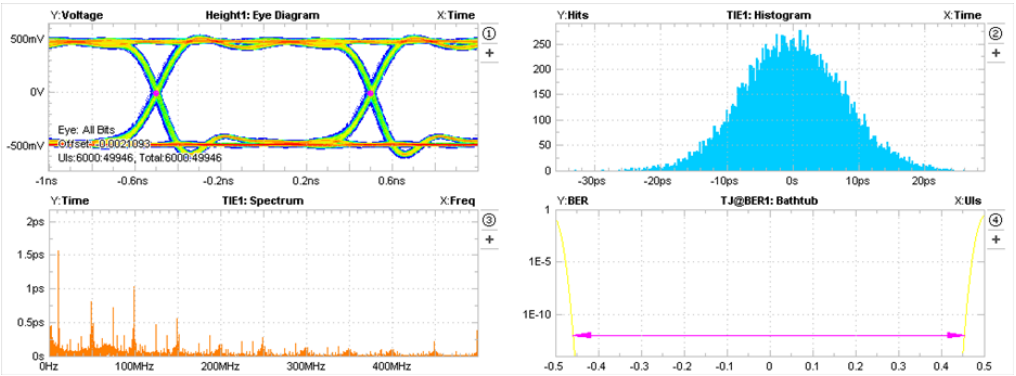
High Speed, Low Power, Long Cryo-Lifetime

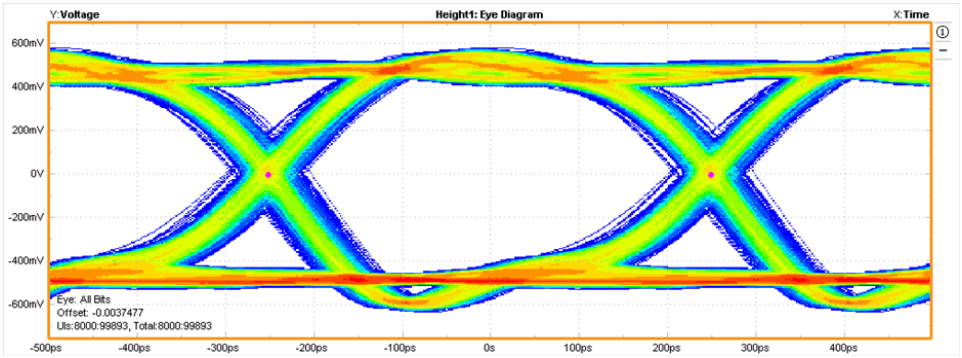




- 16 channels per chip
- Sampling rate up to 2 MS/s
- Resolution 12-bit
- Low power ADC, maximum 5 mW/ch
- Input range 0.2 V to 1.5 V
- Clockless operation, ideal for low noise operation
- Small area favorable for multi-channel system
- Low power mode with < 1 us wake-up
- Adjustable offset
- Multiple options for internal control signals
- ~315,000 MOSFETs
- Designed for long cryo-lifetime
- Technology CMOS 0.18 um, 1.8 V, 6M, MIM, SBRES

Cold FPGA
Qualified FPGA for Cold Operation

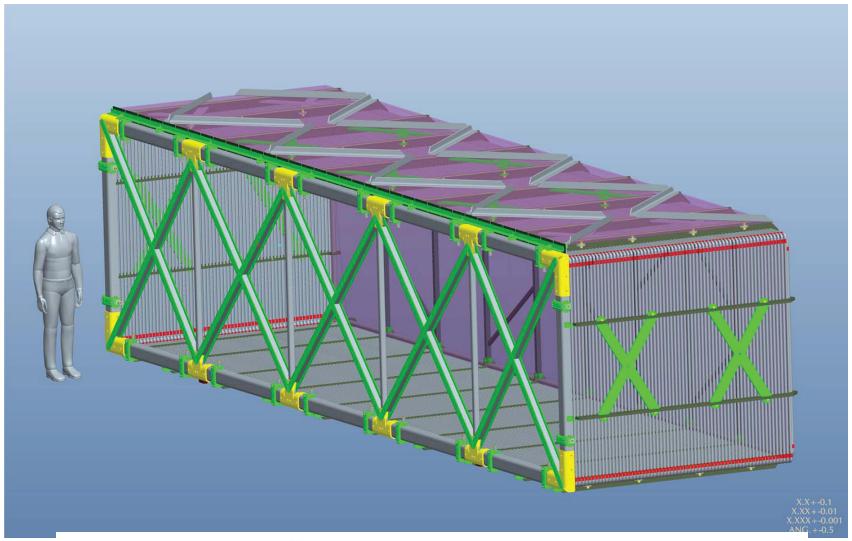


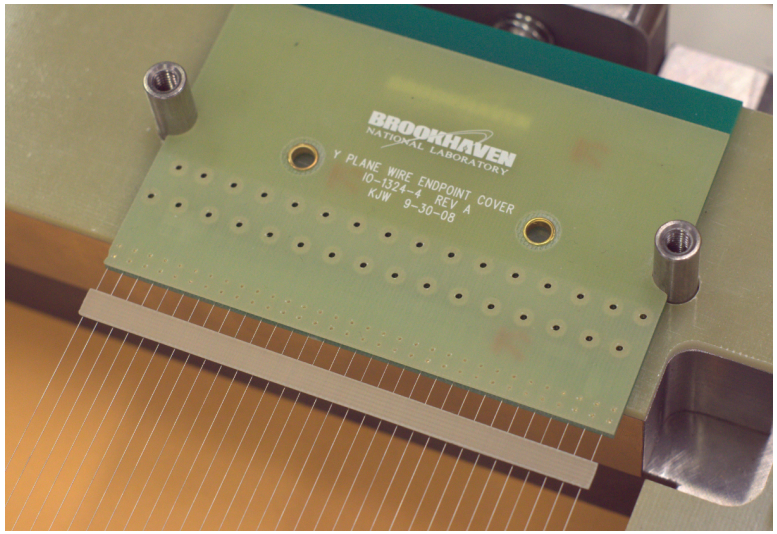


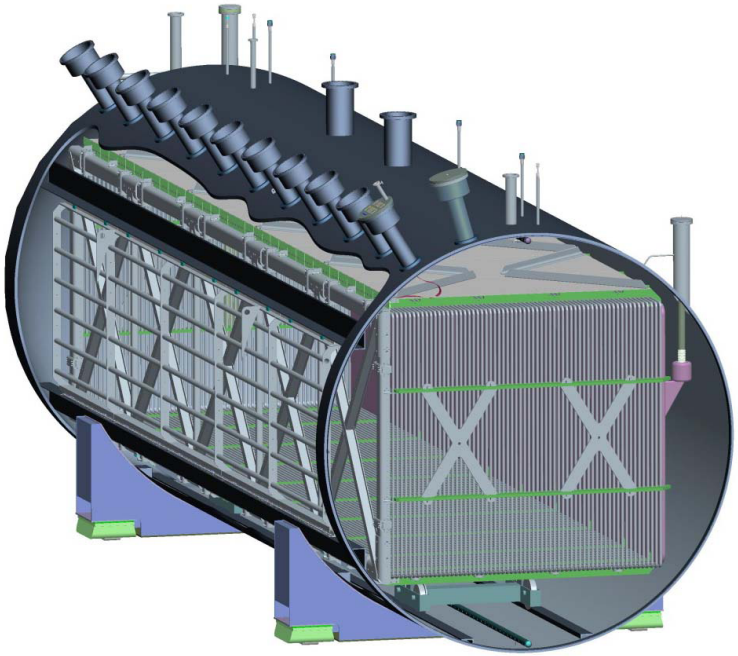
- Test of Cyclone IV GX Transceiver Starter Board in LN_2
  - Transceiver works well at both 1Gbit/s and 2Gbit/s
  - Height
    - 839mV @ 1Gbit/s
    - 823mV @ 2Gbit/s
  - Eye Width
    - 914ps @ 1Gbit/s
    - 357ps @ 2Gbit/s
  - On board SRAM works with BIST
    - 18-Mb SRAM from ISSI IS61VPS102418A-250TQL
    - Cyclone IV GX is running with Nios II processor and utilization of ~80% fabric resources

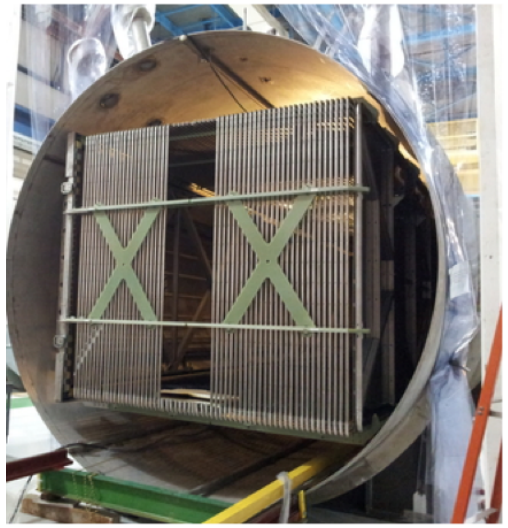
TPC & Electronics Design in Experiments of SBN & LBN

MicroBooNE TPC Designed by BNL

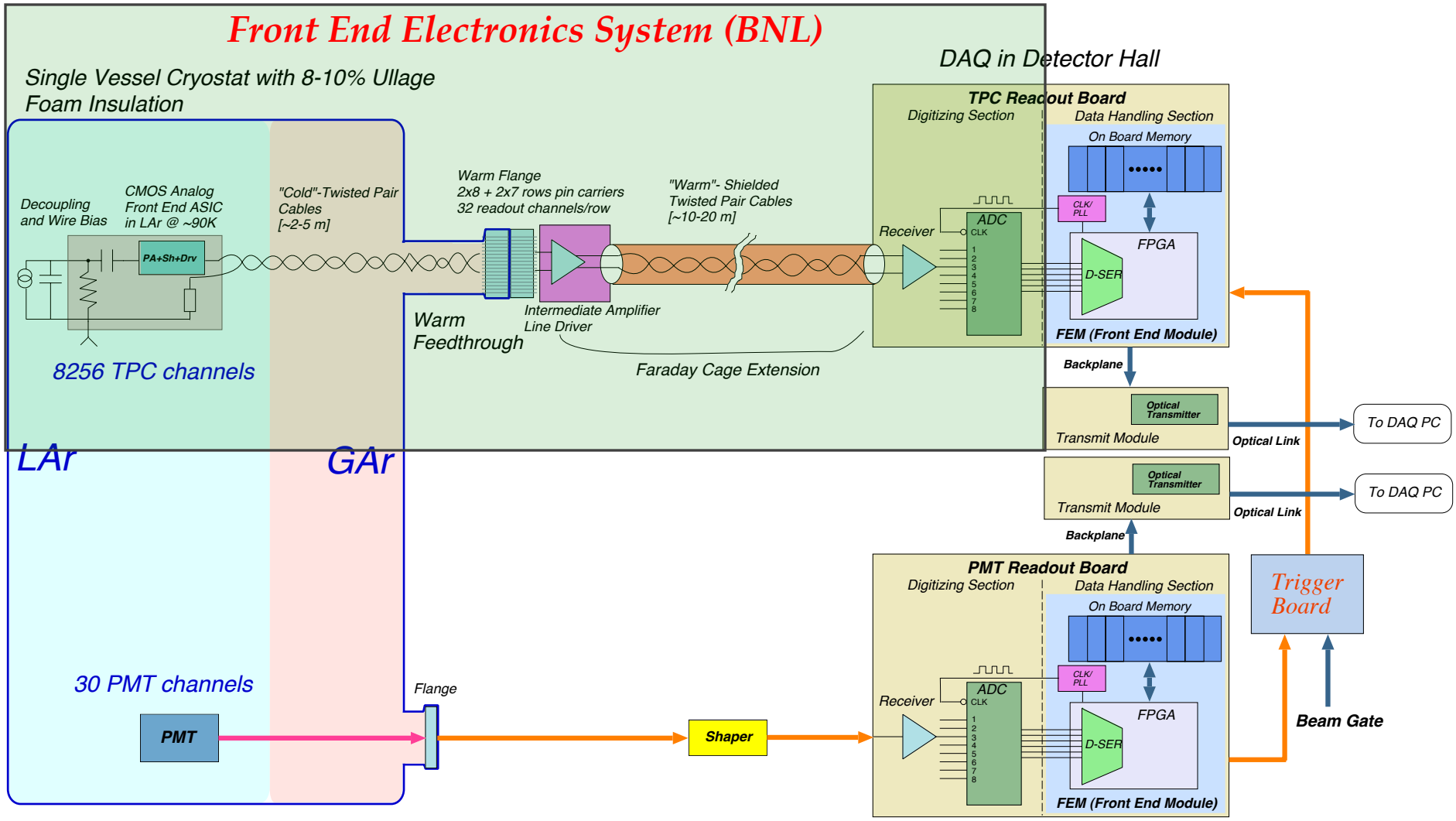




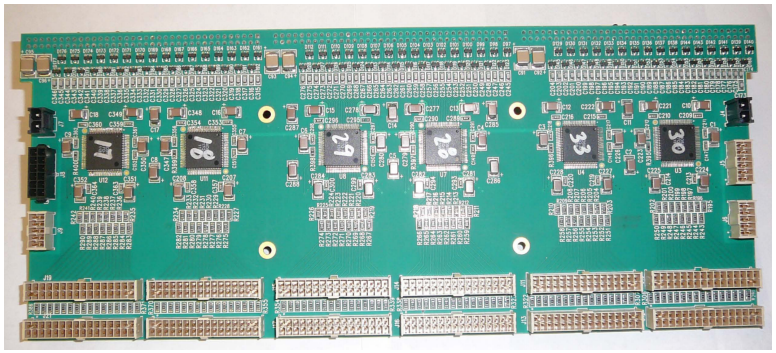




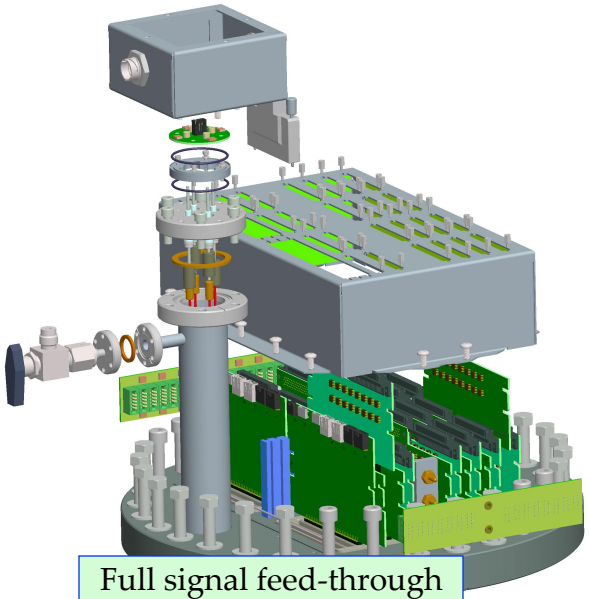
MicroBooNE Electronics Built by BNL



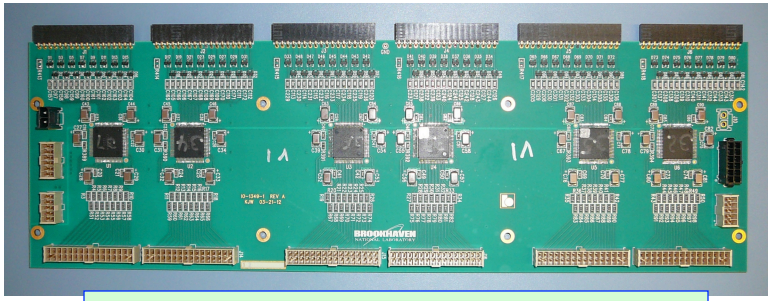
MicroBooNE Cold Electronics & Feed-through



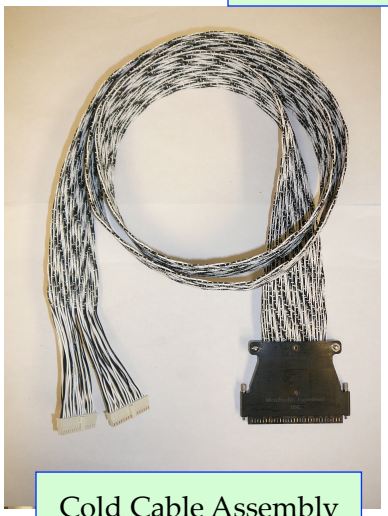
Horizontal cold motherboard with 12 ASIC chips (192 channels) populated



Full signal feed-through assembly drawing



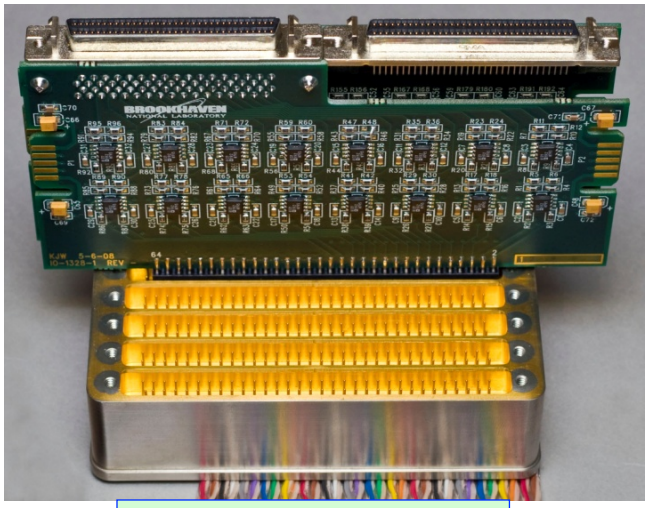
Vertical cold motherboard with 6 ASIC chips (96 channels) populated



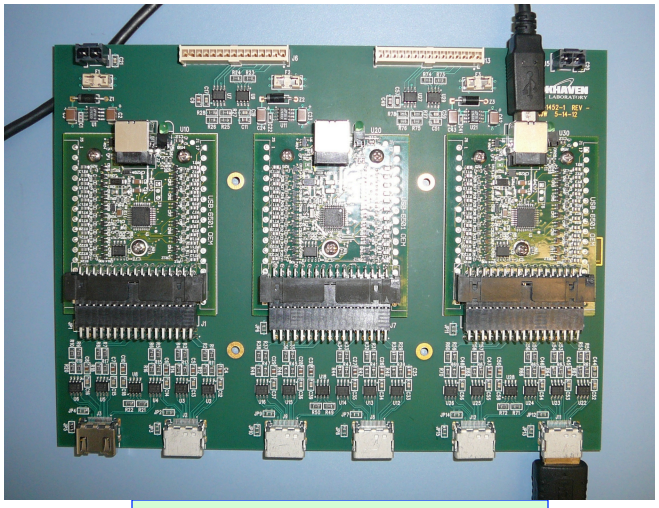
Cold Cable Assembly

Warm Cable Assembly

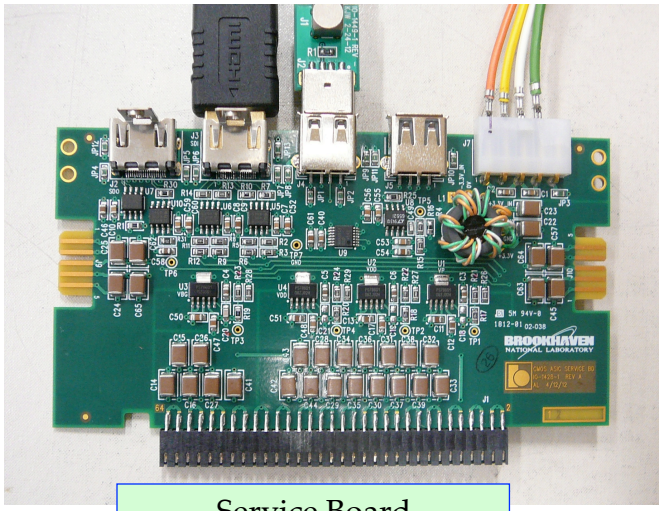
MicroBooNE Warm Electronics



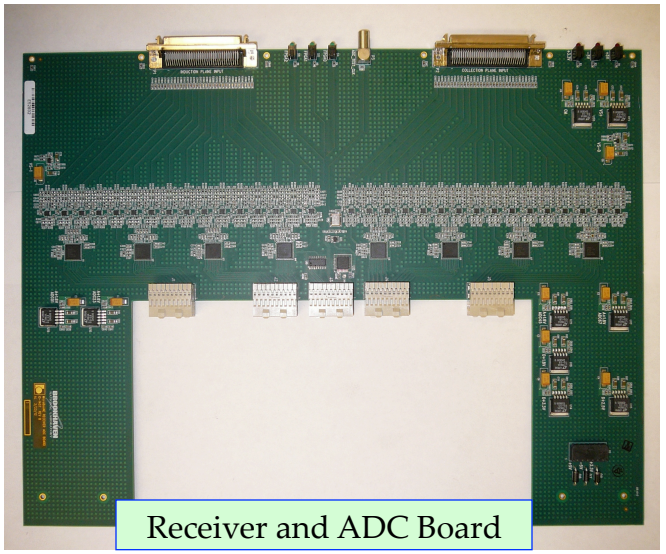
Intermediate Amplifier



ASIC Configuration Board

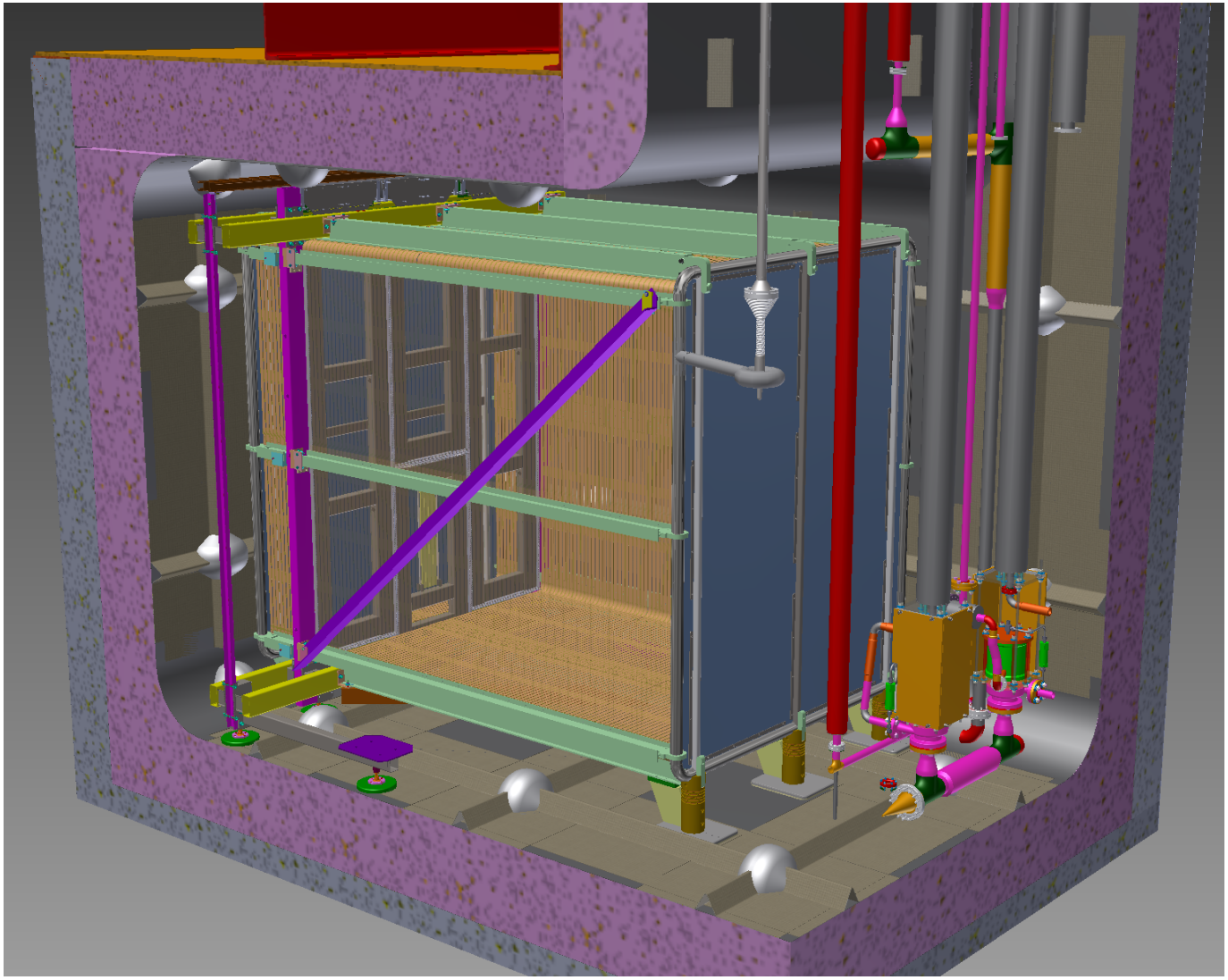


Service Board

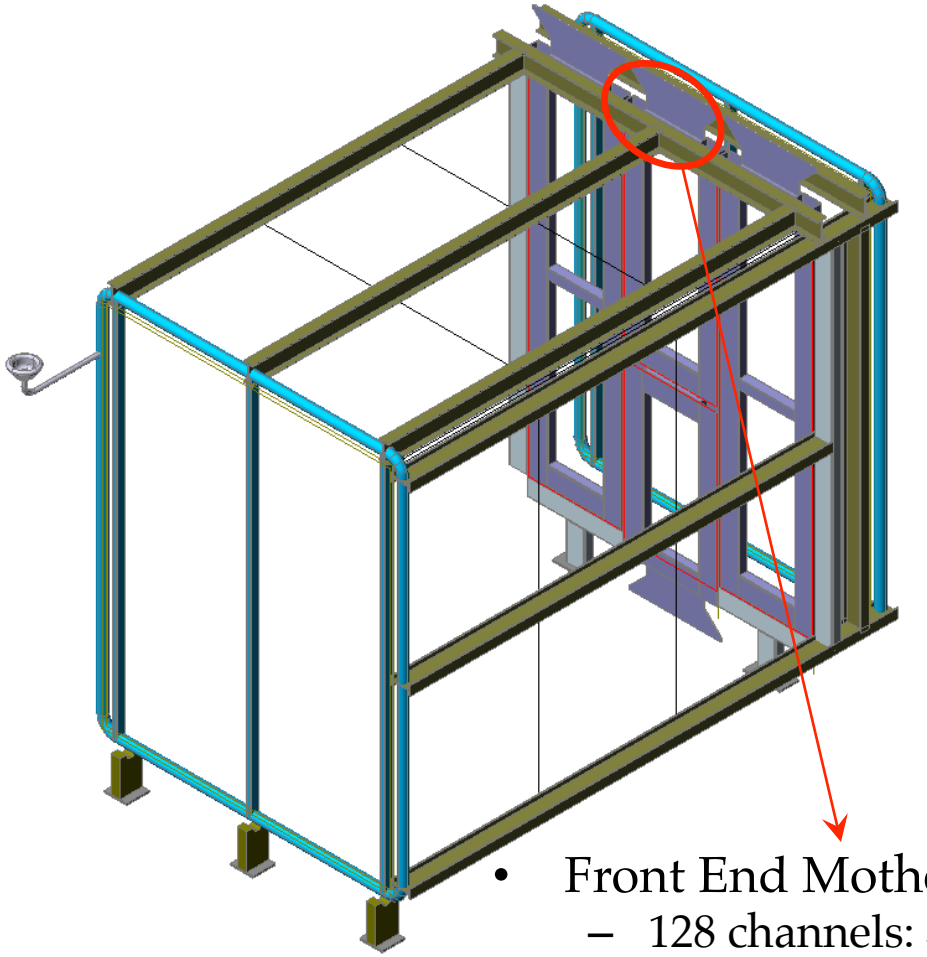


Receiver and ADC Board

LBNF 35 Ton TPC & Electronics Designed by BNL



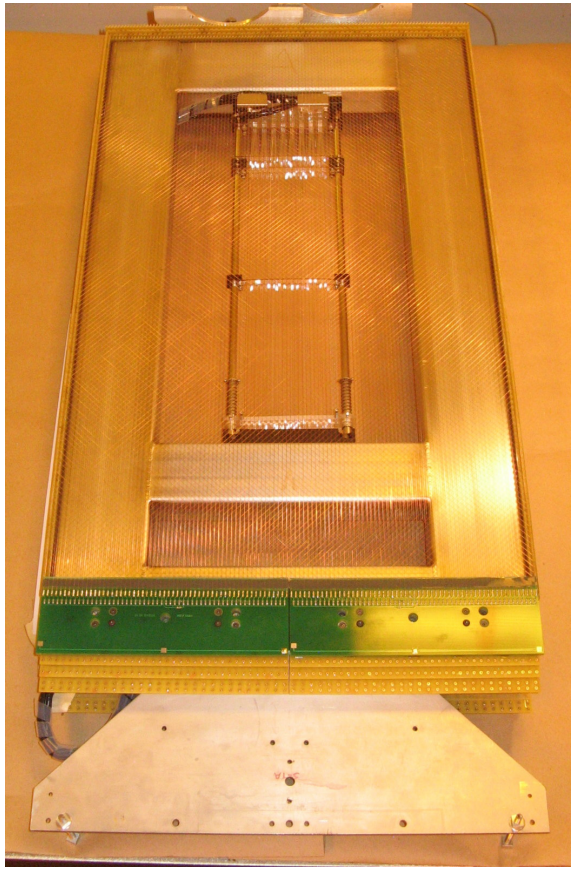
LBNF 35 Ton TPC & Electronics

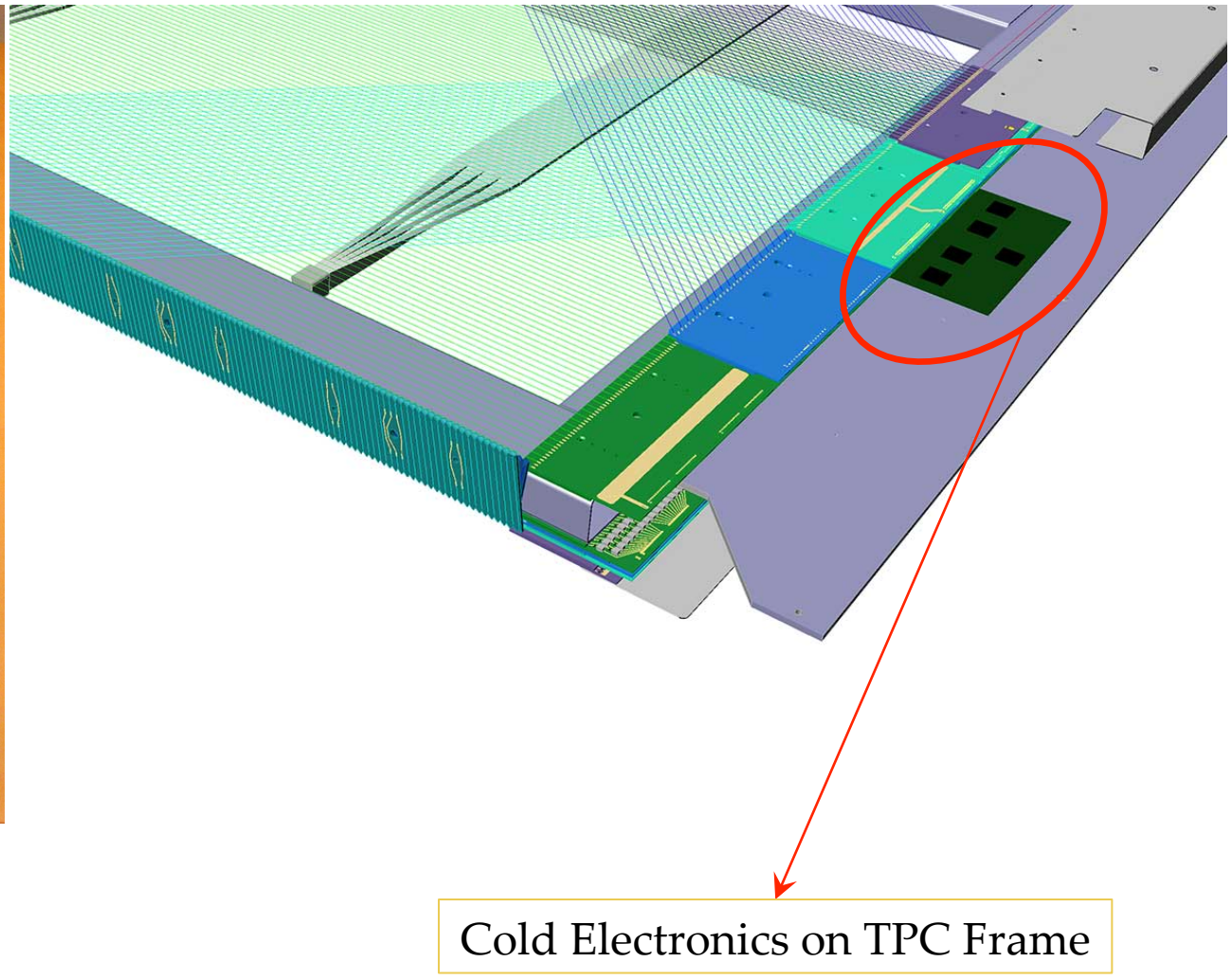


- 4 APA – 2048 wires total
  - Each APA has 512 wires
  - 224 X wires @ 4.5 mm pitch
  - 144 U wires @ 4.9 mm pitch
  - 144 V wires @ 5.0 mm pitch

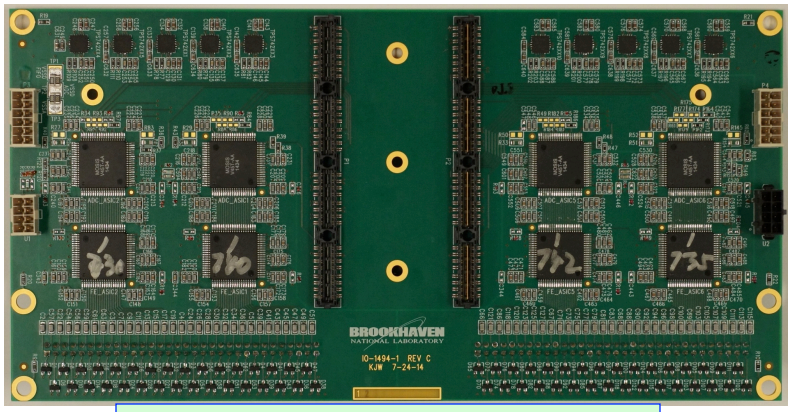
- Front End Mother Board
  - 128 channels: 56 X, 36 U, 36 V
  - 4 mother boards mounted on one end of the APA frame

LBNF 35 Ton TPC – Wire Wrapping

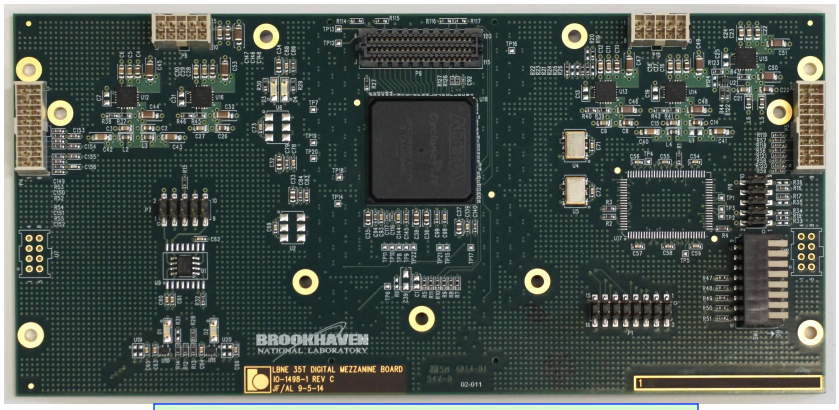




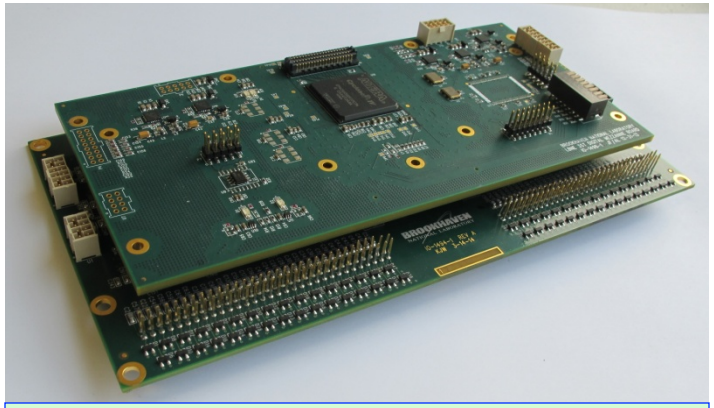
LBNF 35 Ton Cold Electronics



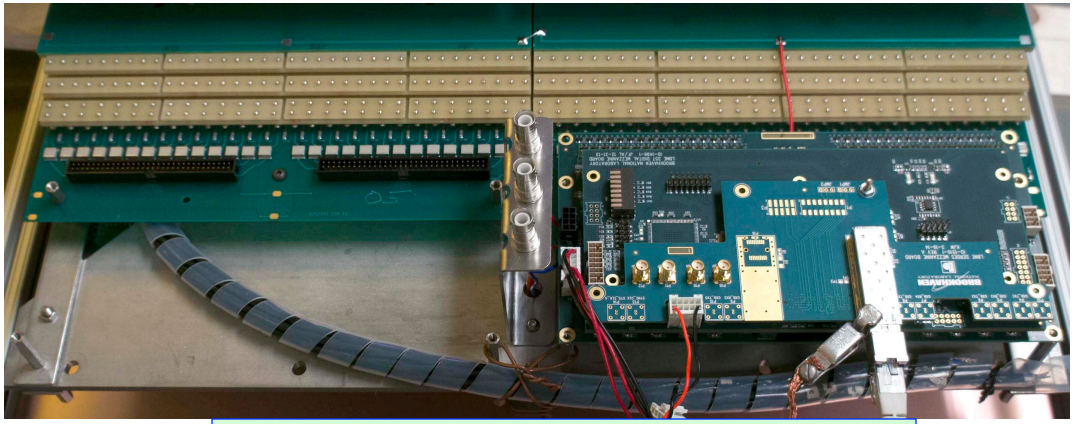
Analog Mother Board



FPGA Mezzanine

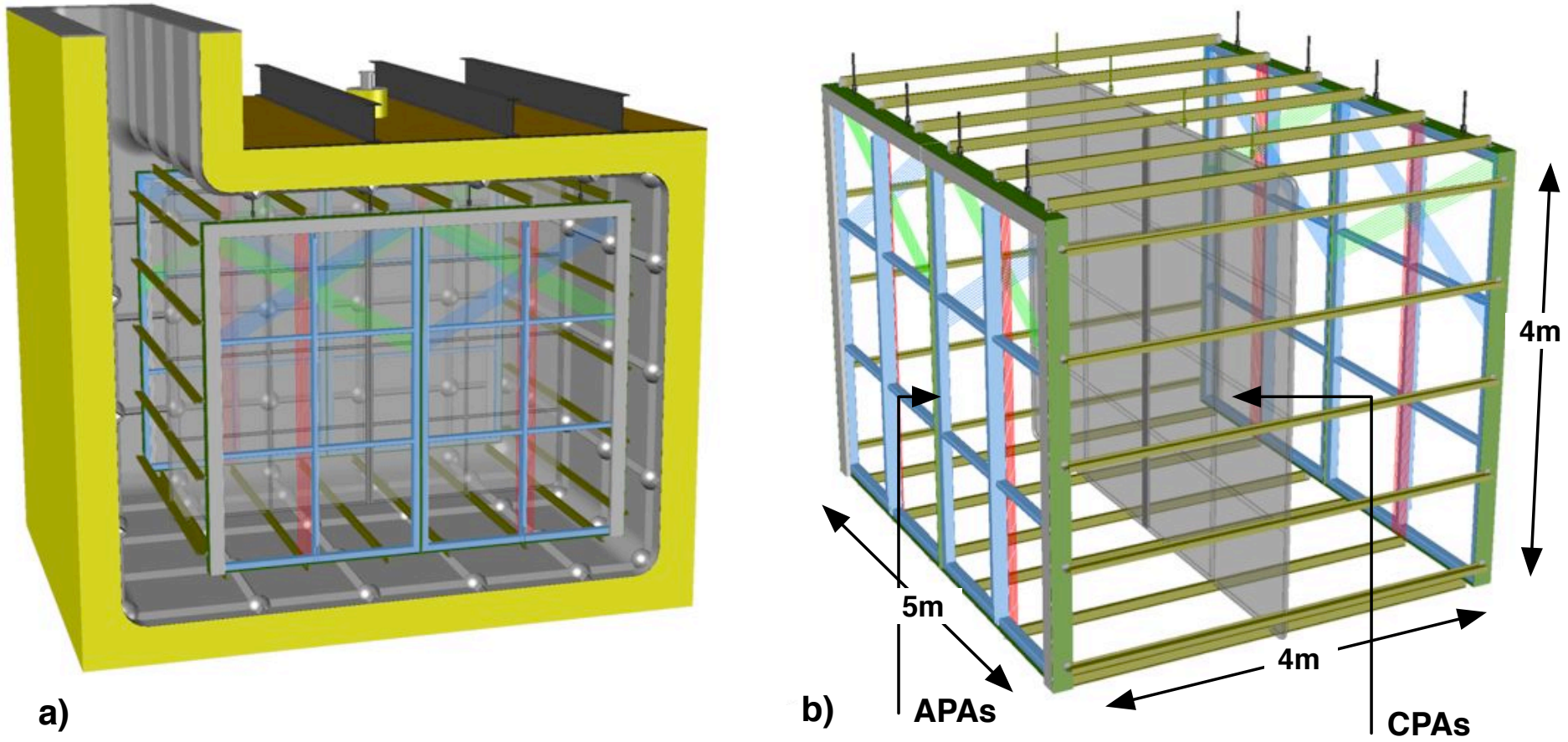


Front End Mother Board Assembly



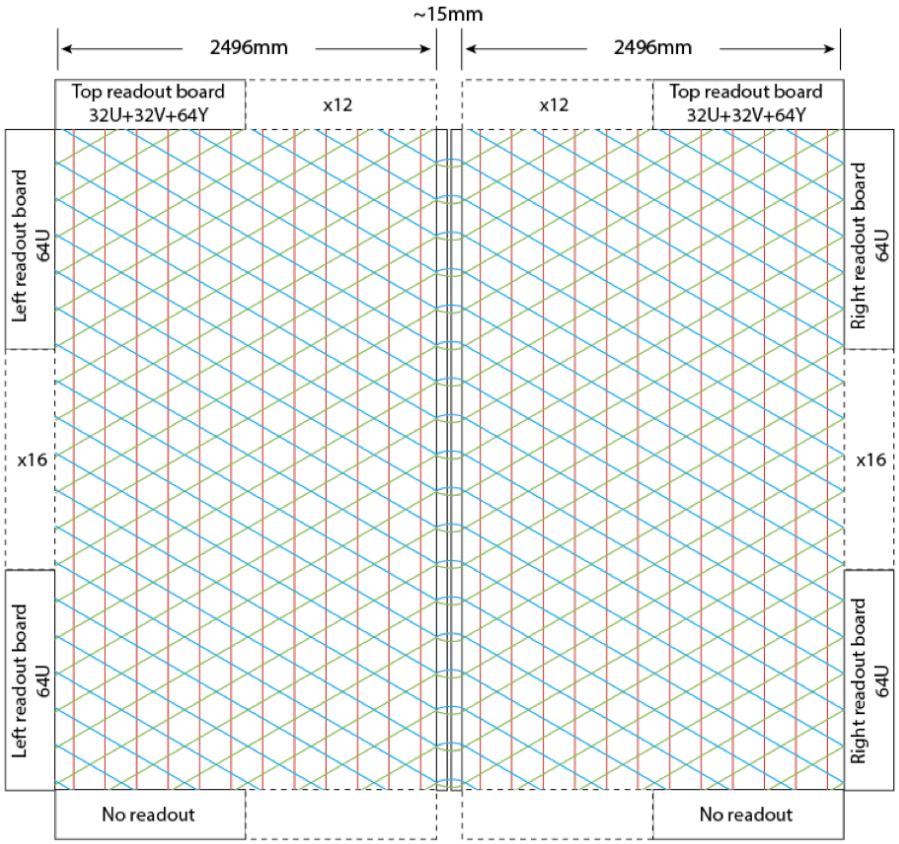
FEMB test with APA

LAr1-ND TPC & Electronics



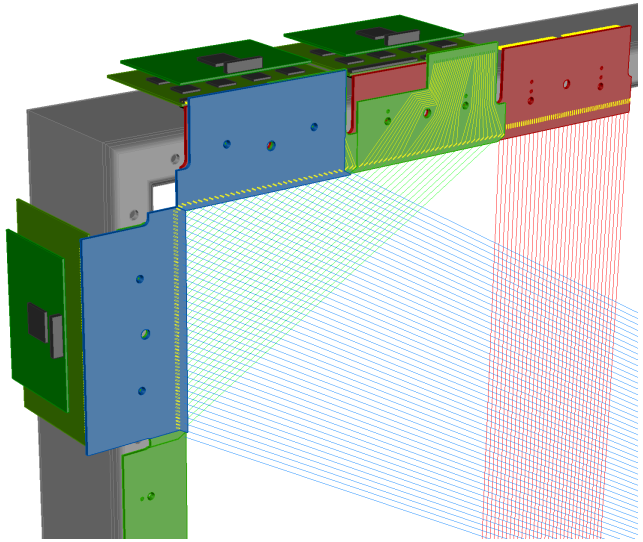
- LAr1-ND TPC: 4 APAs and 2 CPA

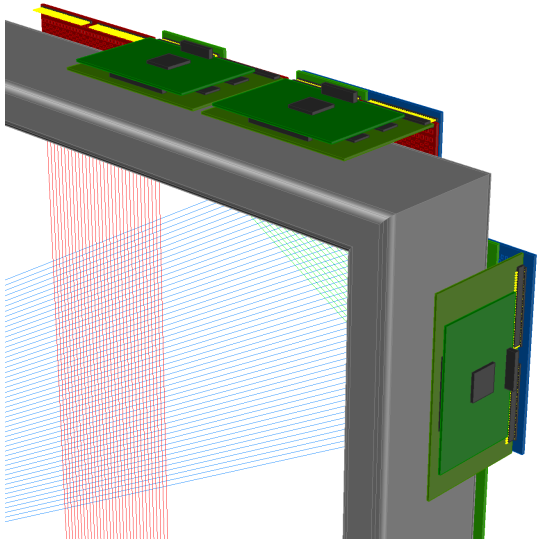
LAr1-ND TPC & Electronics

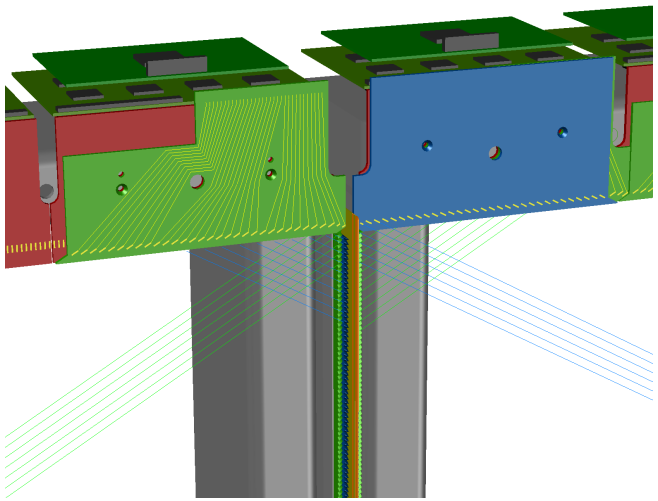


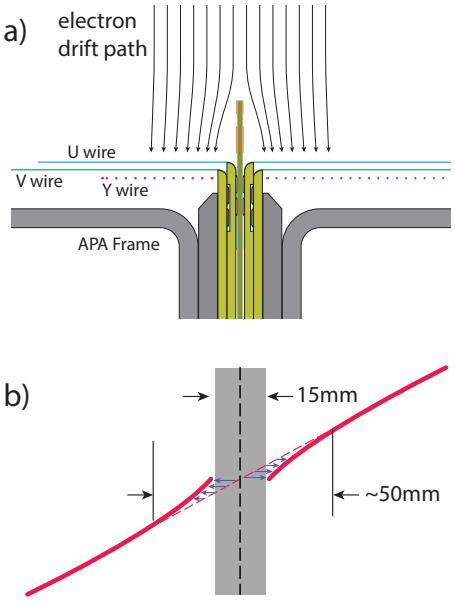
- ***2 bridged APAs***
  - 5,632 channels
  - 26 top mother boards x 128-ch per board
  - 36 side mother boards x 64-ch per board
- LAr1-ND TPC
  - 11,264 readout channels from 4 APAs
  - 4 cold cable bundles to 4 signal feed-throughs

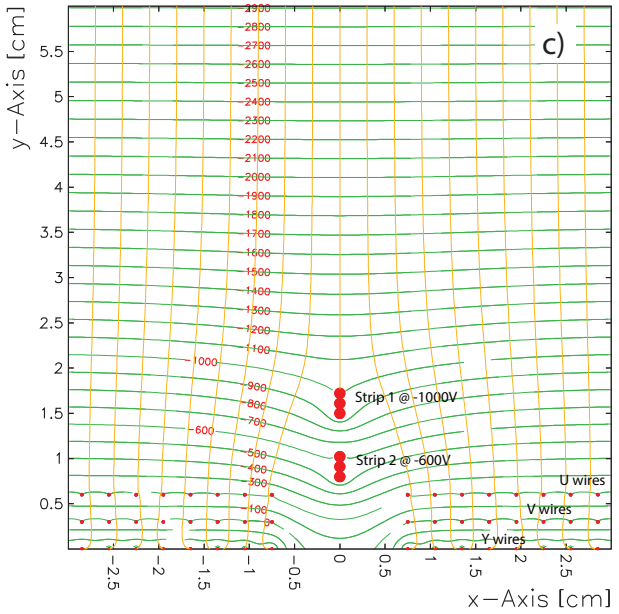
LAr1-ND TPC Design



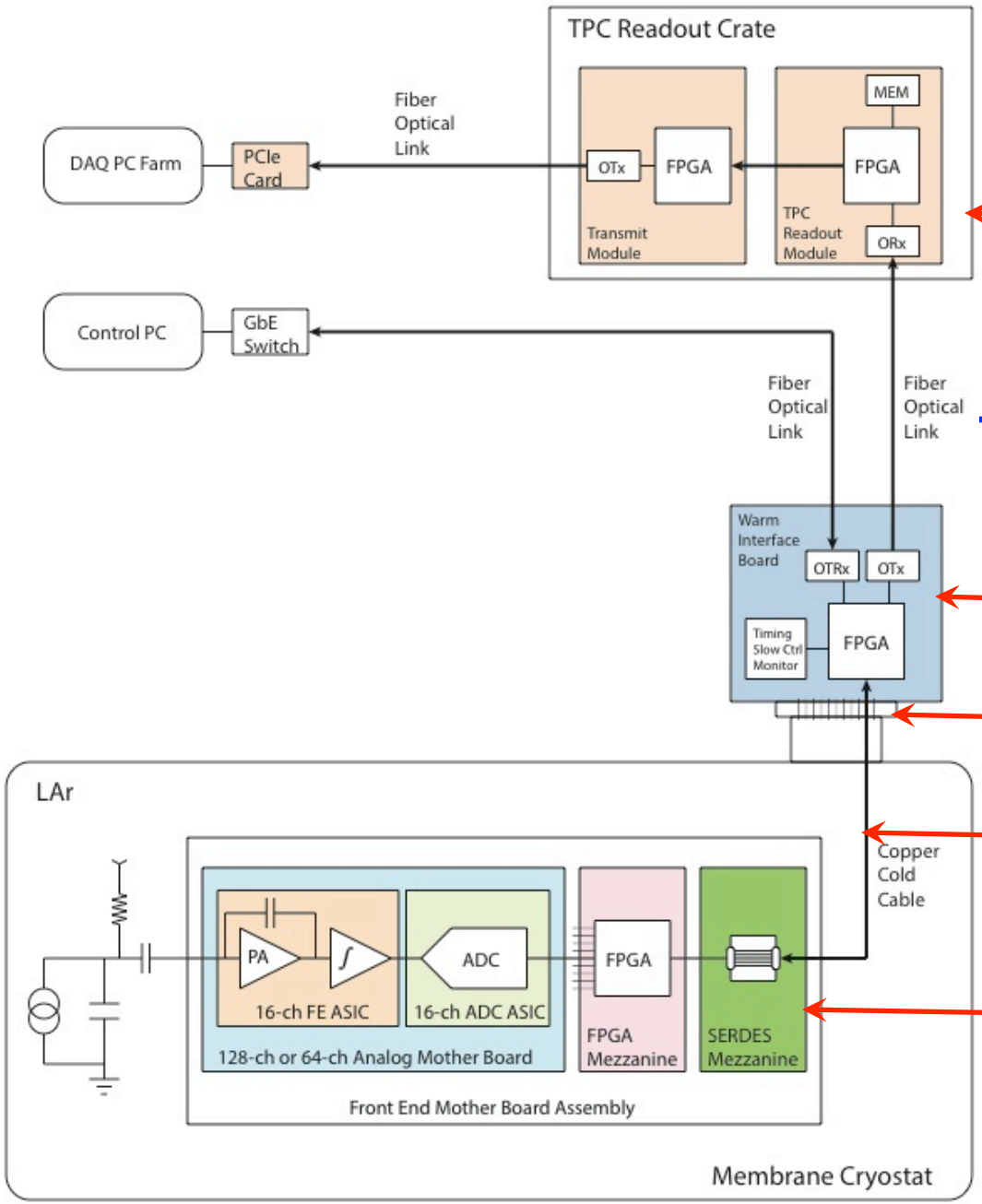








LAr1-ND TPC Electronics



TPC Readout Electronics

Back End Electronics

BNL: Front End Electronics

Warm Interface Electronics

Signal Feed-through

Cold Cable

Cold Electronics

Summary

- R&D of CMOS cold electronics started in 2008
  - Analog FE ASIC was the first one developed, following by ADC ASIC development, studies of cold regulator and FPGA etc.
  - In parallel, studies of CMOS lifetime and reliability at 77 K have been conducted
    - *"LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling," IEEE Trans. on NSci, 60, No: 6, Part: 2, p4737(2013)*
- Cold electronics design is performed jointly with the TPC electrode design for different experiments
- As a part of our future program, finer segmentation electrodes and readout will be explored (planar anodes instead of wires).
- **TPC and Cold Electronics Development Team at BNL:**
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  - Physics Department – (P); Instrumentation Division – (I)