Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

Mathis Kolb
on behalf of the ATLAS LAr Collaboration

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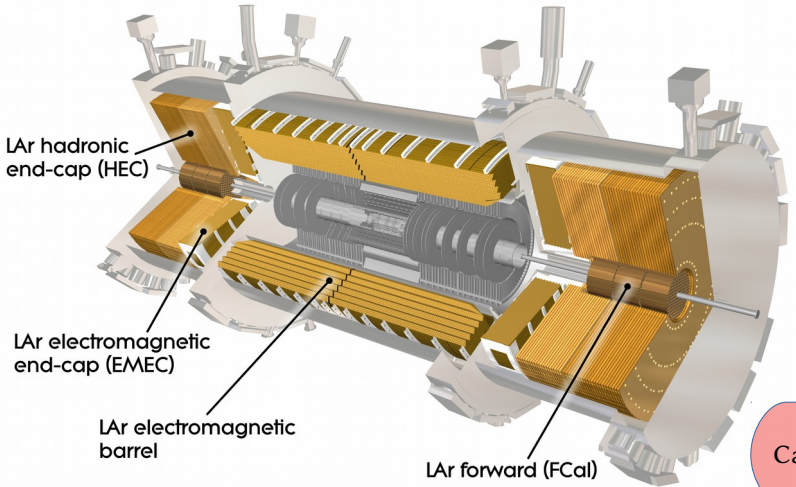
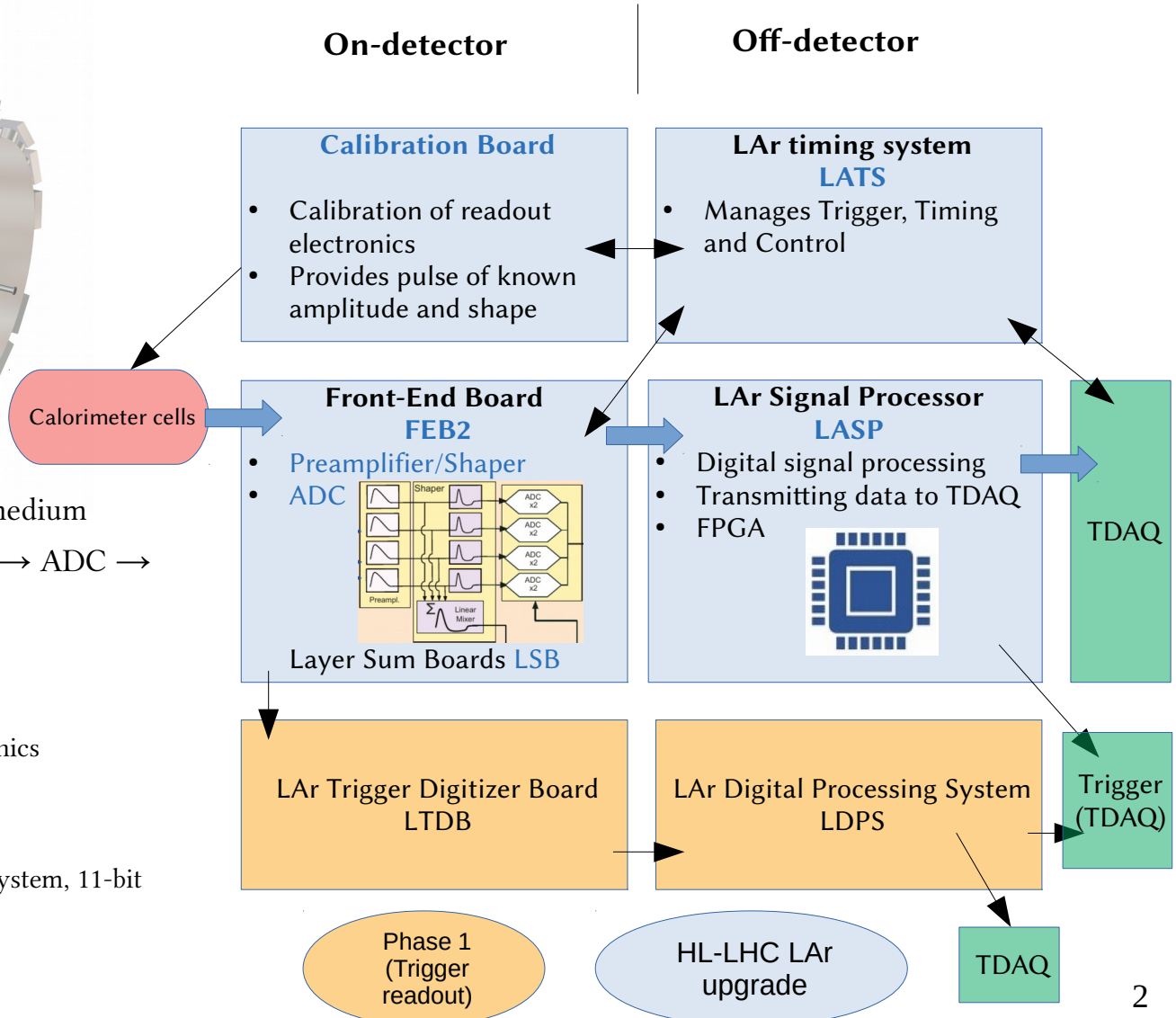
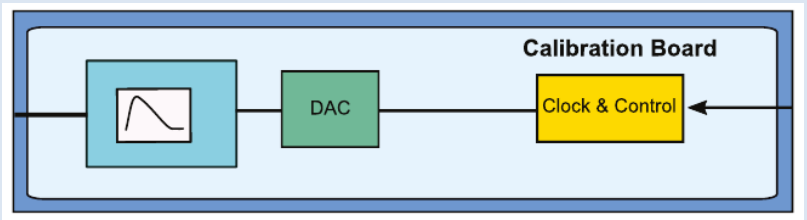
Liquid Argon Calorimeter upgrade



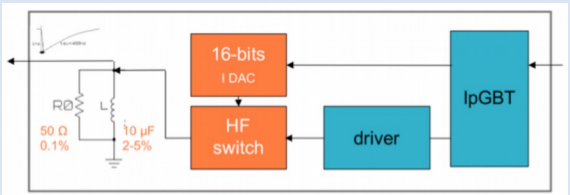
- Sampling calorimeter with liquid argon as active medium
- Signal: Calorimeter Pulse ⟶ Preamplifier-Shaper ⟶ ADC ⟶ Off-detector FPGA (digital filtering)
- High linearity, low noise
- HL-LHC LAr upgrade
  - Main readout chain: On-detector + Off-detector electronics
  - Radiation tolerance
  - Compatibility with updated ATLAS TDAQ system
  - Wide dynamic range: 16-bit dynamic range, two gain system, 11-bit precision
  - Transmit all data off-detector at 40 MHz
  - Updated during LS3



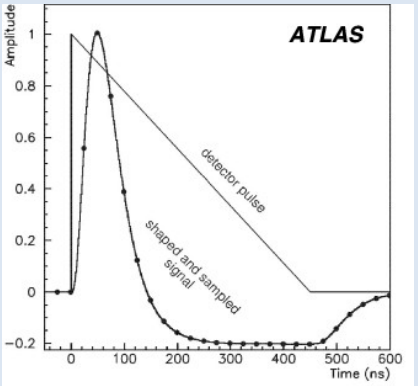
Calibration board

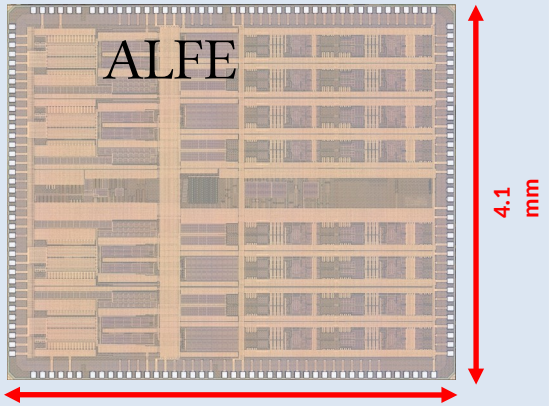


- Provides pulse of known amplitude and shape
- 2 ASICs
  - Claroc: High-frequency switch, analog, 180nm XFab
  - Ladoc: DAC, digital, 130nm TSMC
- Characteristics
  - 16 bit dynamic range
  - Linearity < 0.1%
  - Radiation hard up to 180 kRad
- 130 boards with 128 channels each
- 4 channels / ASIC



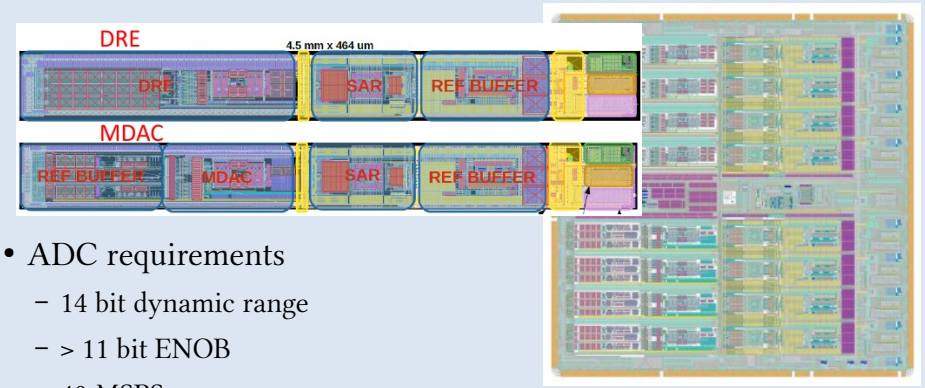
Preamplifier-Shaper





- Analog signal processing
  - Amplification, CR-RC2 shaping, split on Hi/Low gain (overlapping), analog sums for trigger
- 16 bit dynamic range, gain ratio ~23, 130nm TSMC
- Highly configurable via I2C
- Final prototype submitted for fabrication
- ALFE: ASIC for EM and FCAL
  - Full density 4 channels
  - Pre-Amplifier + Shaper
- HPS: ASIC for HEC
  - Pre-Amplifier replaced by Pre-Shaper

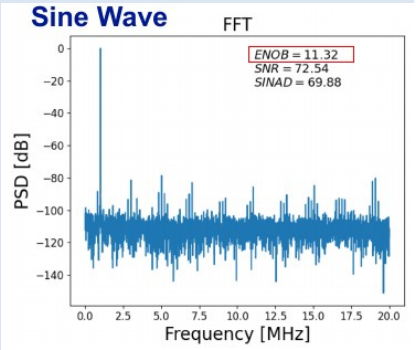
ADC



- ADC requirements
  - 14 bit dynamic range
  - > 11 bit ENOB
  - 40 MSPS
  - Low power < 100 mW / channel
  - Radiation hardness

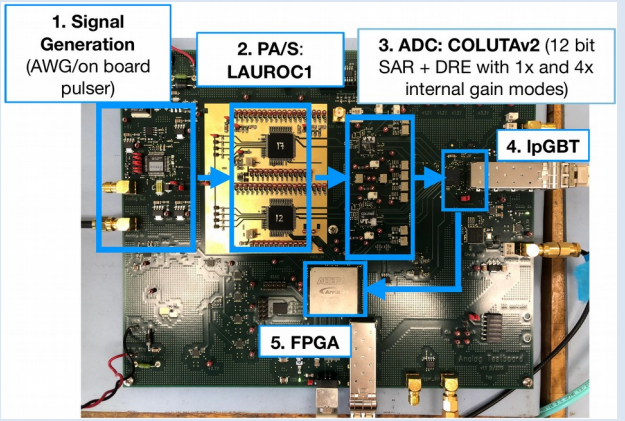
TID [kGy]	Si-NIEL [n_{eq}/cm^2]	SEE [$\mathrm{h}_{>20\mathrm{MeV}}/\mathrm{cm}^2$]
1.3(1.5)	$4.3 \times 10^{13}(2)$	$1.1 \times 10^{13}(3)$

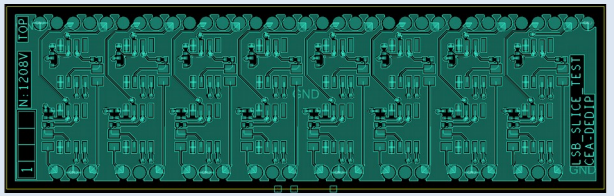
- COLUTA ADC
  - 65nm TSMC
  - MDAC ⟶ 12-bit SAR, digitizes at 40 MHz with two gains
  - 4 channels, 8 ADC/ASIC
  - Low noise and good long-term stability
  - Highly configurable via I2C



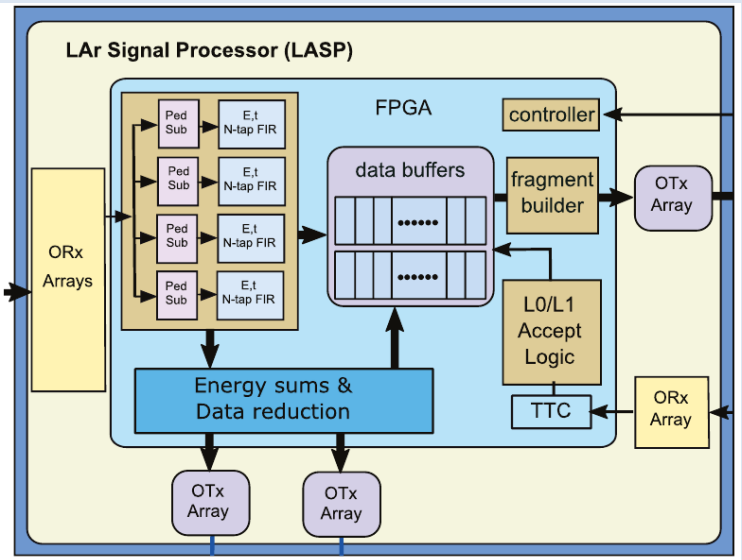
Front-End-Board FEB2

- Analog testboard
  - 2 channels
  - Pre-prototype ASICs
  - Full readout chain working
- Slice testboard
  - 32 channels
  - Updated ASICs
  - Demonstrate multi-channel performance
  - Control and readout on all channels tested
- Layer Sum Board
  - Connects main readout with trigger readout
  - Summing: main readout granularity ⟶ coarser trigger granularity



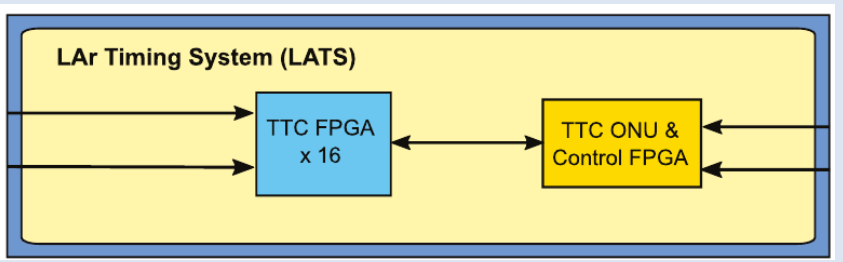


LAr Signal Processor LASP

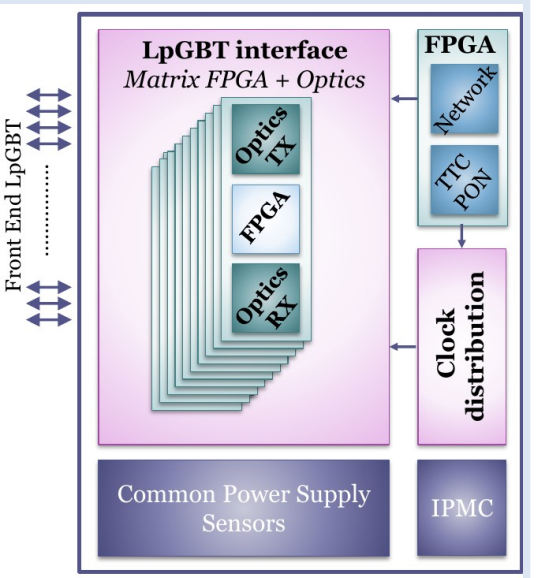


- Data from FEB2, ~512 channels / LASP
- Digital filtering
- Provides signal energy and time
- Buffering and transmission to TDAQ
- ATCA main blade (2 FPGAs)
- RTM (controller FPGA + optical tranceivers)
- Pre-prototype production started

LAr Timing System LATS



- Configuration, monitoring and Trigger Timing and Control (TTC) distribution for on-detector boards
- LATOURNETT: ATCA board
- Test of LATS concept with Cyclone10 devkit
  - FMC Dual SFP
  - Hardware interfaces validated



Backup

Readout scheme