The ABC130 ASIC Design for the ATLAS Silicon Strip Update

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CERN-PH-ESE-FE

On behalf of the ITK-Strips Collaboration in the ATLAS experiment

Specifications, Design & Test Team

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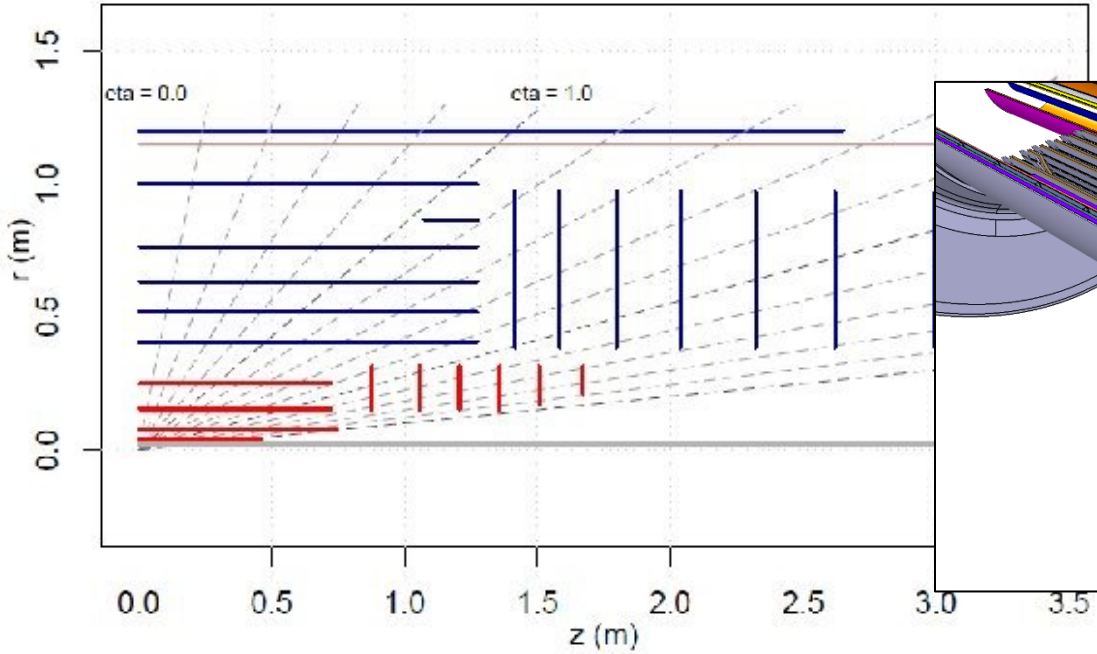
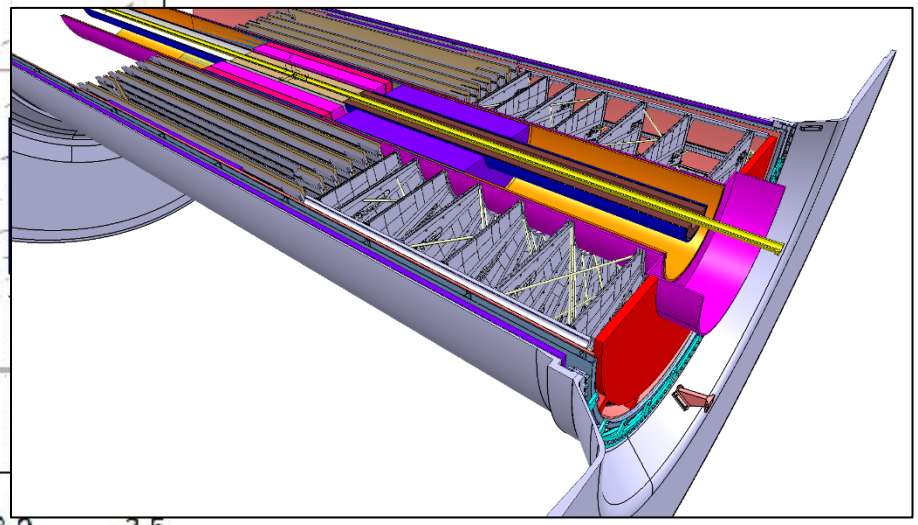
- Gregory Farquhar (Oxford University (UK))
- Kazuki Todome (Tokyo University of Technology (JP))

ITK Strips Layout



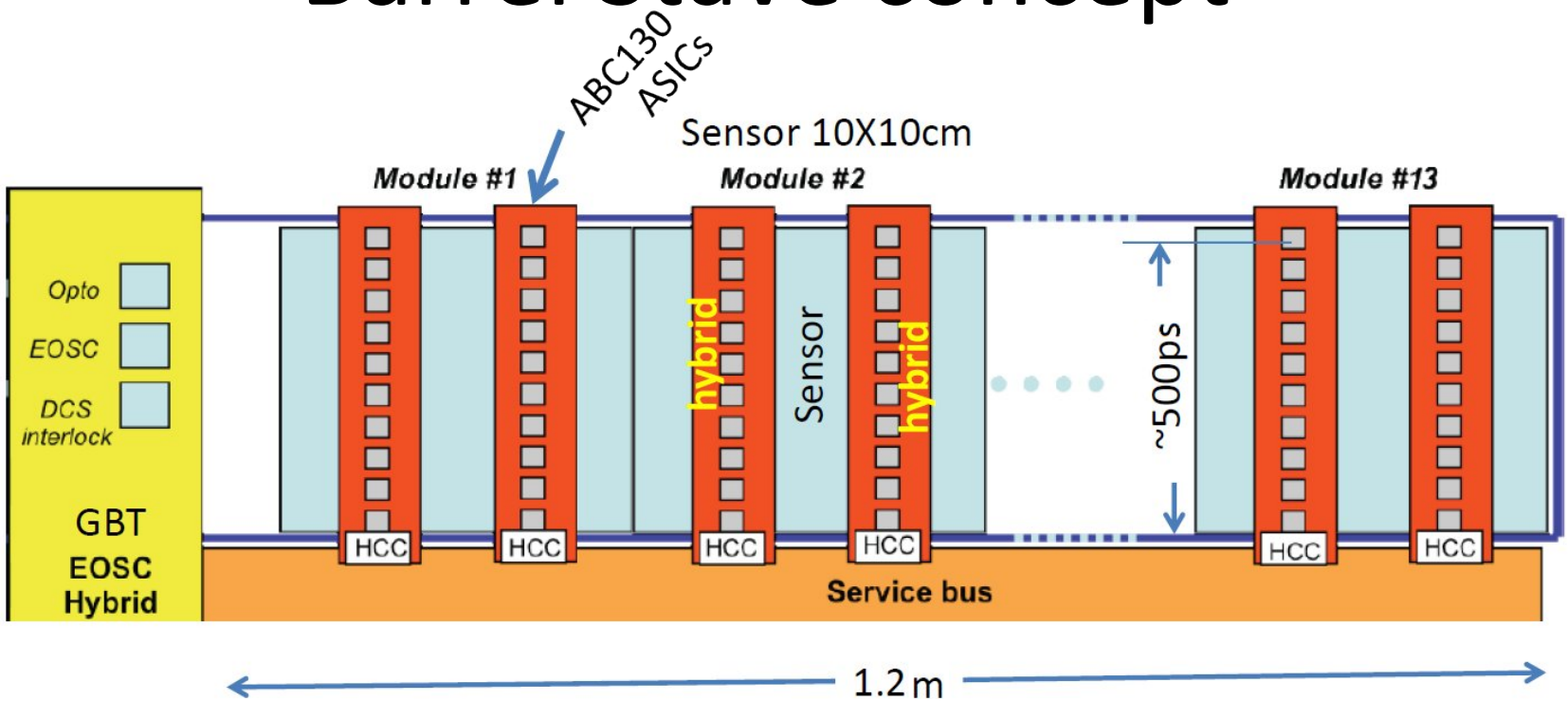


* Not Final *

Endcap	Totals	After Yield Totals
Modules	8064	**8552**
Hybrids	13440	**15515**
ASICs	118272	**131699**

Barrel	Totals	After Yield Totals
Modules	12784	**13557**
Hybrids	18400	**20489**
ASICs	184000	**225377**

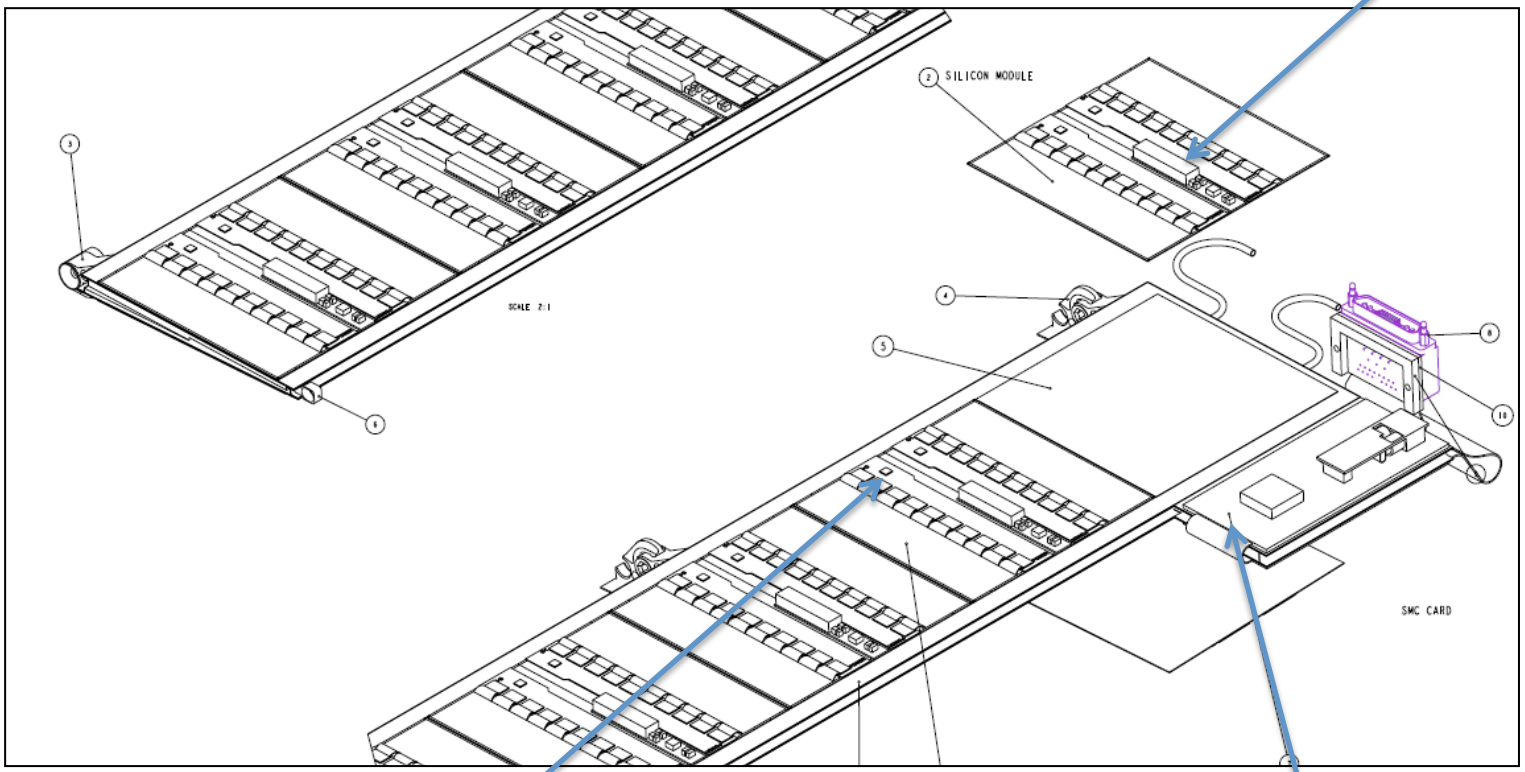
Barrel Stave concept



- Barrel "short" strips stave
  - 26 sensors of 10x10cm
  - 2 hybrids per sensor
  - 52 hybrids in stave, each with 10 ABC130 and single HCC
- Sensor:
  - 4 columns of strips
  - 1280 strips in a column
  - 74.5 um pitch
  - 2.5 cm strip length

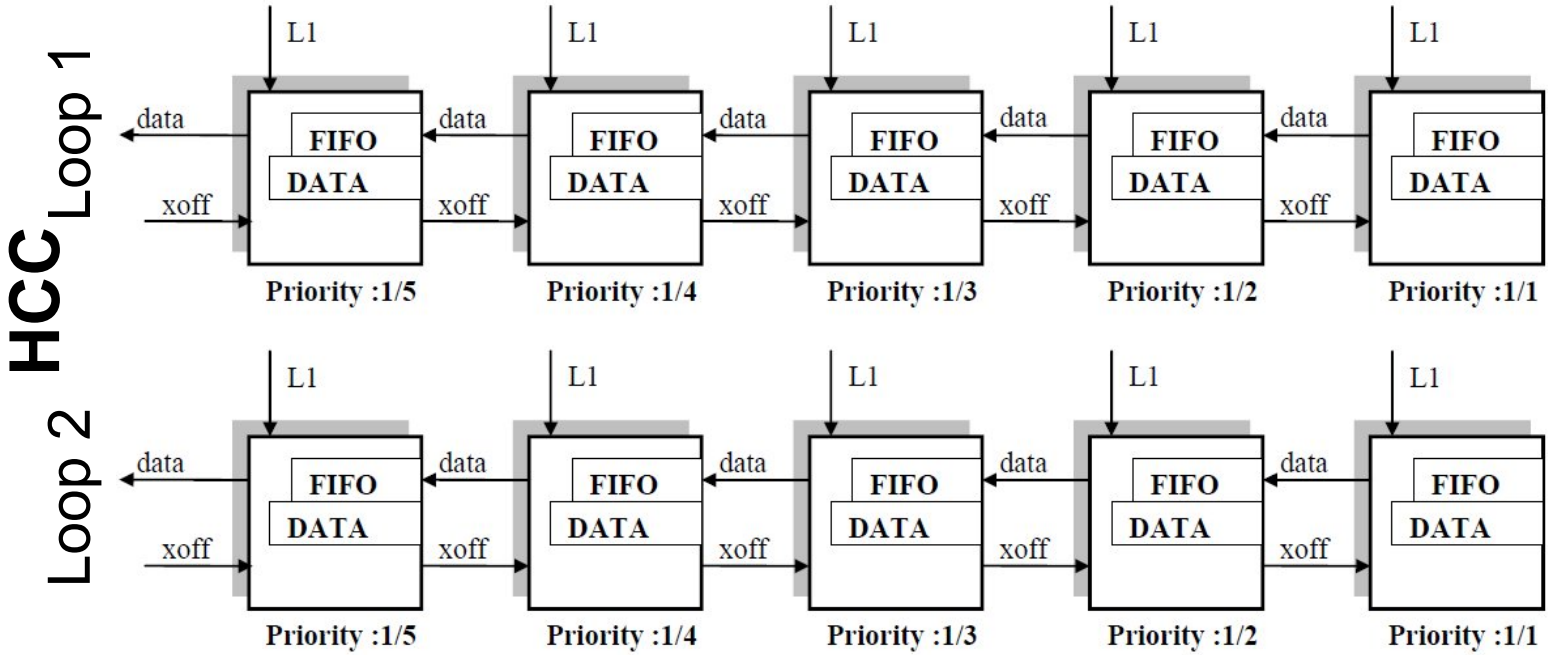
Barrel Stave concept

- Local DC-DC



- Companion HCC – Hybrid Controller Chip
  - GBT interface
  - clock generator with phase adjustment
  - Data concentrator
  - Monitoring functions
- EOS : GBT, opto devices

Hybrid Readout Concept

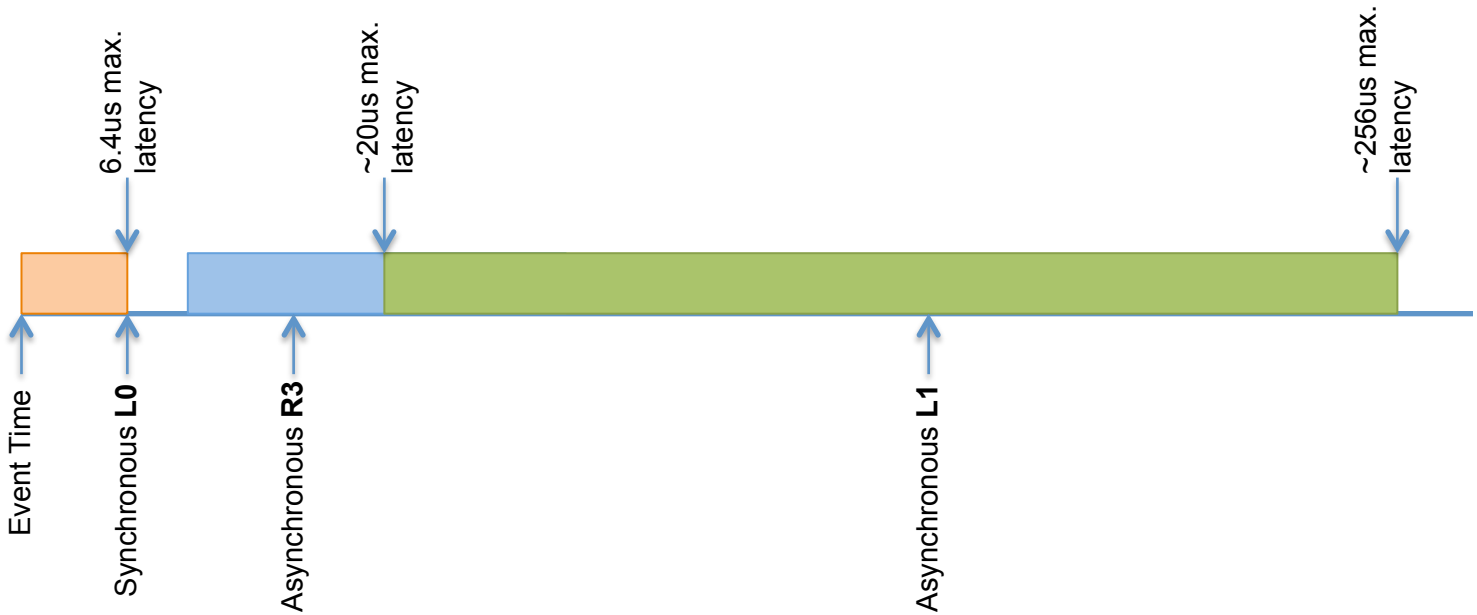


Estimated data rate :
1x64 bits packet per ABC per trigger

Trigger Rate 200KHz (L1) + 50KHz (Regional Readout Request R3)

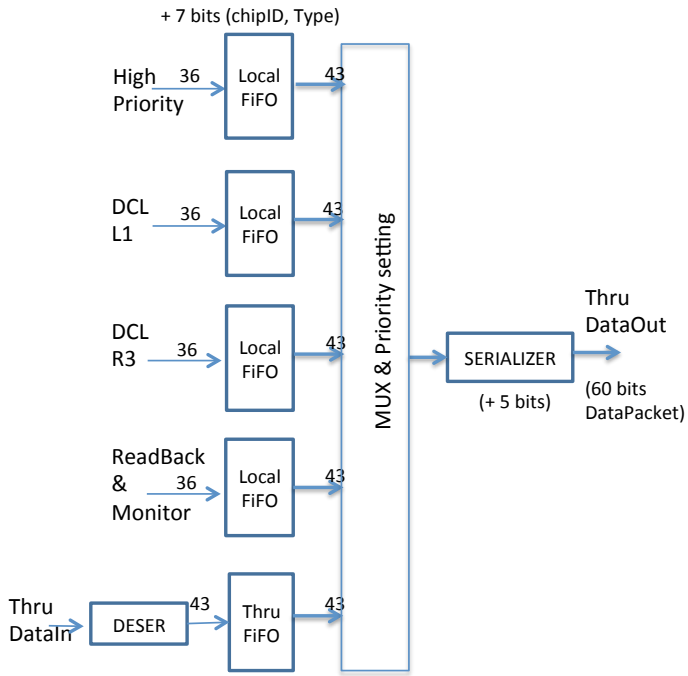
Hybrid link @ 320Mb/s

Triggers



- Three triggers
  - L0 – synchronous (@ 500KHz)
  - R3 – Regional Readout Request (~10% of detector) – input for L1 decision @ 50KHz
  - L1 – Whole detector readout @ 200KHz
- R3 prioritised over L1
- Non sequential readout – self describing data blocks

READOUT

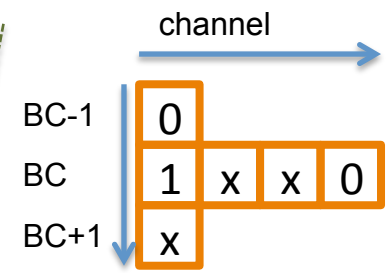


ABC130 Packet format

26 bits Header	34 bits Payload
60 bits packet size	

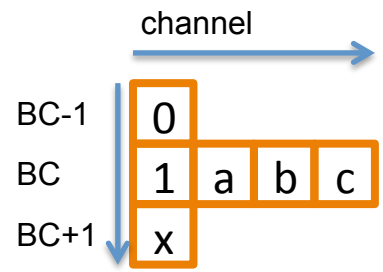
Start Bit	ChipID	TYP	L0ID	BCID
1	5	4	8	8

Cluster formation



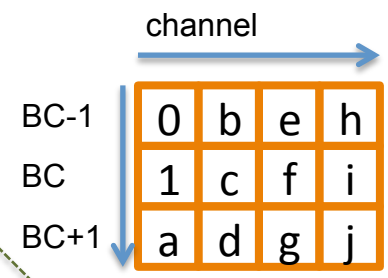
R3

4 clusters
max@1packet



L1-1BC

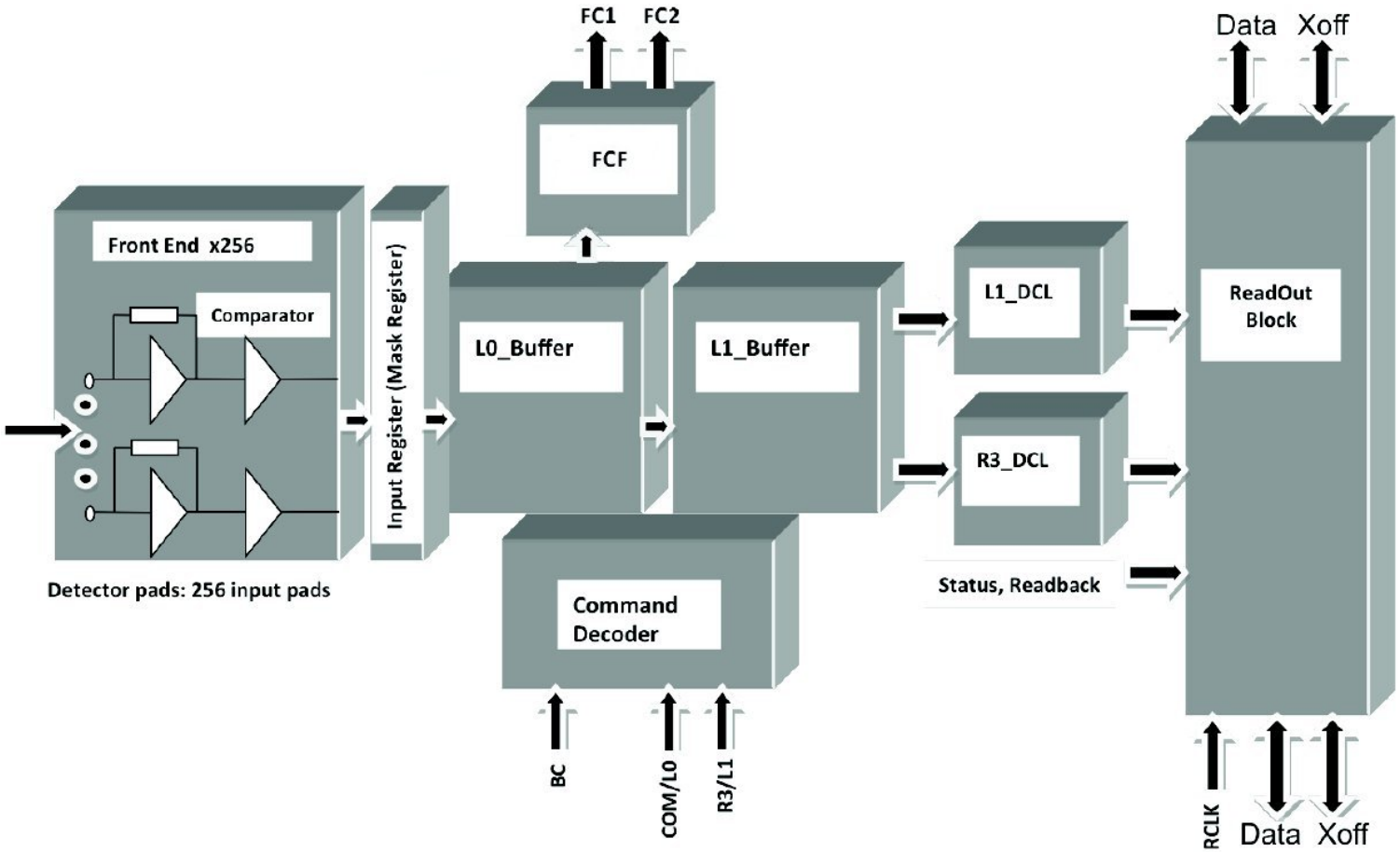
3 clusters/packet
All clusters



L1-3BC

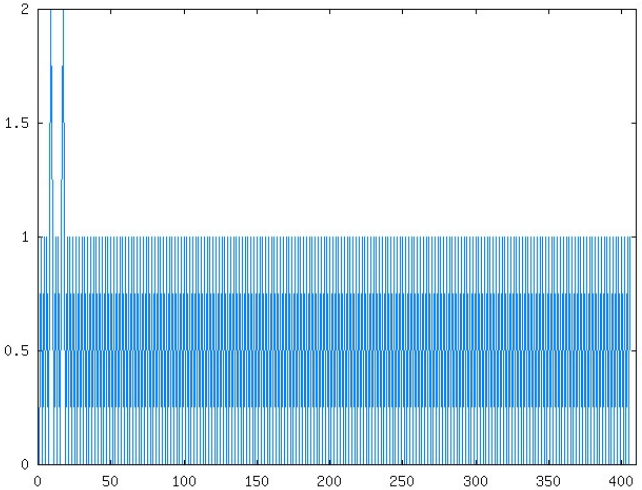
1 cluster/packet
All clusters

ABC130 block diagram



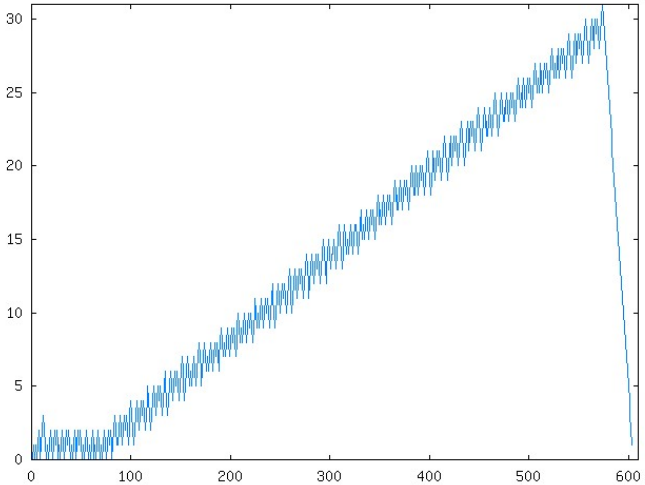
- Two RAM buffers L0 & L1/R3
- Different data compression logic (DCL) for L1 & R3

FUNCTIONAL SIMULATION



L1 packet FIFO filling index

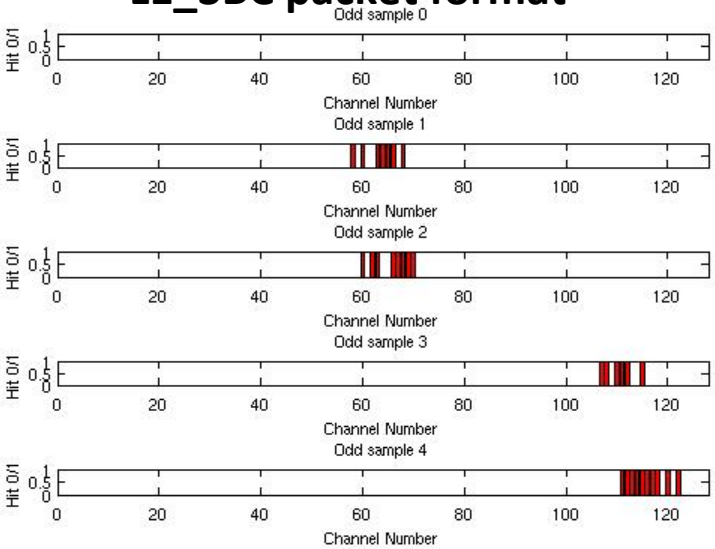
200KHz L1 rate, 5 ABC130, 160Mb/s, chip1, 2 packets/L1 (3-6 cl.)



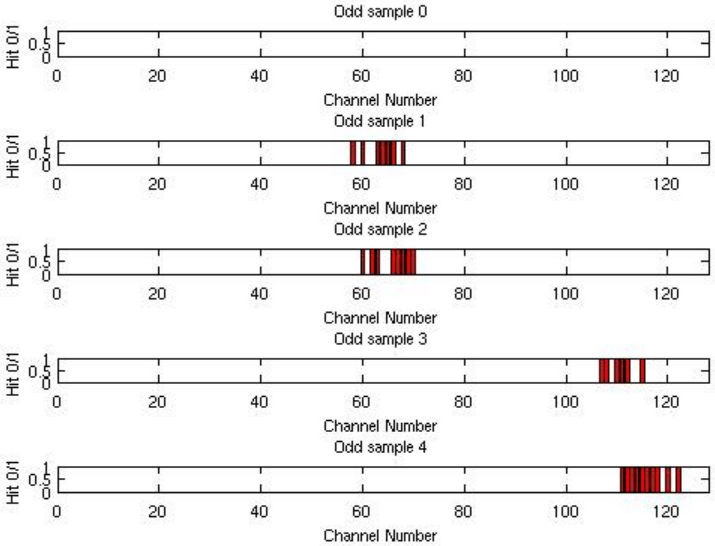
L1 packet FIFO filling index

200KHz L1 rate, 5 ABC130, 160Mb/s, chip1, 3 packets/L1 (6-9 cl.)

L1_3BC packet format

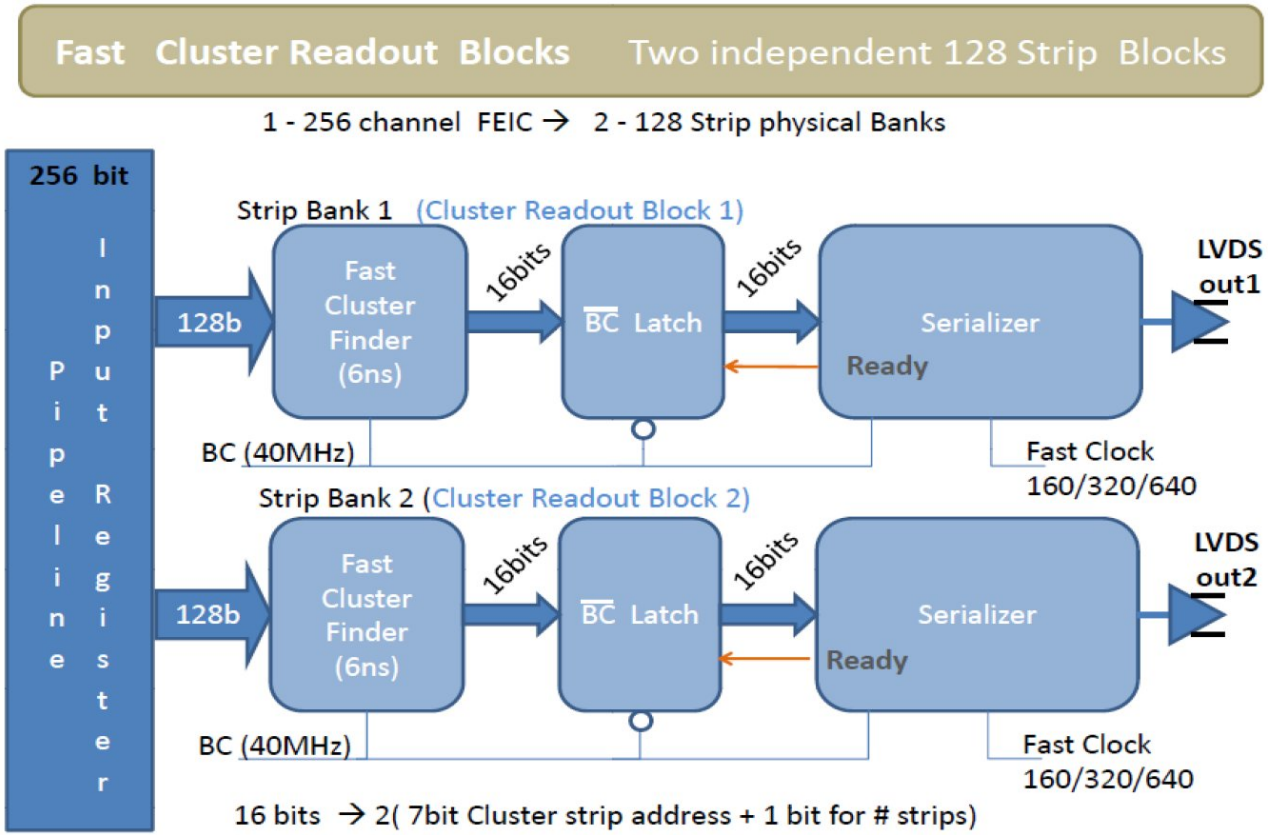


Matlab: DUT_2



Verilog: DUT_2

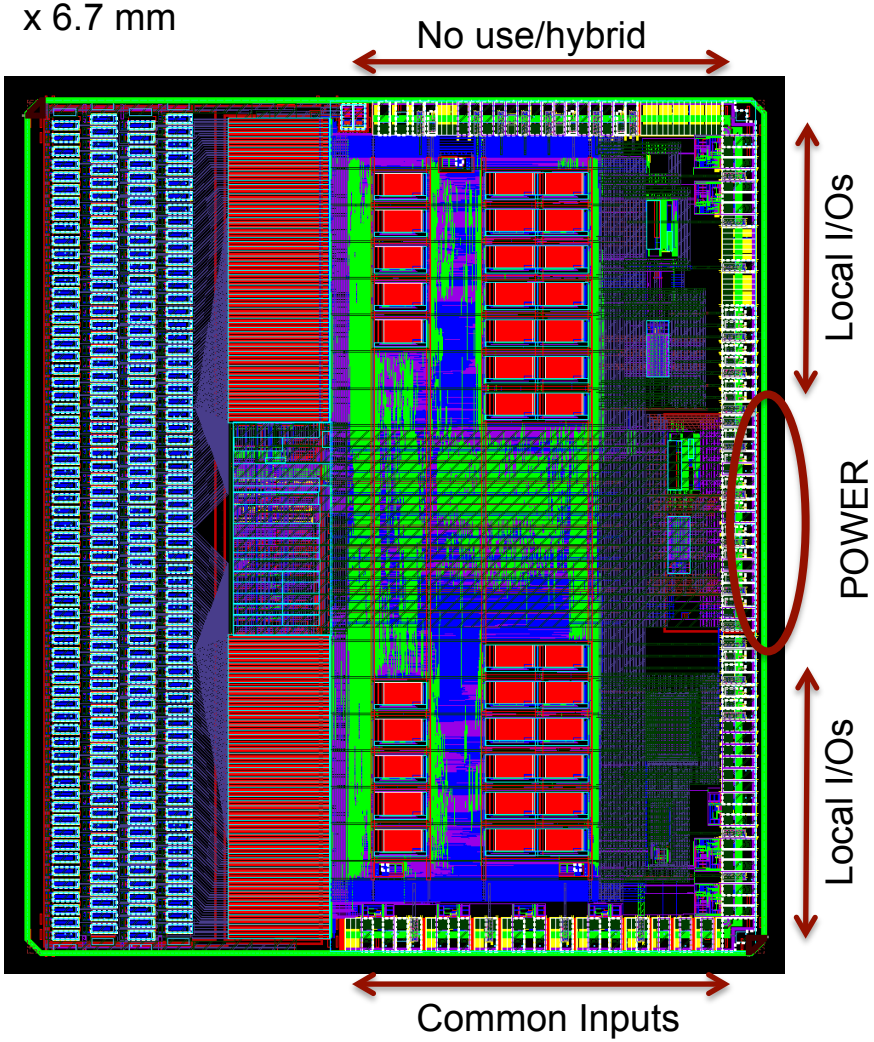
FCF block diagram



- Cluster size limited to 2 strips or less, to reject low pT tracks
- Up to 2 clusters per 128 strips can be detected
- Data transmitted at 640Mb/s rate

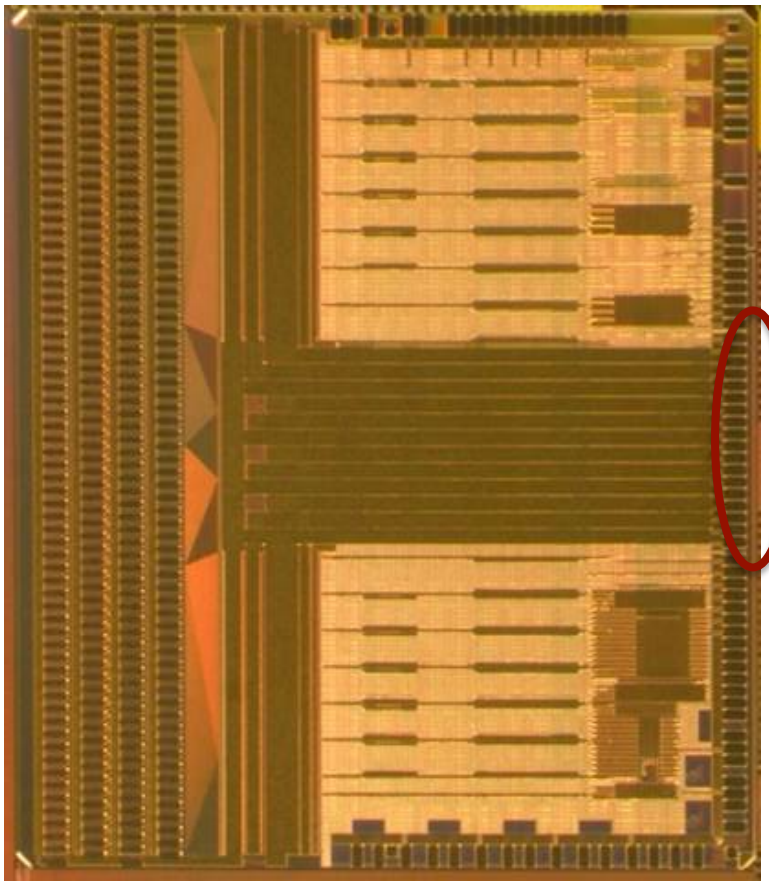
ABC130 layout

Size: 7.9
x 6.7 mm



- 2 adj. voltage regulators 1.5V-> 1.2V
- One shunt transistor for serial powering schema
- 3 Bandgap References
- All power pads at the “back-side”
- 22um FE channel pitch
- 4 x 64 I/P rows@119 um pitch

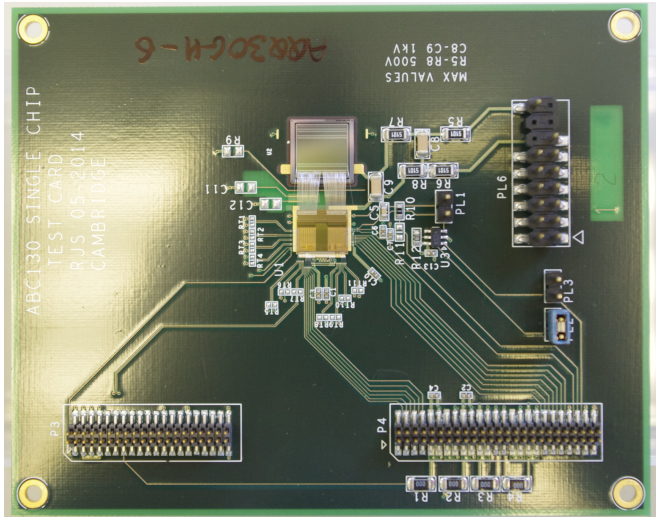
ABC130 Performances

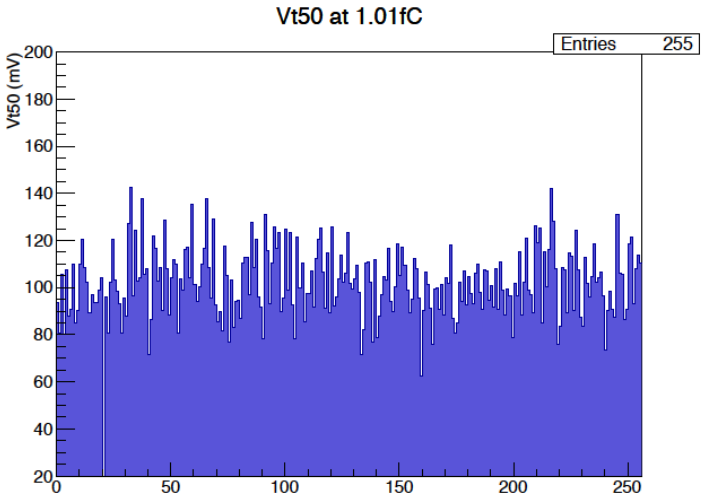


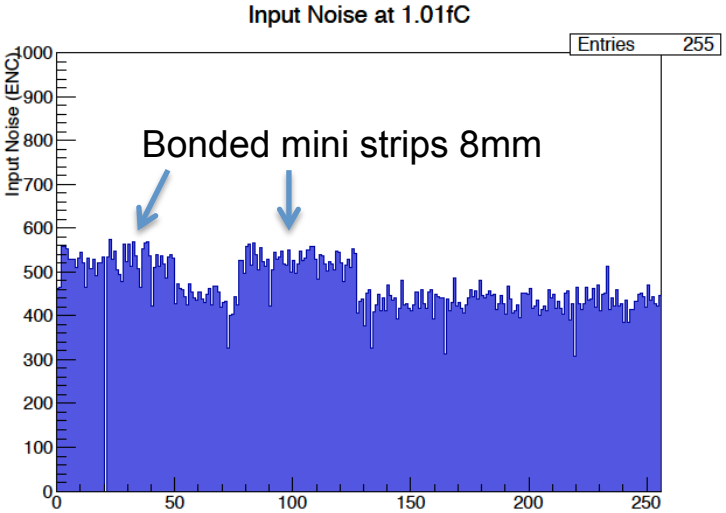
IBM 130nm technology

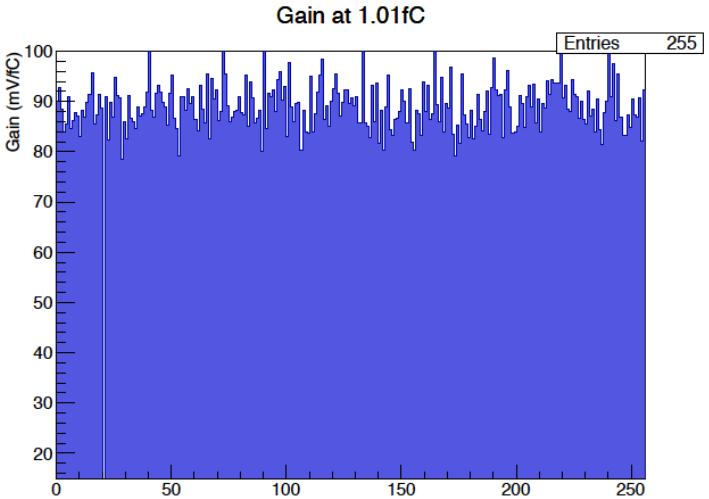
- Power Tests
  - Current Consumption
    - Before configuration
    - After configuration
  - *SP Shunt*
    - *Correct V for CI*
- DAC Characterisation
  - LDO characteristics
  - Parameters available through MUX
  - SLVS levels vs driver current
- Digital Test Vectors
  1. Write/read most registers
  2. Decoding of all chip addresses
  3. Reception of XOFF (both ways)
  4. Data through (both ways)
  5. *Function of priority mechanism*
- Analogue Characterisation
  - Three Point Gain
    - 0.5, 1.0, 1.5fC
  - Trim check
    - Additional scan with 1.5fC charge

ABC130 Performances

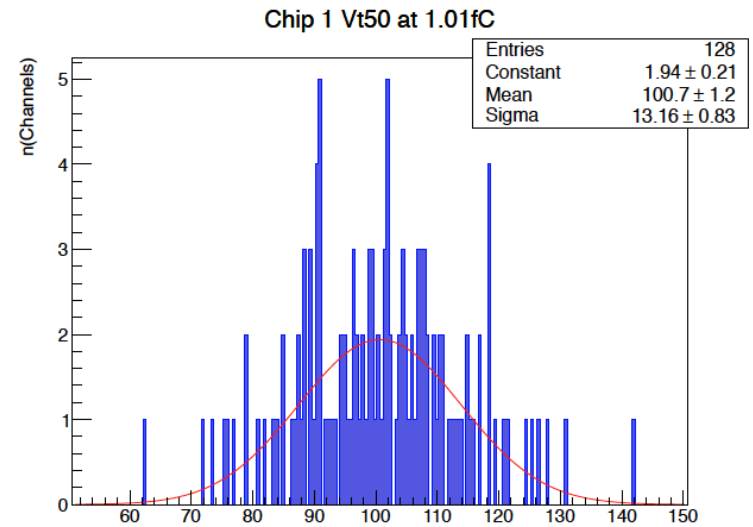


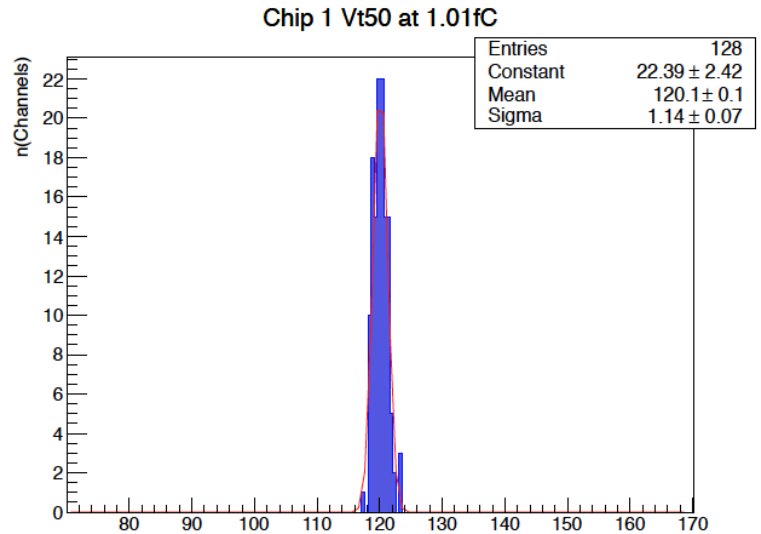




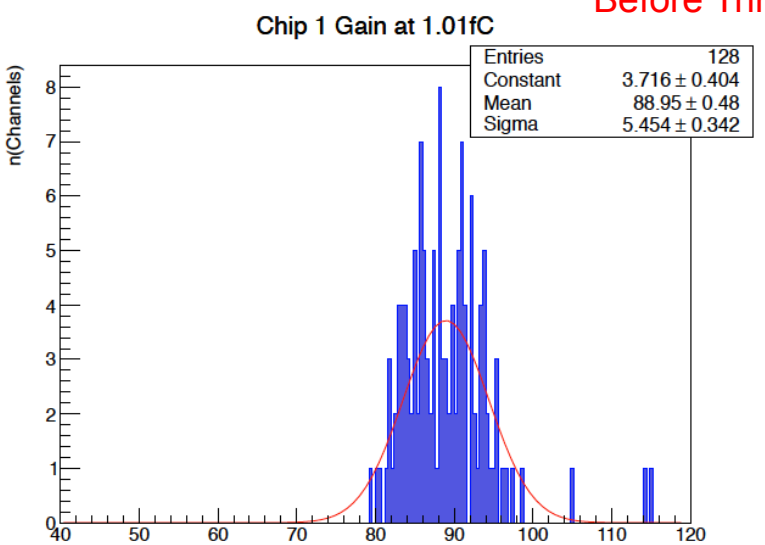


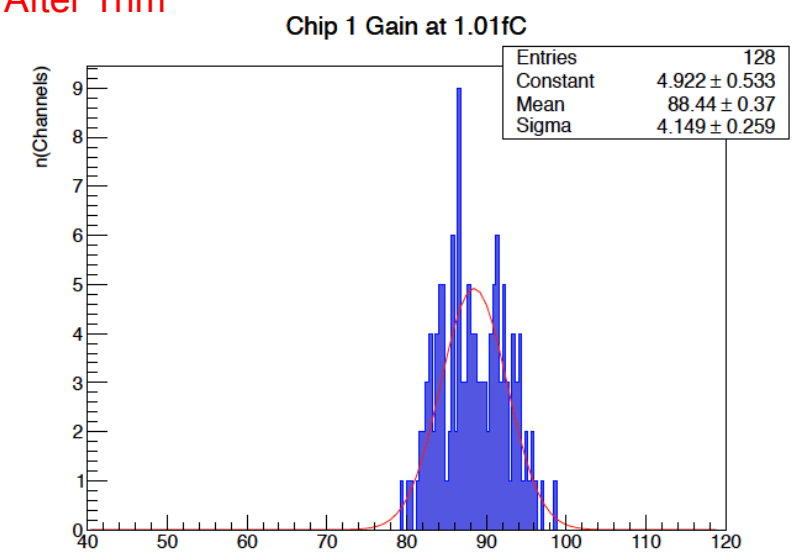
ABC130 Performances



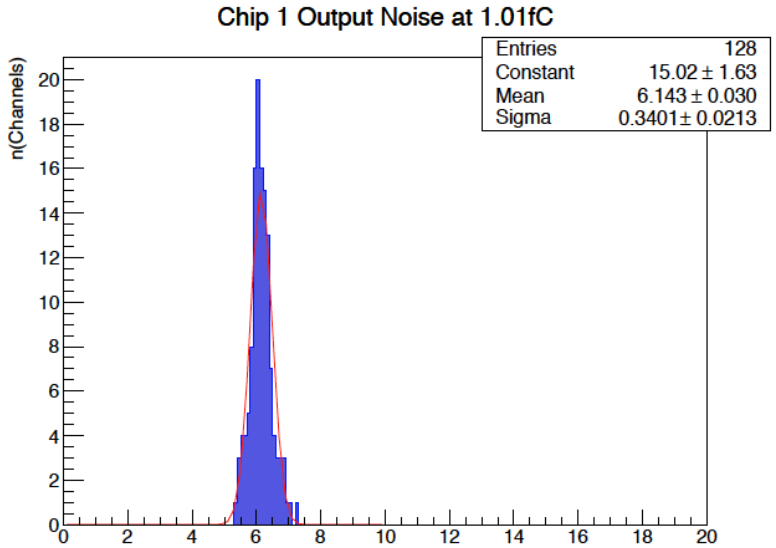


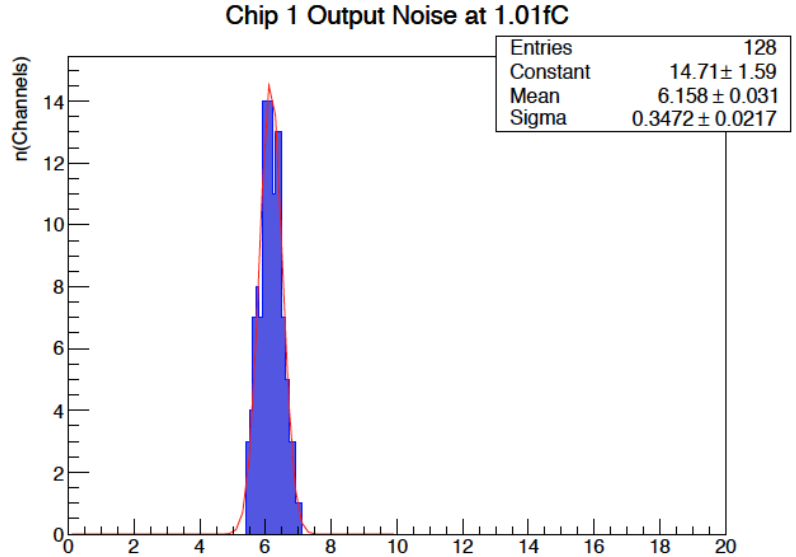
Before Trim | After Trim





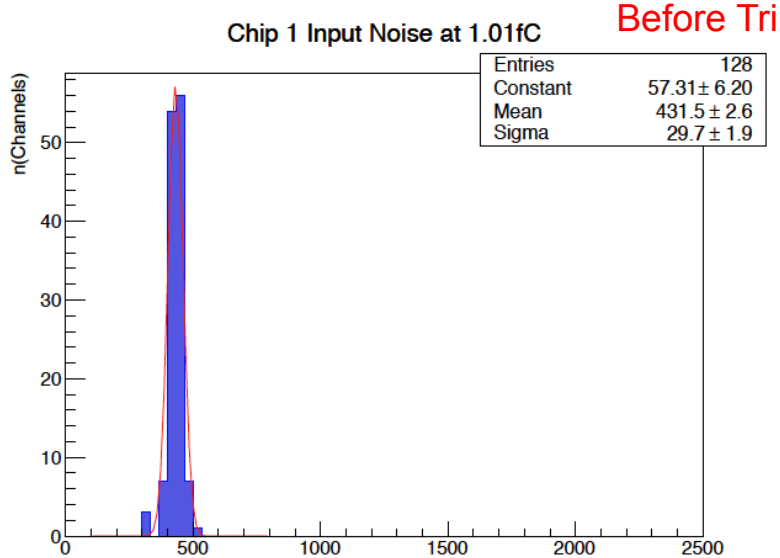
ABC130 Performances

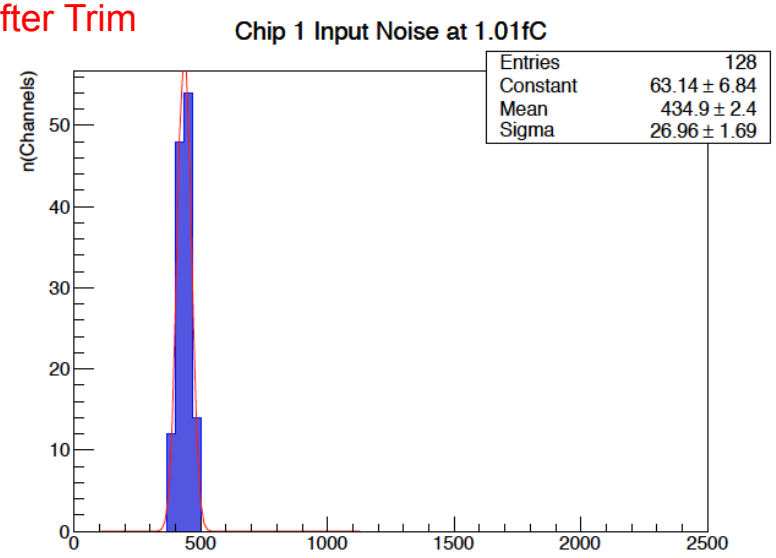




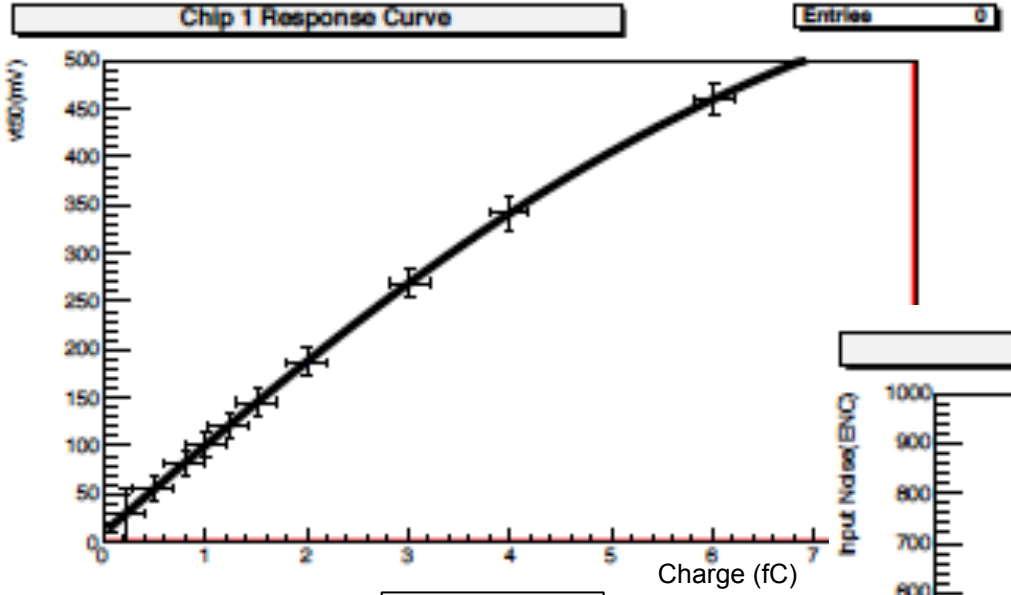
Before Trim

After Trim

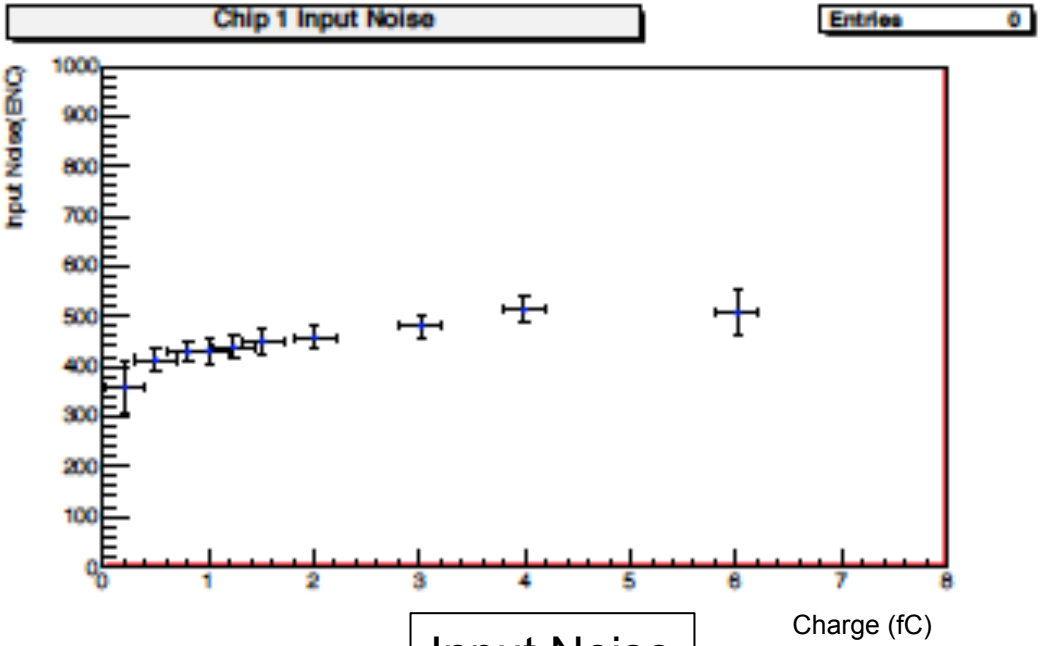




ABC130 Performances



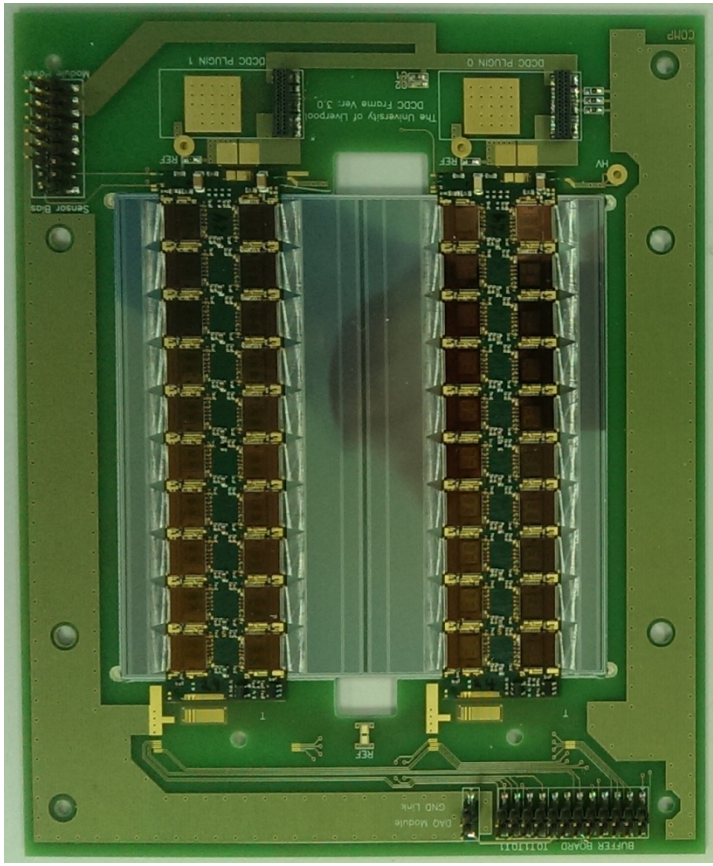
Linearity

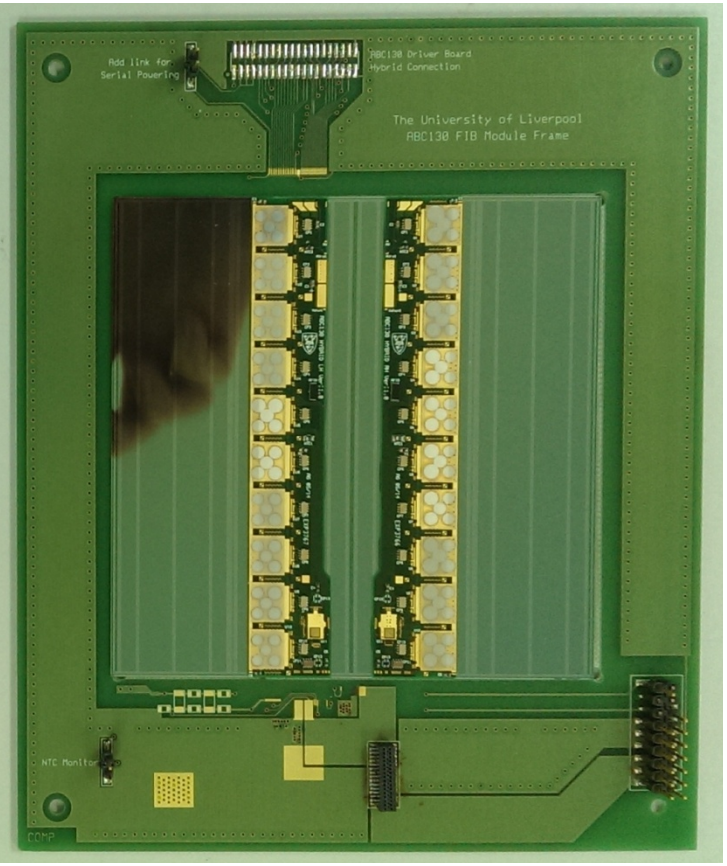


Input Noise

~3.6A/hybrid, 18W/module

~1A/hybrid, 3W/module

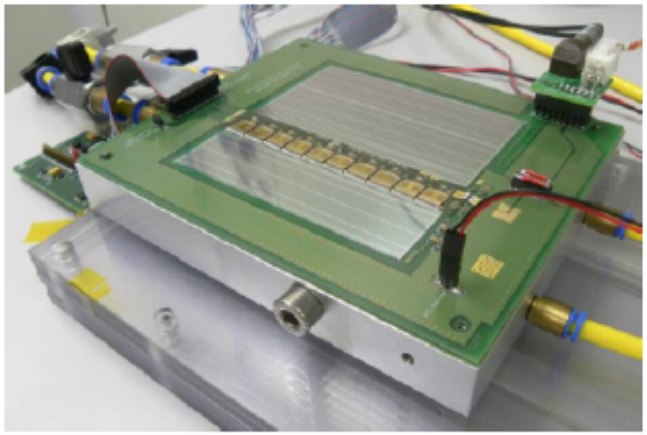




ABCN-25 module
- 4-layer circuit with 40 asics (5120 channels)
- Off-module powering and digital I/O buffering

ABC130 module
- 3-layer circuit with 20 asics (5120 channels)
- Comes with integrated powering and digital I/O buffering

Preliminary Results with the ITK Barrel Hybrid



- Prototype hybrid with 10 x ABC130s has been shown to work successfully
  - Able to configure devices
    - All LDO's programmed to ~1.2V
    - On board termination working
  - Serial readout chain of "FIB'd" devices operating at 80MHz shown to pass data correctly
    - Allowing characterisation of Front-end analogue performance
- Power Consumption better than specification
  - FDR predication was 92mA/ABC130
  - Measured is ~80mA
- No evidence of instability at low charge injection (1fC)
  - DTN not yet performed – better indicator
- Output noise in agreement with expectation but "gain" is low
  - Using analysis adopted for ABCN-25 (and ABCD) chipsets
  - Still to be understood but points to calibration circuit and or procedural error
  - Ideally would like to crosscheck by use of external calibration source (laser, radiation, etc.)

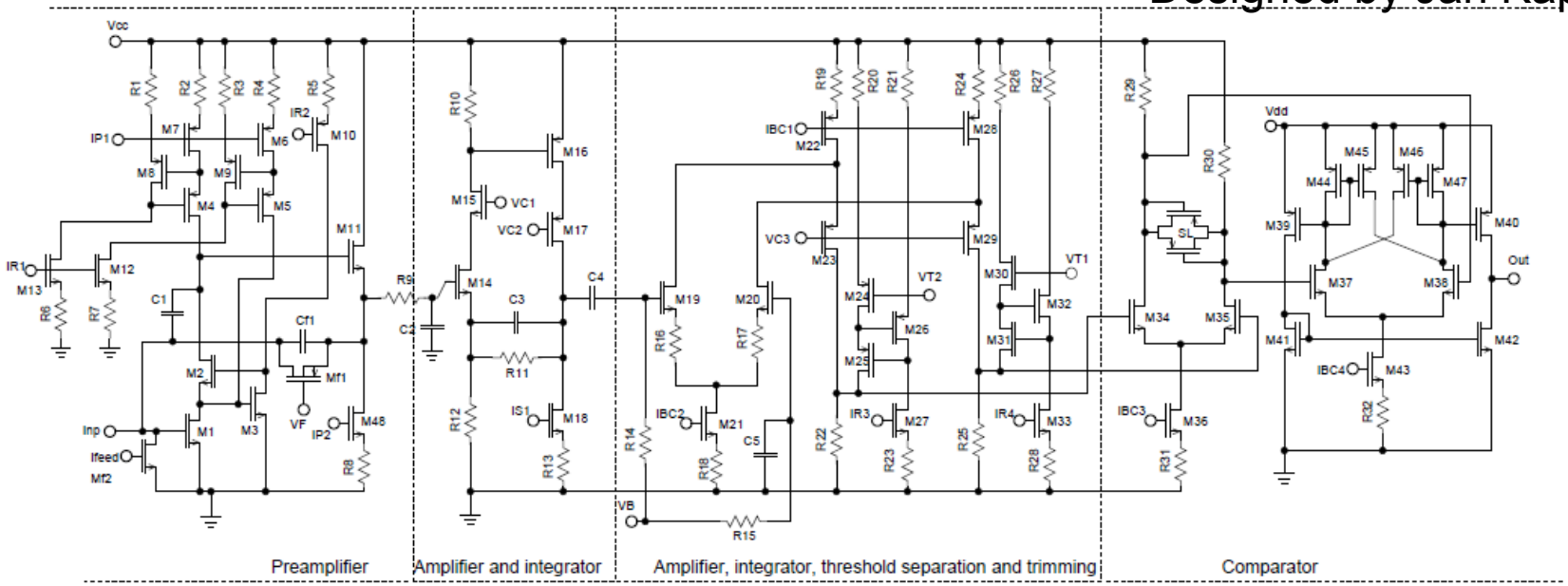
Summary

- ABC130 is a fairly complicated ASIC with two level memory, prioritised data multiplexer and bidirectional data outputs
- The power is low (~85mA/chip) thanks to advanced design techniques
- Fully operational, first modules being built
- This is *NOT* the final chip for the ATLAS ITK as
  - Trigger requirements are changing
  - SEU robustness has to be measured -> improved ?

Backup Slides

Front-end Design

Designed by Jan Kaplon



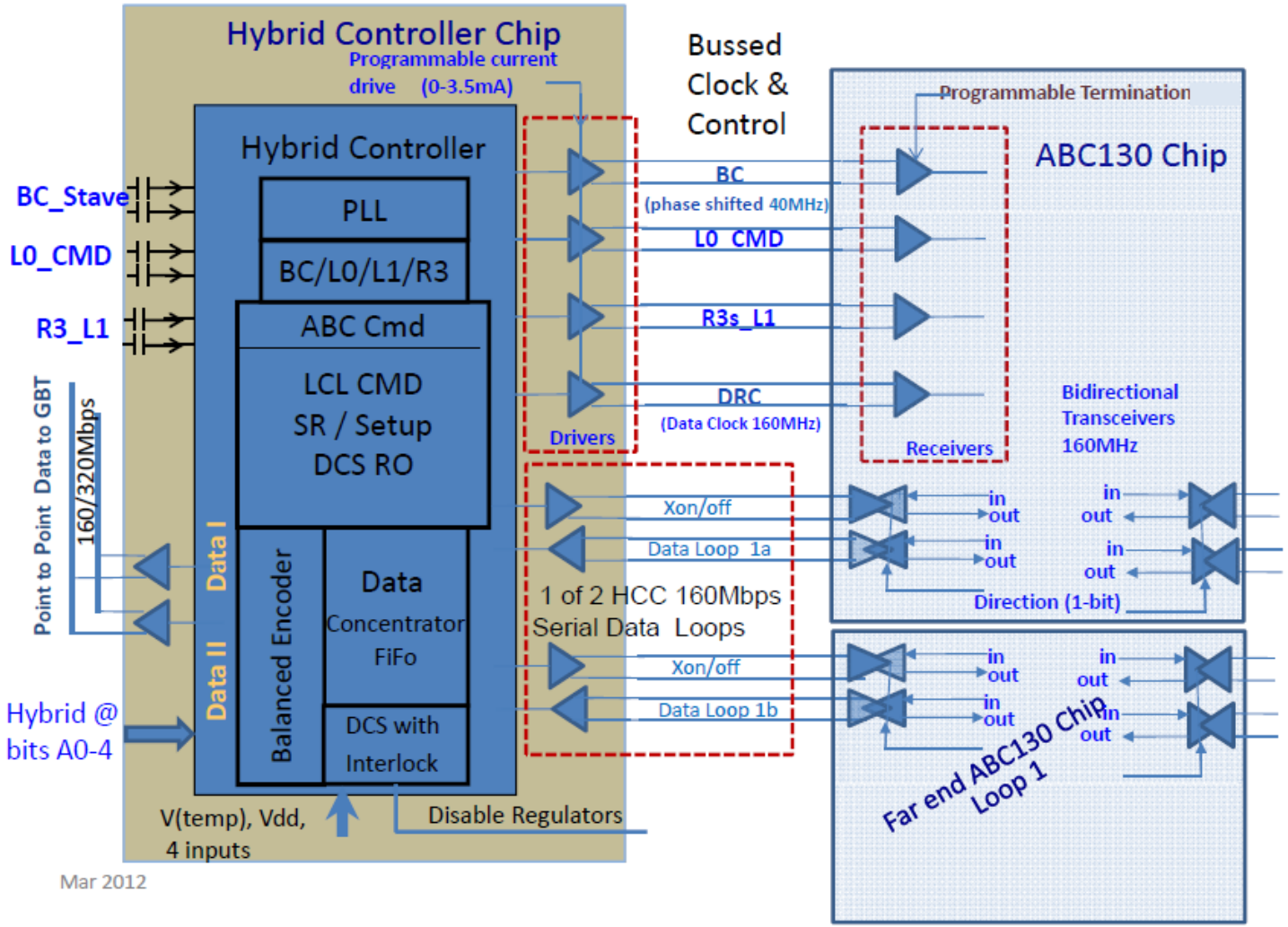
Requirements:

- ENC <1000e- @3pF
- ENC <1500e- @10pF
- Low power consumption (<300uW/ channel)
- Peaking time <25ns (time walk <16ns)

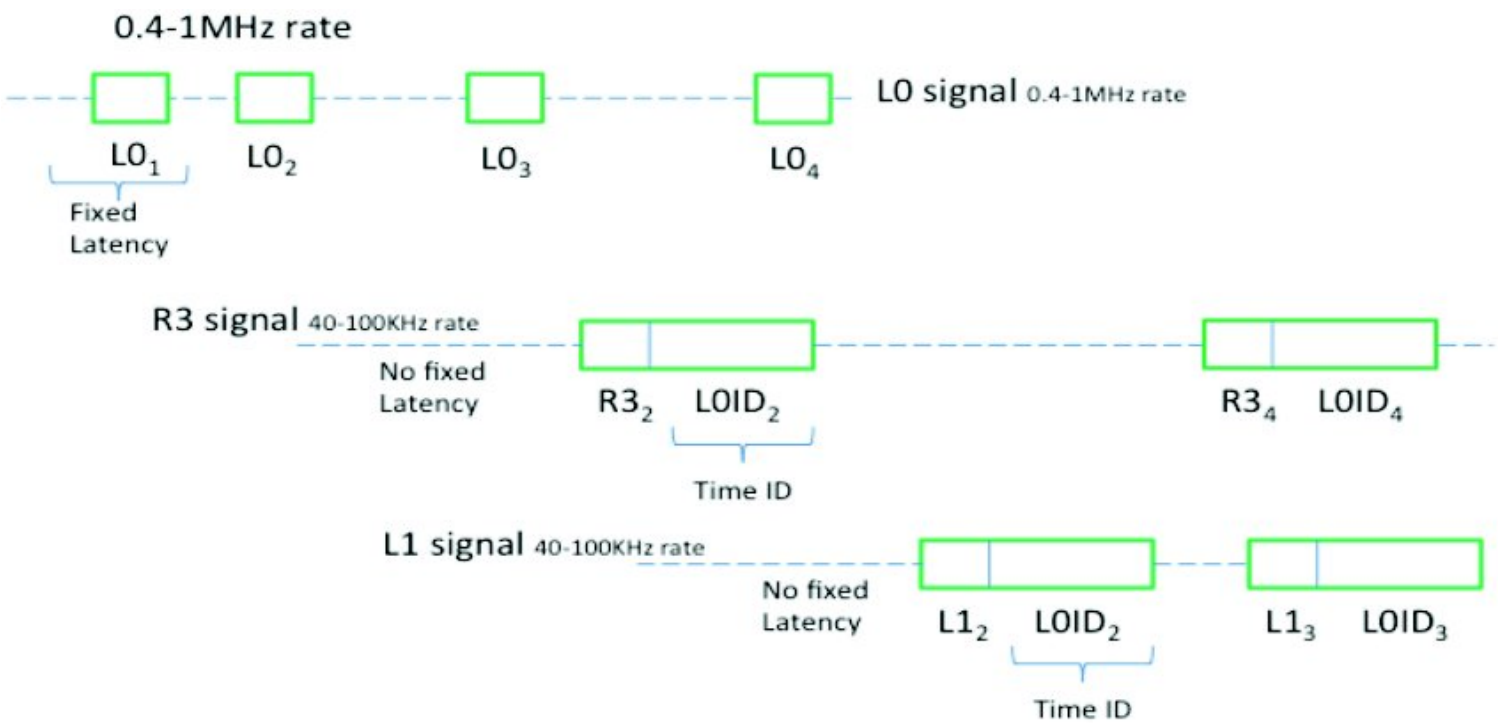
Architecture:

- binary output
- 5-bit current DAC in each channel
- single 8-bit threshold DAC for 256 channels

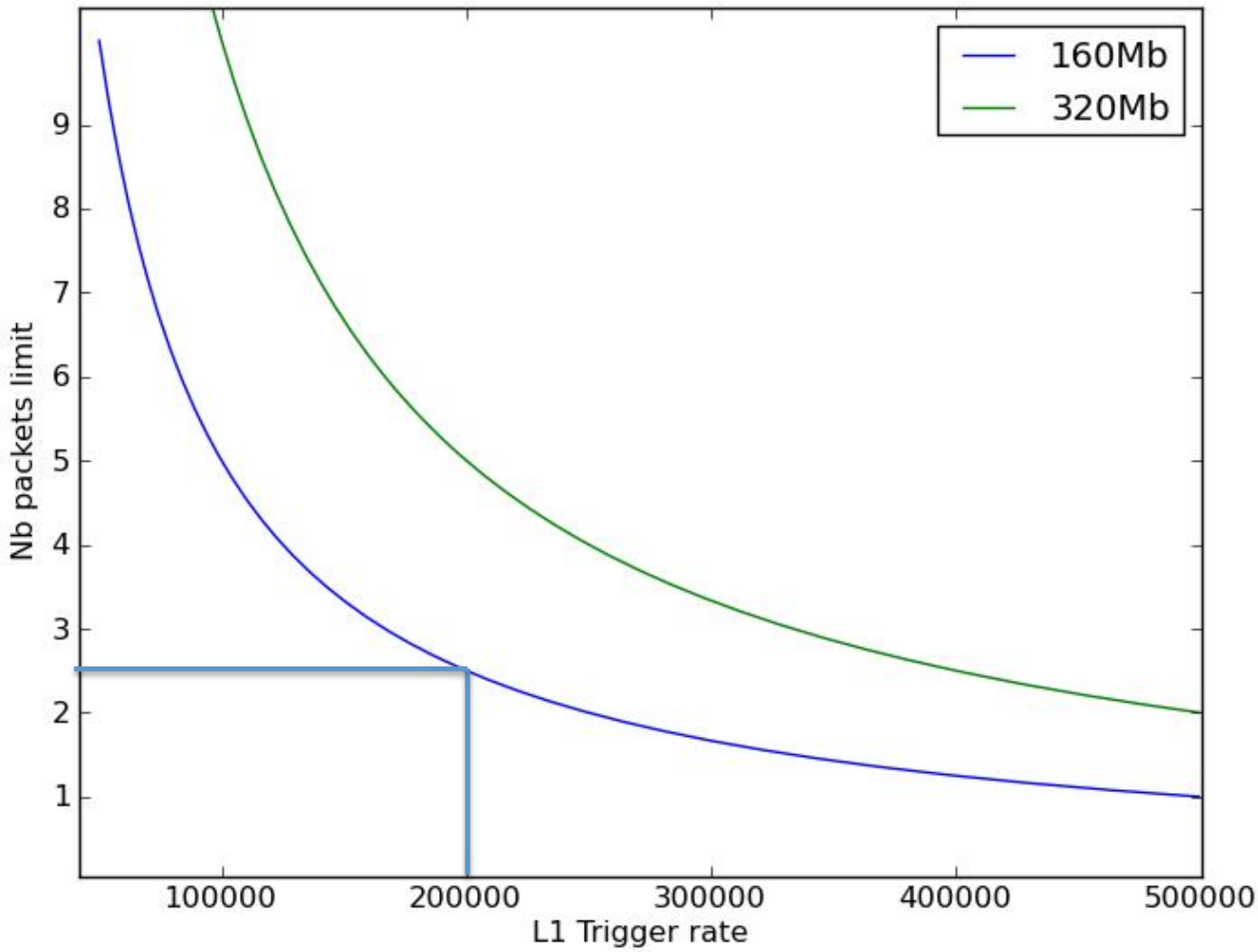
HCC Block Diagram



Example of Triggers Sequence

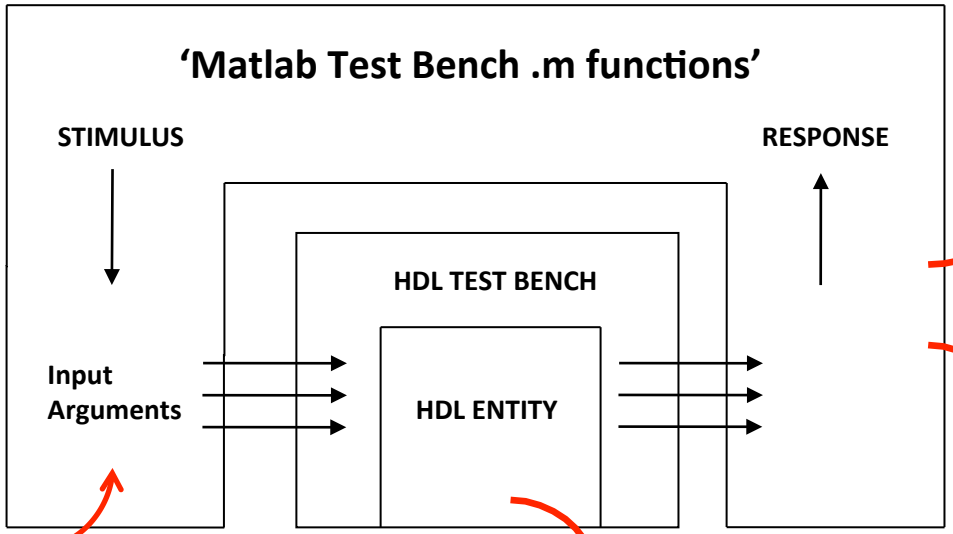


ABC130 rtl

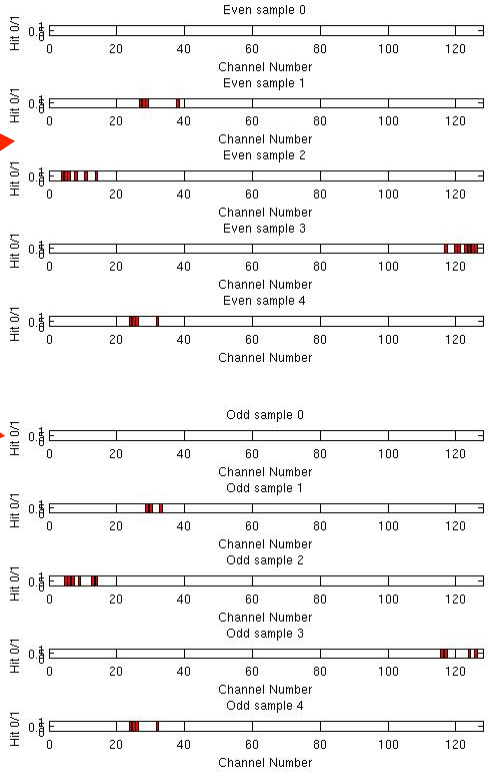

160Mb
320Mb
Nb packets limit
1
2
3
4
5
6
7
8
9
100000
200000
300000
400000
500000
L1 Trigger rate

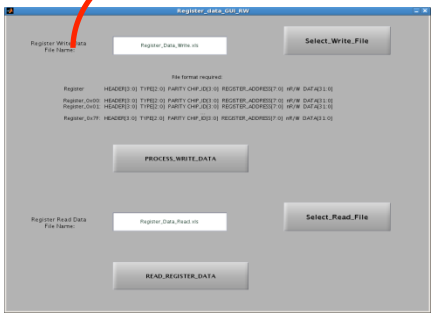
TestBench with MatLab, physics data

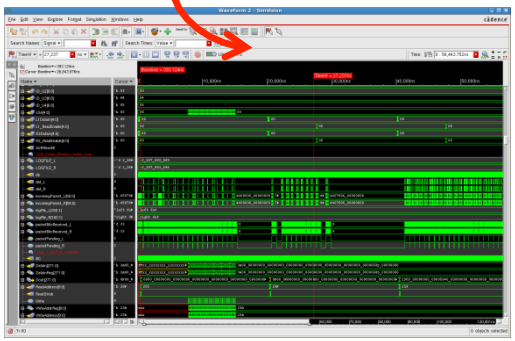
- Contribution by Michelle Key-Charriere



Matlab GUI output

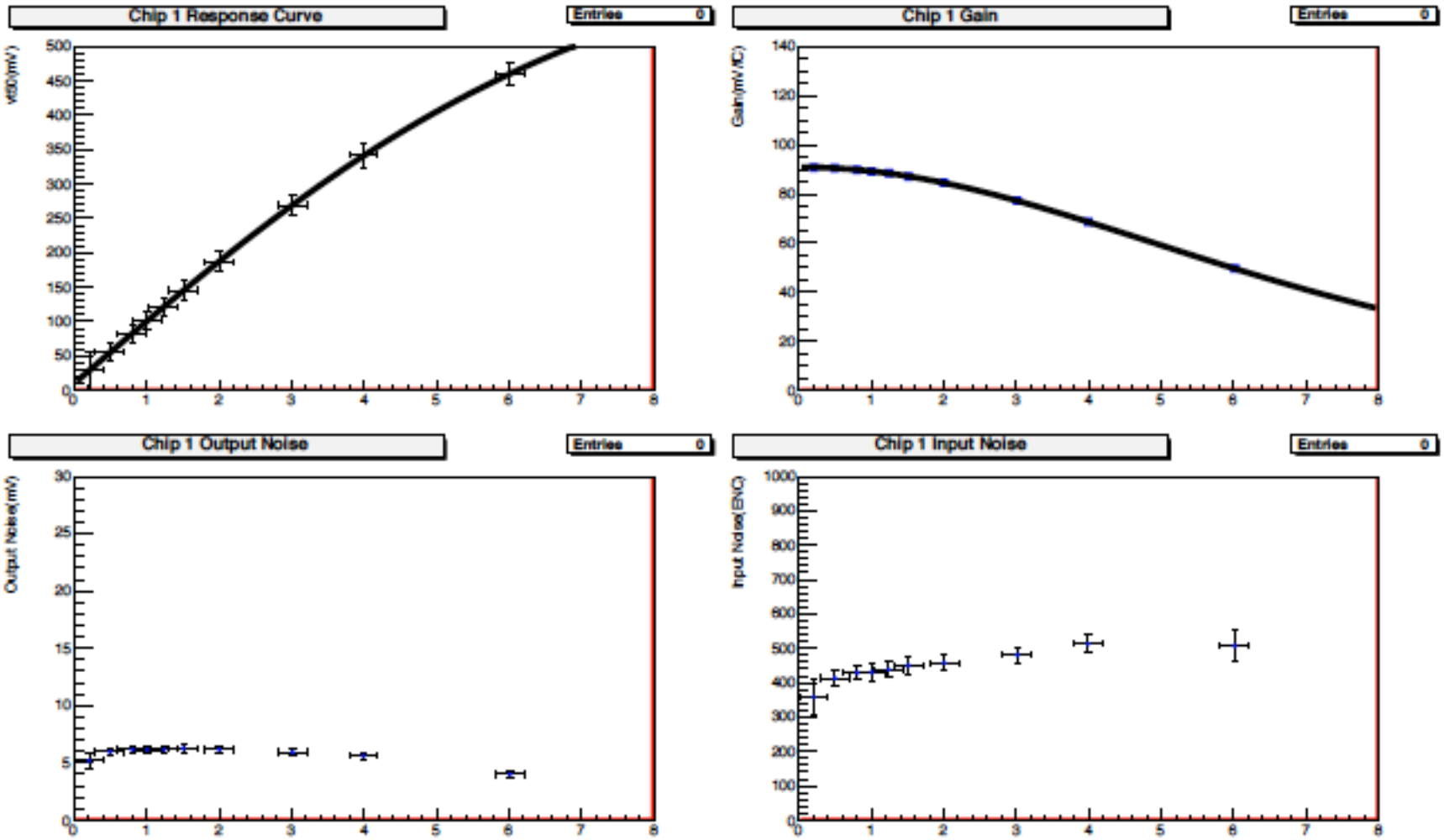






Algorithm Development Using Matlab and Cadence Incisive

ABC130 Performances



Design methodology – design

- Analogue part designed fully custom
- Digital part written in Verilog with macros delivered by CERN or designed by our team
  - memories delivered by CERN (corrections and abstracts generation necessary)
  - pads design fully custom then Verilog models, abstracts and liberty description created
  - for other blocks (e.g. regulators) only Verilog models and abstracts created
- Extensive simulation based verification done
  - Verilog scripts to verify ASIC basic operations
  - Matlab based framework for a chain of ASICs with realistic trigger and data structure

Design methodology – implementation

- Whole digital part synthesised in single step (finally FCF delivered as macro block)
  - clock gating applied
  - scan chain added
- Place & route done in flat flow
  - floorplan (very time consuming)
  - placement (power filtering capacitance added)
  - clock tree synthesis with clock grouping
  - routing with antenna removal
- Hand DRC error removal (remaining after P&R)
- Digital and analogue parts put together and verified – DRC, LVS with Calibre and Assura