Summary of ASIC Review and Revised protoDUNE/SBND Schedule

BNL DUNE Group Meeting

January 27, 2016

Outcome of Review (Summary)

- FE ASIC: Submit as planned in early February
- ADC ASIC: Study of V* chip (essentially a bonus prototype) is just beginning. Decision to take 2 extra months to study this chip and implement any changes before submitting 1st DUNE/SBND prototype.
- Register readback functionality not implemented, not recommended by developers
- Terri Shaw working on official report of review (draft circulating among reviewers now)

Accelerated Schedule

- Details: See ETW talk in DUNE CE meeting 1/25/2016

protoDUNE Goals

- Instrument APA 1 at CERN by April 2017
- Instrument APA 2-3 at CERN by August 2017
- Instrument APA 4-6 at CERN by September 2017
- protoDUNE installation complete by December 2017

Summary of CE Plan I

- FEMB/ASICs expected to be on critical path for CE
  - Current effort (and this talk) focused on setting a schedule to produce fully populated & tested FEMBs in timeframe required for protoDUNE
  - Detailed schedule exists for ASIC design/QA/production/QC
  - All the other components (feedthrus, flanges, WIBs, cables) are also necessary; will look at updating schedule for these in upcoming weeks
- Two rounds of ASIC prototyping planned for 2016
  - V* chip provides "bonus" round of prototyping for ADC ASIC (in progress now)
  - Schedule includes delay in submission of SBND/DUNE ADC ASIC 1st prototype to take advantage of V* prototype
  - Compression of chip characterization and design efforts not desirable; current plan maintains both rounds of prototyping

Summary of CE Plan II

- To meet accelerated schedule
  - Deliver prototype FEMBs populated with 2nd round prototype ASICs in April 2017 to facilitate integration tests at CERN
  - Replace these prototypes with production FEMBs by July 2017
  - Remaining FEMBs follow in August & September 2017
  - Compression in original schedule results from parallelization of tasks and movement of some integration tests to CERN
    - Original schedule for production boards included 2 months for all chip QC + 1 month for all FEMB population + 3 months for all board evaluations & integration tests
    - Accelerated schedule for first round of 20 production boards is 1 month for chip QC + 1 month for FEMB population + 1 month for board evaluations & integration tests with expectation that further integration tests will happen after delivery at CERN; next 40 follow ~1 month behind, etc.

Detailed slides from ASIC Review

Front-End ASIC Modifications

- Integrate internal pulse generator *K. Yethiraj*
  - 6-bit, controlled by TCK, with option for external bypass
- Increase buffer-off drive capability of last stage *G. De Geronimo*
  - to prevent distortion on positive (switches) and negative pulses
- Increase front-end leakage current capability *G. De Geronimo*
  - add x10 option (1nA, 5nA) and control bit (to prevent possible "chirping")
- Implement smart reset *G. De Geronimo*
  - RST generated at CK high when CS high, keep RST pin
- Revise BGR start-up circuit *G. De Geronimo*
  - to mitigate possible residual yield issues
- Modify configuration interface *G. De Geronimo*
  - SDO tri-stating, SCK enable with CS, TCK enable with nCS
- Increase ESD protection on test and configuration IOs *W. Hou*
  - logic IOs (SDI, SDO, CS, SCK, RST) and test input
- Investigate read-back configuration option *G. De Geronimo*

ADC ASIC Modifications

- Improve ADC INL/DNL *N. Nambiar*
  - to correct for MSB accumulation effects (ref. to as "spikes" or "stuck bit")
- Extend soft-control functions *E. Vernon*
  - add dedicated test-pattern generation command and FIFO soft reset
- Implement COLDATA-compatible interface *E. Vernon*
  - ADC-conv & ADC-busy signals
- Implement power-on default configuration *W. Hou*
  - data-collection mode
- Revise BGR start-up circuit *G. De Geronimo*
  - to mitigate possible yield issues
- Modify configuration interface *W. Hou*
  - from LVDS to single-ended for compatibility with FE ASIC
- Increase ESD protection on test and configuration IOs *W. Hou*
  - logic IOs (SDI, SDO, CS, SCK) and test input
- Investigate read-back configuration option *G. De Geronimo*

ADC ASIC Modifications: V* version

- A V* version of the LAr ADC ASIC has been designed and fabricated and is being tested.
- The V*, required by other projects, also aims at evaluating if the proposed changes, listed below, move us in the right direction.
- Very preliminary results will be shown.

* Improve ADC INL/DNL (partial changes) *N. Nambiar* (✓)
  - to correct for MSB accumulation effects (ref. to as "spikes" or "stuck bit")
* Extend soft-control functions *E. Vernon* ✓
  - add dedicated test-pattern generation command and FIFO soft reset
* Implement COLDATA-compatible interface *E. Vernon* ✓
  - ADC-conv & ADC-busy signals

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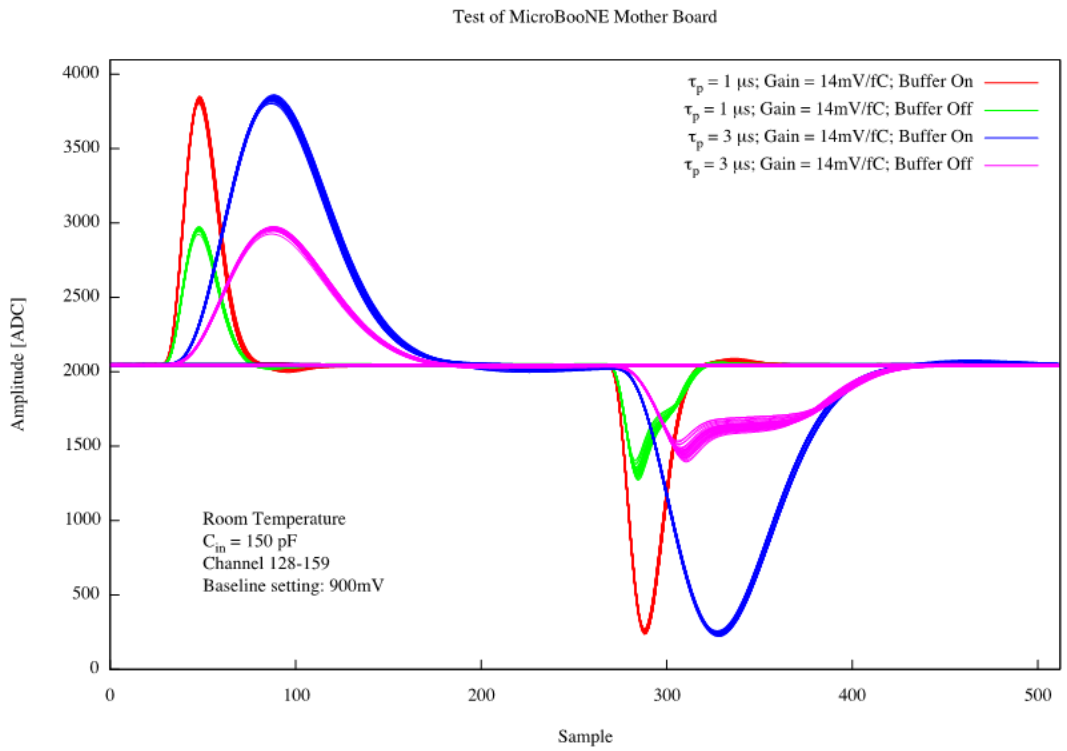
Distortion - measured

Bench Test



- Distortion is verified with bench test again recently
- Confirmed the distortion is disappeared when buffer is on

03/10/2015 H. Chen - BNL MicroBooNE Meeting

Distortion occurs when driving 1kΩ with buffer off (μBooNE)

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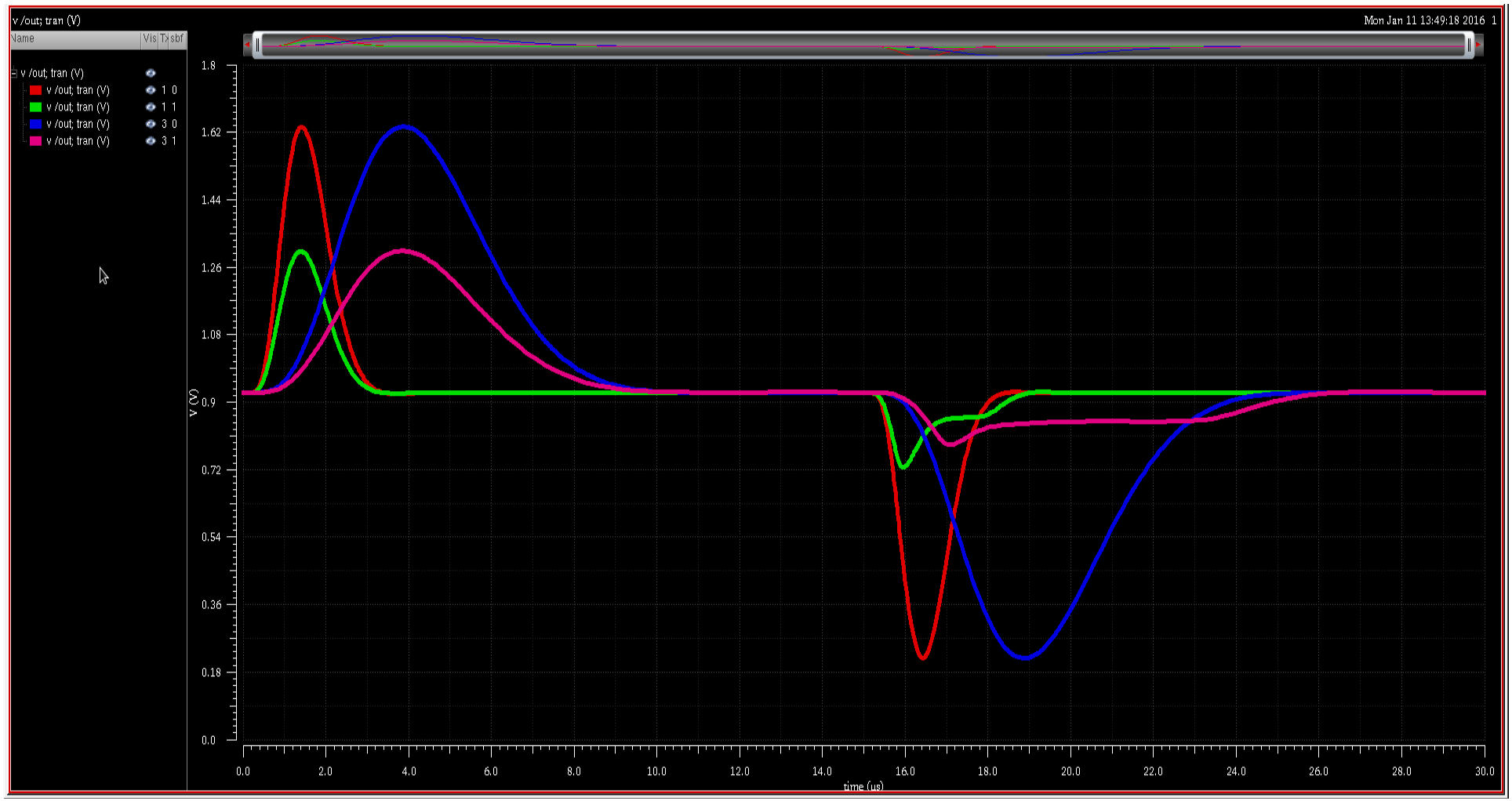
Distortion - simulated



Distortion due to drive capability of pre-buffer stage

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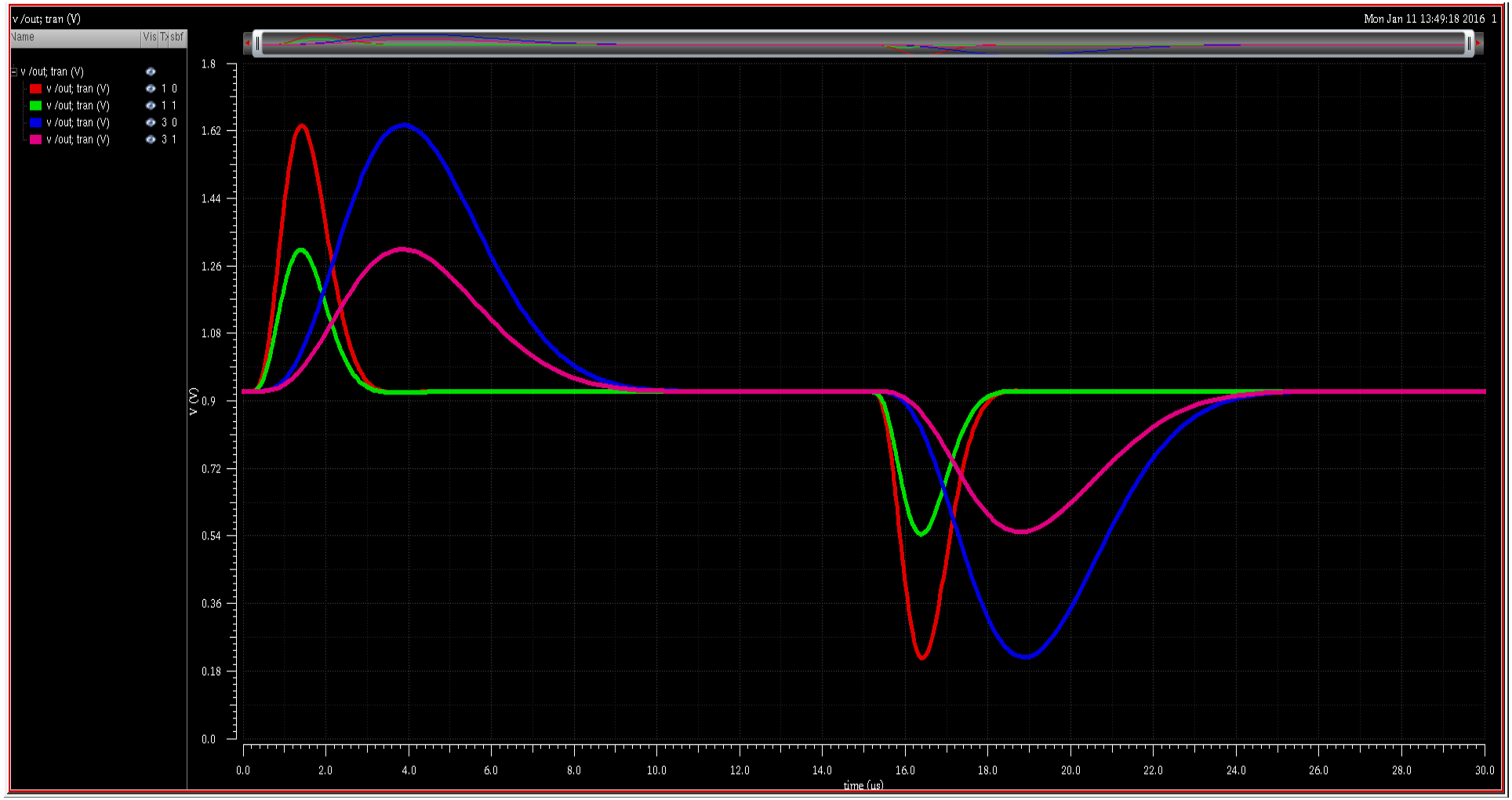
MOSRES Bootstrap - Simulated



Drive capability of 1kΩ with buffer off is achieved

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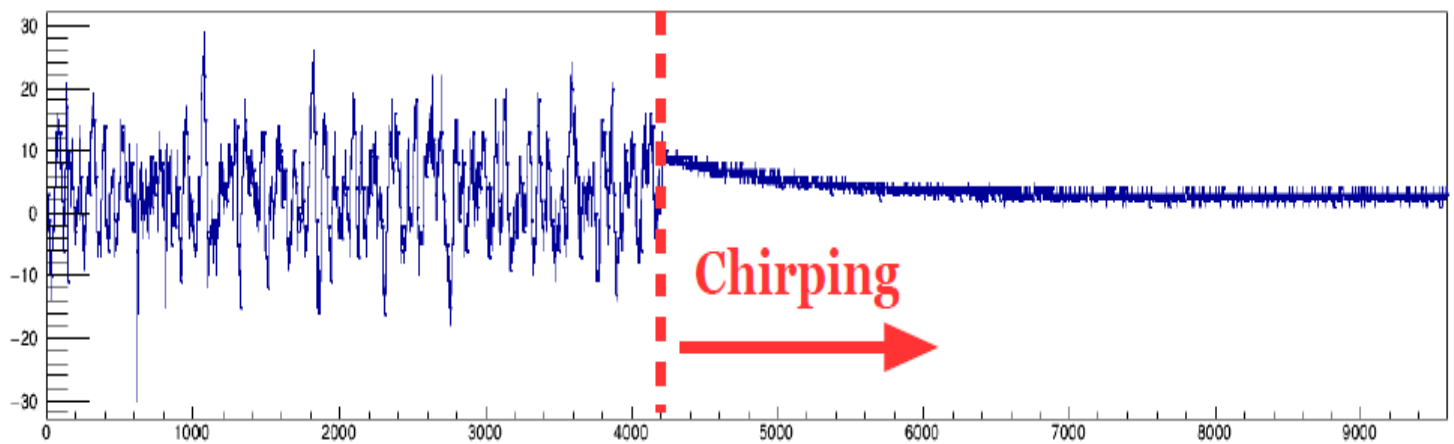
Saturation from Low-Frequency Ripples

- Intermittent dead regions on waveform (10-15% of channels/event)
- Happens only with wire bias HV on, changes event to event



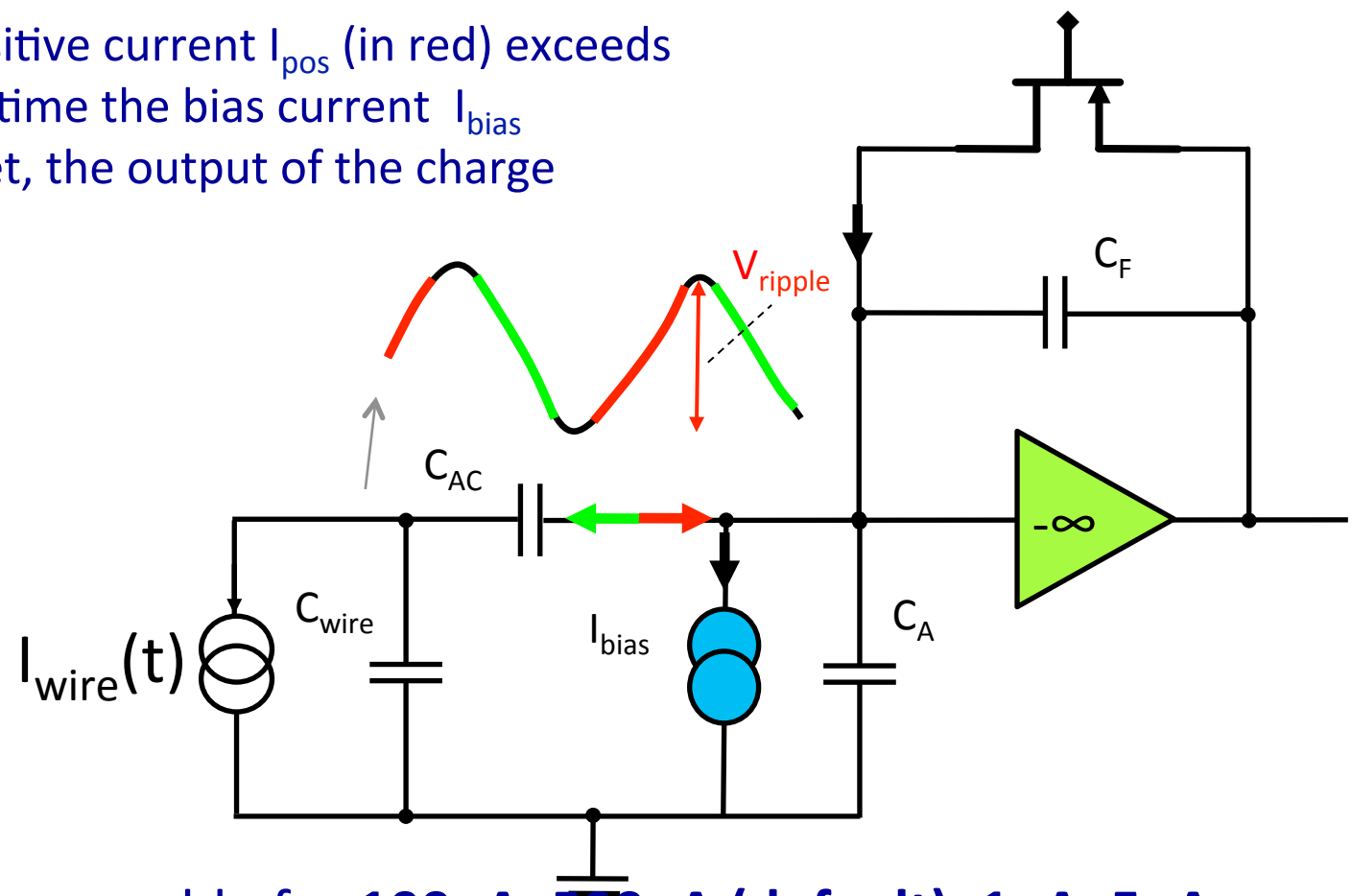
Saturation was eliminated with correct FE ASIC setting

See also:
- M. Mooney, µBooNE 4971-v1 & 4973-v1, Oct. 2015
- G. De Geronimo, µBooNE 5013-v1: "FE ASIC Charge Amplifier Reset", Nov 2015
- H. Hucheng et al., µBooNE 5117-v1: "LArASIC -5 Saturation Effects (aka “Chirping”): An Interpretation", Dec 2015

Saturation from LF Ripple on Wires

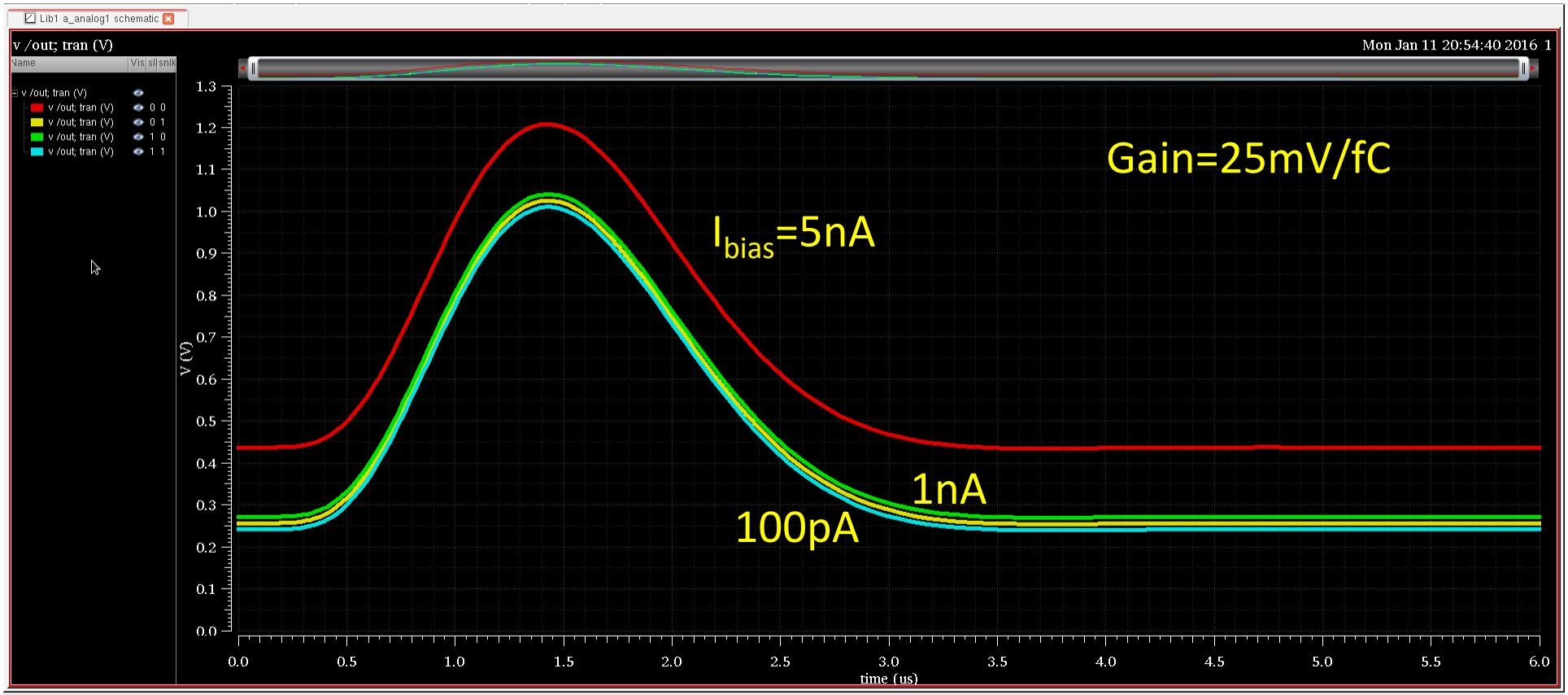
Low-frequency voltage ripple V_{ripple} on the wire (from the HV supply, from wire vibrations, or from pick-up) generates a current through C_{AC}.

If the generated positive current I_{pos} (in red) exceeds for a relatively long time the bias current I_{bias} required by the reset, the output of the charge amplifier saturates.



I_{bias} is now programmable for **100pA, 500pA (default), 1nA, 5nA**

Output Baseline Shift from High I_{bias}



Output baseline shift occurs at high I_{bias} settings and high gain

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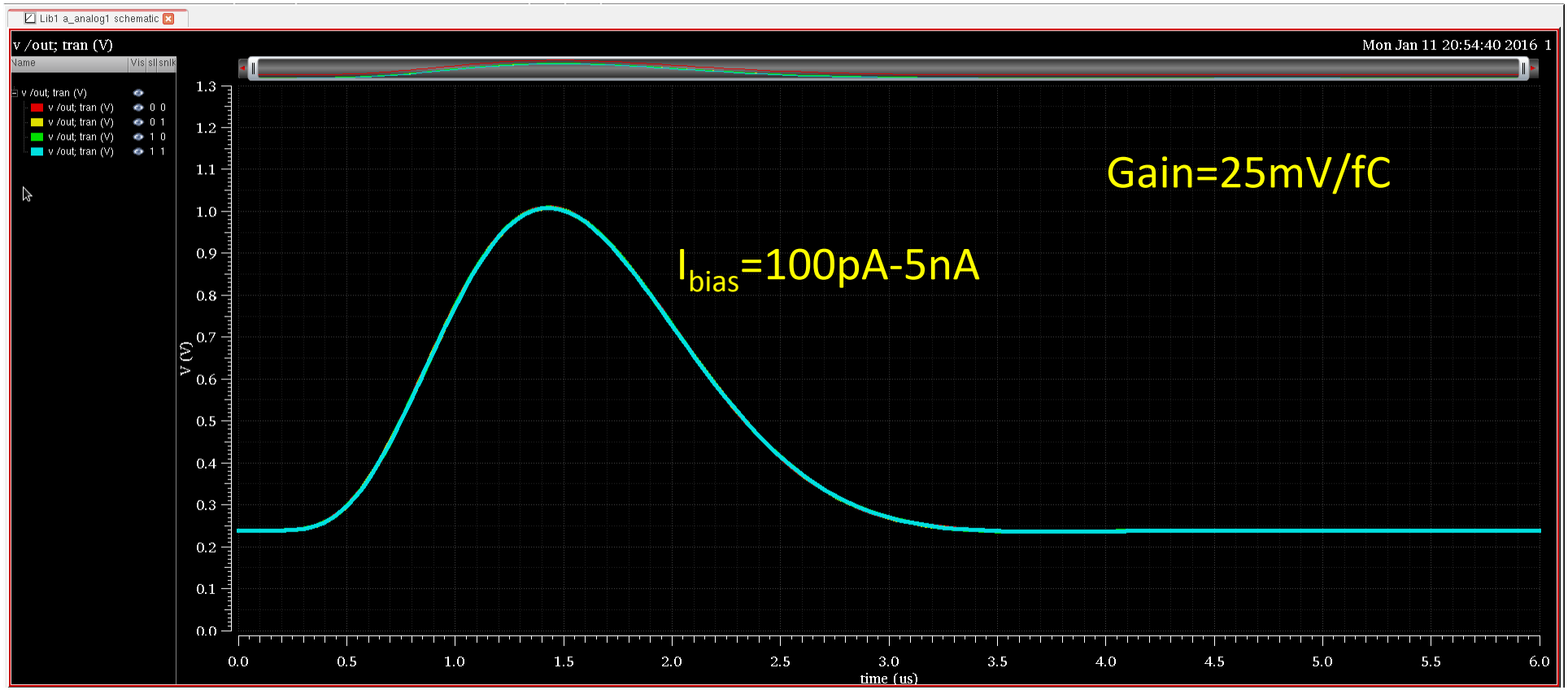
Compensated Baseline



Output baseline shift is now properly compensated

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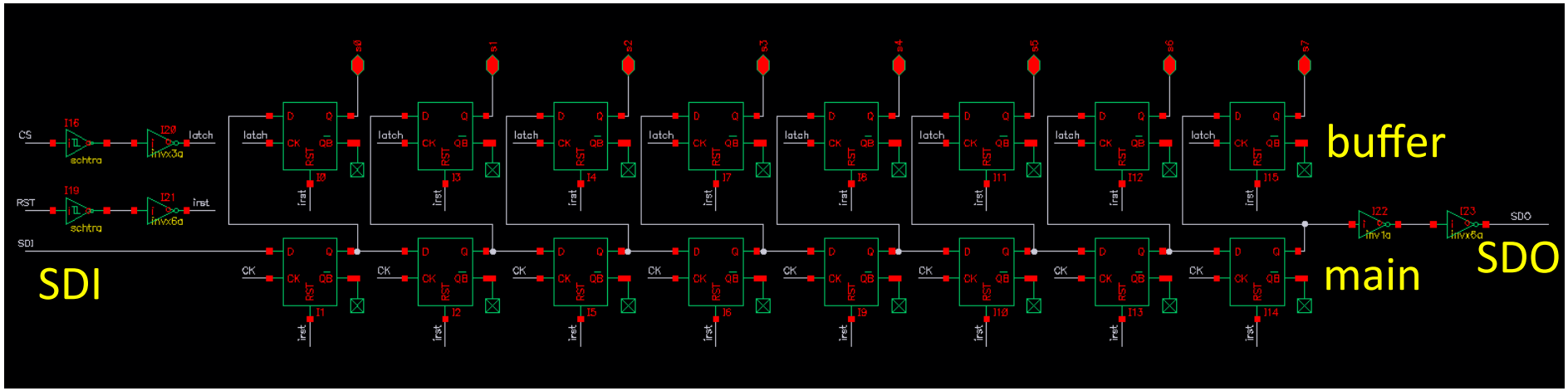
Configuration Registers



- With CS high, configuration data is shifted in the main registers
- At fall of CS, the **main register is locked** and the **data is copied to the buffer registers**
- Buffering is required to avoid abrupt changes to analog circuits
- Configuration data can be **read out at SDO by performing a second configuration cycle** identical to the first. As long as the same data is written, the system remains unchanged.
- We have been asked: which modifications are required to access also the buffer registers?

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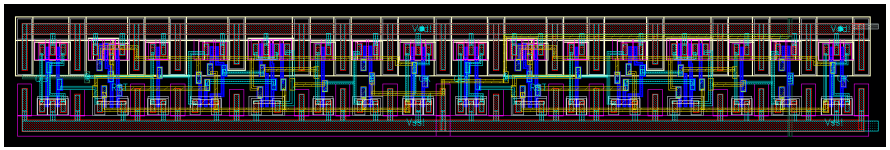
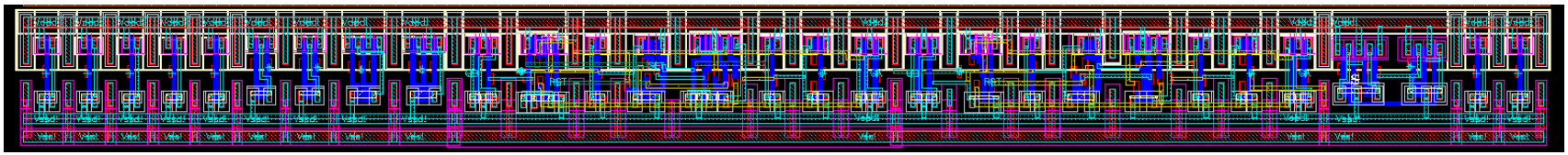
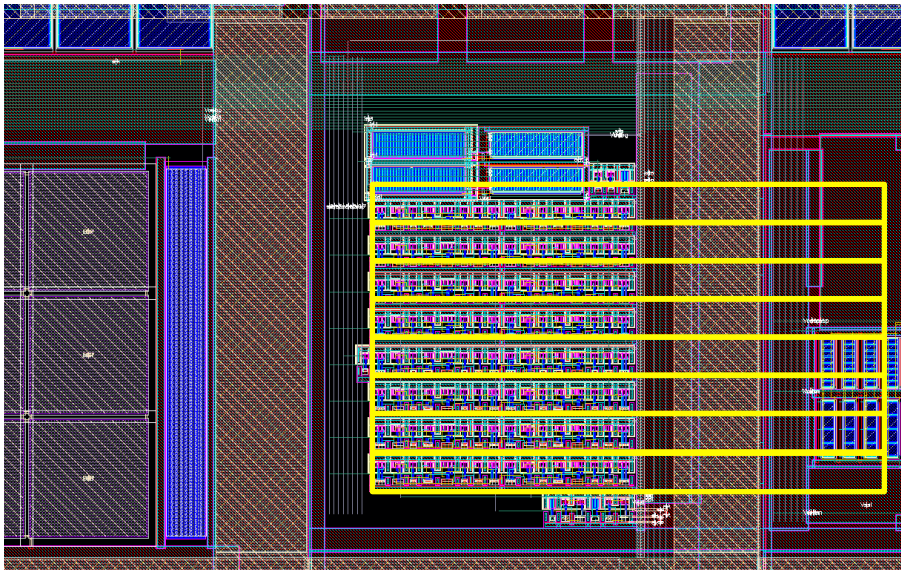
Modifications to Access the Buffer



Note from RVB: "I certainly agree that SEU† are not a serious worry for this device and that changing the design to a full read write register scheme should probably not be thought of as an absolute requirement - it seems, to me, to be more in the realm of good design practice - ***not, primarily for hardware, but software problems*** *and, especially, during the commissioning and turning on of a large system where it can give you an invaluable reality check."*

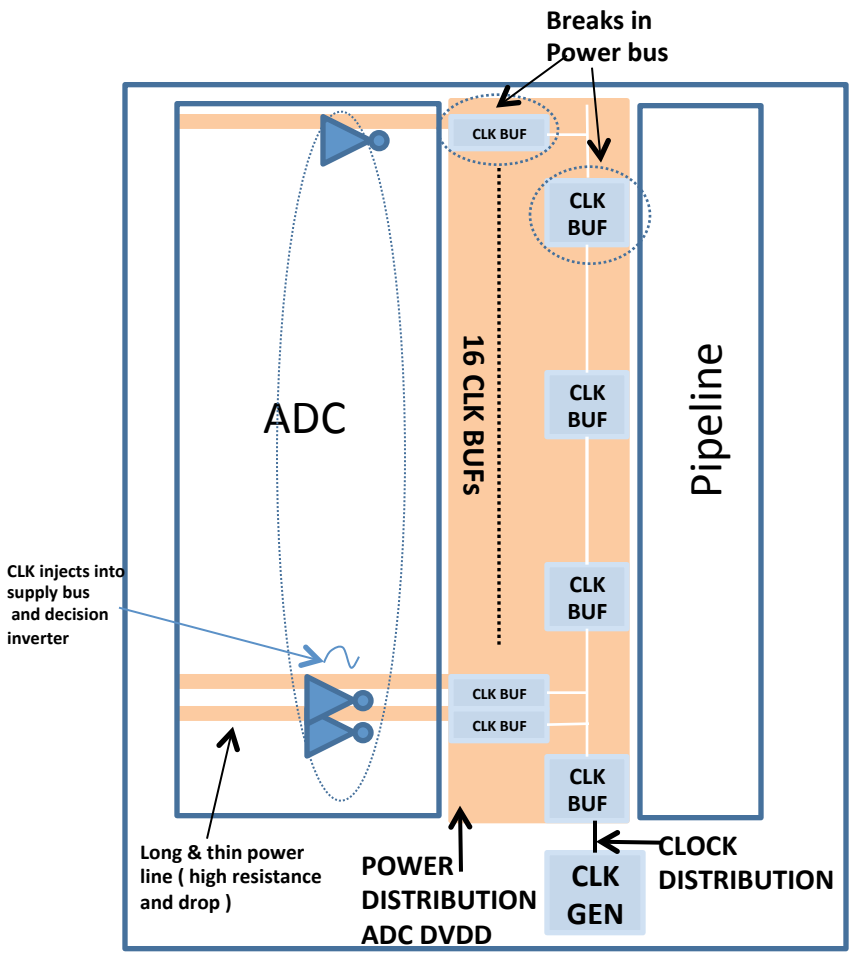




- Requires an increase of almost a factor two in the registry width
- Requires major and top-level layout modifications, with possible increase in overall size and/or impact on the analog performance
- Estimate on the order of 2 months including verifications

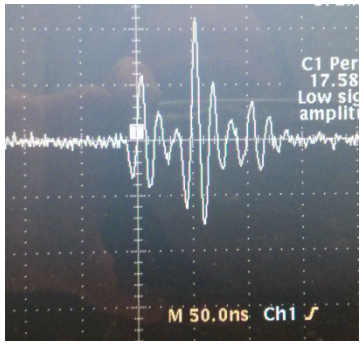
†SEU probability per ASIC: 1 flip / 100k years ($\sigma=10^{-14}$, flux=0.1, cells=144)

Power and Clock Distribution ADC Chip (VMCB)



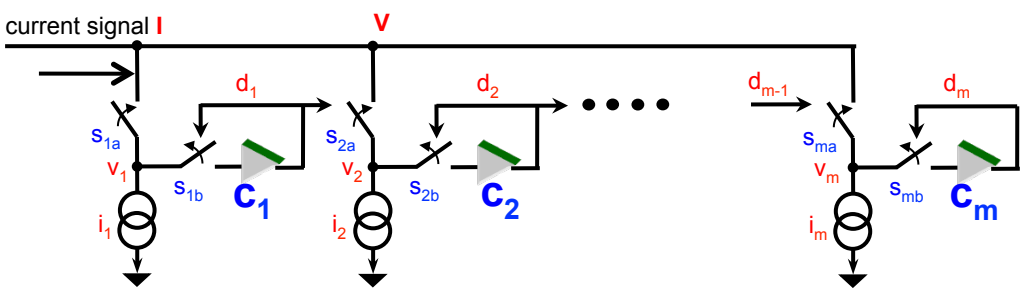
Block Diagram ADC Layout

- ADC DVDD supplies both *Clock Generator* and *Clock Buffers* and the *Decision Inverters*
- The Clock buffers are located in the power bus, creating *breaks in the power bus* and increasing the resistance of the power line.
- *Single metal layer,* long and thin supply lines run the width of the chip to power the MSBs. Resistance at the end (*180 ohms*)
- Clock buffer and generator *transitions inject* into supply causing decision inverter thresholds to move.



Supply Noise Oscilloscope

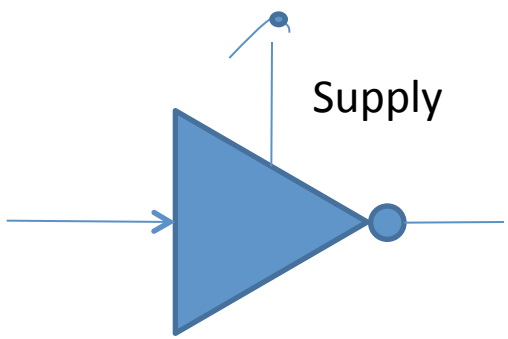
Decision Inverter



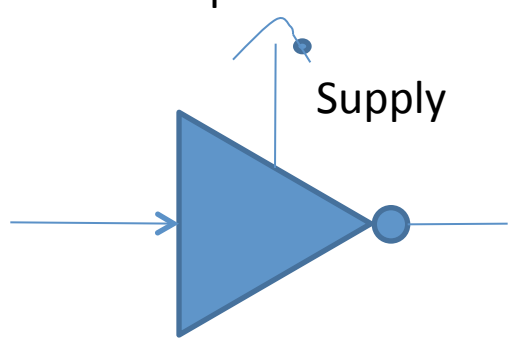
Simplified Schematic MSB/LSB Section ADC

- c_1, c_2 and c_m are the *decision inverters* acting as comparators.
- MSB (upper 6 bits) and LSB (lower 6 bits) each has 64 decision inverters.

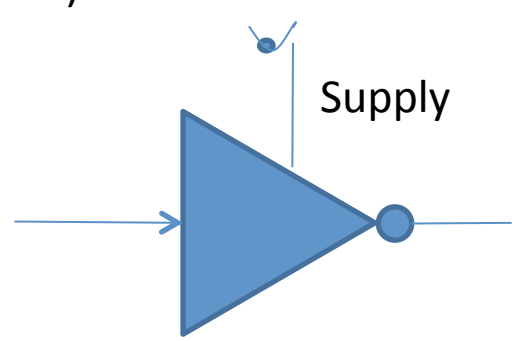
- MSB makes a decision every 64 counts.
- Noise on the supply to inverter moves the threshold of the inverter up or down.
- This results in incorrect decision. Example MSB 3 below (192)



Sampling time t=290ns DVDD = 1.82 V
Inv threshold = high
Decision = 128 counts (incorrect)

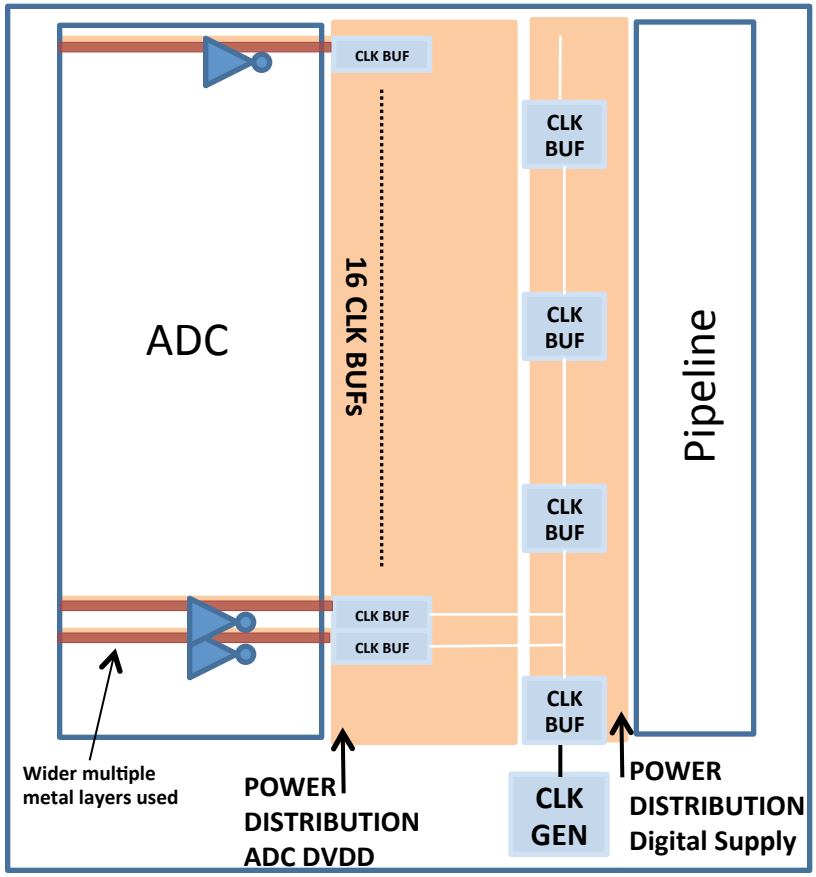


Sampling time t=1190ns DVDD = 1.8 V
Inv threshold = Set
Decision = 192 counts (correct)



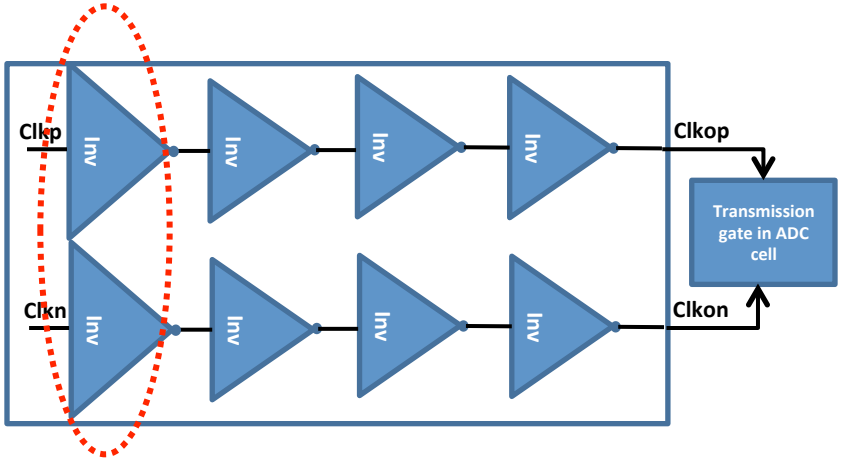
Sampling time t=2190ns DVDD = 1.78 V
Inv threshold = low
Decision = 256 counts (incorrect)

Fixes Implemented on V*



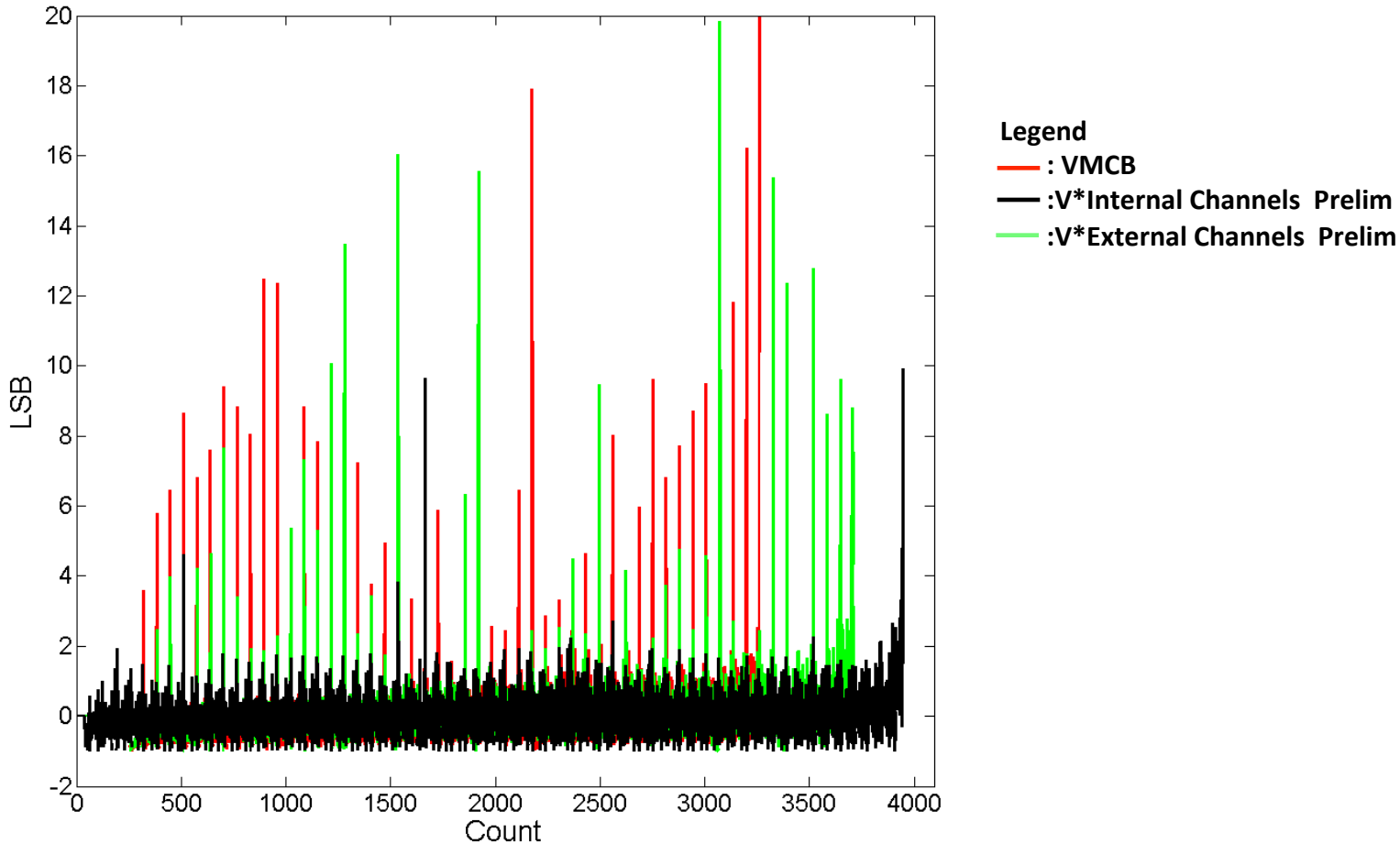
Block Diagram Modified ADC Layout

- Move clock generator and buffers to digital supply.
- Wider and unbroken power supply bus for ADC DVDD.
- Use multiple metal layers to supply power across the chip to MSBs.
- Replace Schmitt trigger in the clock buffer with Inverter



Modified clock Buffer

Measurement Results LN2



- **Preliminary results show improved performance over VMCB.**
- **Internal channels exhibit a considerable improvement in DNL.**
- **With the given power limitation and speed specification the achieved results are very close to the technology limit without adding complex error-correction circuitry**
- **External channels, even though much improved, still show several residual spikes.**
- **Data is still being collected and the issue being investigated.**
- **Further improvements have been integrated and simulations are being done.(parasitics and mismatch)**