ADC performance in bench tests

BNL DUNE

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Updated Dec 1 1830

Introduction

I started looking at ADC data taken at BNL

- Same data that Xin has shown in these meetings
- Explanation of data here:
  - http://www.phy.bnl.gov/~chc/LArTPC/ADCASIC/20161014
- Many ADC samples are read out for voltage steps
  - Approximately 3-4 steps with 200+ samples for each ADC bin
- Data does not include the full waveforms
  - Instead, the number of samples for each ADC bin (0, 1, …, 4095) and voltage step
- Data for two ADC versions: VSTAR and P1
  - 35-ton used an earlier version
- Data taken under different conditions
  - Warm (room temp) and cold (LN2)
  - Different sampling rates (1 and 2 MHz)
  - I show results for 2 MHz cold

Samples

Samples are summarized in table:

Name	
Oct VSTAR	VSTAR_1S/LN2_vstar_1s_200MHz_vstar_adc_09_28_2016_15_03_35
Oct P1	P1_ADC_DIE1/LN2_die1_200MHz_p1_adc_09_27_2016_19_18_27
Nov VSTAR	Vstar_old/LN_2MHz/CSV/Vstar_B-2_ADC6_LN_2MHz…
Nov P1 clkint	P1_die1/intClk_full_LN_2MHz/CSV
Nov P1 clkfac	P1_die1/extClk_factory_full_LN_2MHz/CSV
Nov P1 clklvd	P1_die1/extClk_LVdefault_full_LN_2MHz/CSV

Notes:

- Oct data was taken with voltage steps of 0.1 mV over (0, 1700) mV
- Nov data was taken with a sawtooth from -50 to 1800 mV
- External clock indicated with clkfac and clklvd. Others samples use internal clock.

Data taking

Data taken by the following team

- Hucheng Chen, Shanshan Gao, Jack Fried (BNL)
- Damian Goeldi (Univ. of Bern)

Thanks to them to making this data available to me

Data format

- I get a summary table show the number of samples in V_{in}-ADC bins
- I have not yet seen the raw wave form data
  - I would like to get this to study stuck bit time coherence
  - And perhaps to improve the V_{in} precision

Response

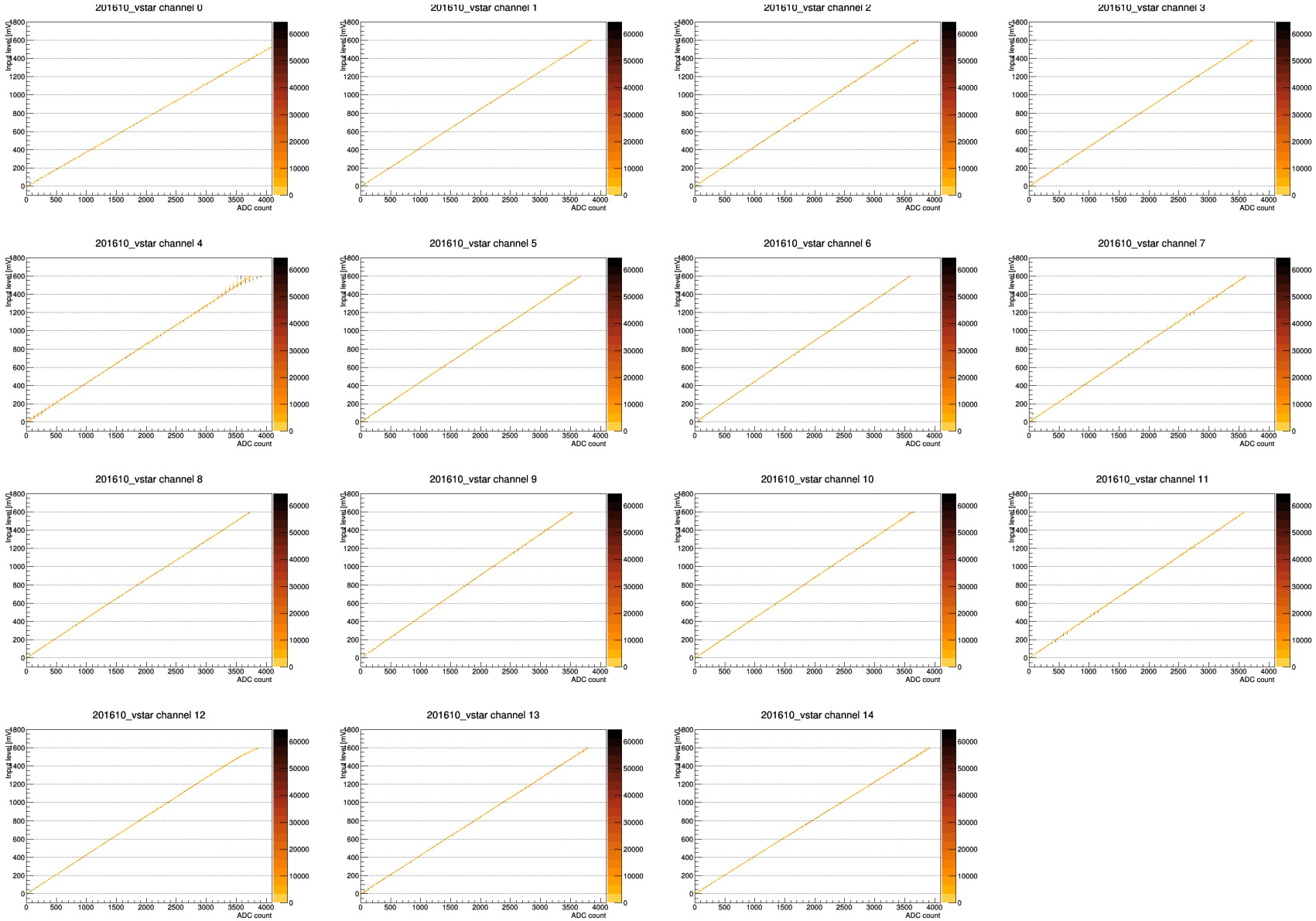
Following slides have response plots

- Input signal vs. ADC signal
- For all samples
- Followed by the same zooming in on the low end

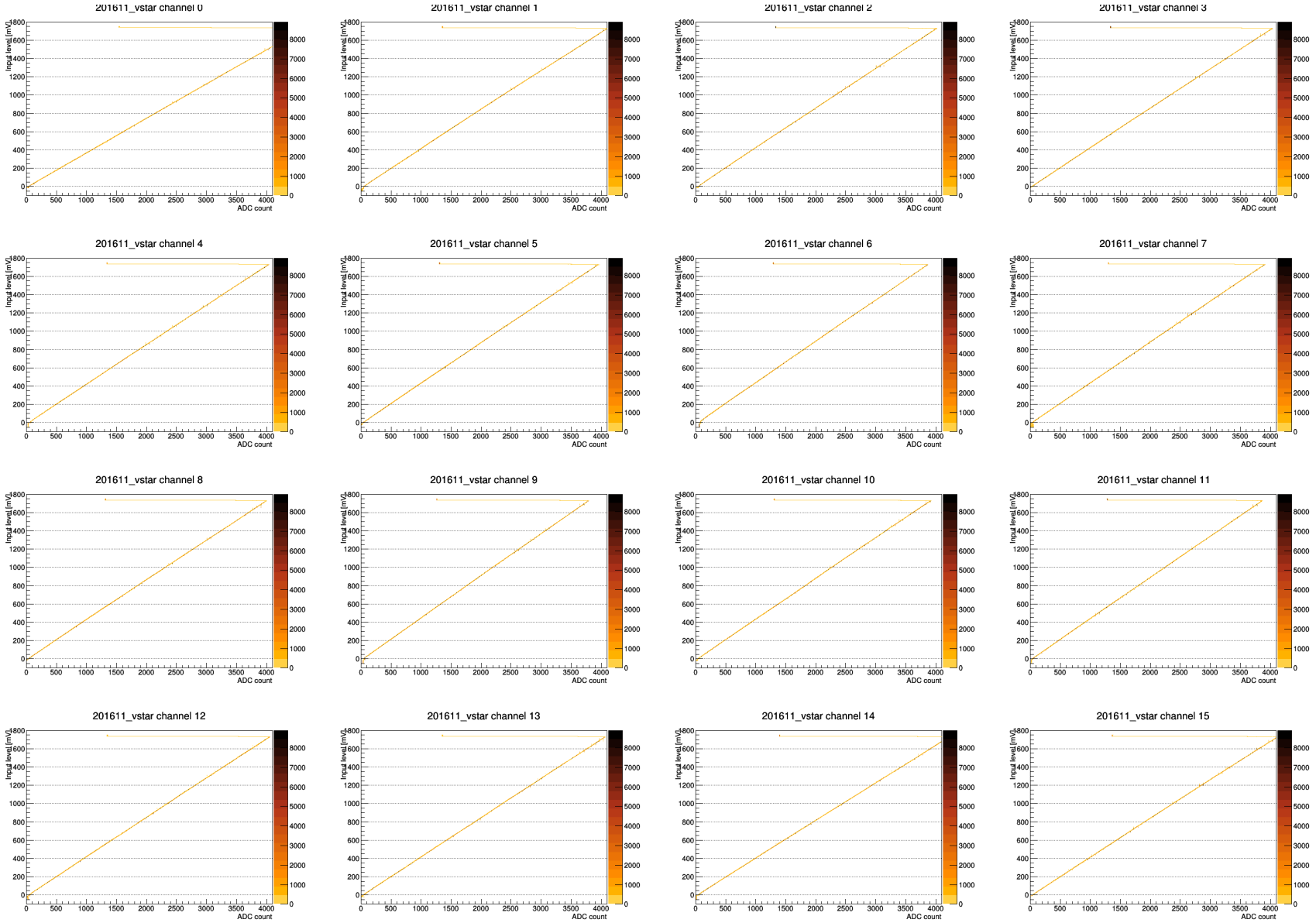
Comments

- Plots look linear by eye (fits coming later)
- Nov VSTAR shows that overflows are not handled properly
  - Response fold back to in-range values
- Zooms show problems at the low end
  - VSTAR below 128
  - P1 with internal clock out to 200
  - P1 with external clock below 64

Oct VSTAR


201610_vstar channel 0
201610_vstar channel 1
201610_vstar channel 2
201610_vstar channel 3
201610_vstar channel 4
201610_vstar channel 5
201610_vstar channel 6
201610_vstar channel 7
201610_vstar channel 8
201610_vstar channel 9
201610_vstar channel 10
201610_vstar channel 11
201610_vstar channel 12
201610_vstar channel 13
201610_vstar channel 14
Input level [mV]
ADC count

Nov VSTAR


201611_vstar channel 0
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201611_vstar channel 2
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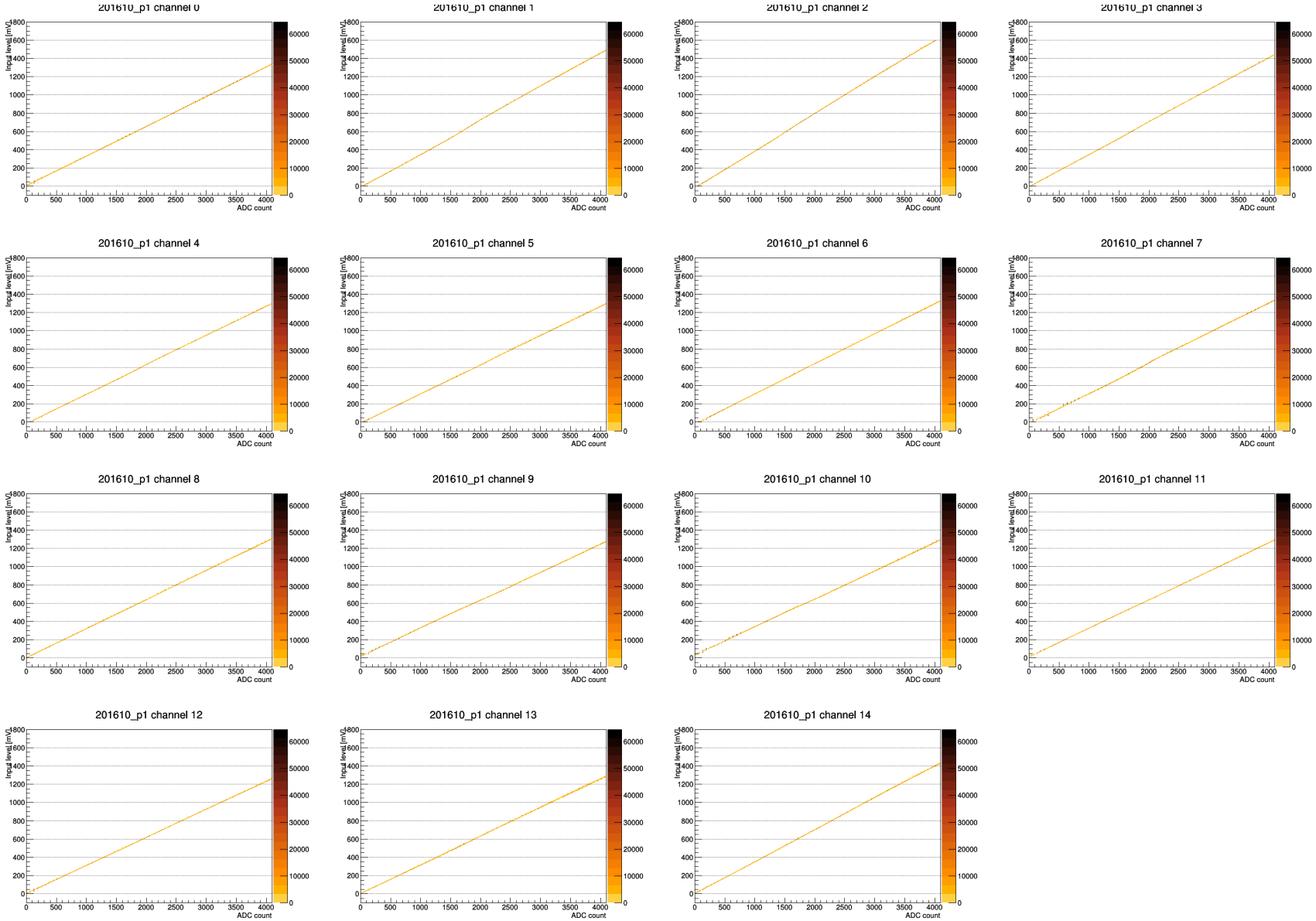
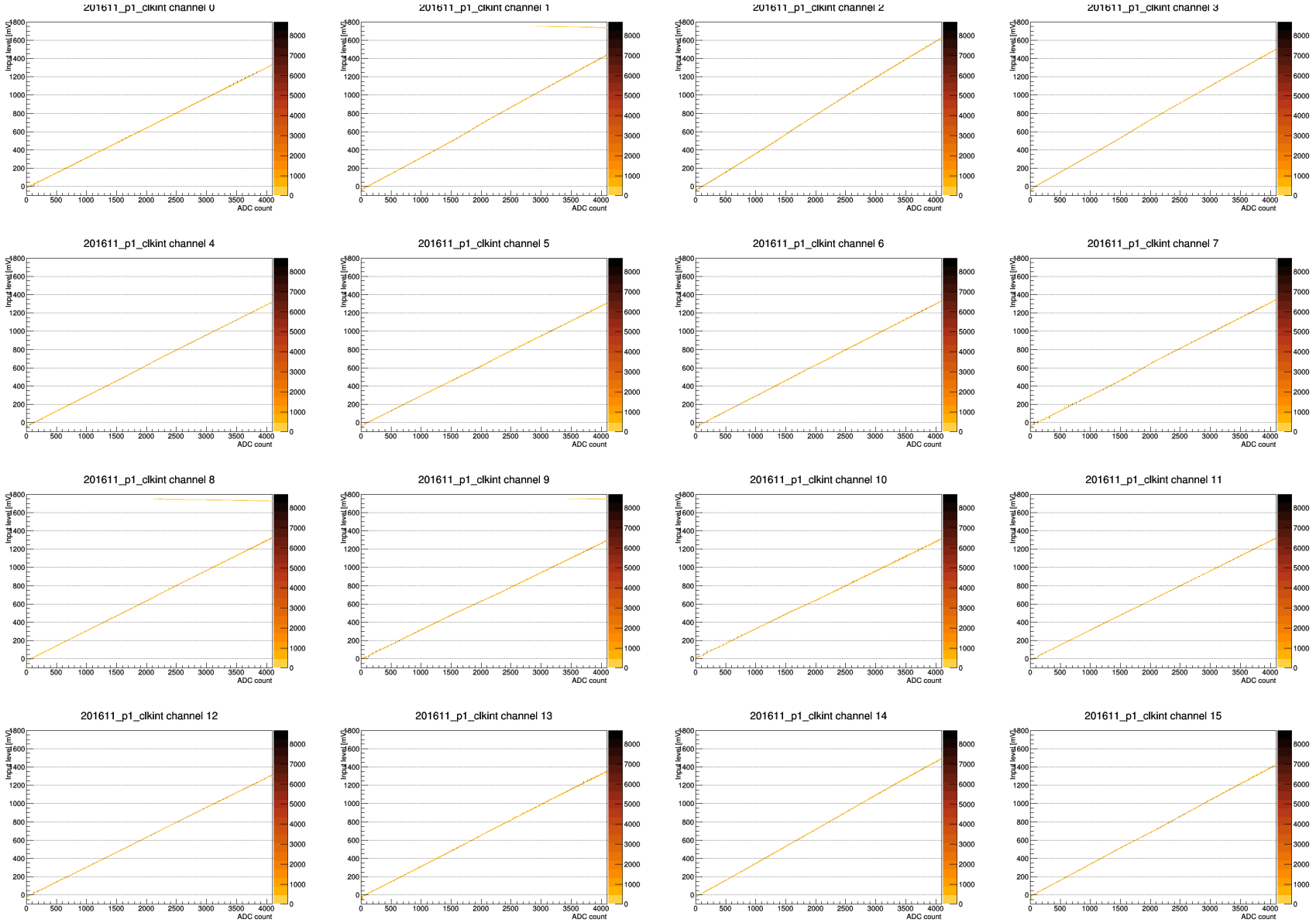
201611_vstar channel 5
201611_vstar channel 6
201611_vstar channel 7
201611_vstar channel 8
201611_vstar channel 9
201611_vstar channel 10
201611_vstar channel 11
201611_vstar channel 12
201611_vstar channel 13
201611_vstar channel 14
201611_vstar channel 15
Input level [mV]
ADC count

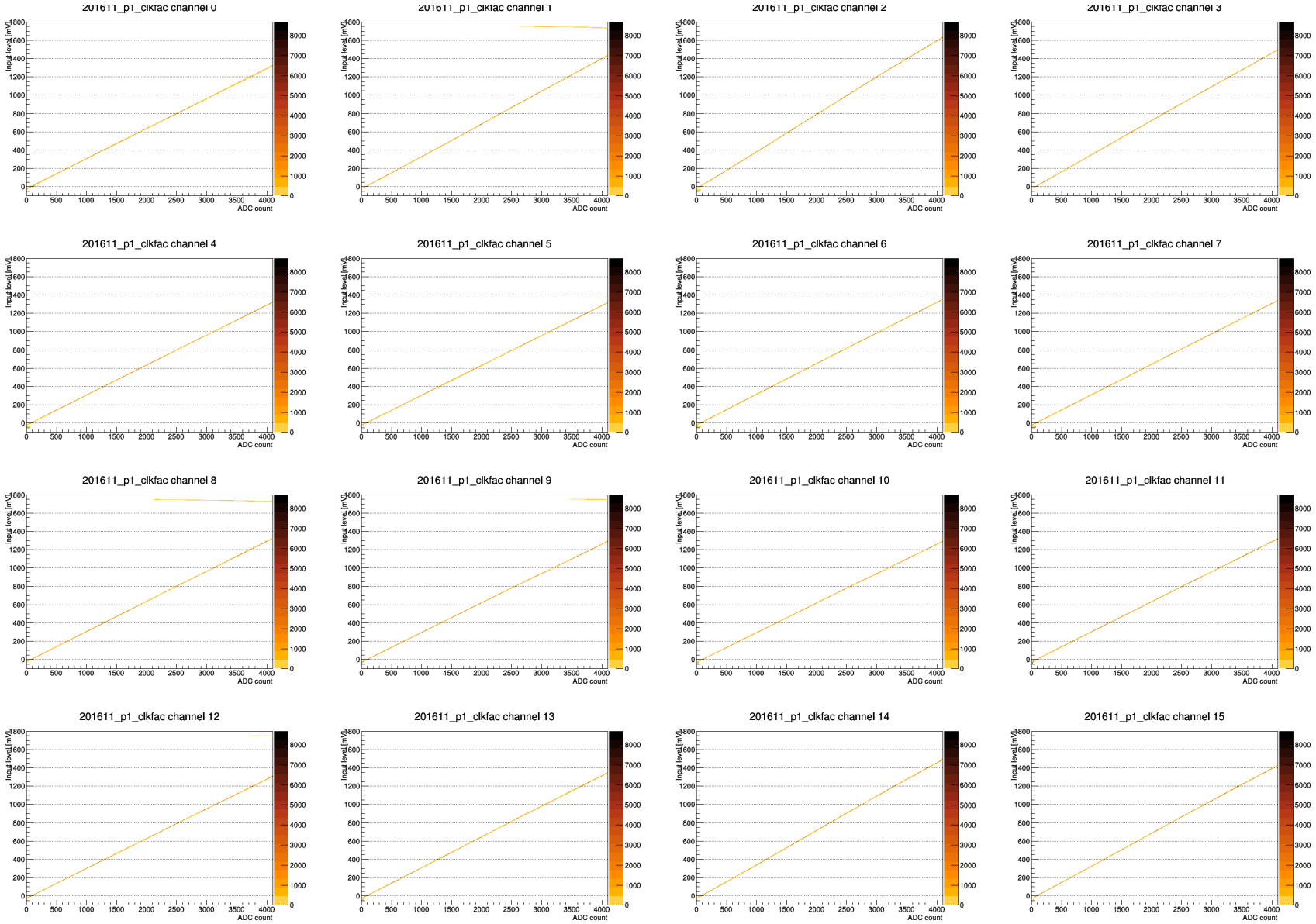
Oct P1


201610_p1 channel 0
201610_p1 channel 1
201610_p1 channel 2
201610_p1 channel 3
201610_p1 channel 4
201610_p1 channel 5
201610_p1 channel 6
201610_p1 channel 7
201610_p1 channel 8
201610_p1 channel 9
201610_p1 channel 10
201610_p1 channel 11
201610_p1 channel 12
201610_p1 channel 13
201610_p1 channel 14
Input level [mV]
ADC count

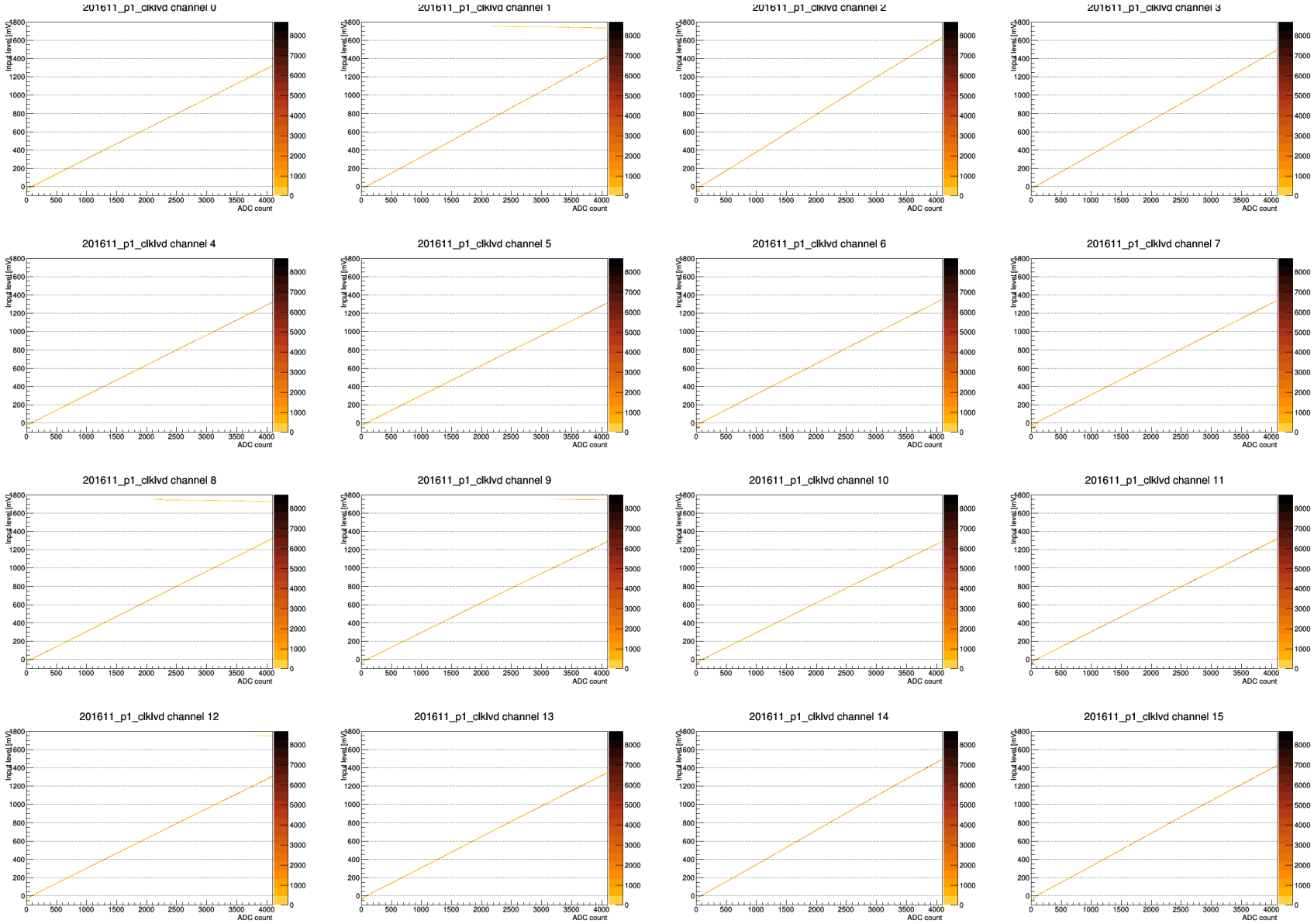
Nov P1 clkint



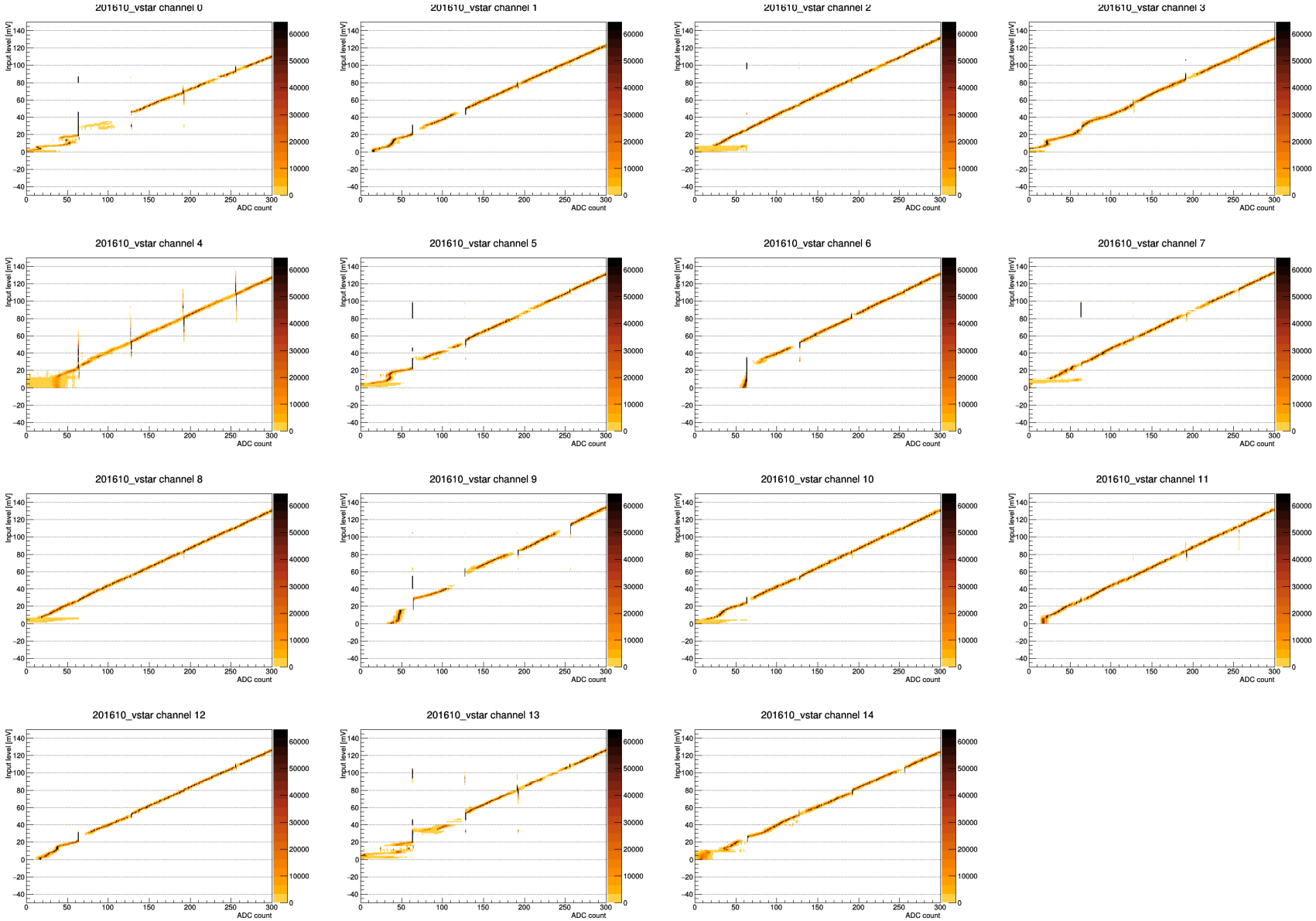
Nov P1 clkfac



Nov P1 clklvd



Oct VSTAR


201610_vstar channel 0
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201610_vstar channel 4
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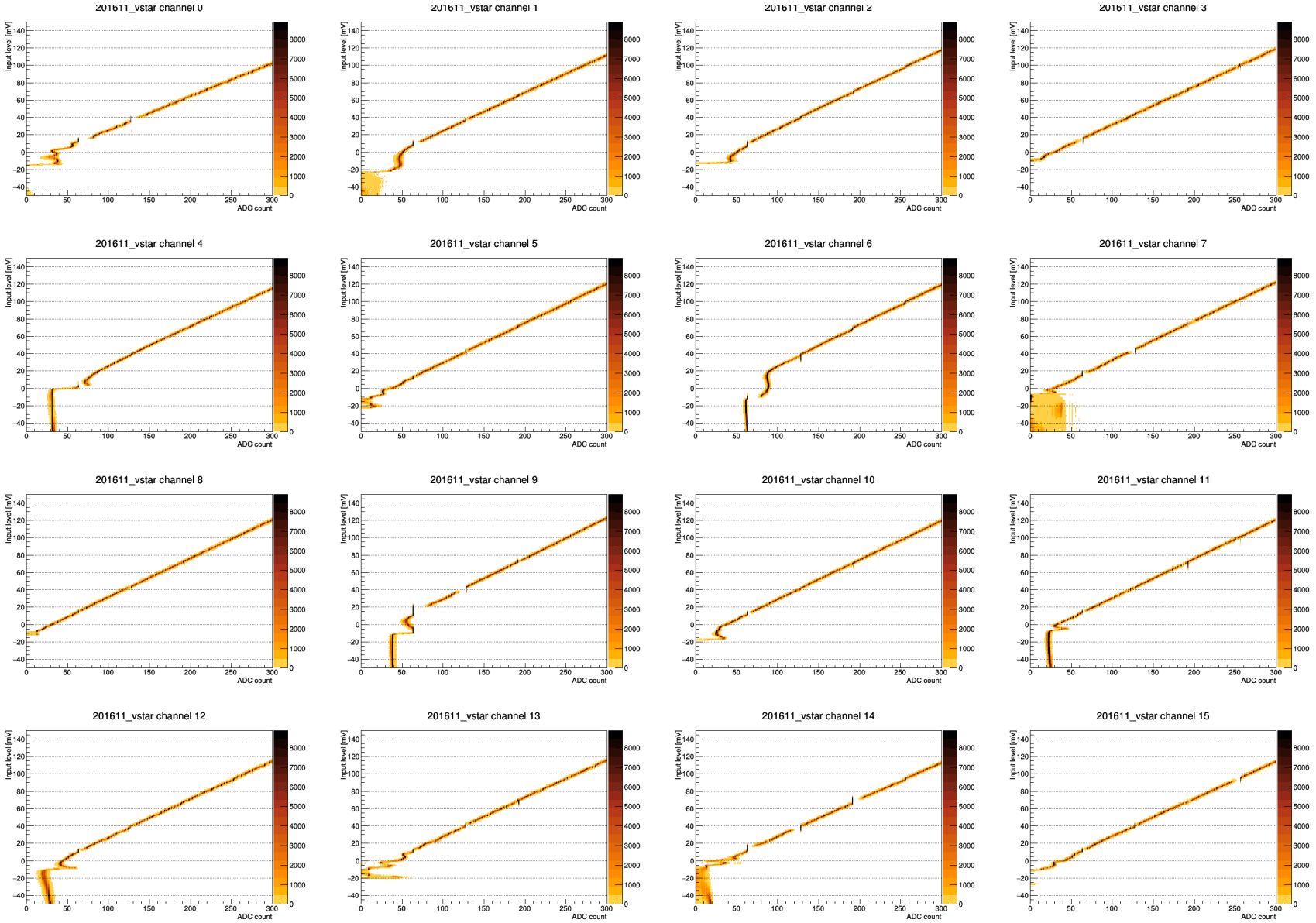
201610_vstar channel 7
201610_vstar channel 8
201610_vstar channel 9
201610_vstar channel 10
201610_vstar channel 11
201610_vstar channel 12
201610_vstar channel 13
201610_vstar channel 14
Input level [mV]
ADC count

Nov VSTAR


201611_vstar channel 0
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201611_vstar channel 4
201611_vstar channel 5
201611_vstar channel 6
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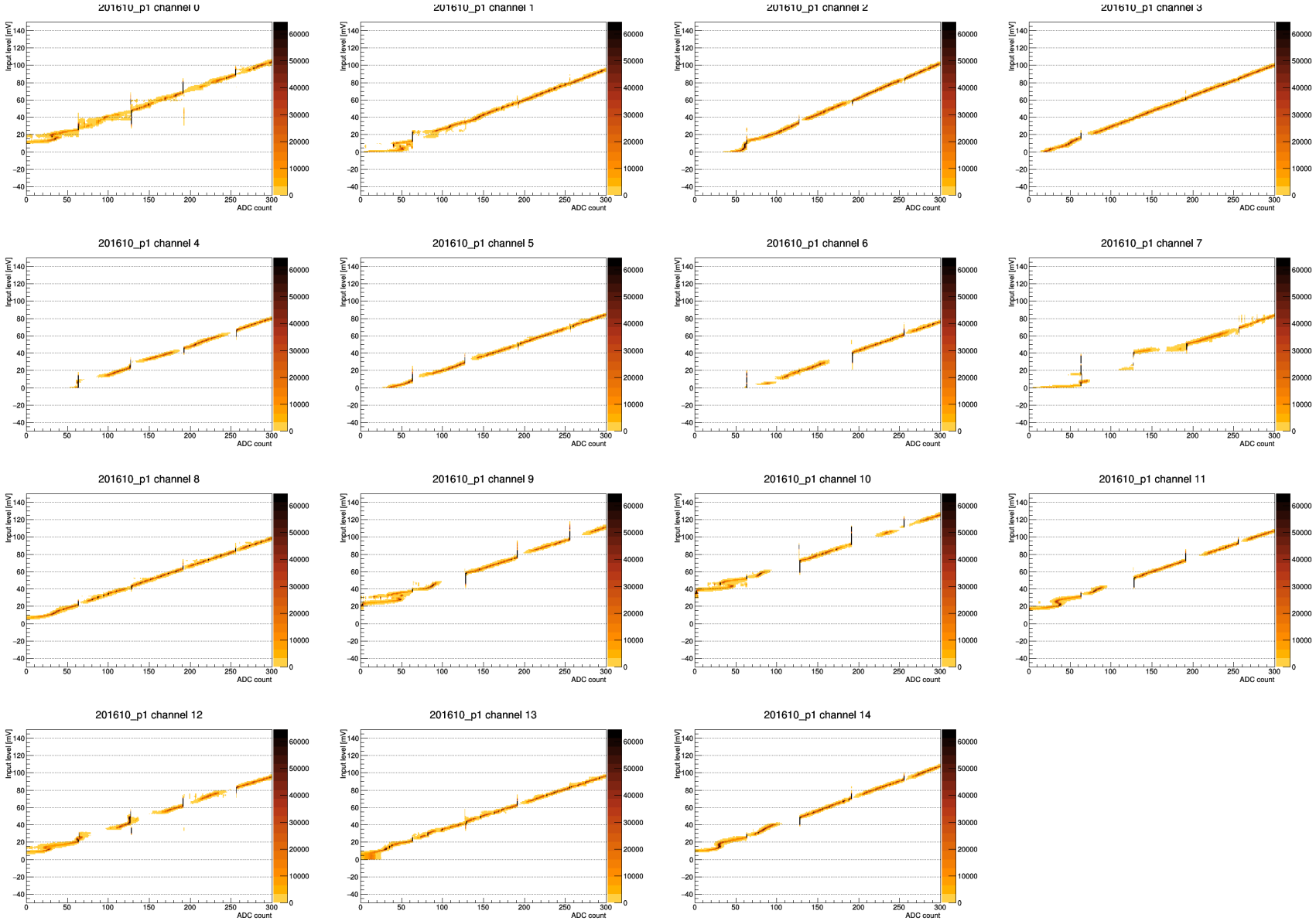
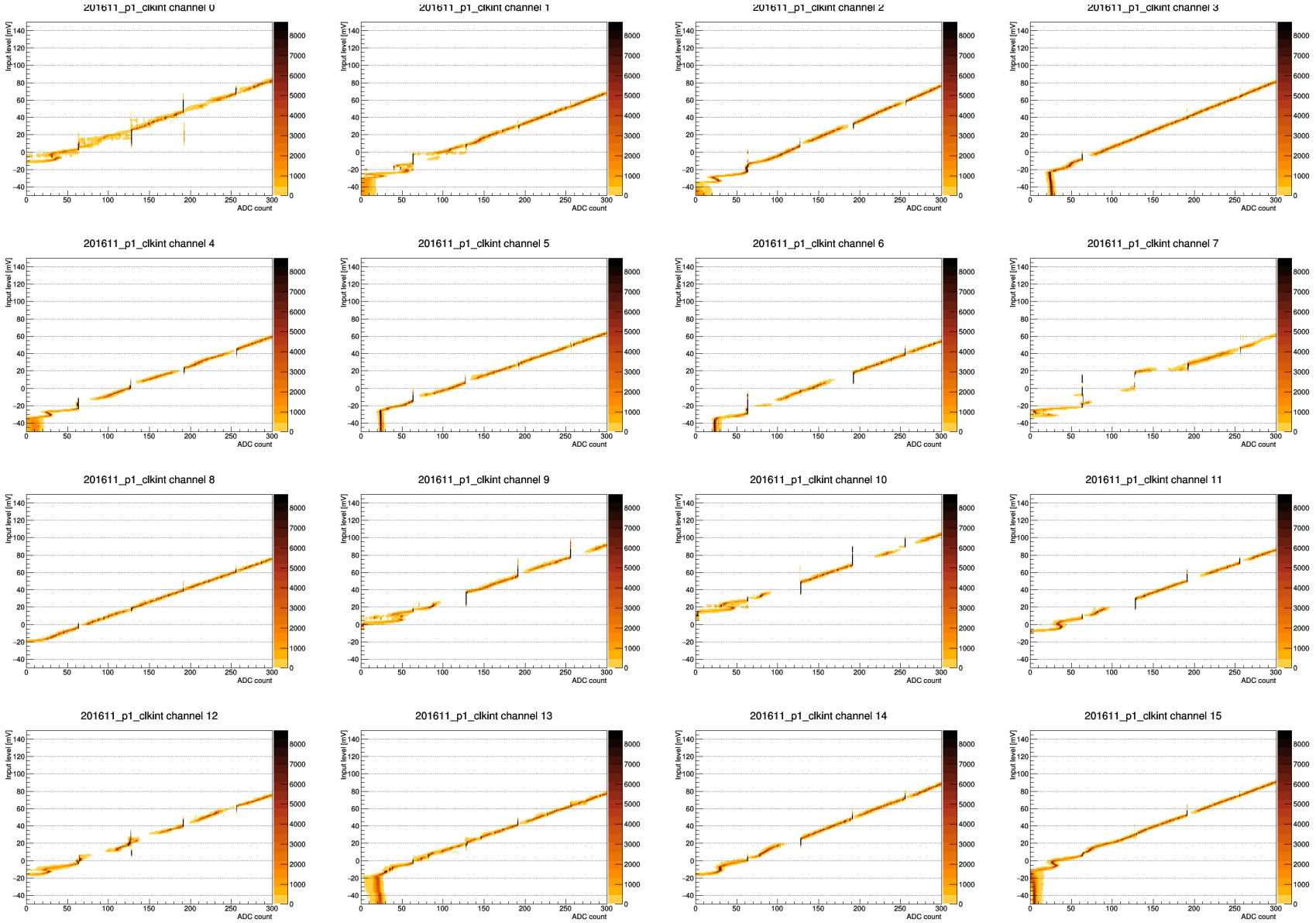
201611_vstar channel 9
201611_vstar channel 10
201611_vstar channel 11
201611_vstar channel 12
201611_vstar channel 13
201611_vstar channel 14
201611_vstar channel 15
Input level [mV]
ADC count

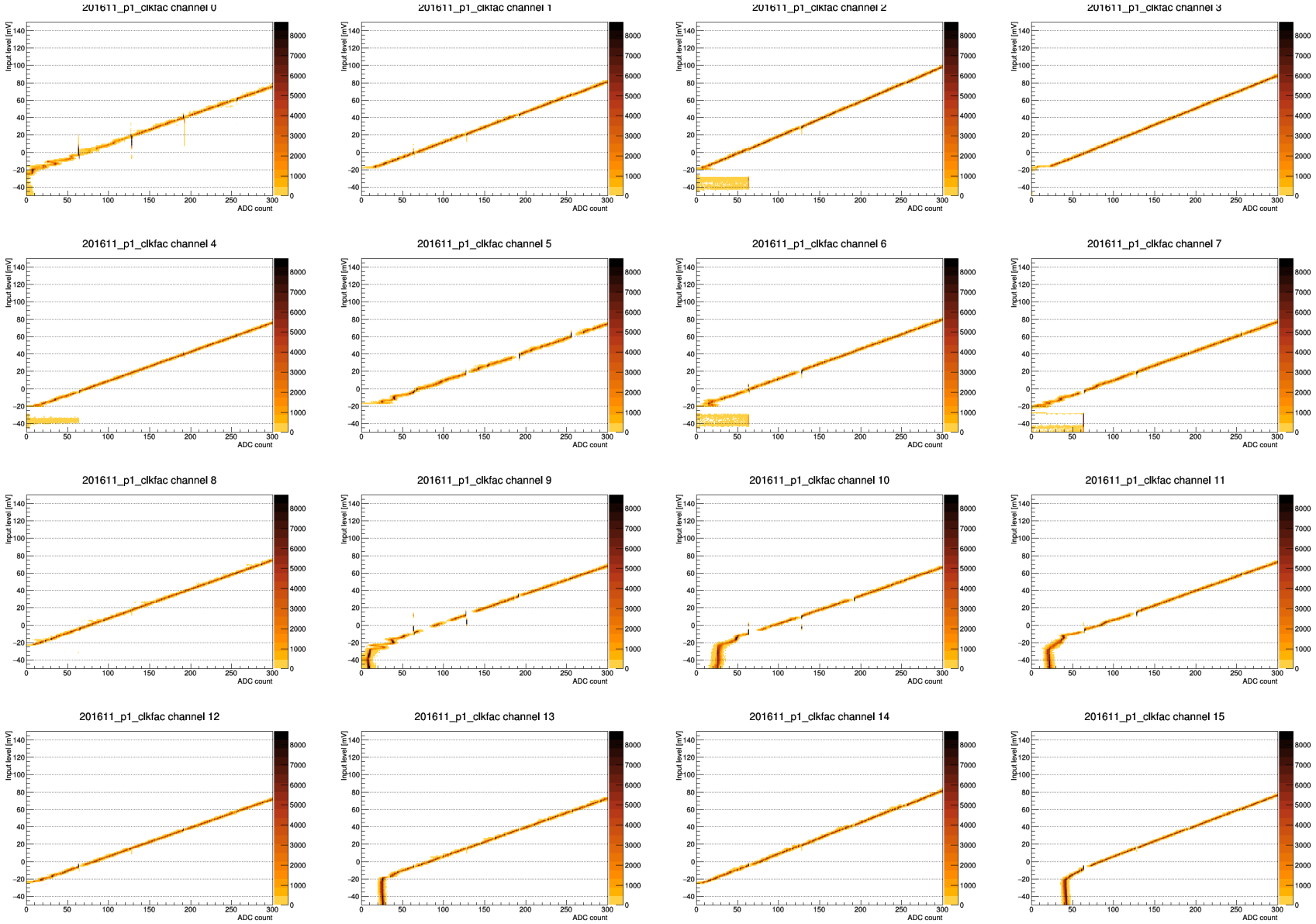
Oct P1


201610_p1 channel 0
201610_p1 channel 1
201610_p1 channel 2
201610_p1 channel 3
201610_p1 channel 4
201610_p1 channel 5
201610_p1 channel 6
201610_p1 channel 7
201610_p1 channel 8
201610_p1 channel 9
201610_p1 channel 10
201610_p1 channel 11
201610_p1 channel 12
201610_p1 channel 13
201610_p1 channel 14
Input level [mV]
ADC count

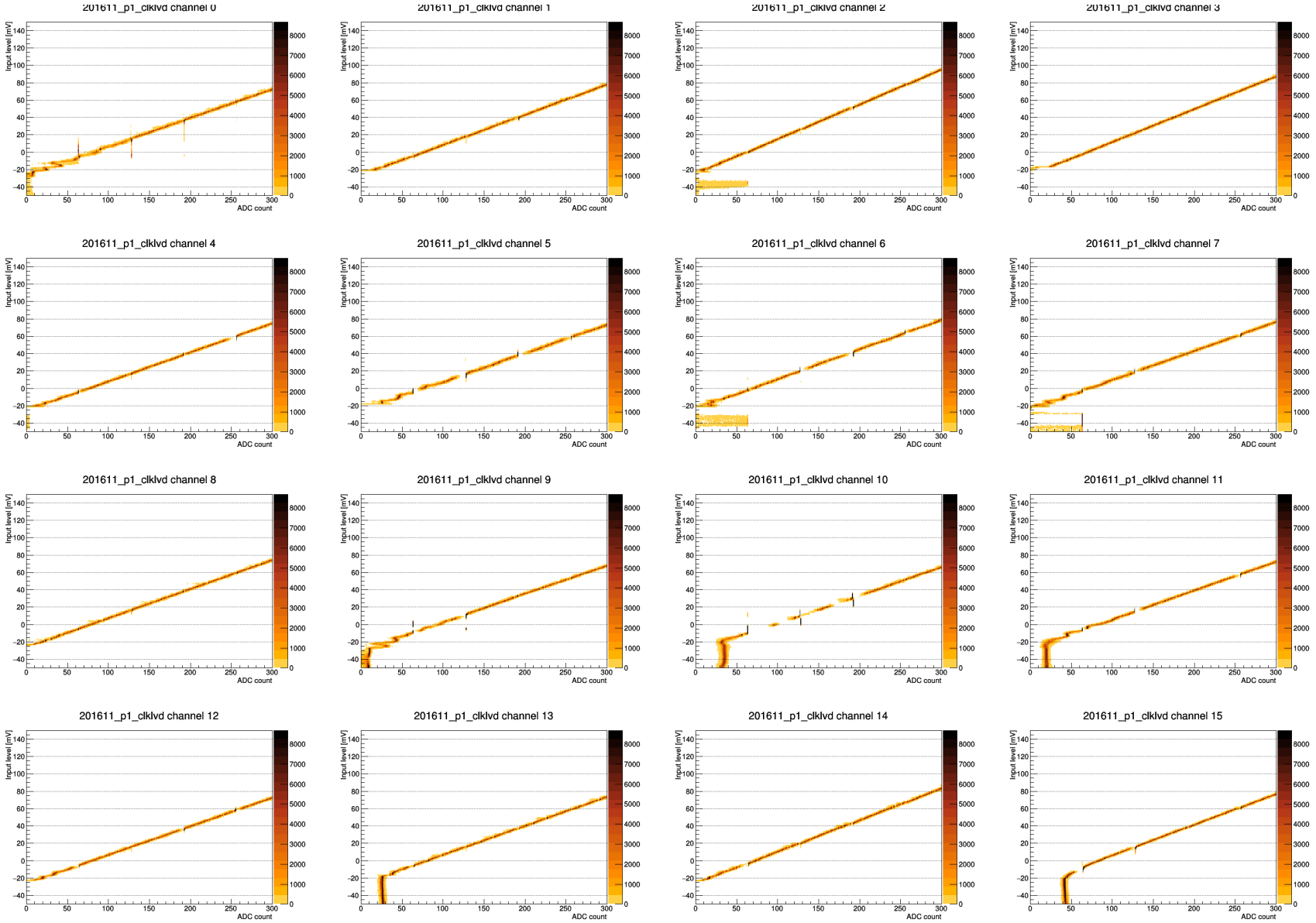
Nov P1 clkint



Nov P1 clkfac



Nov P1 clklvd

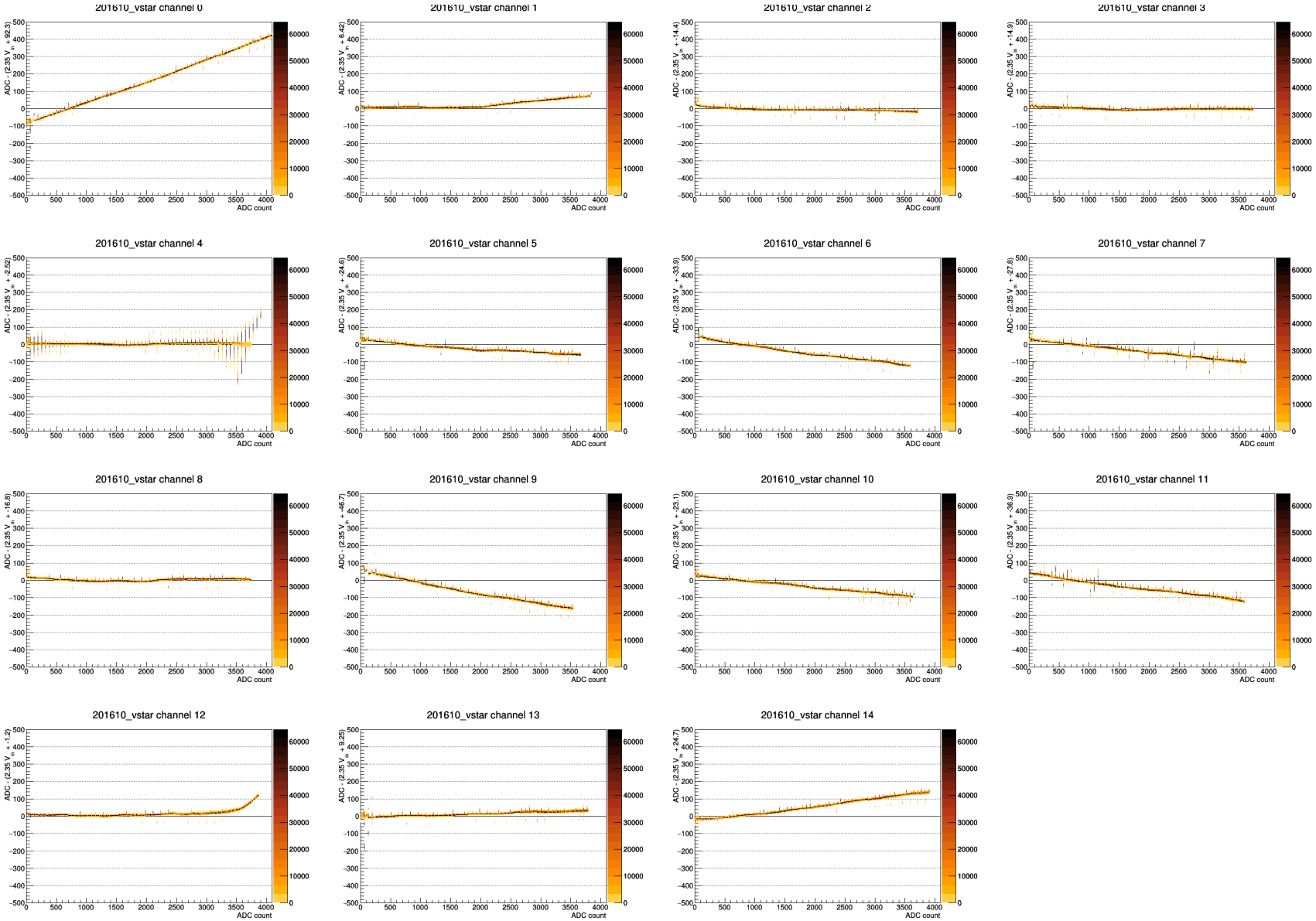


Nominal performance

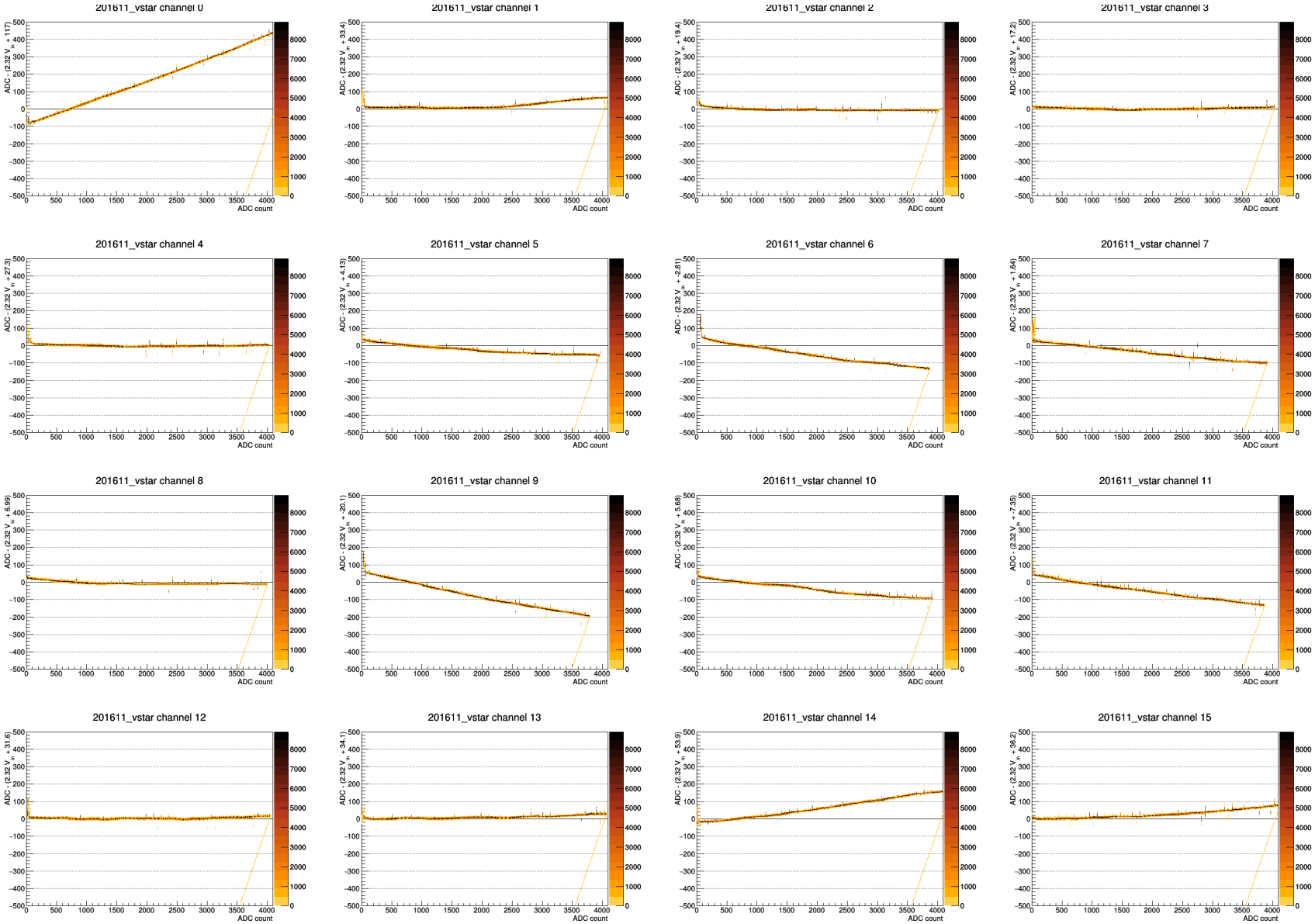
First assess performance using current reco strategy

- Expected ADC count is offset plus gain times V_{in}
- Gain is assumed the same for all channels
- Gain here is obtained by averaging the values obtain for each channel
  - See linear fits later in the talk
- Pedestal chosen to make expected ADC match true value at 750
- Plots show the difference between observed and predicted values as a function of ADC count

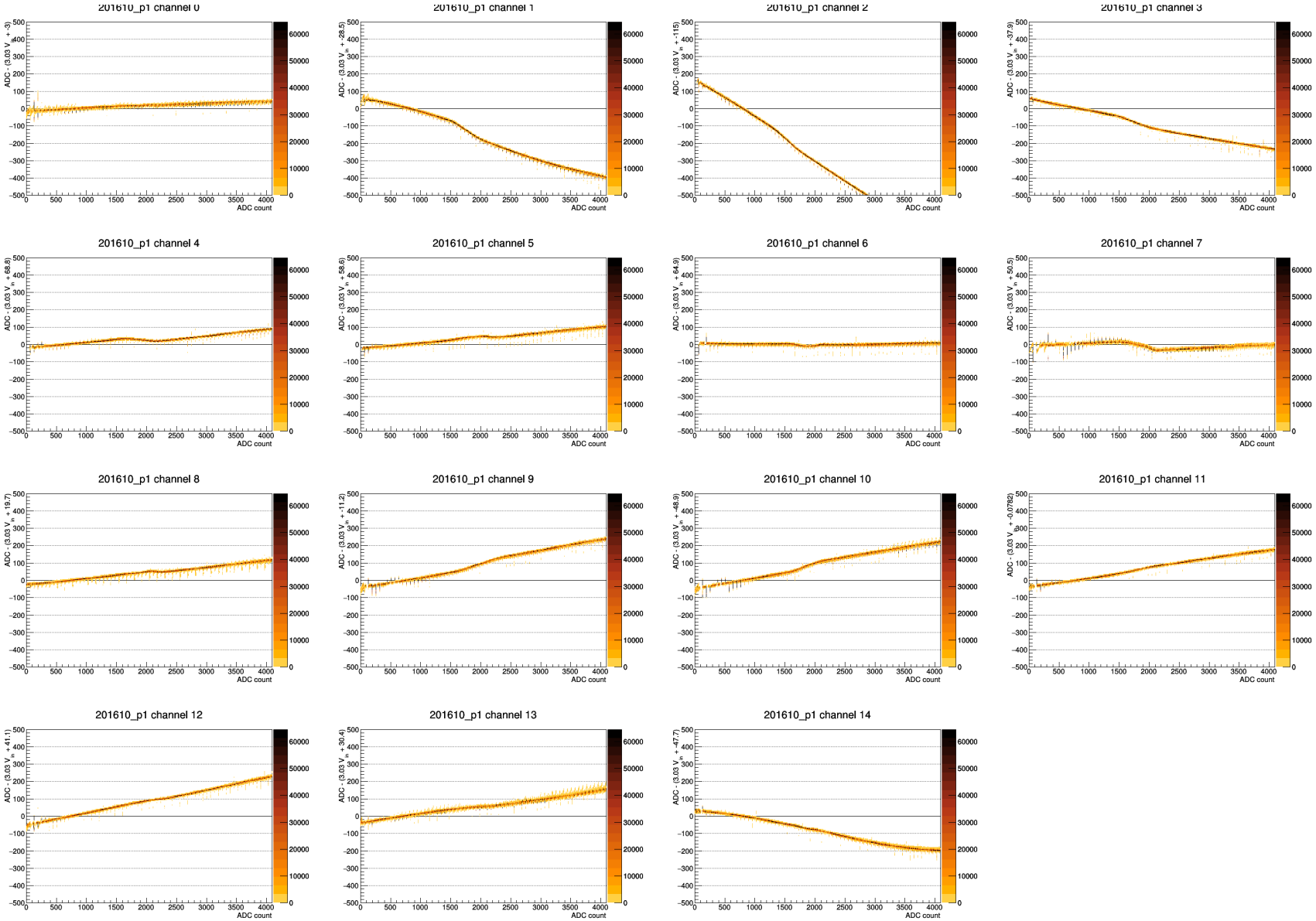
Oct VSTAR nominal residuals



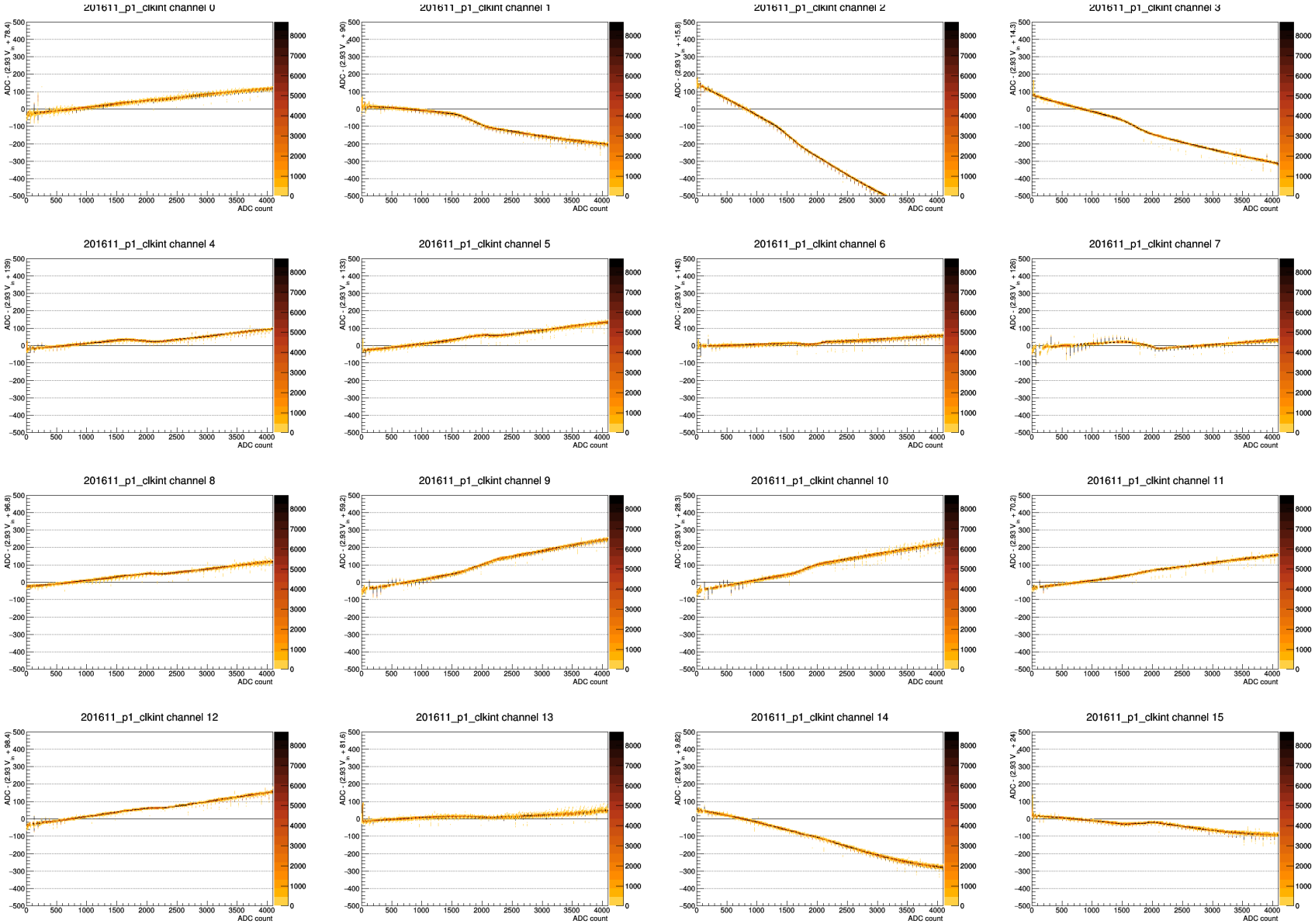
Nov VSTAR nominal residuals



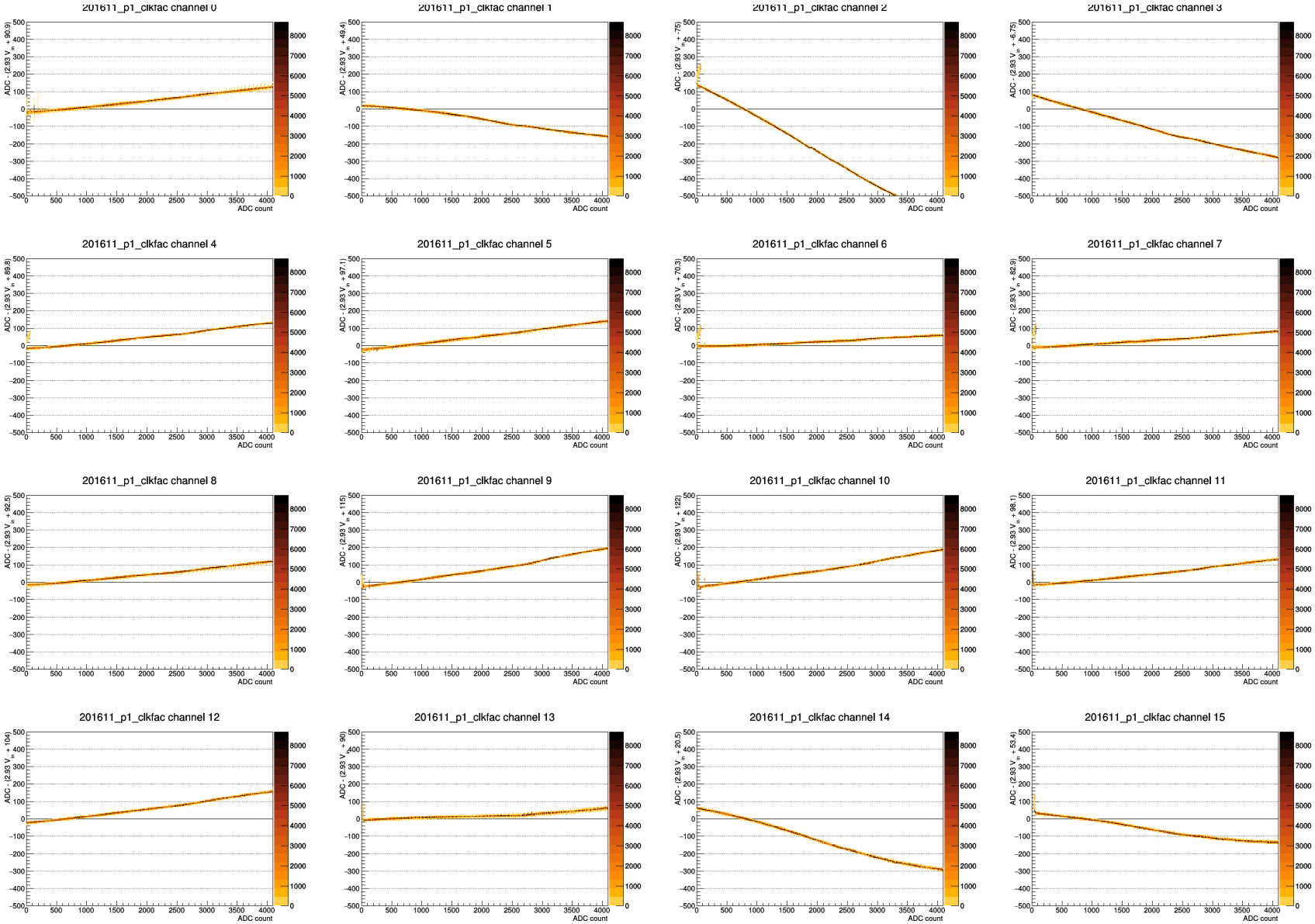
Oct P1 nominal residuals



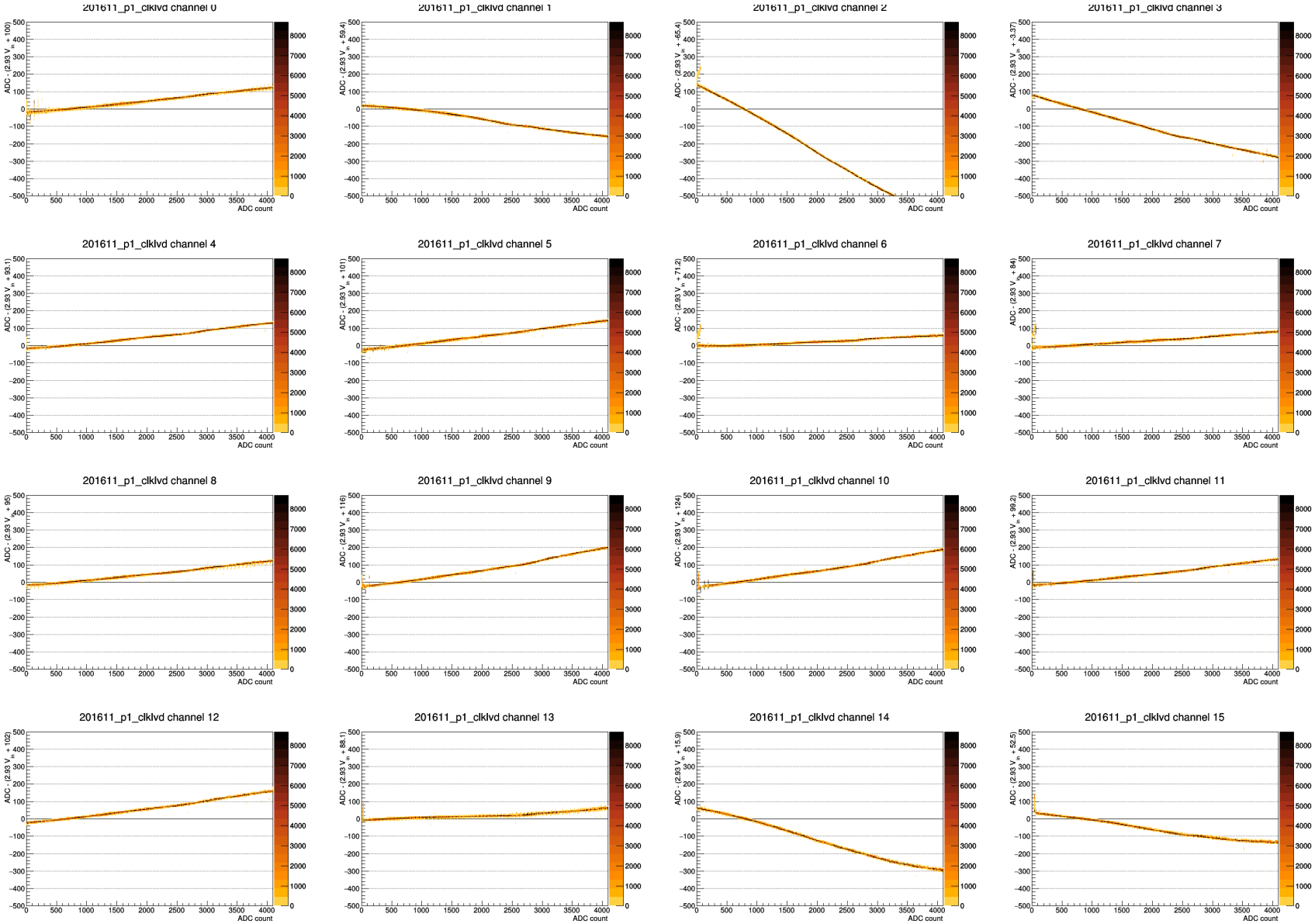
Nov P1 clkint nominal residuals



Nov P1 clkfac nominal residuals



Nov P1 clklvd nominal residuals

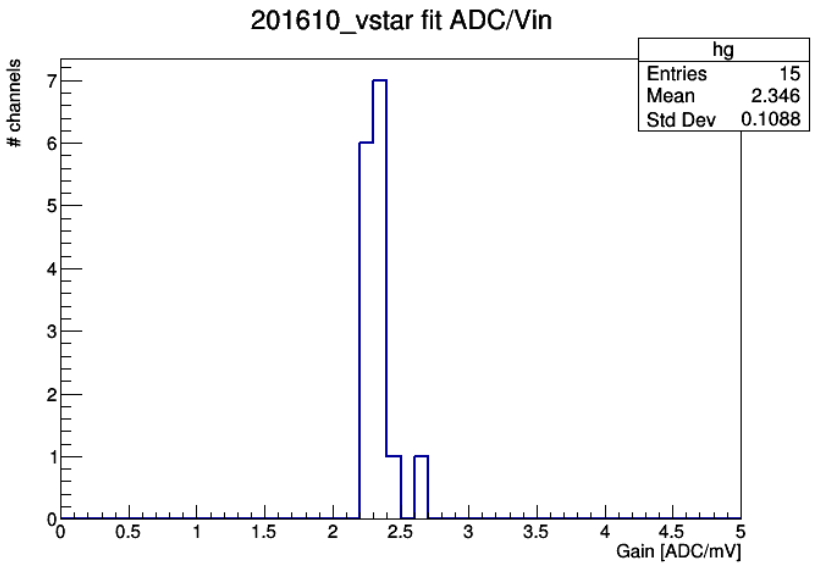


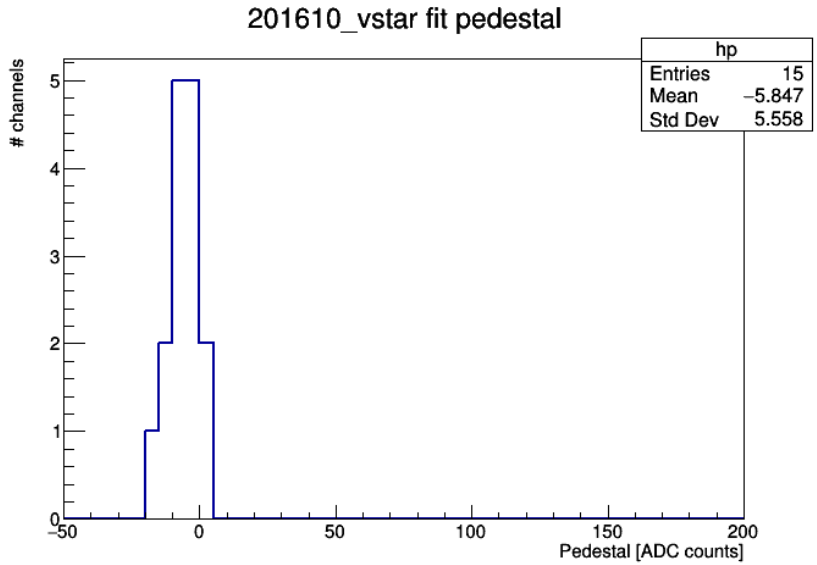
Fits and residuals

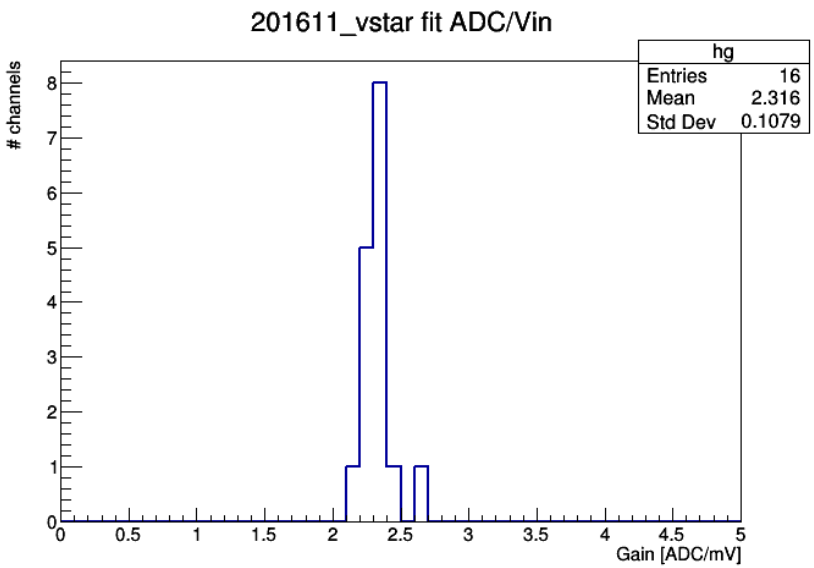
Use residuals to look at resolution and linearity

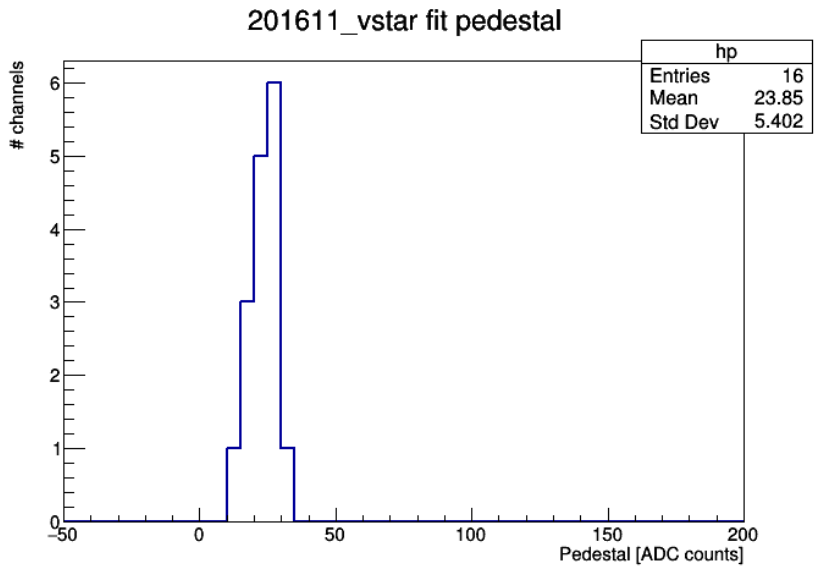
- Response (V_{in} vs. ADC) is fit to a straight line over the range (65, 4095)
  - Stuck codes (low bits all 0 or 1) are excluded in fit (shown in plots)
  - V_{in} > 1700 mV is excluded
- First plots show the distributions of fit parameters
  - Parameters are the gain (slope) and pedestal (ADC offset)
- Next plots show the difference between ADC count and this fit vs. ADC count

Old and new VSTAR fit gains and pedestals

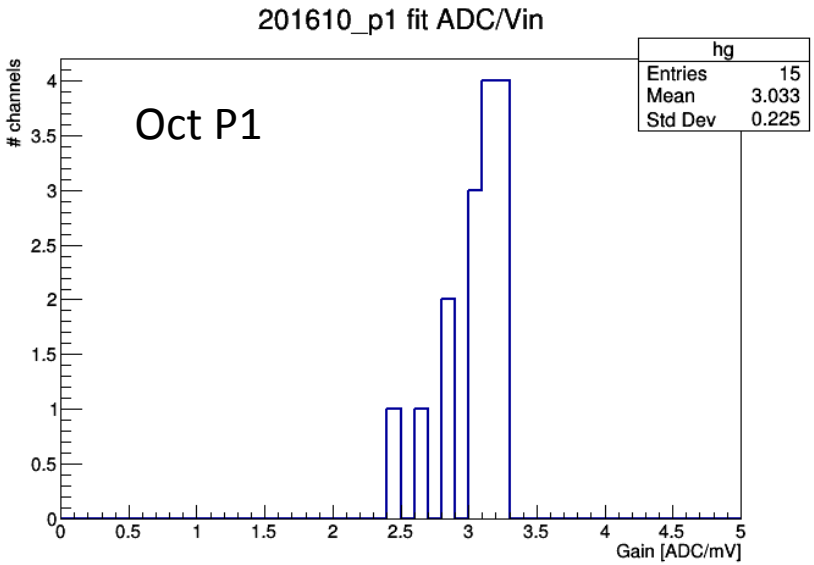


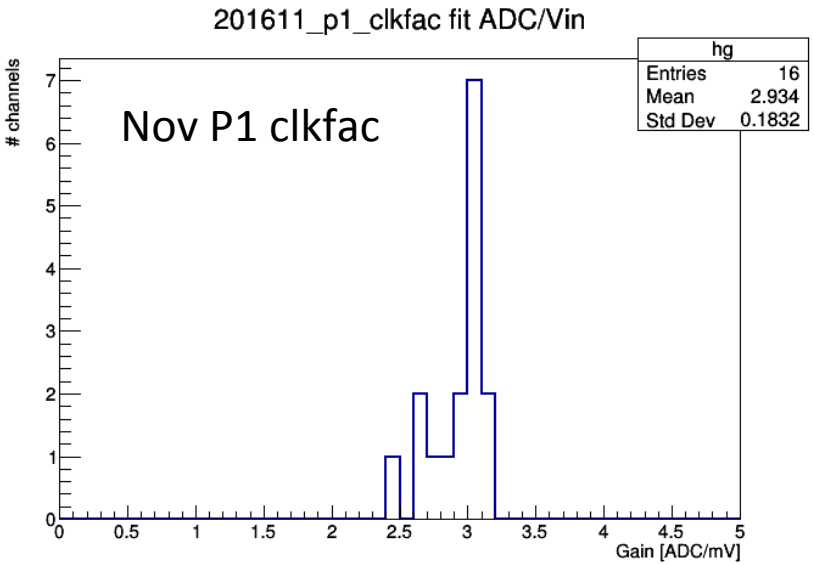


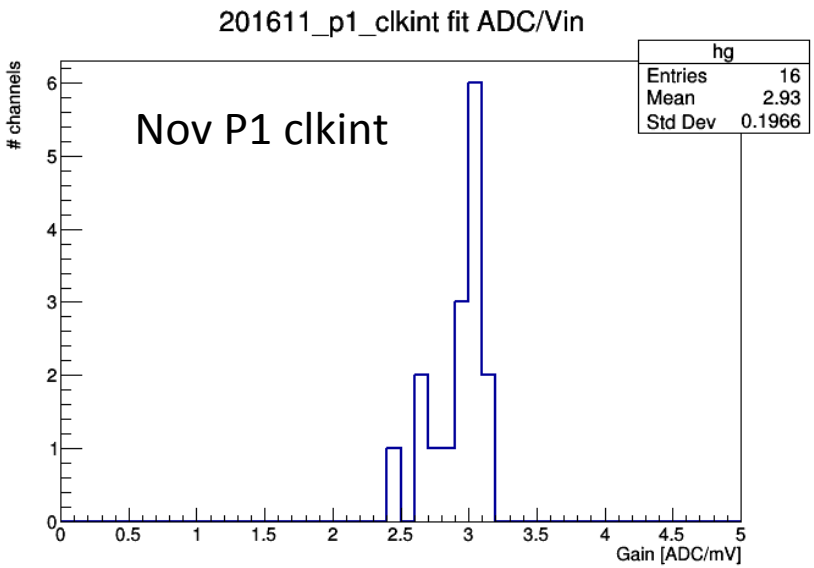


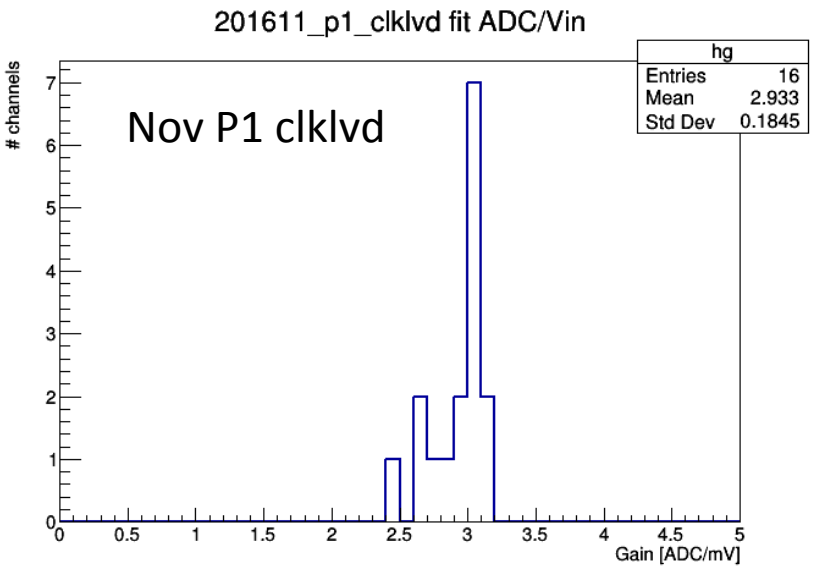


Old and new P1 fit gains

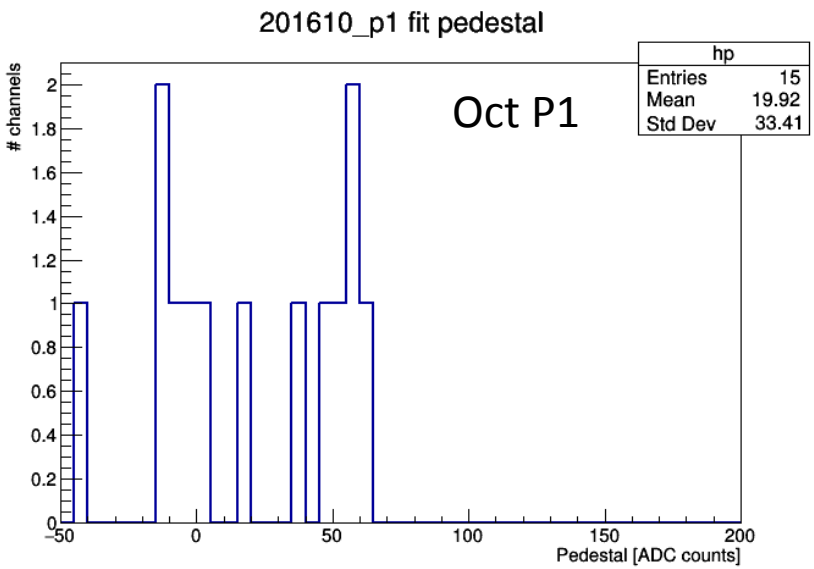


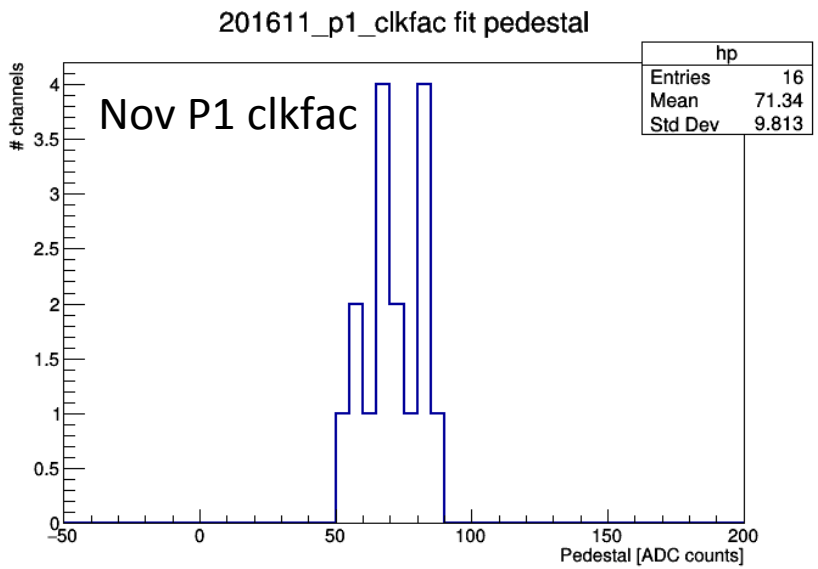


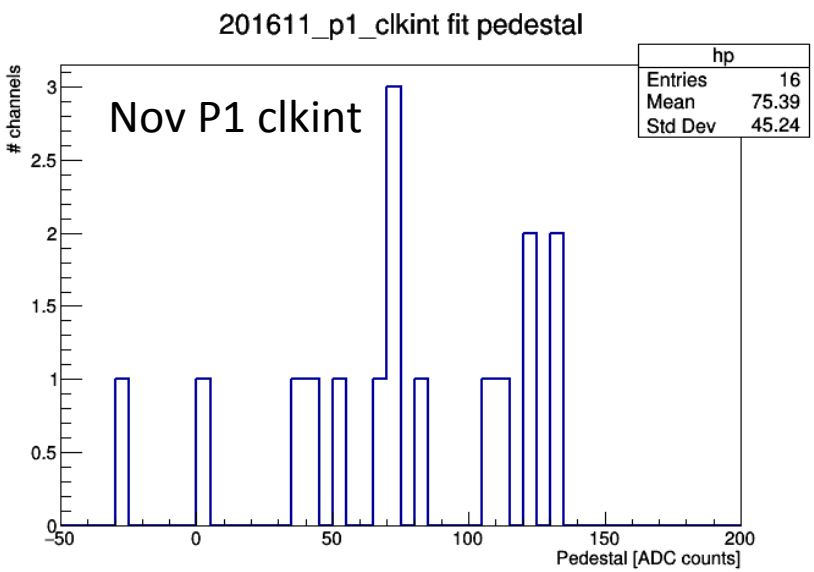


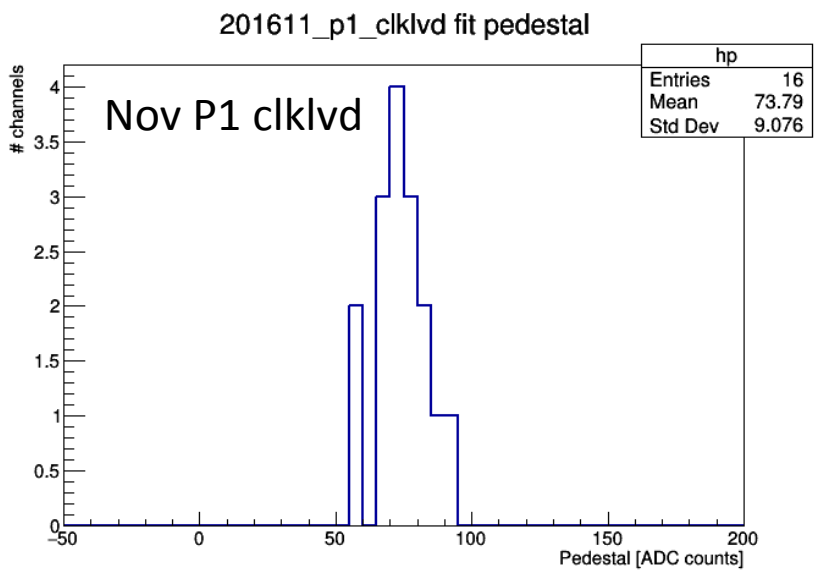


Old and new P1 fit pedestals

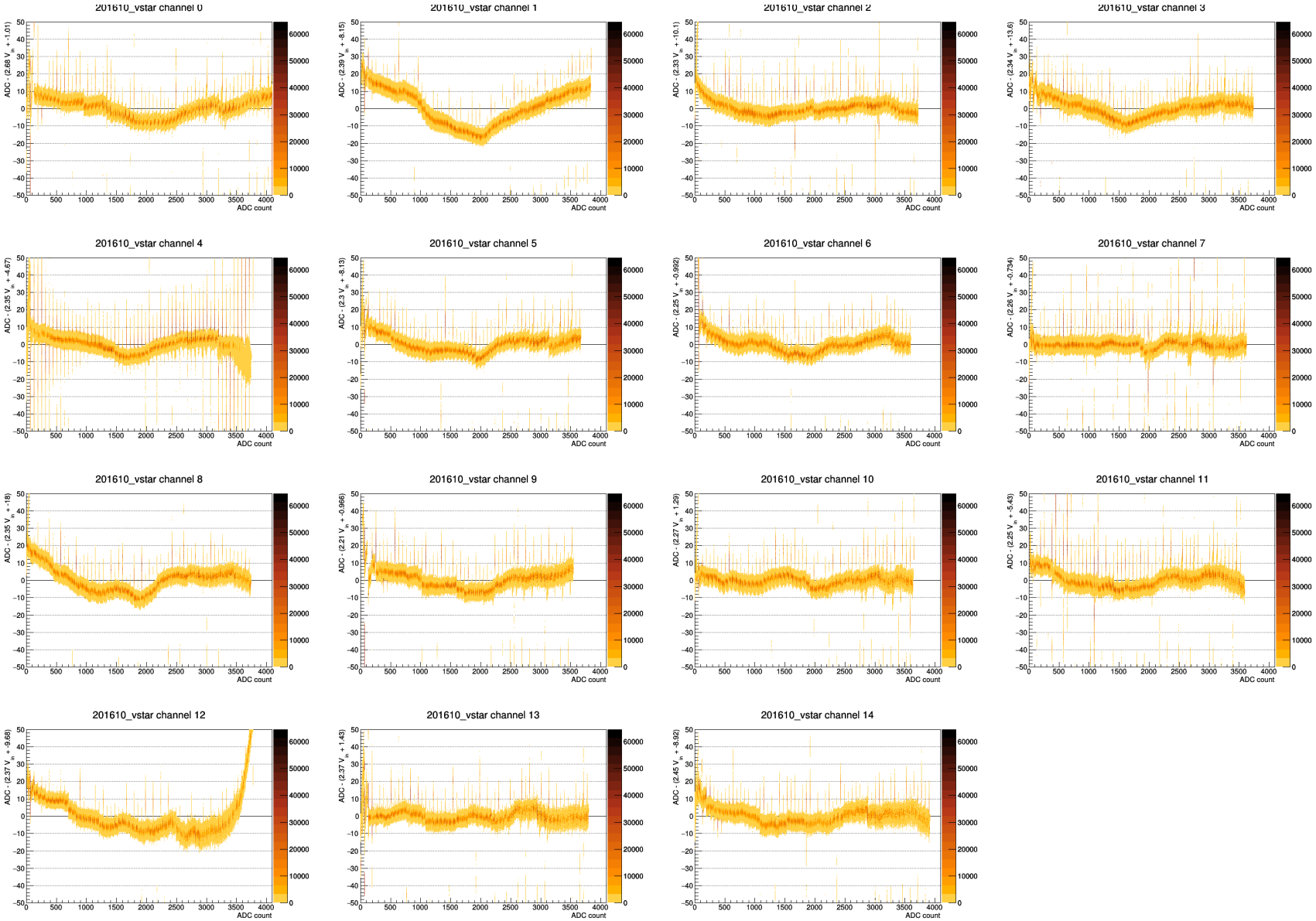




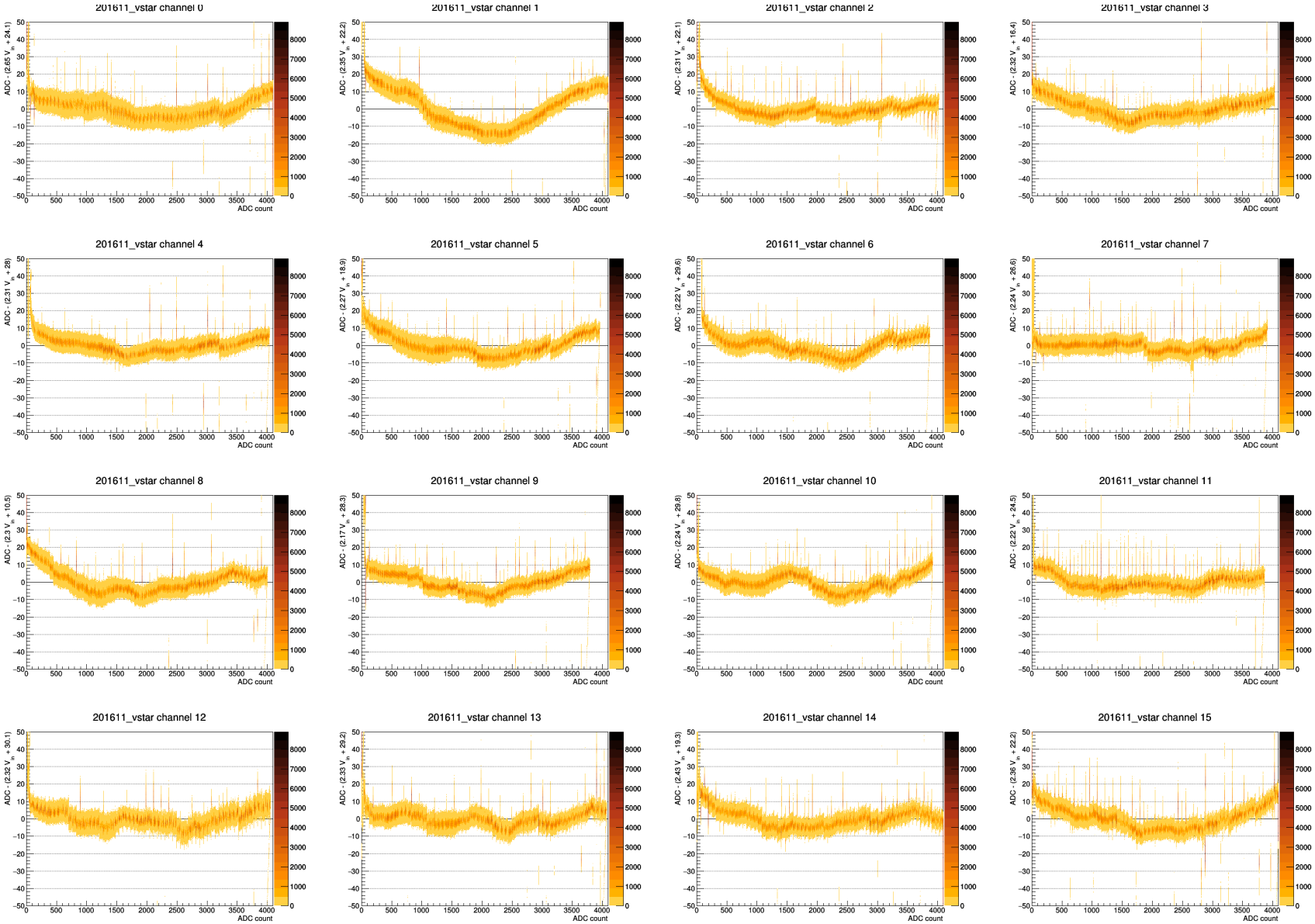




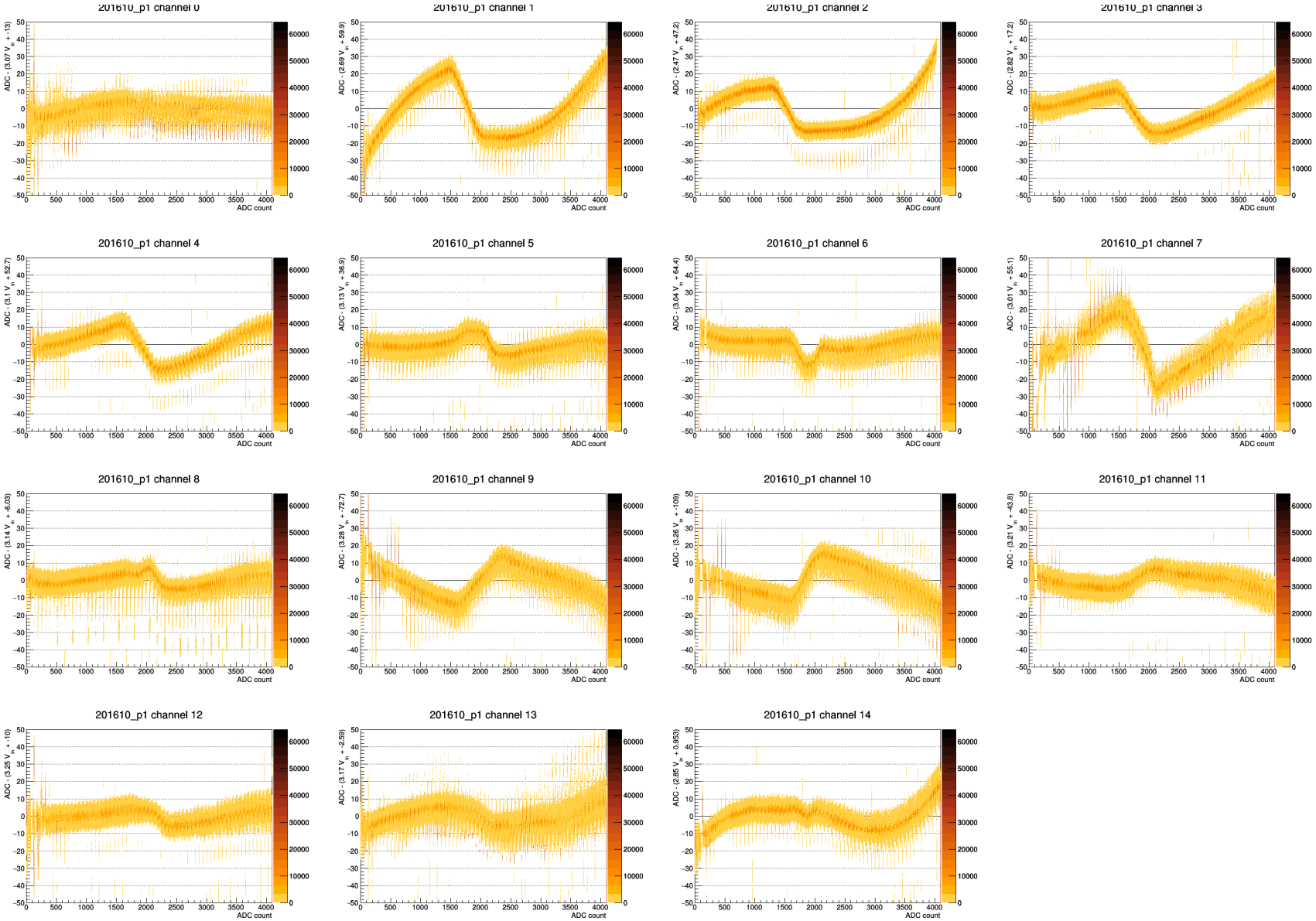
Oct VSTAR fit residuals



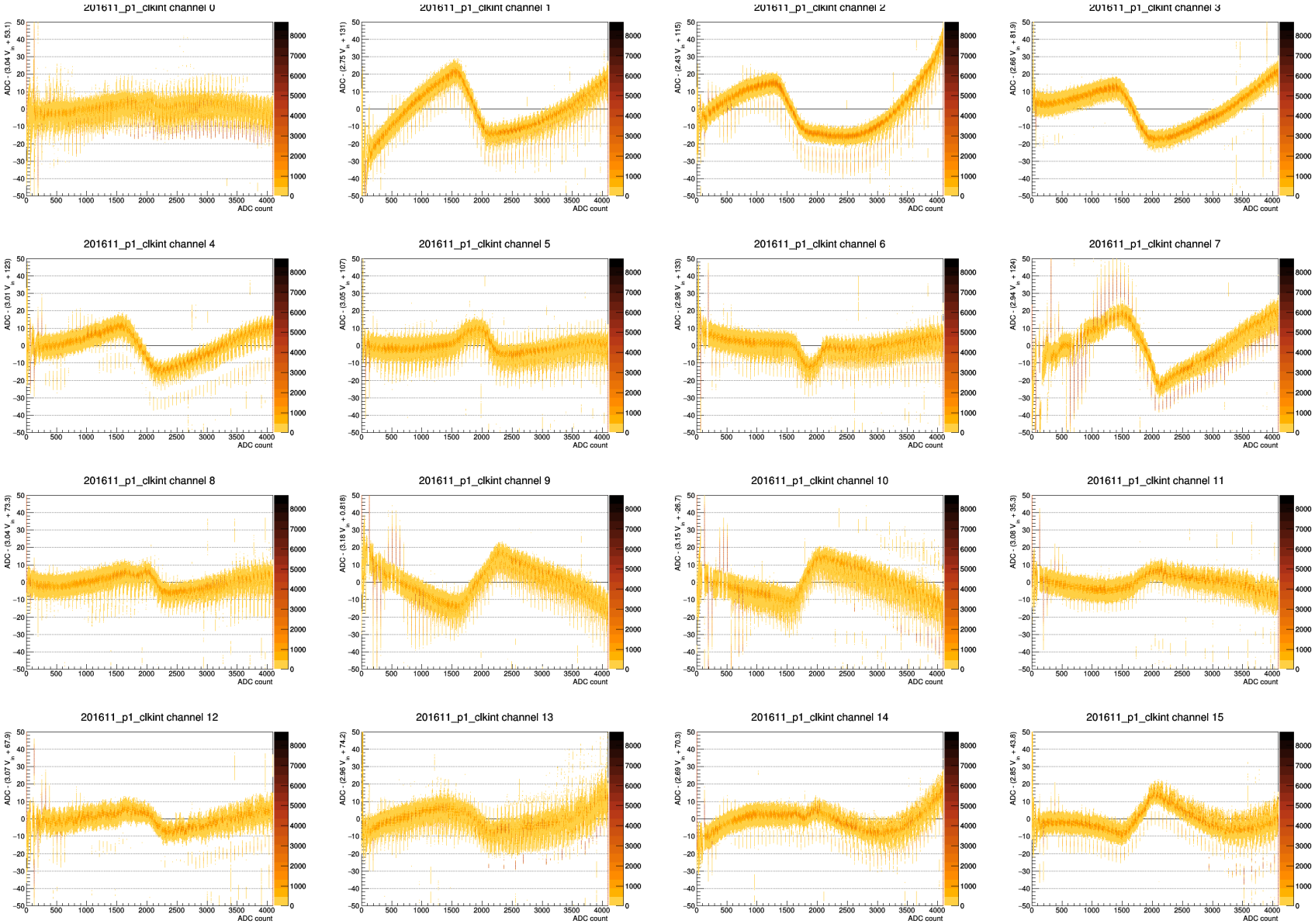
Nov VSTAR fit residuals



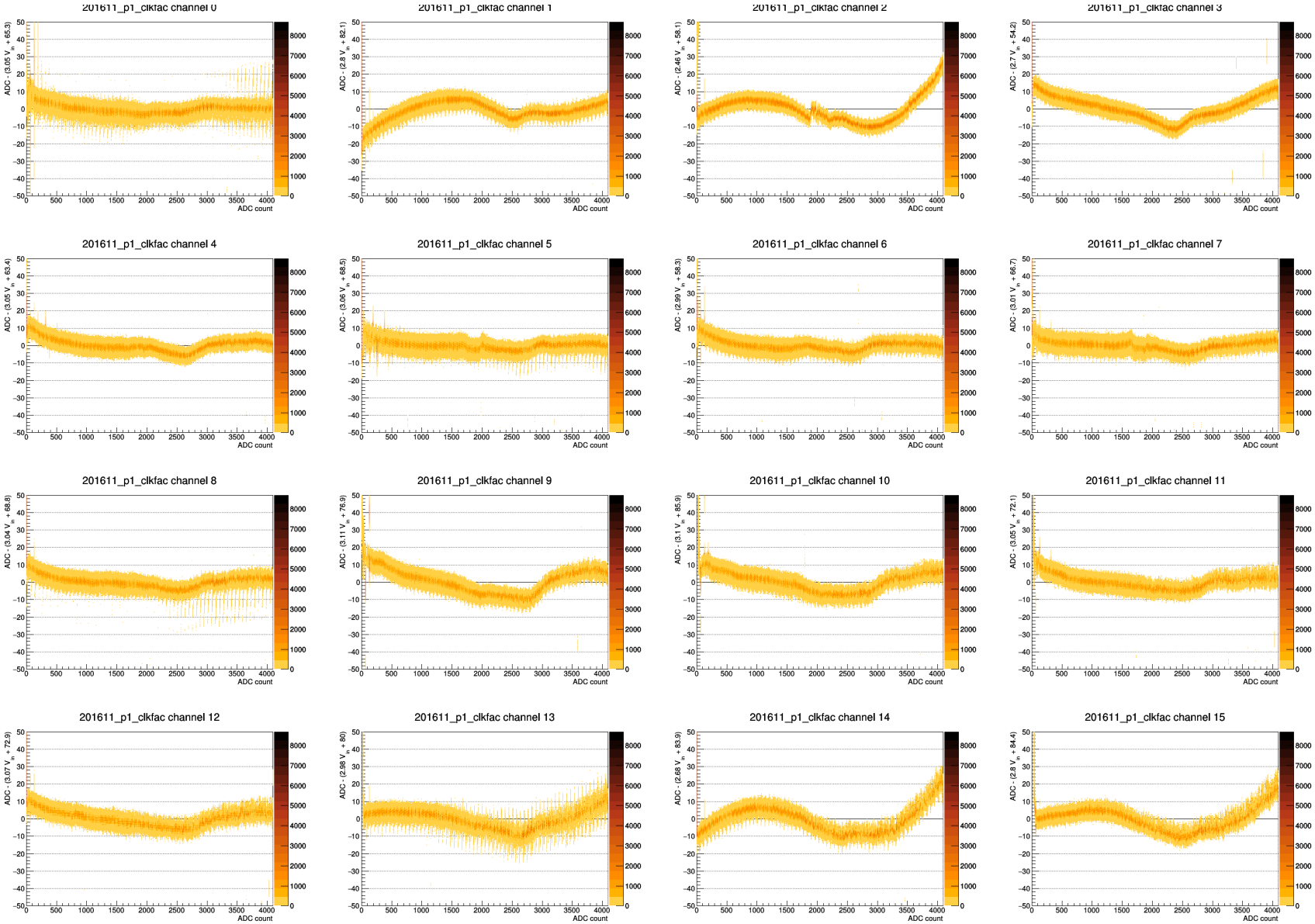
Oct P1 fit residuals



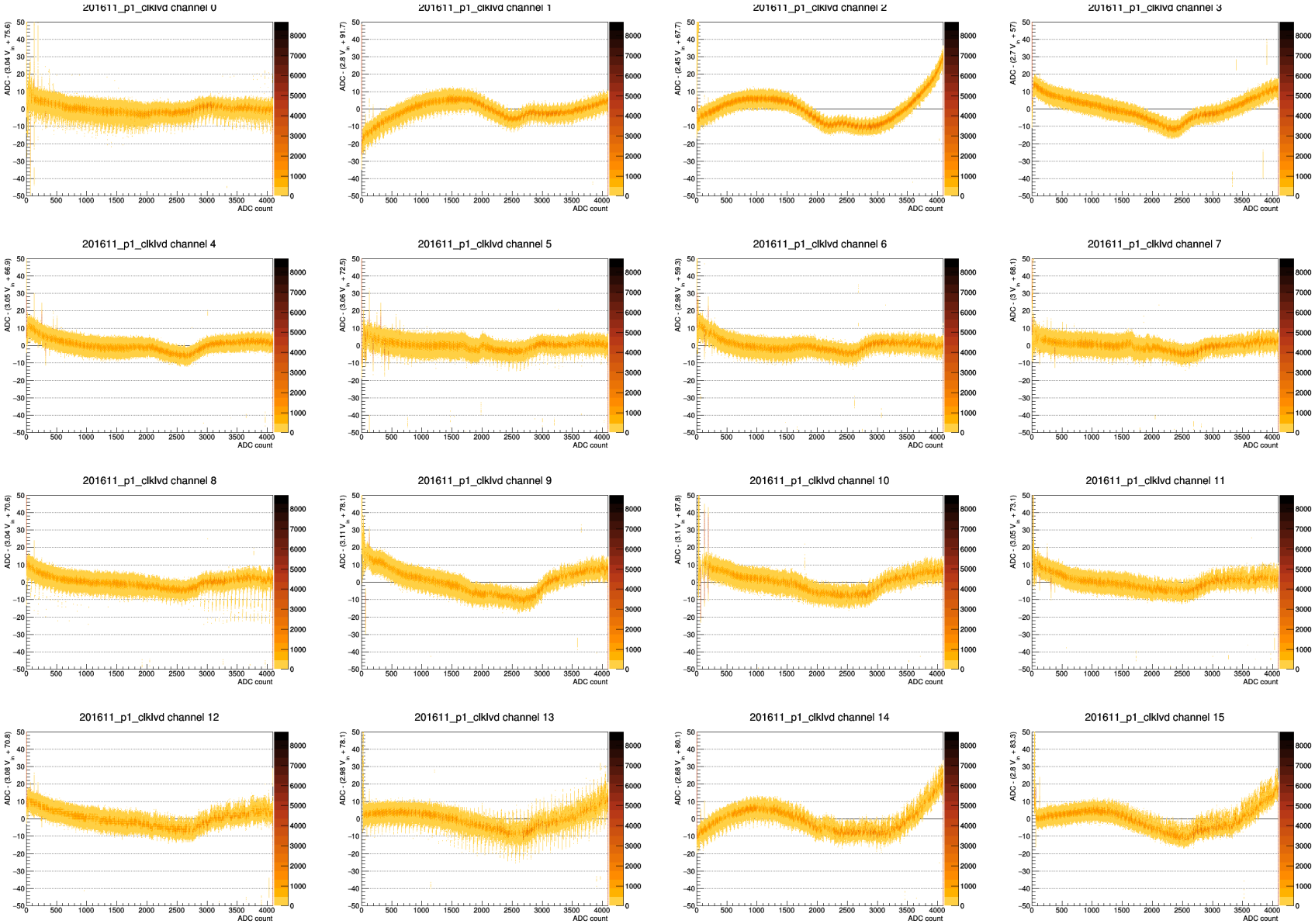
Nov P1 clkint fit residuals



Nov P1 clkfac fit residuals



Nov P1 clklvd fit residuals

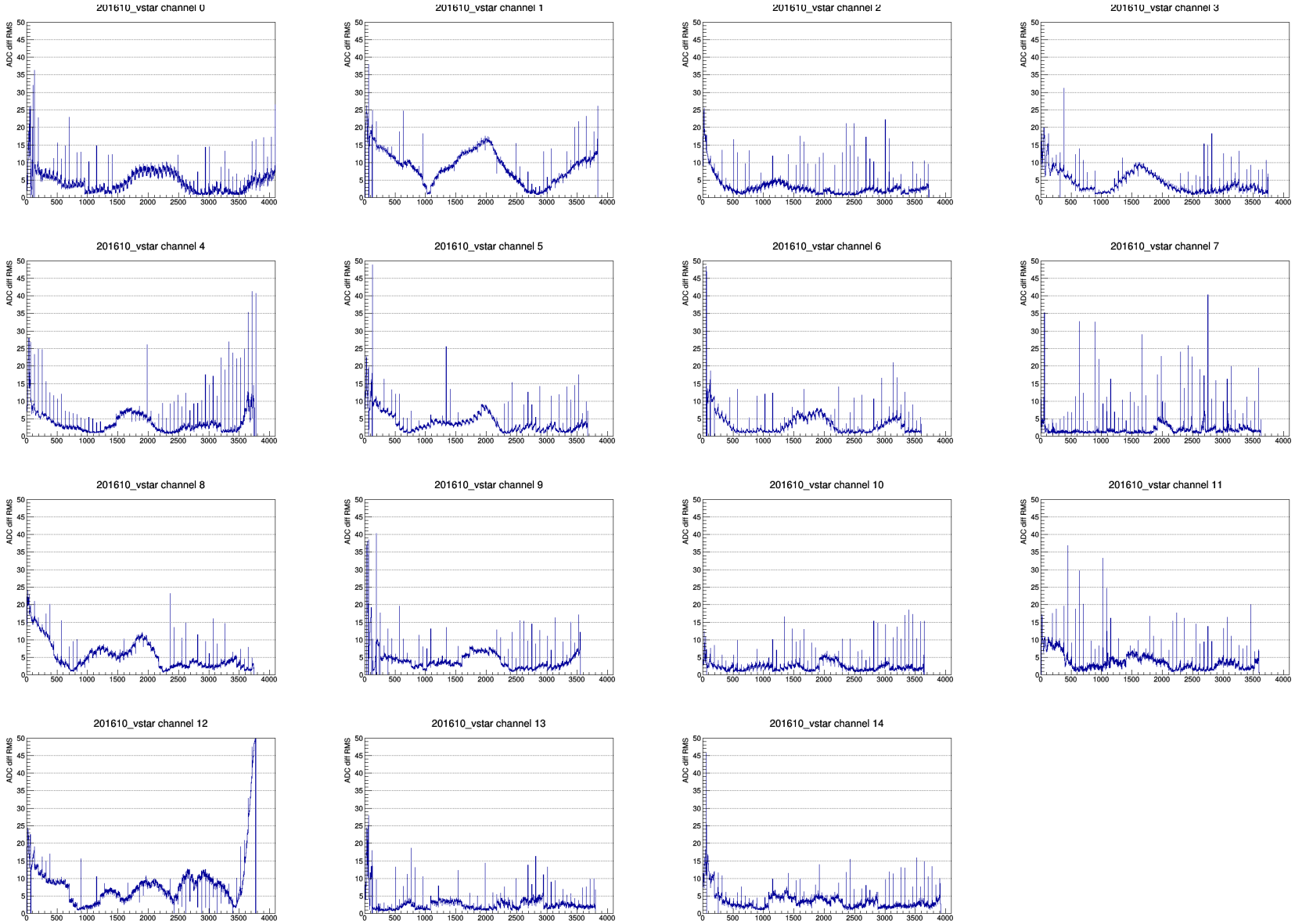


Resolutions

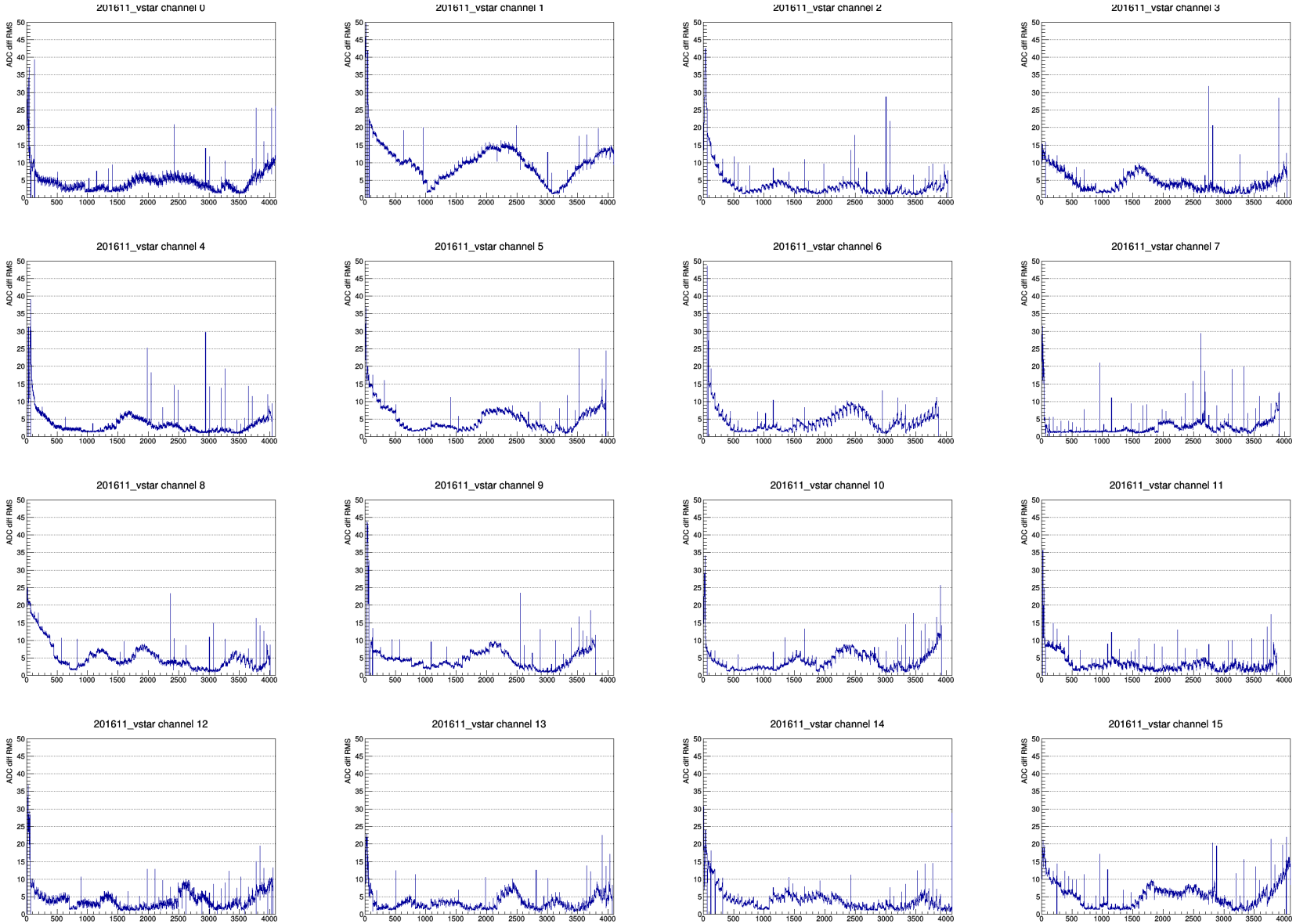
We extract stats from the preceding residual plots

- Mean for each ADC bin
- RMS of the deviation from zero
  - This is the resolution we get with the linear calibration
- Standard deviation (sigma) is the RMS of deviation from its mean
  - This is the resolution we get if we calibrate out the non-linearity

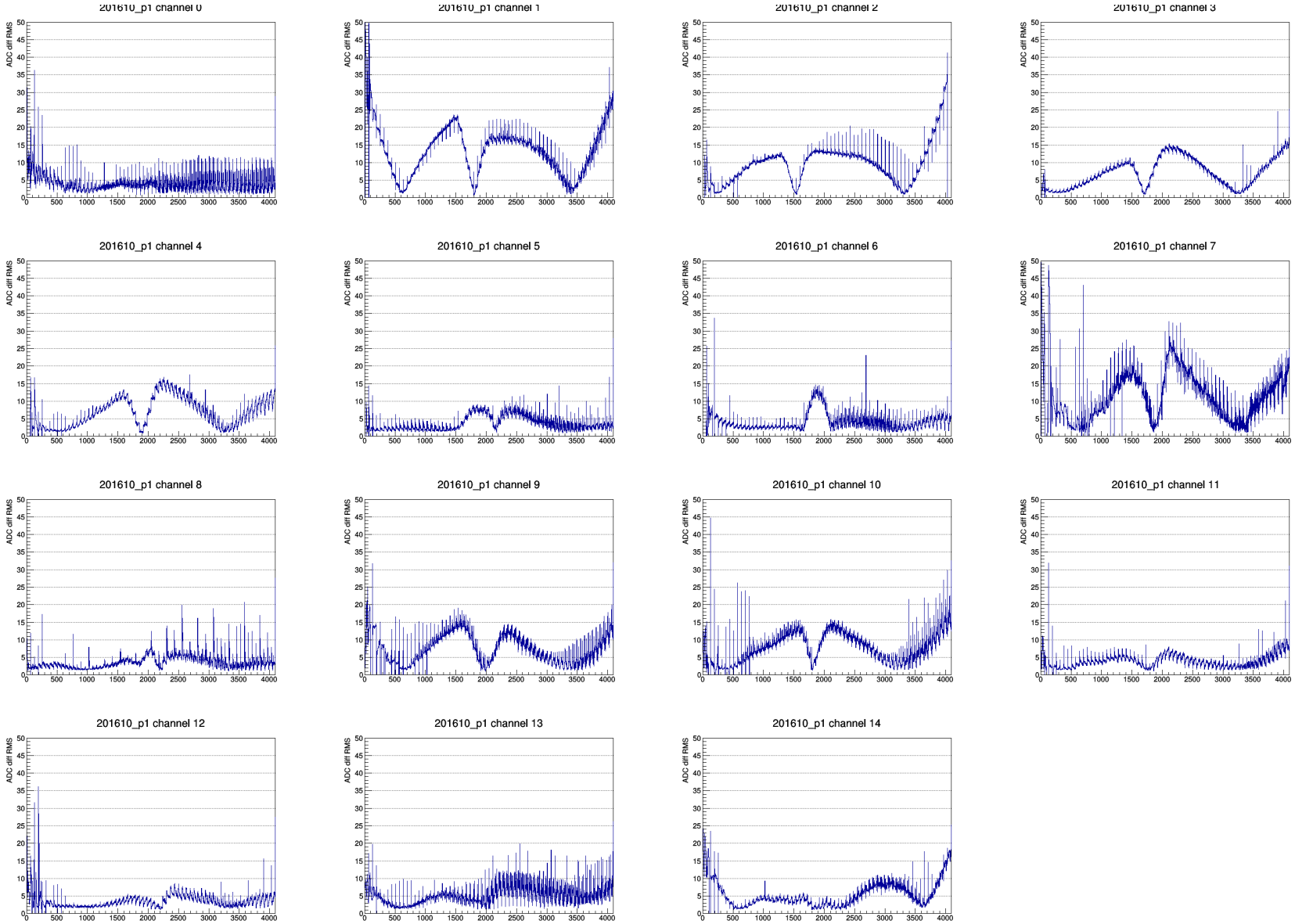
Oct VSTAR fit RMS



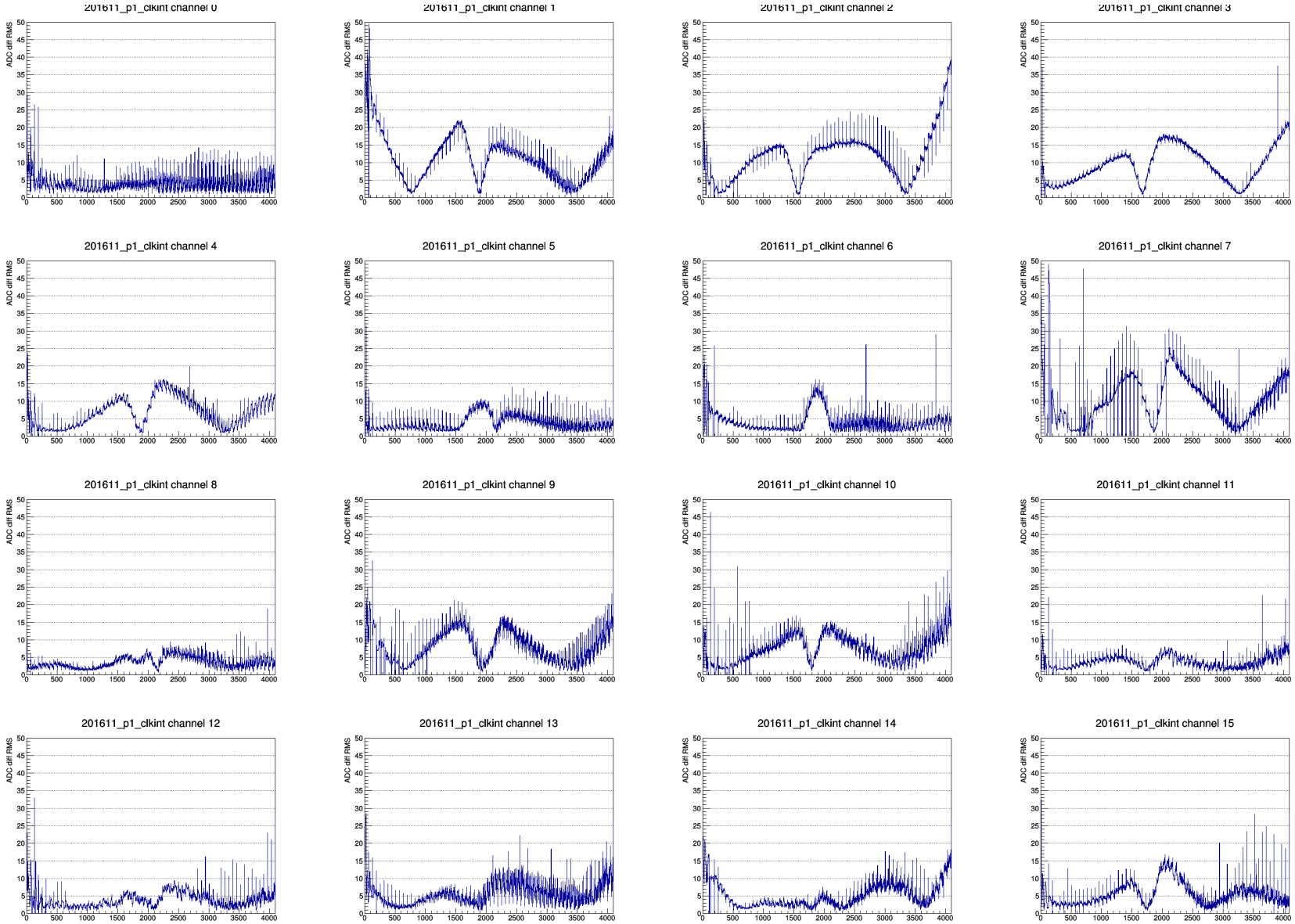
Nov VSTAR fit RMS



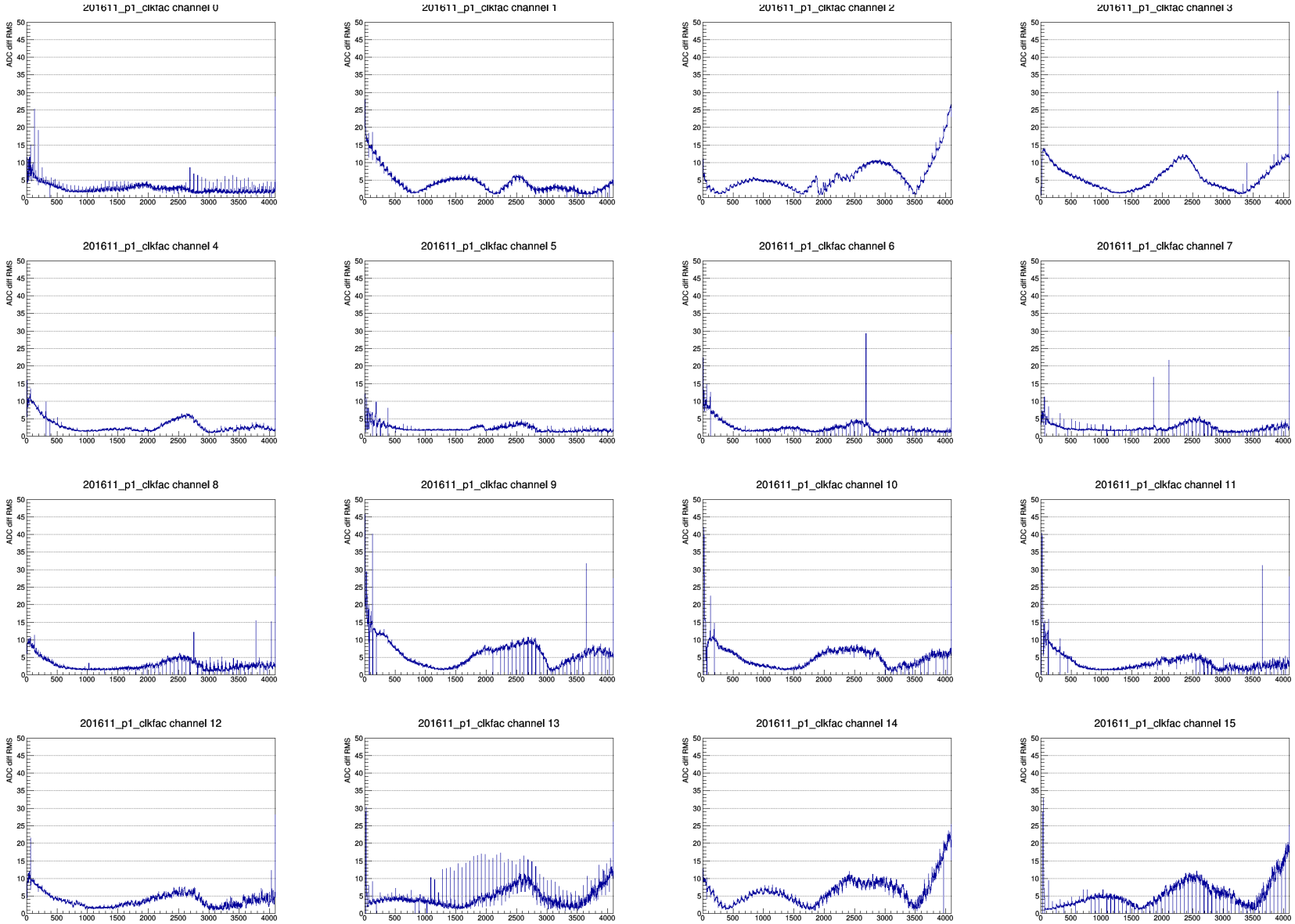
Oct P1 fit RMS



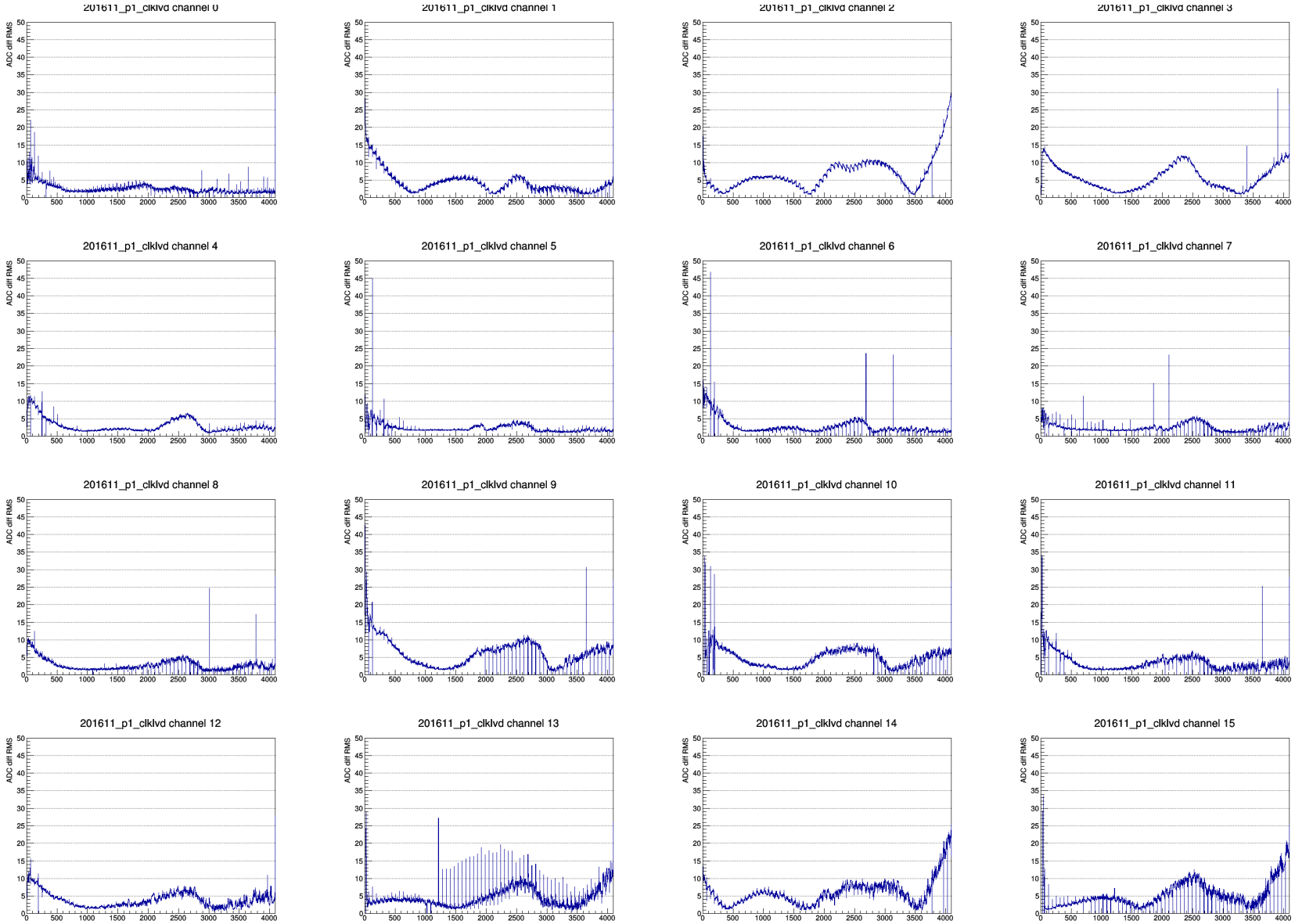
Nov P1 clkint fit RMS



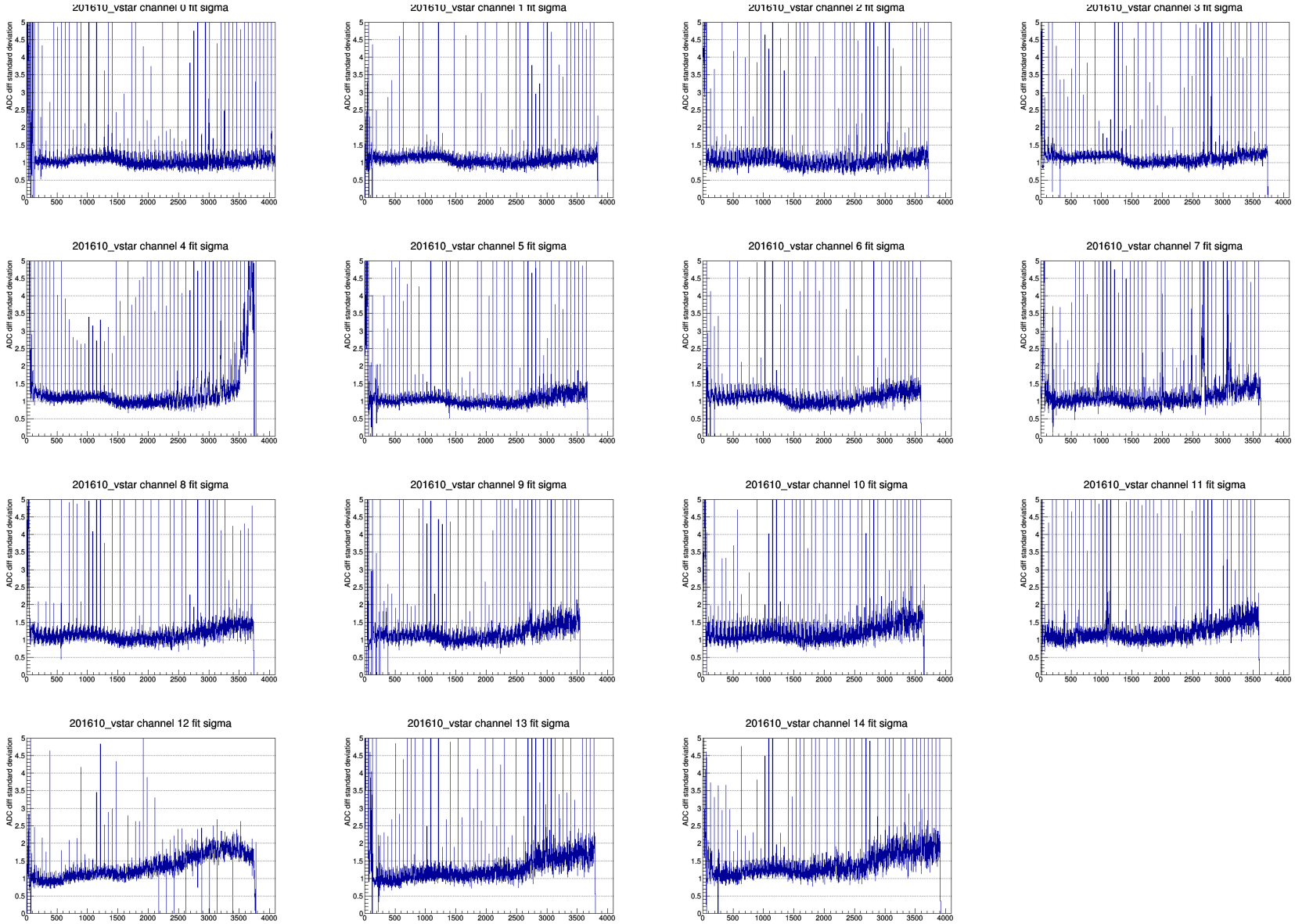
Nov P1 clkfac fit RMS



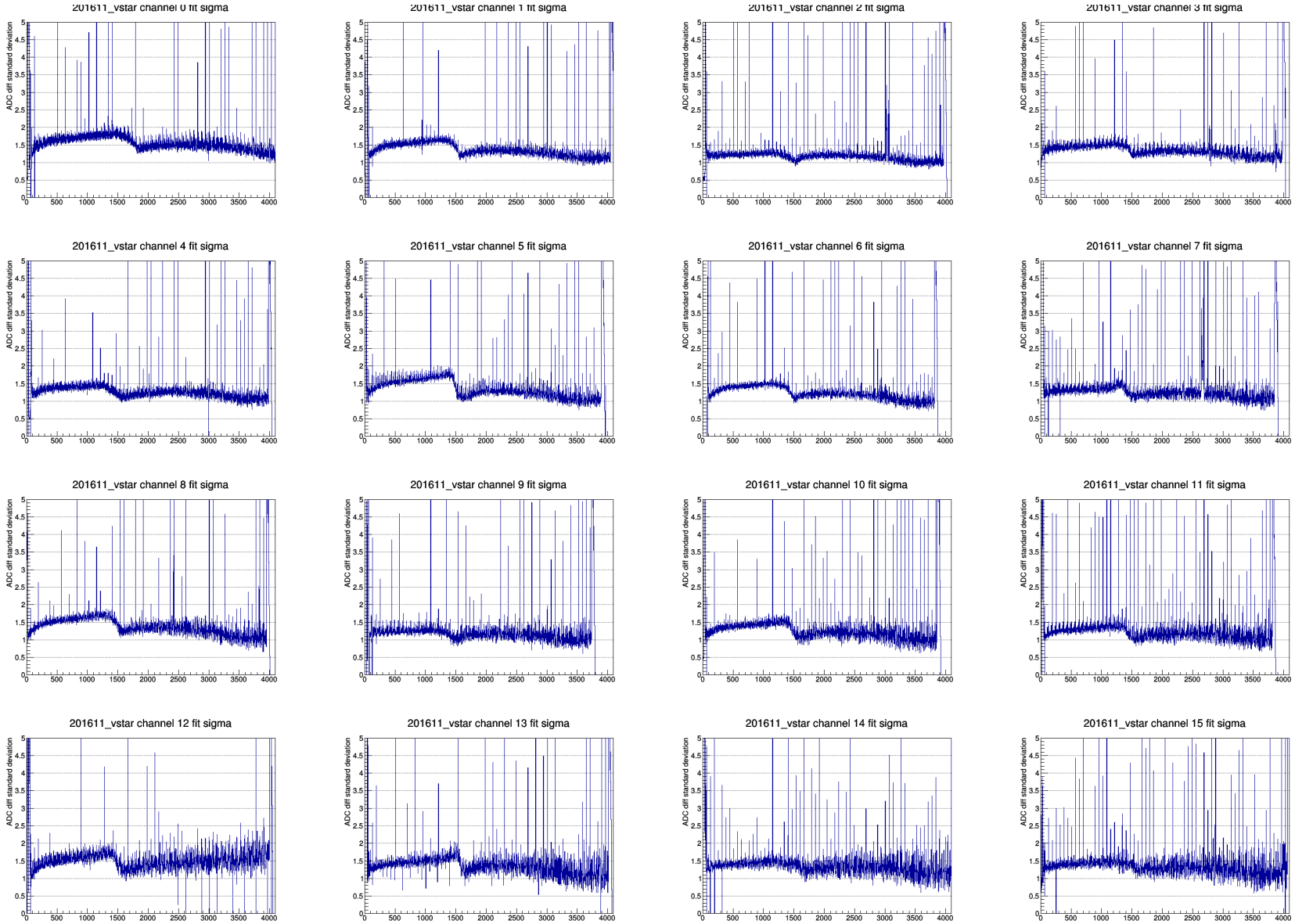
Nov P1 clklvd fit RMS



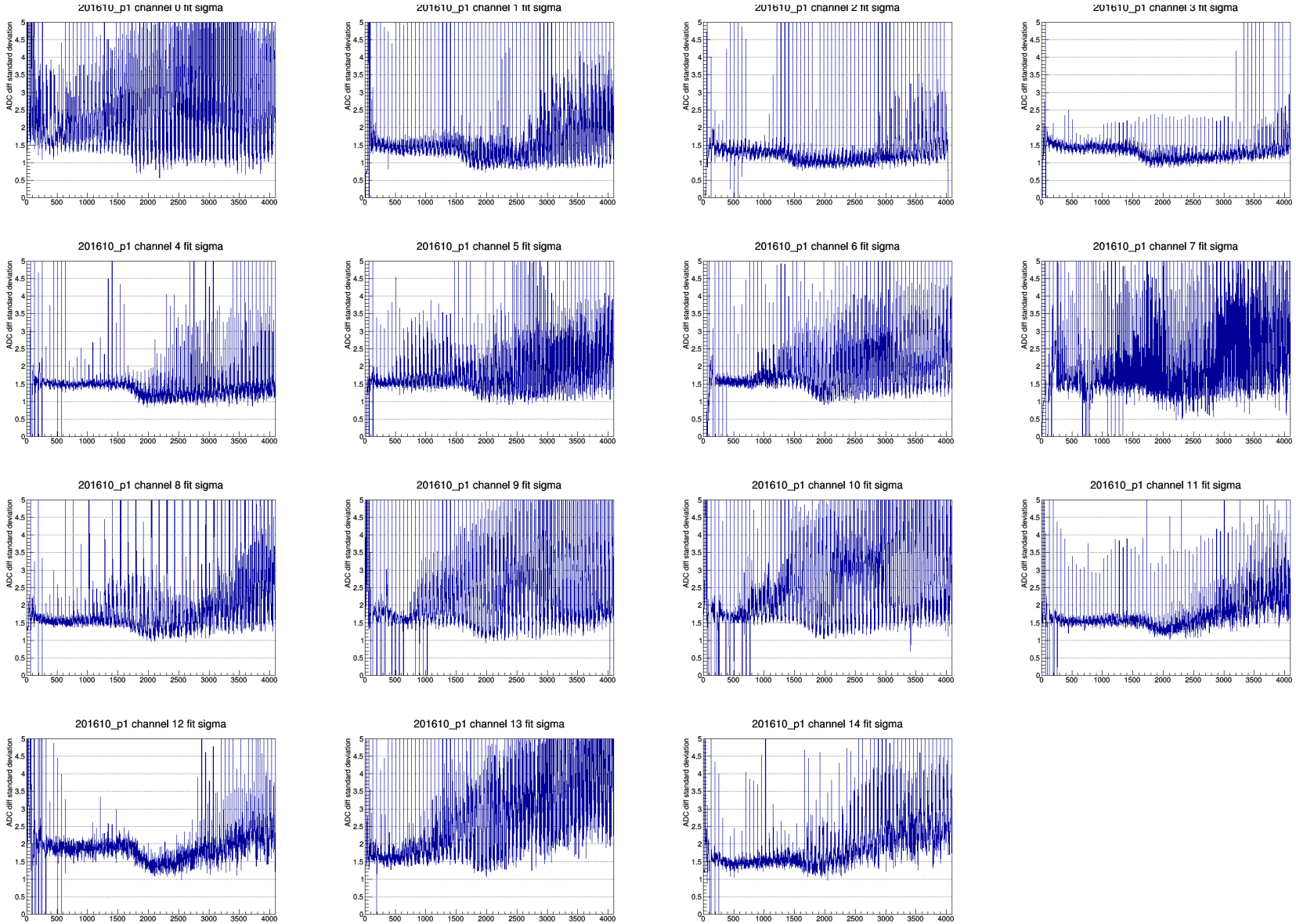
Oct VSTAR fit sigma



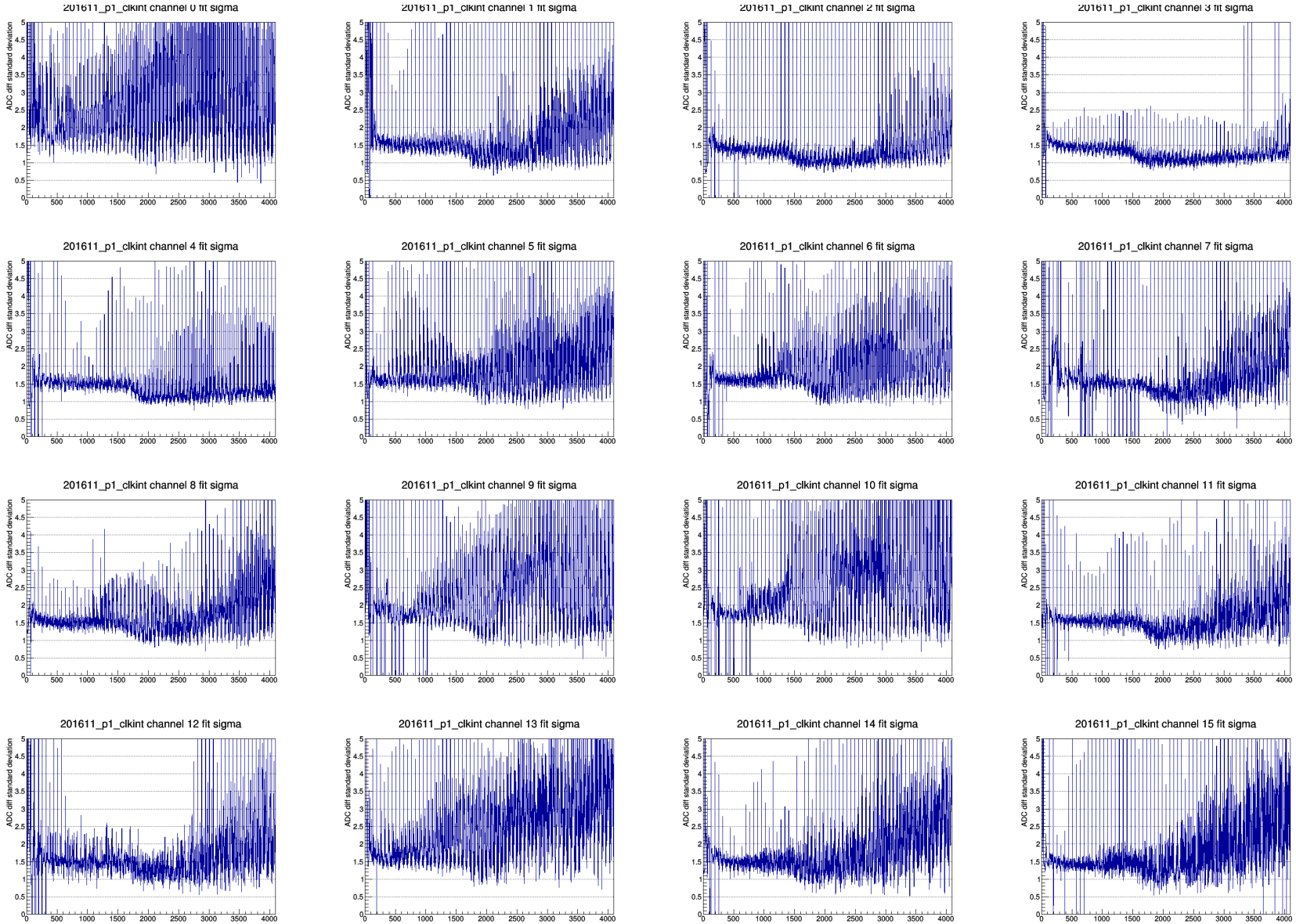
Nov VSTAR fit sigma



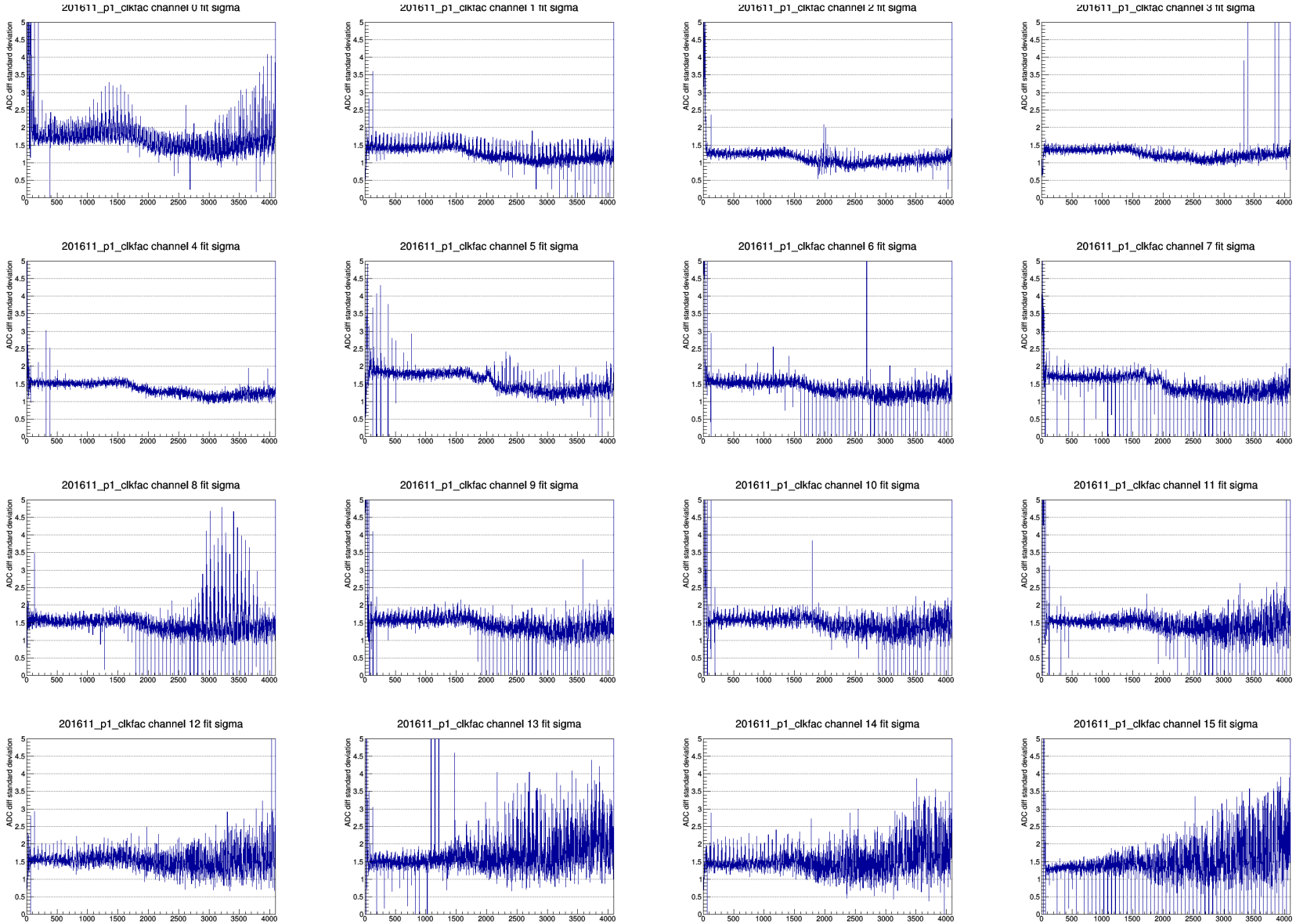
Oct P1 fit sigma



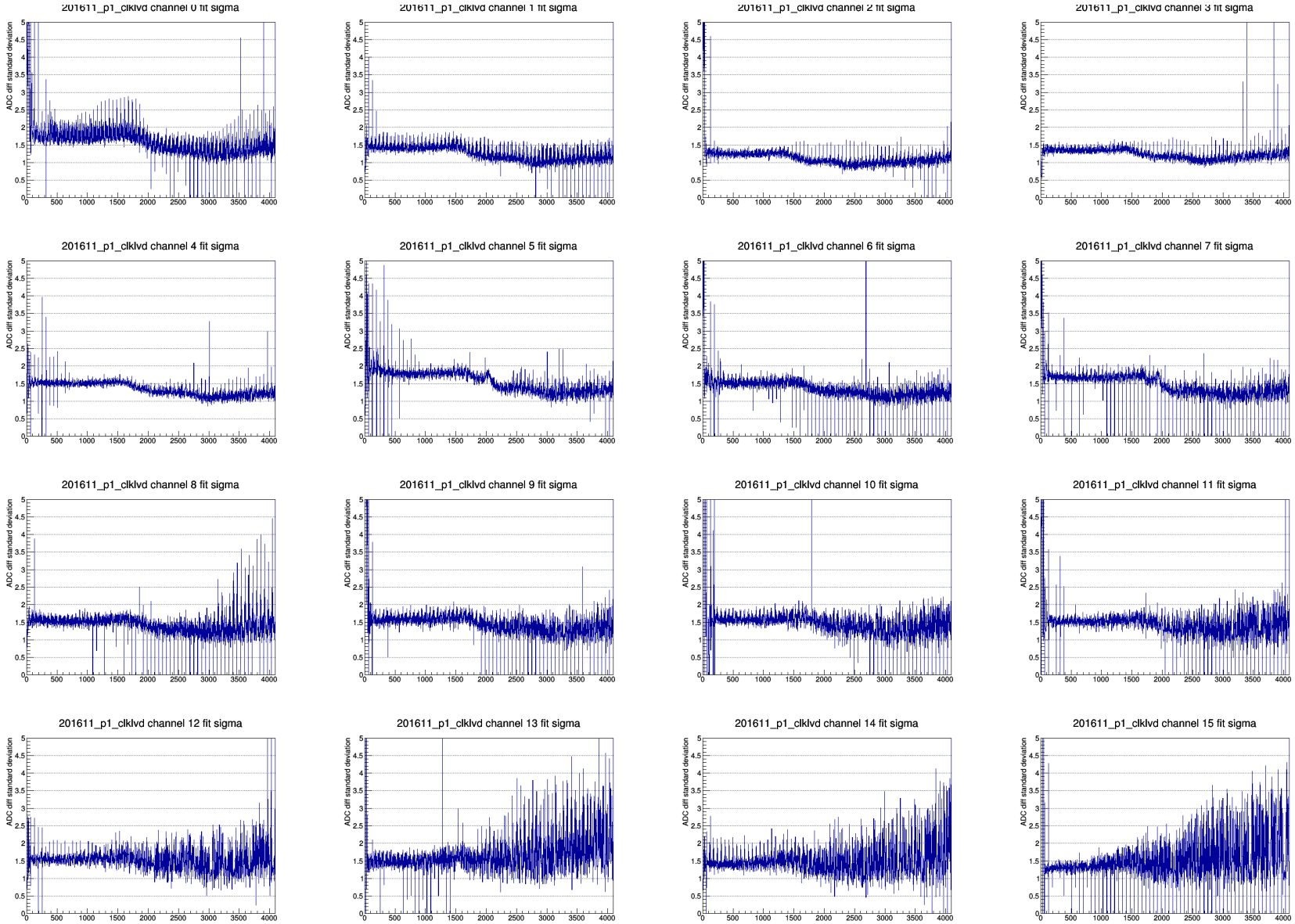
Nov P1 clkint fit sigma



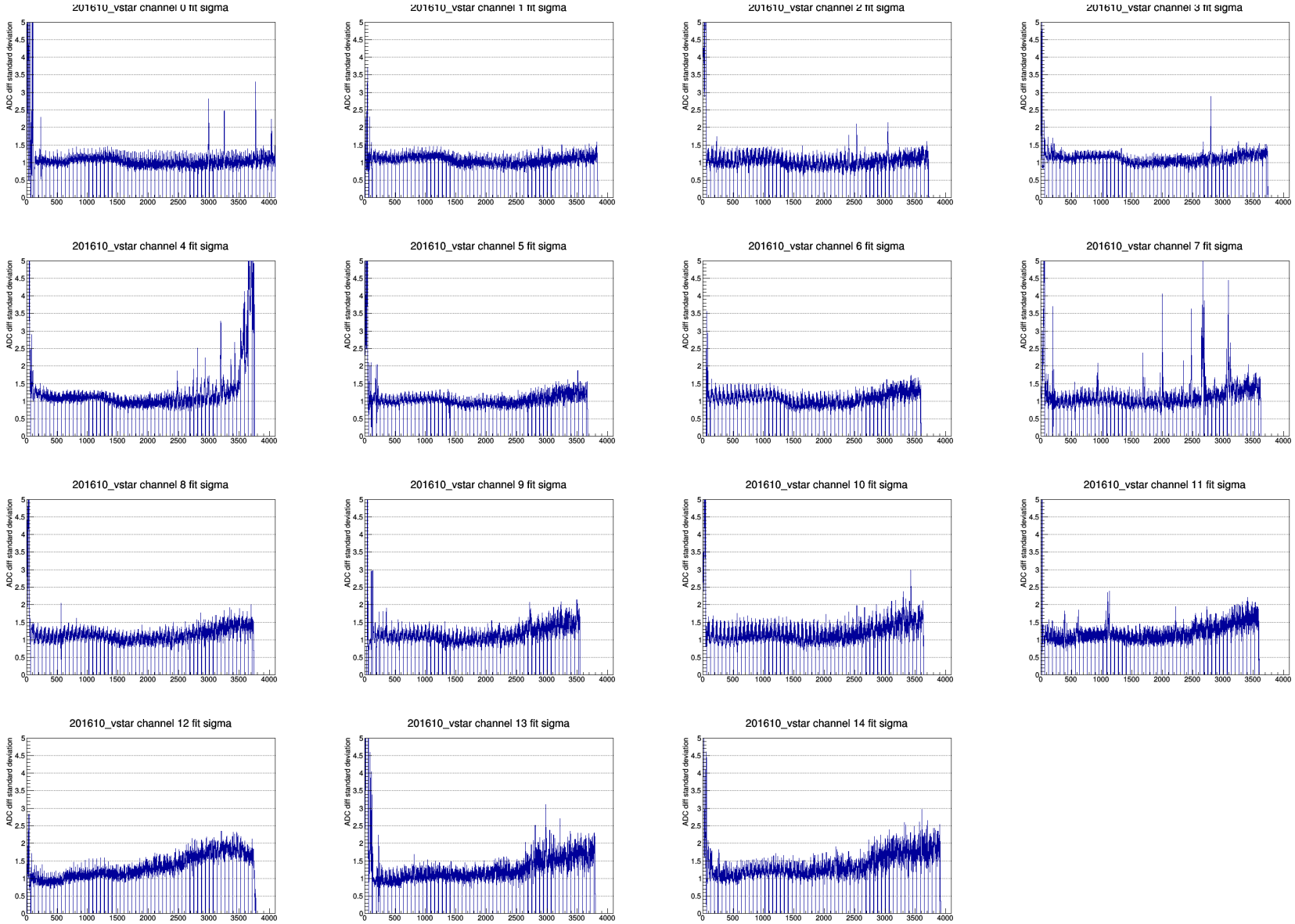
Nov P1 clkfac fit sigma



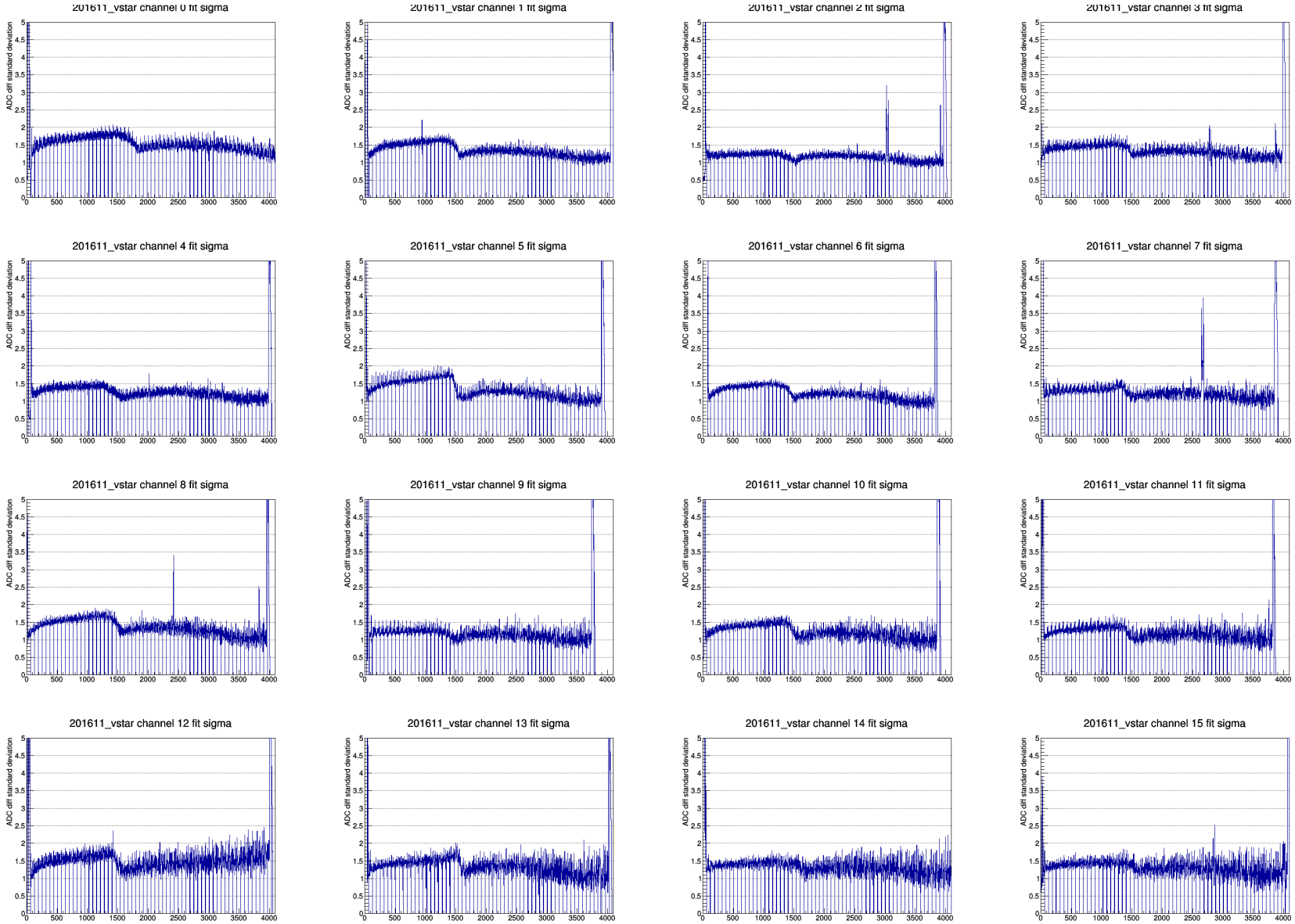
Nov P1 clklvd fit sigma



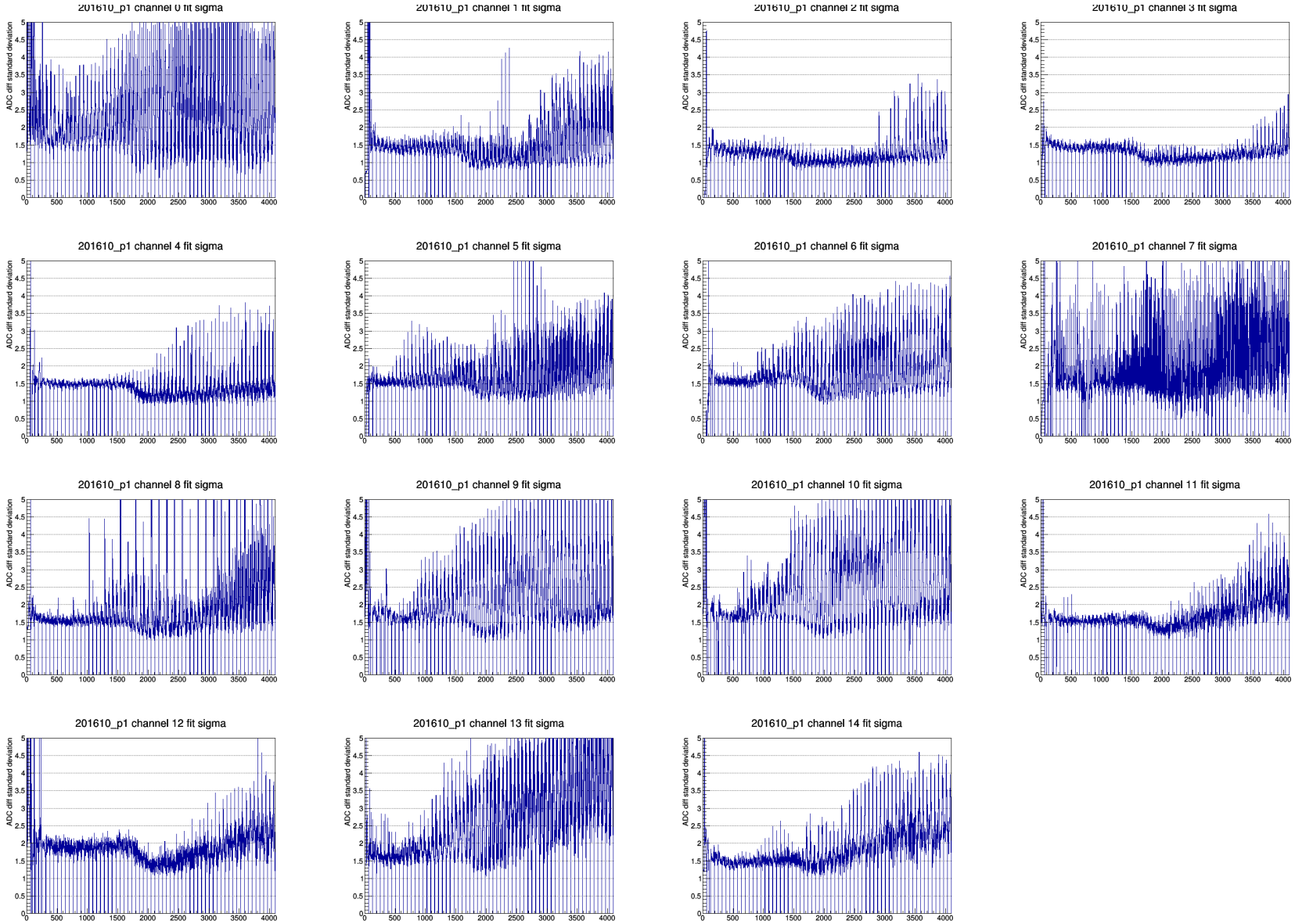
Oct VSTAR fit sigma (not stuck)



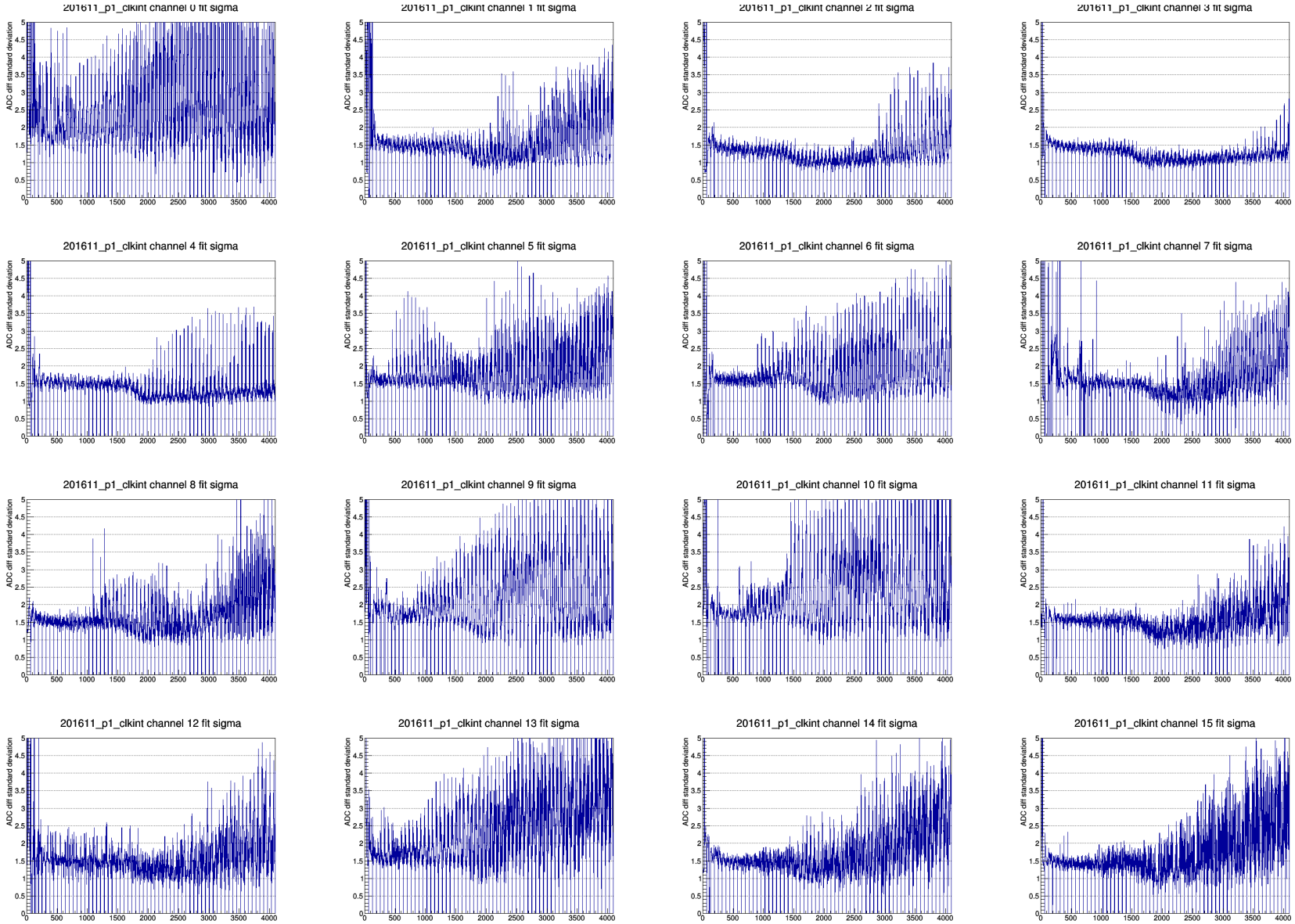
Nov VSTAR fit sigma (not stuck)



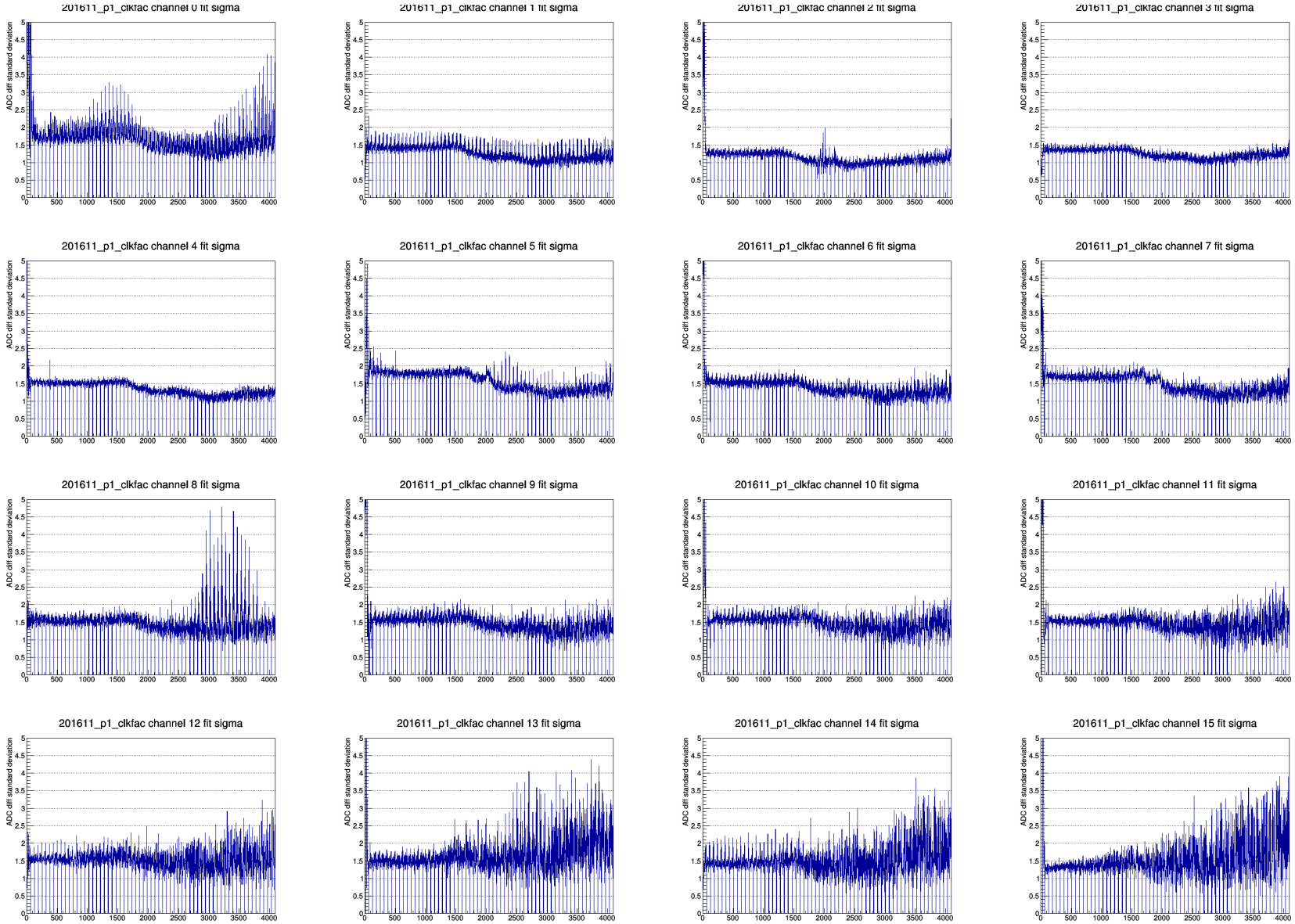
Oct P1 fit sigma (not stuck)



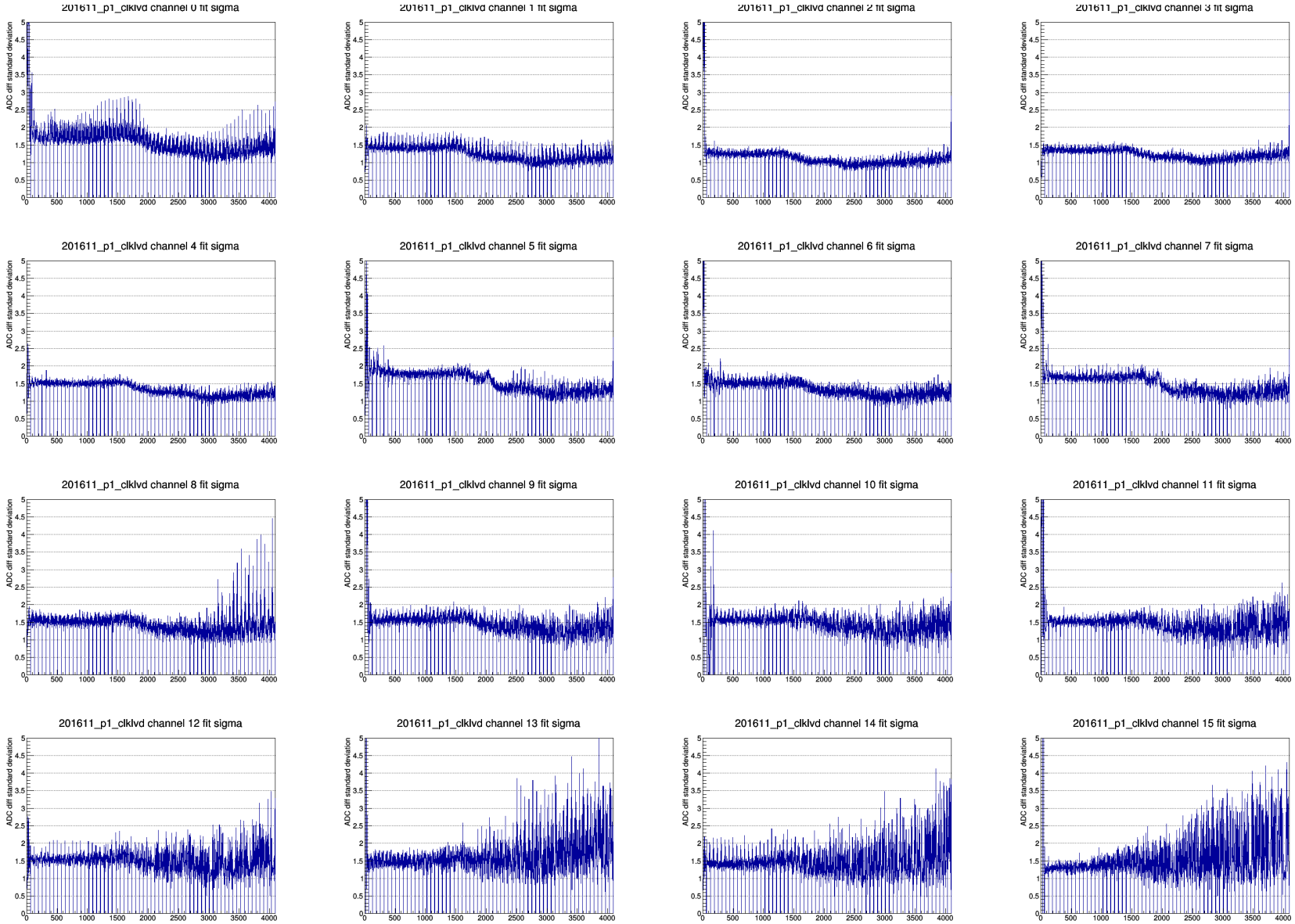
Nov P1 clkint fit sigma (not stuck)



Nov P1 clkfac fit sigma (not stuck)



Nov P1 clklvd fit sigma (not stuck)

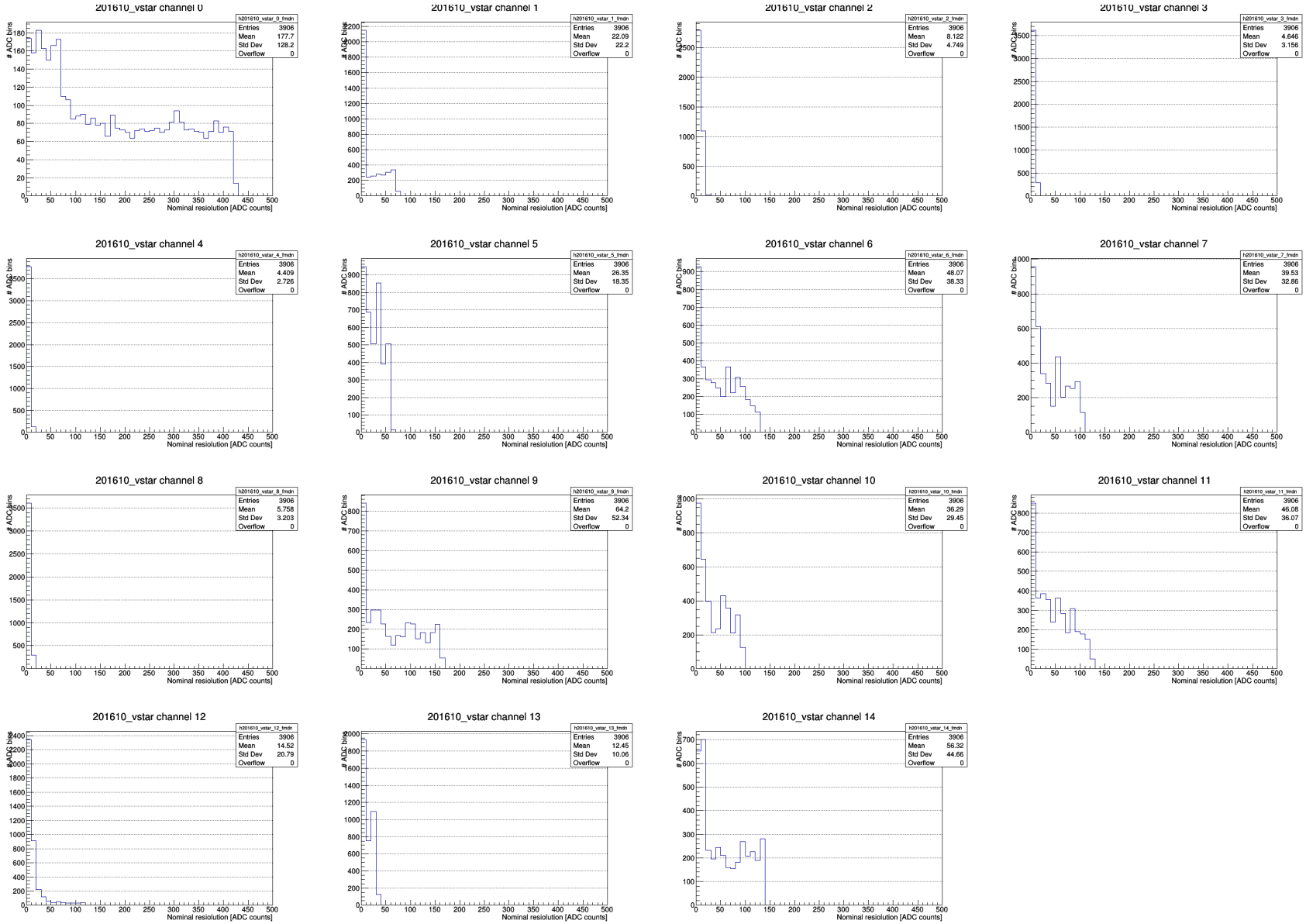


Nominal resolutions

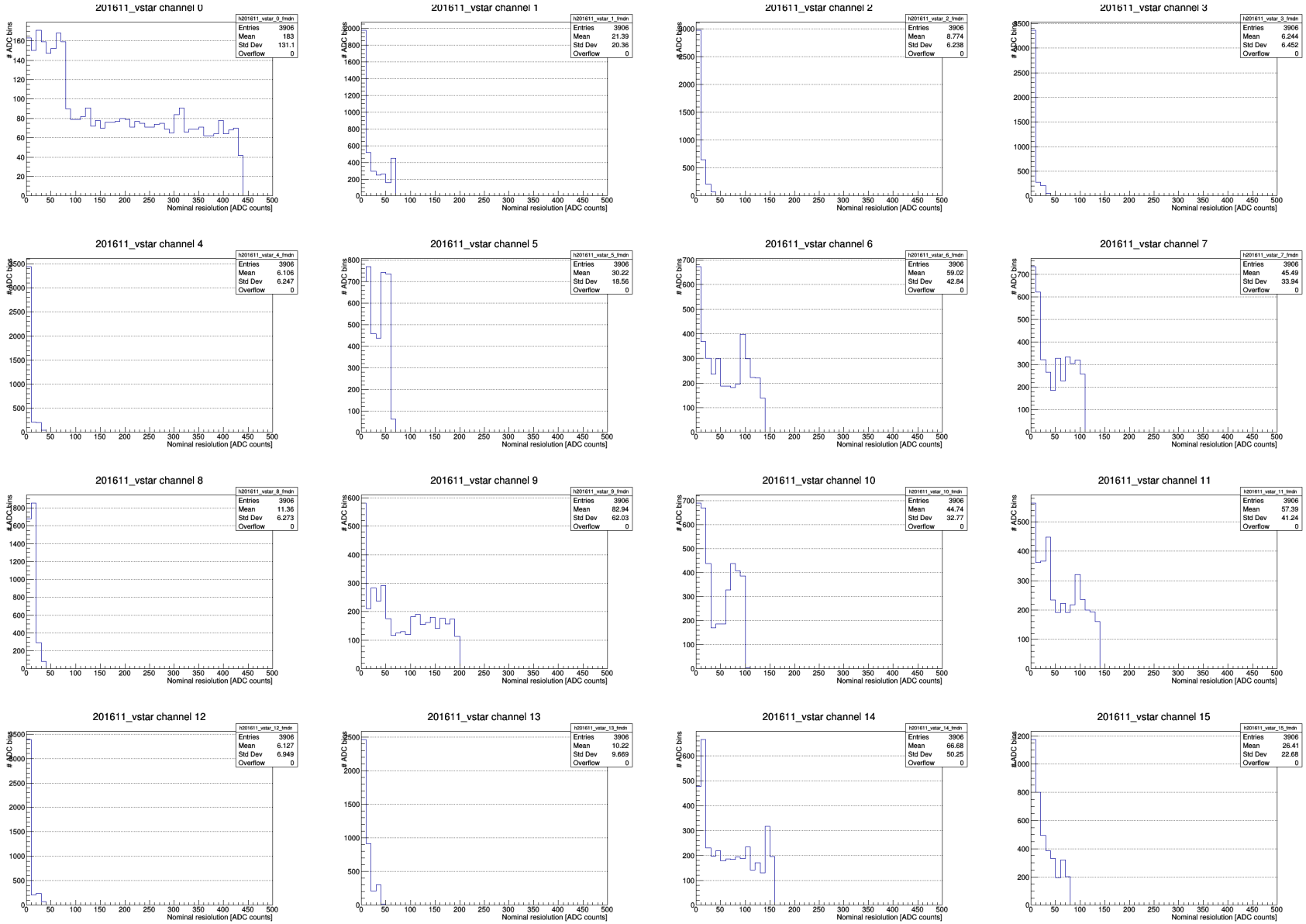
Following plots are distributions of nominal resolution

- Nominal means a common gain is assumed for all channels
  - Value used here is the mean from the linear fit
  - May have worse results when many devices are included
  - This is our current offline reconstruction strategy
- Separate distribution shown for each channel
  - Stuck bins and ADC < 64 are excluded
  - Sum over all channels shown later
- Dominant contribution to the resolution is the channel-to-channel gain variation

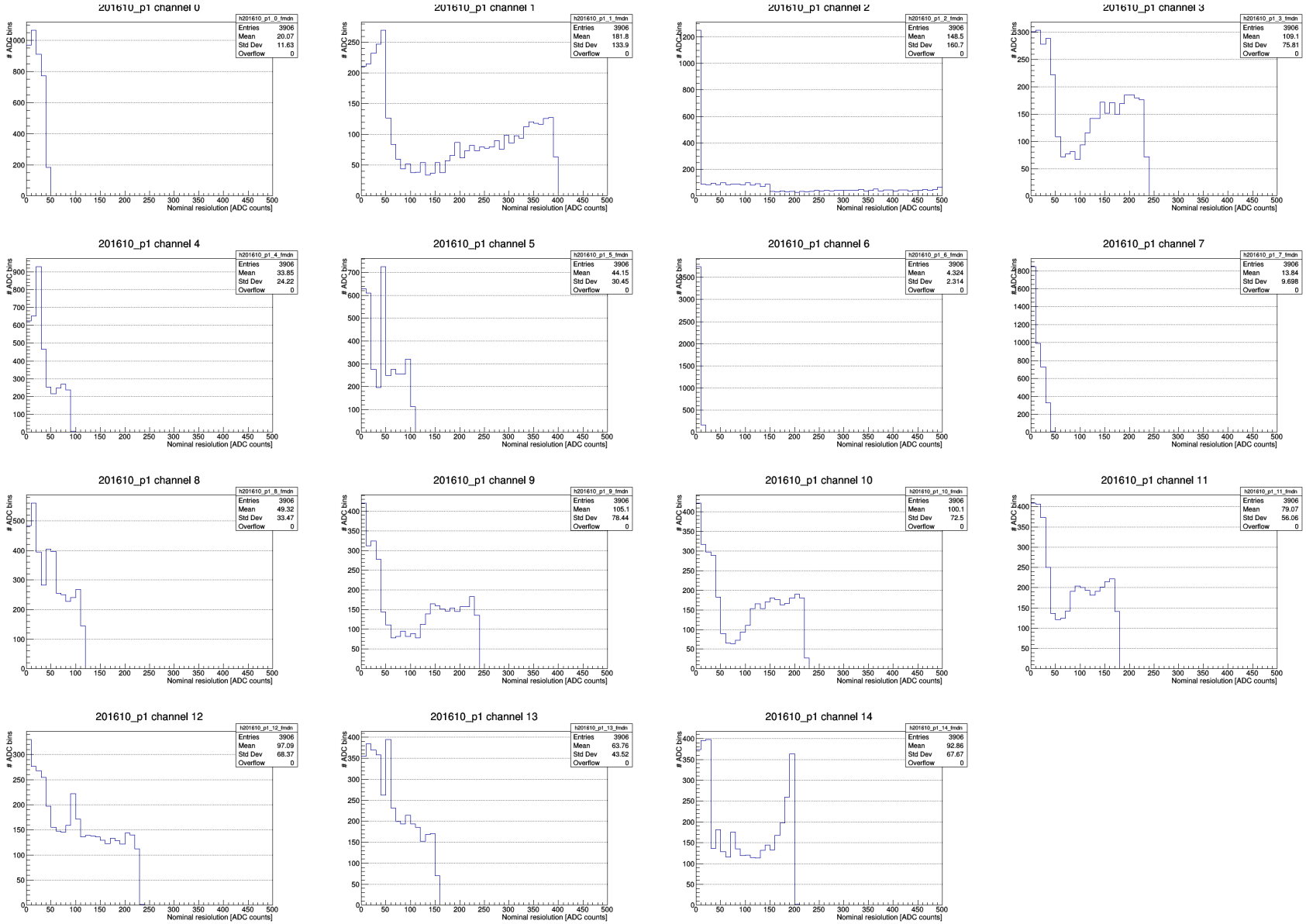
Oct VSTAR nominal resolution



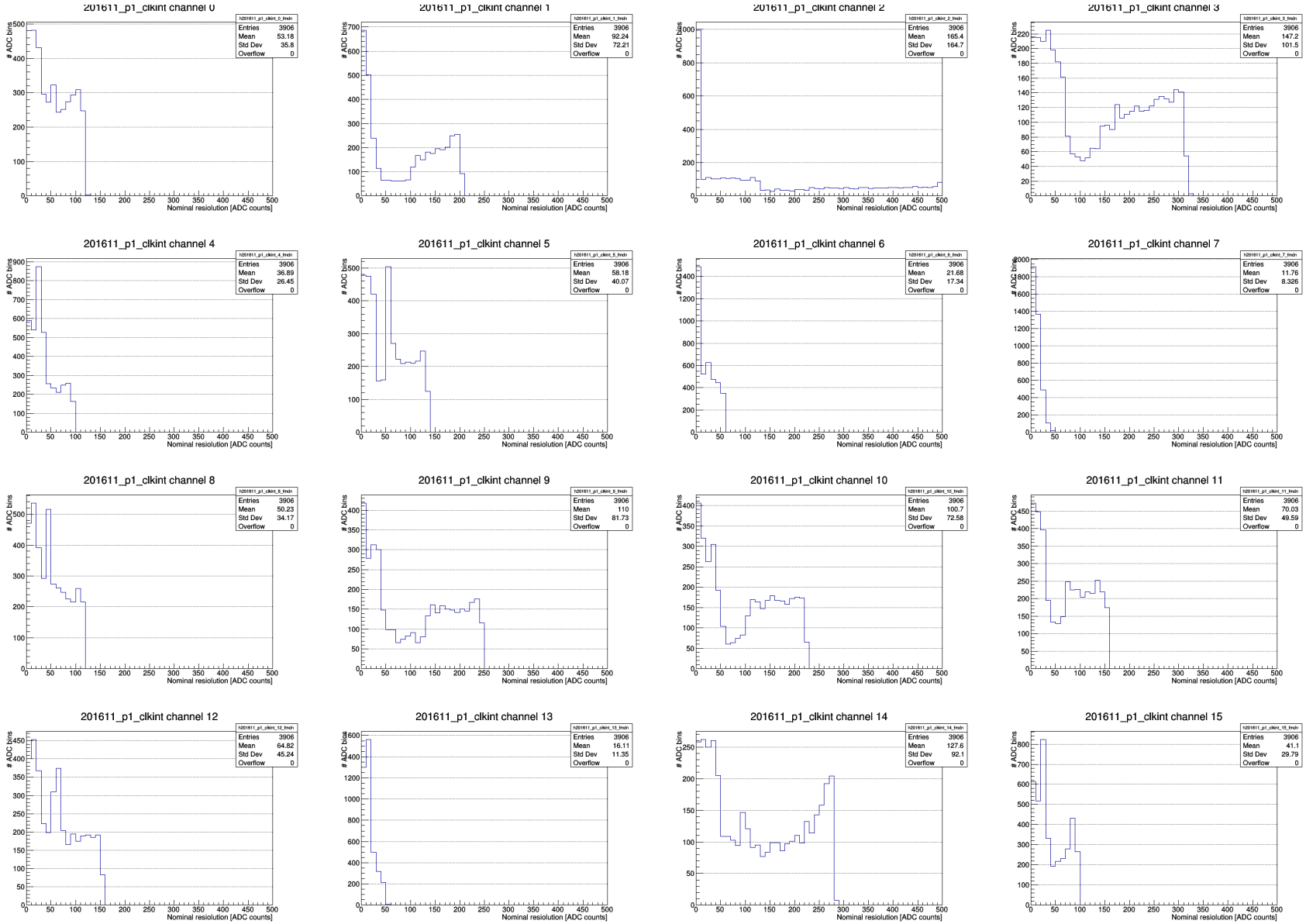
Nov VSTAR nominal resolution



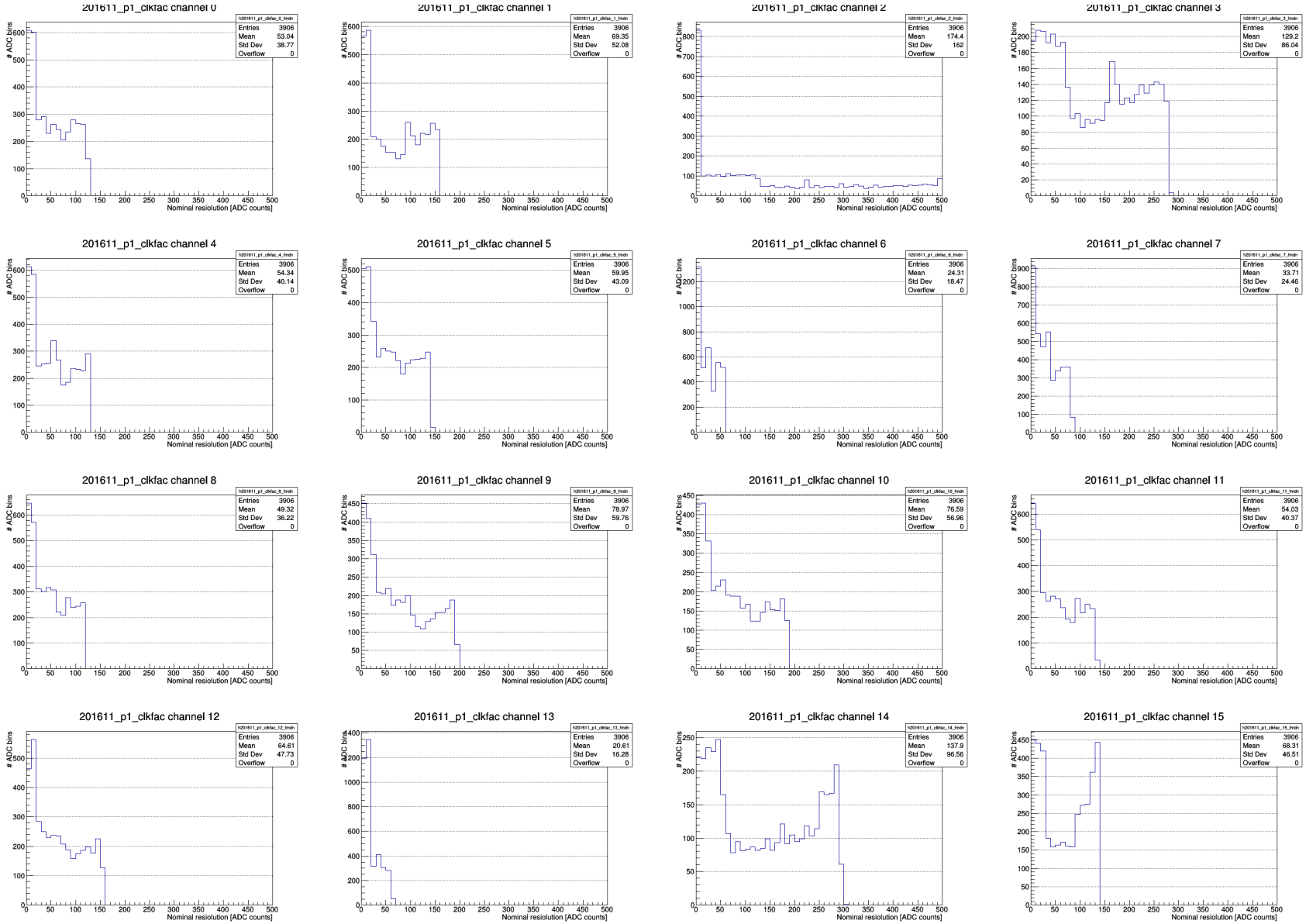
Oct P1 nominal resolution



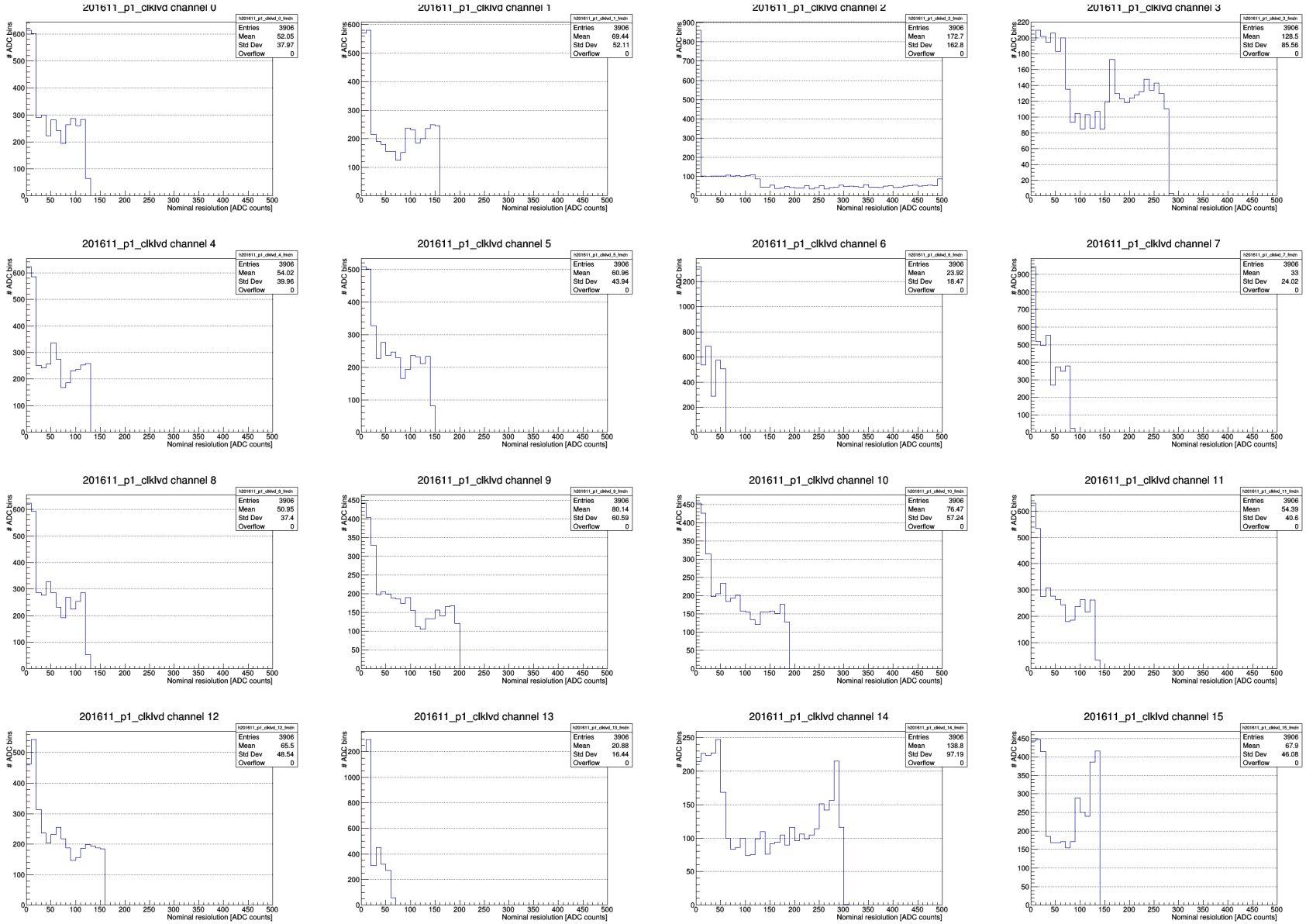
Nov P1 clkint nominal resolution



Nov P1 clkfac nominal resolution



Nov P1 clklvd nominal resolution

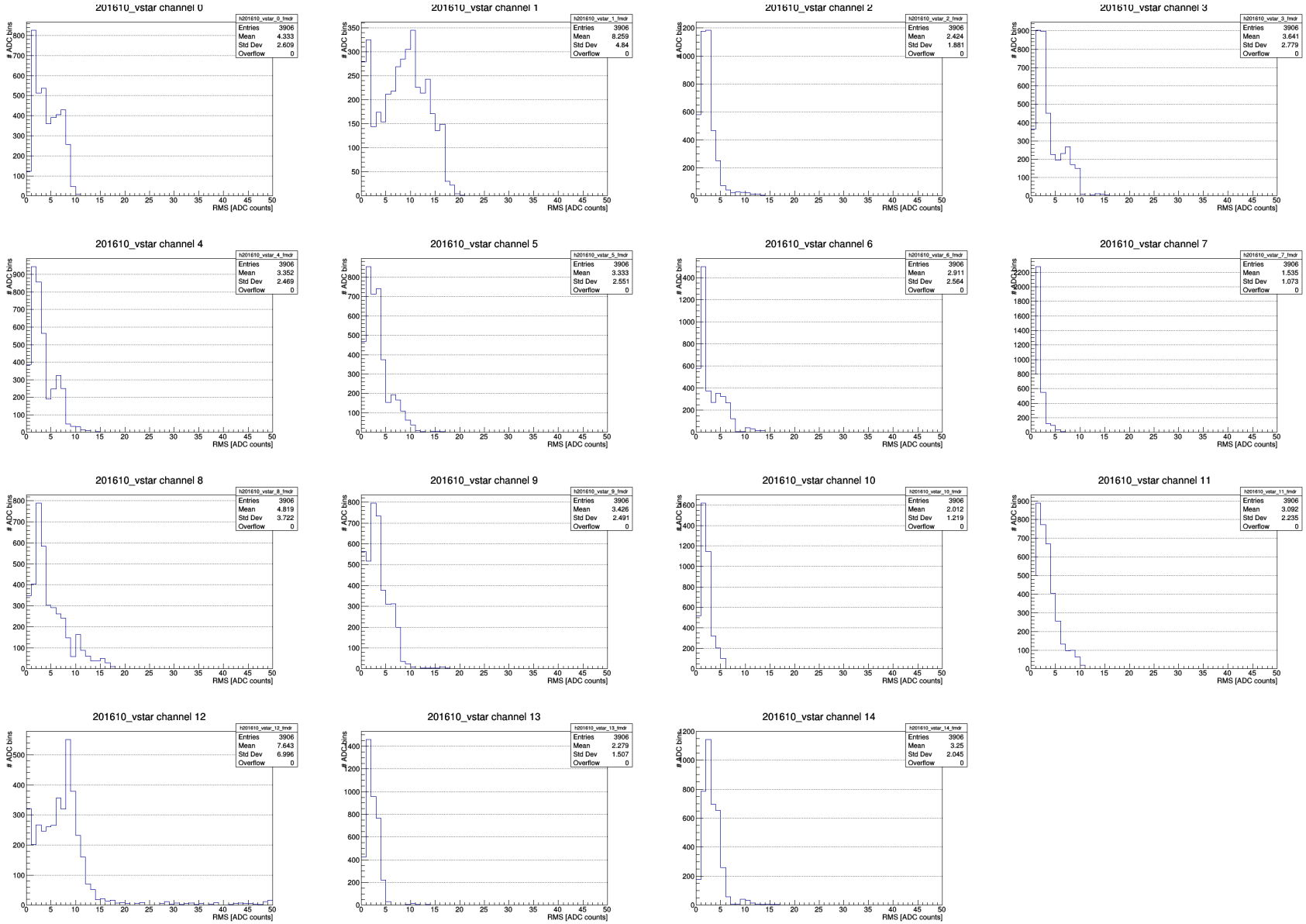


Linear calibrated resolutions

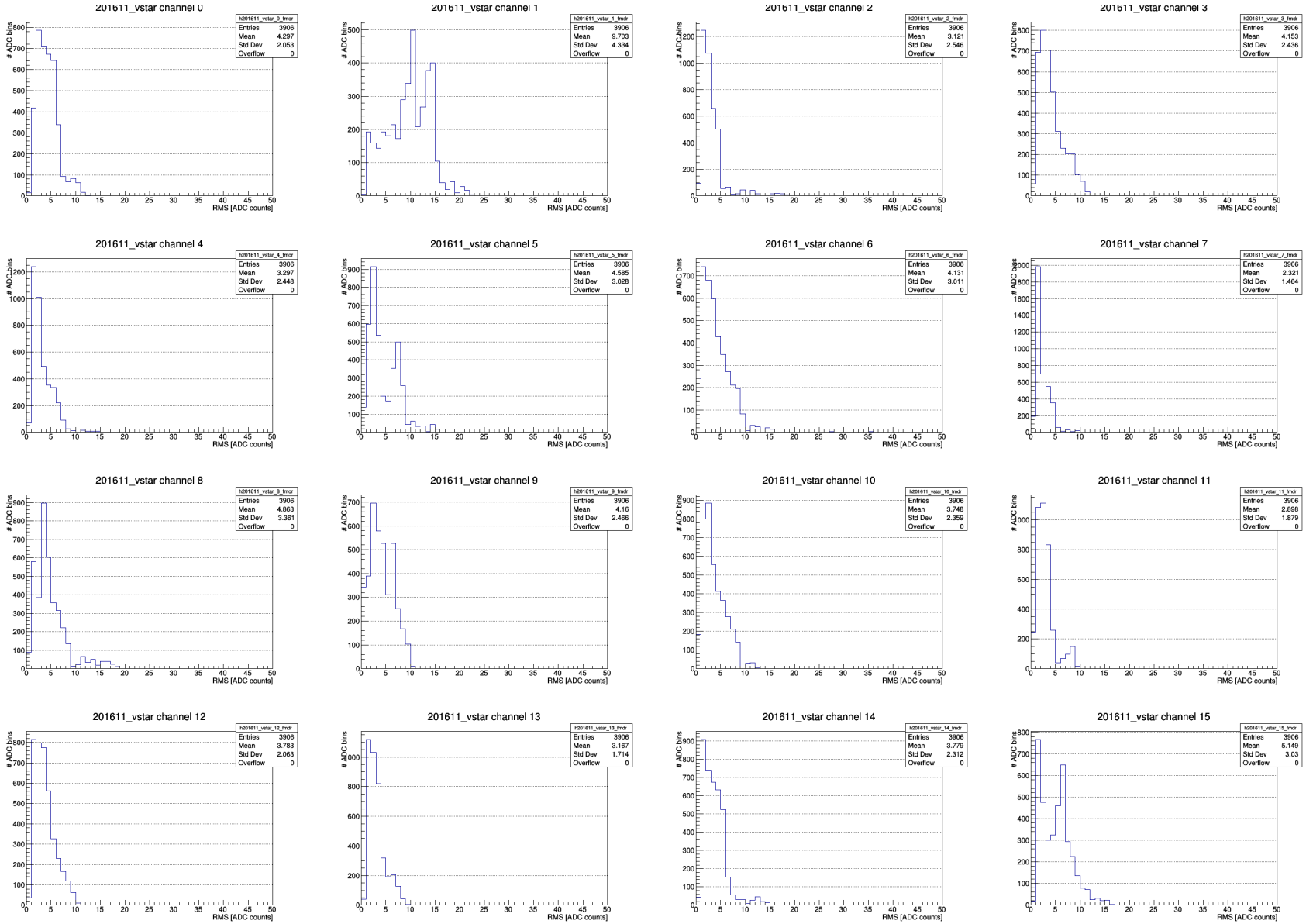
Following are distributions of resolution after linear calibration

- I.e. separate gain (and pedestal) for each channels
  - From the fits shown earlier
- Separate distribution shown for each channel
  - Stuck bins and ADC < 64 are excluded
  - Sum over all channels shown later
- Note horizontal scale is 10X smaller that for preceding nominal plots
- Dominant contribution to the resolution is the non-linearity

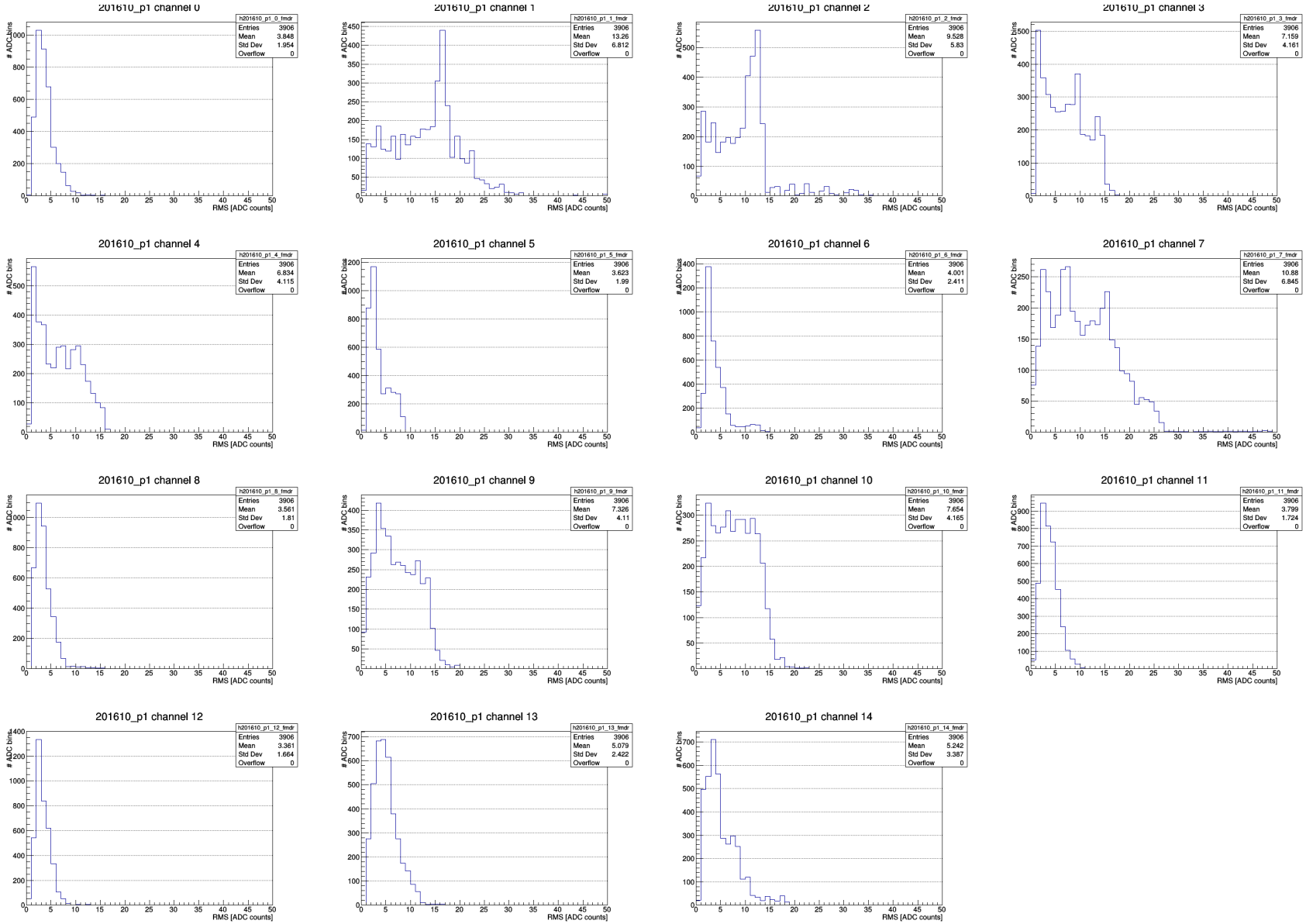
Oct VSTAR fit RMS



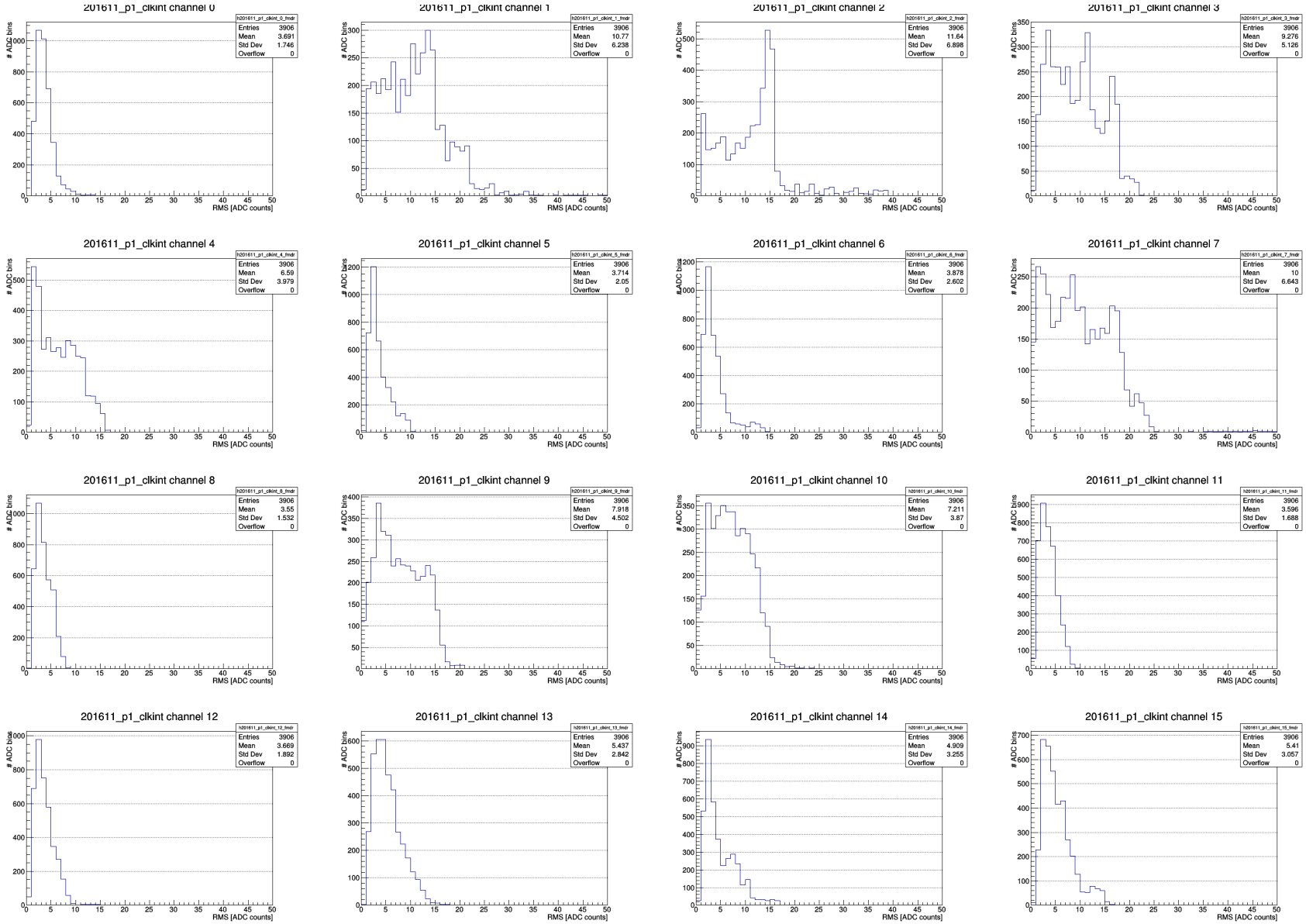
Nov VSTAR fit RMS



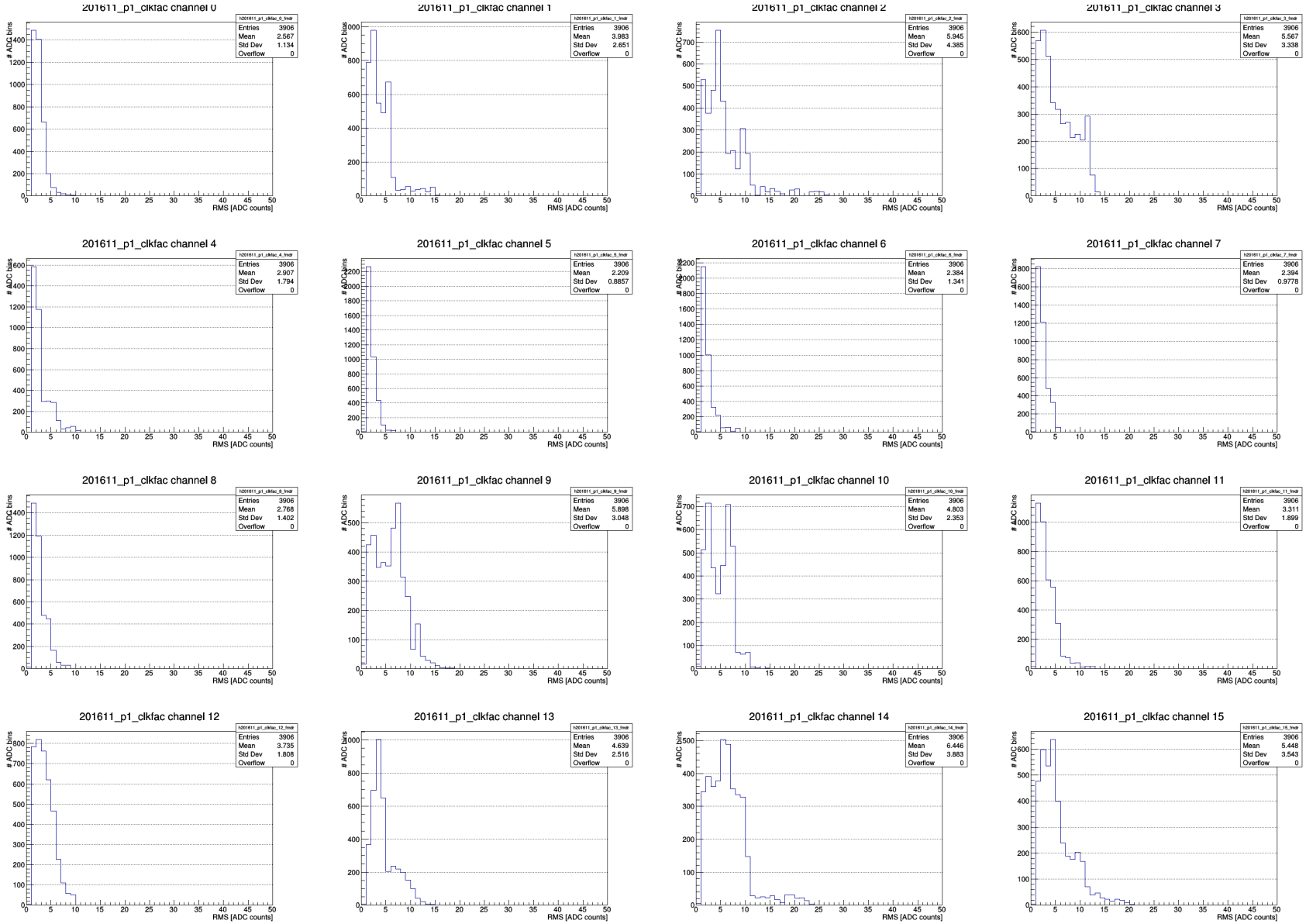
Oct P1 fit RMS



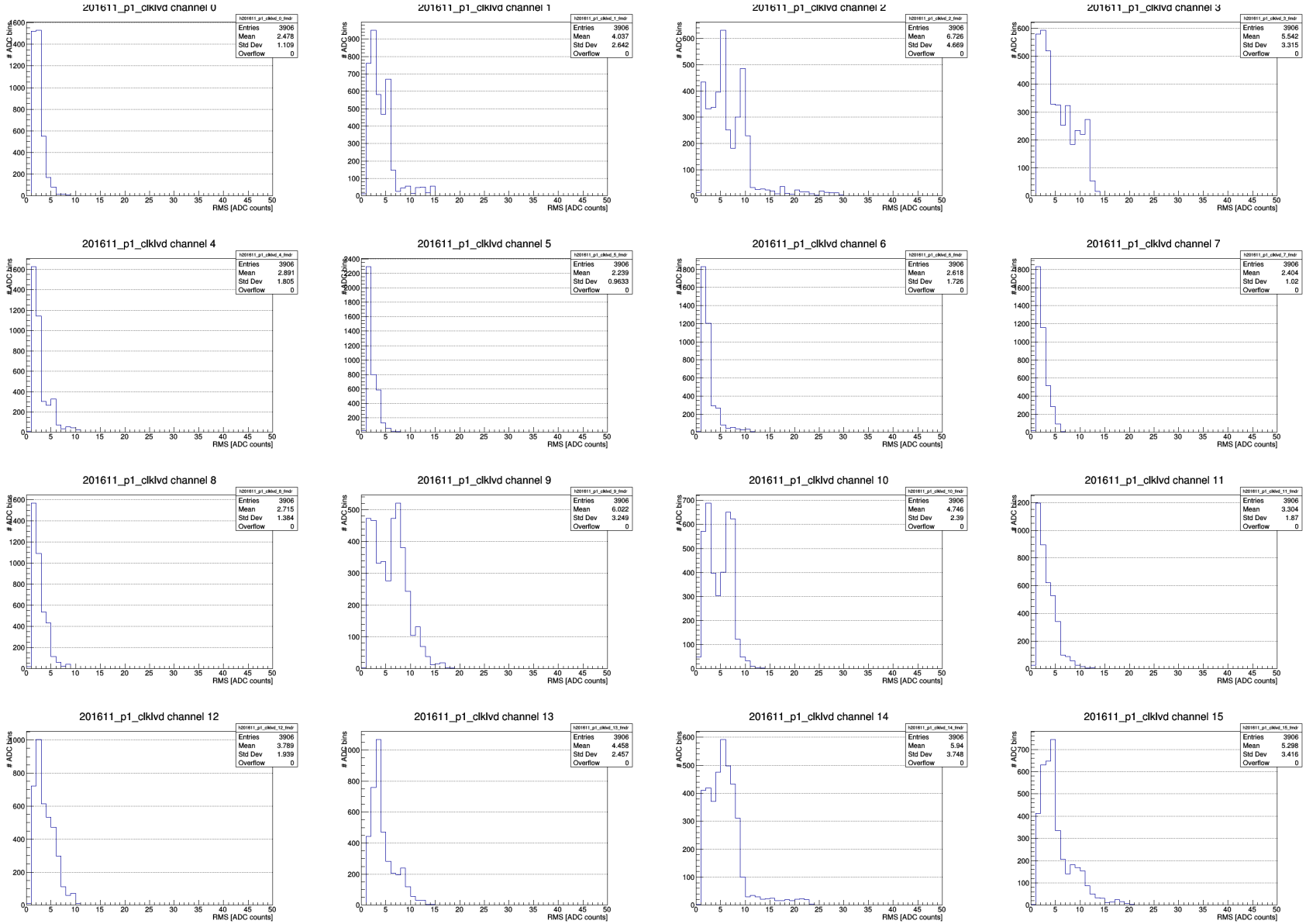
Nov P1 clkint fit RMS



Nov P1 clkfac fit RMS



Nov P1 clklvd fit RMS

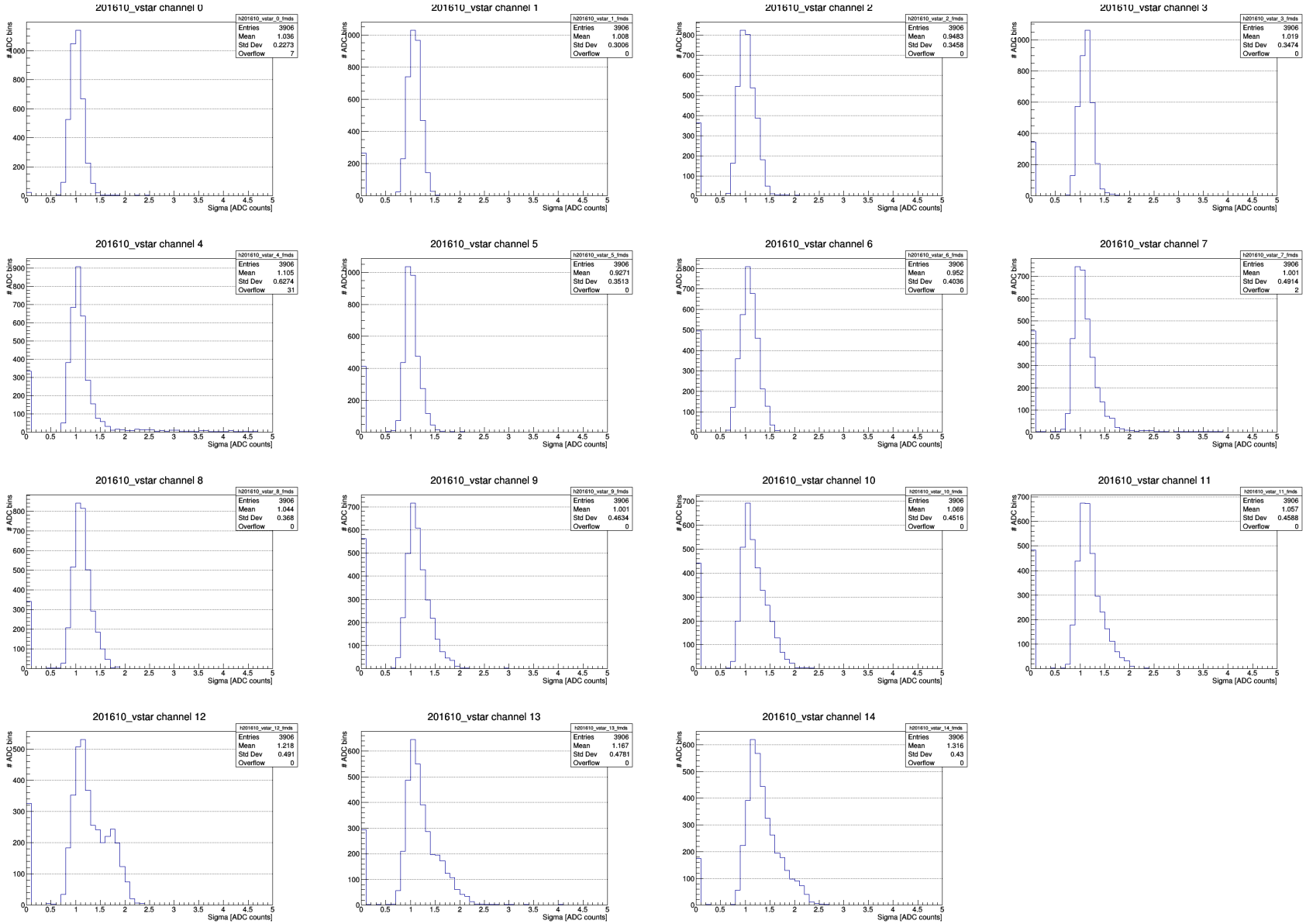


Ultimate resolutions

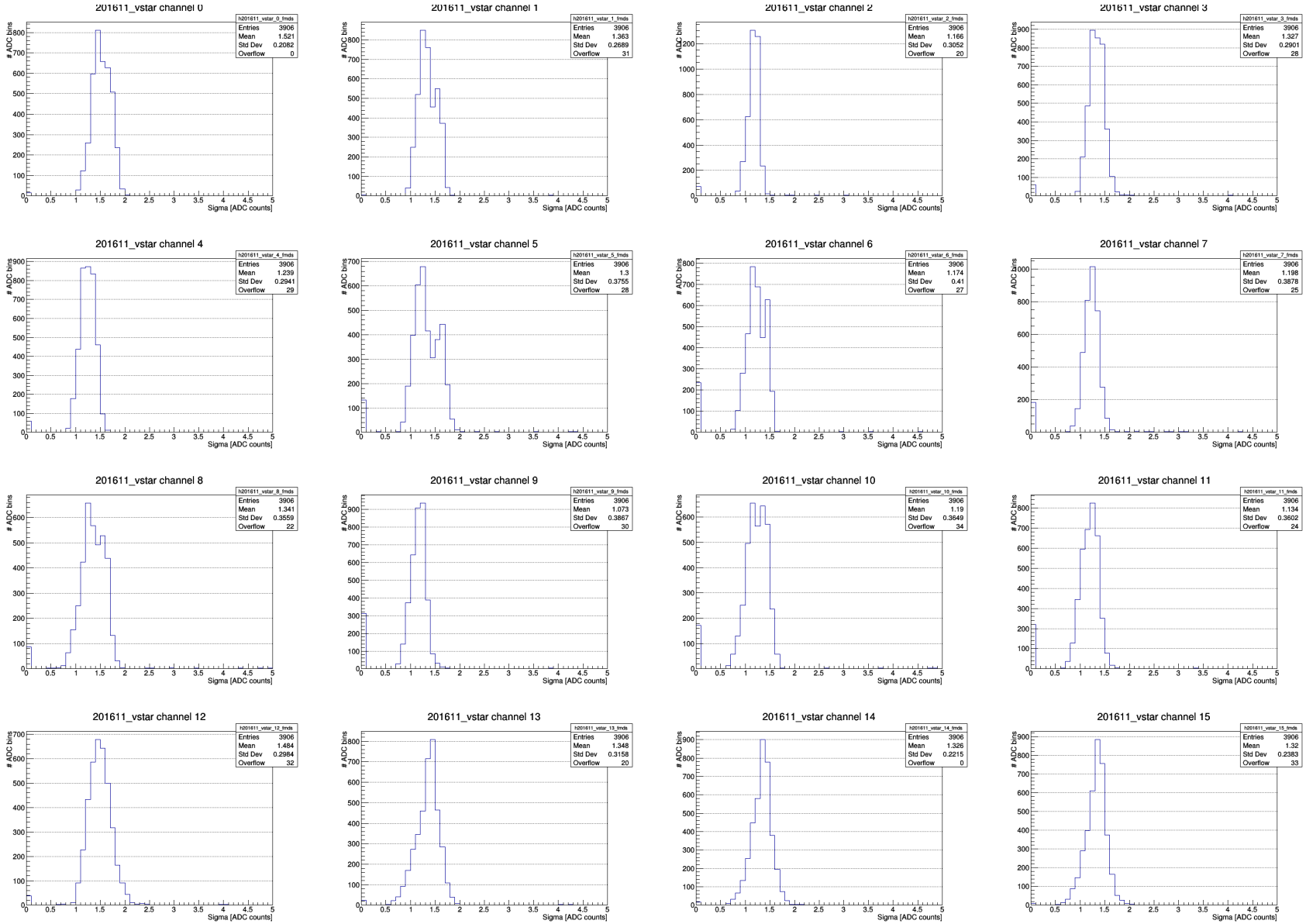
Following are distributions of “ultimate” resolution

- I.e. as though we had a lookup for each channel and ADC bin
- Using the standard deviation from the fits shown earlier
- Separate distribution shown for each channel
  - Stuck bins and ADC < 64 are excluded
  - Sum over all channels shown later
- Note horizontal scale is 10X smaller that for preceding plots
- Resolution is presumably that of the ADC or the measurement system
  - Result for integerization would be 1/sqrt(12) = 0.29

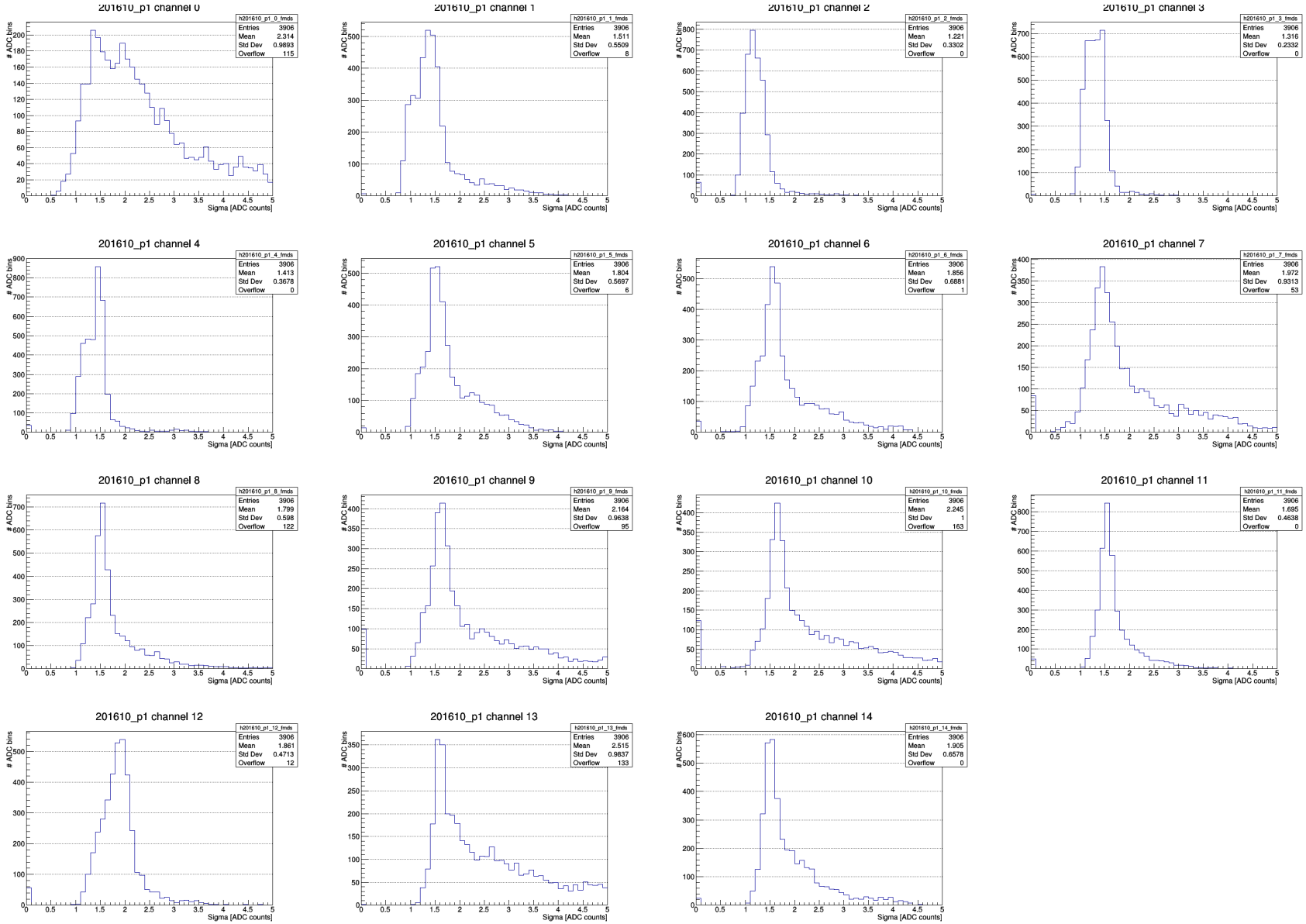
Oct VSTAR fit sigma



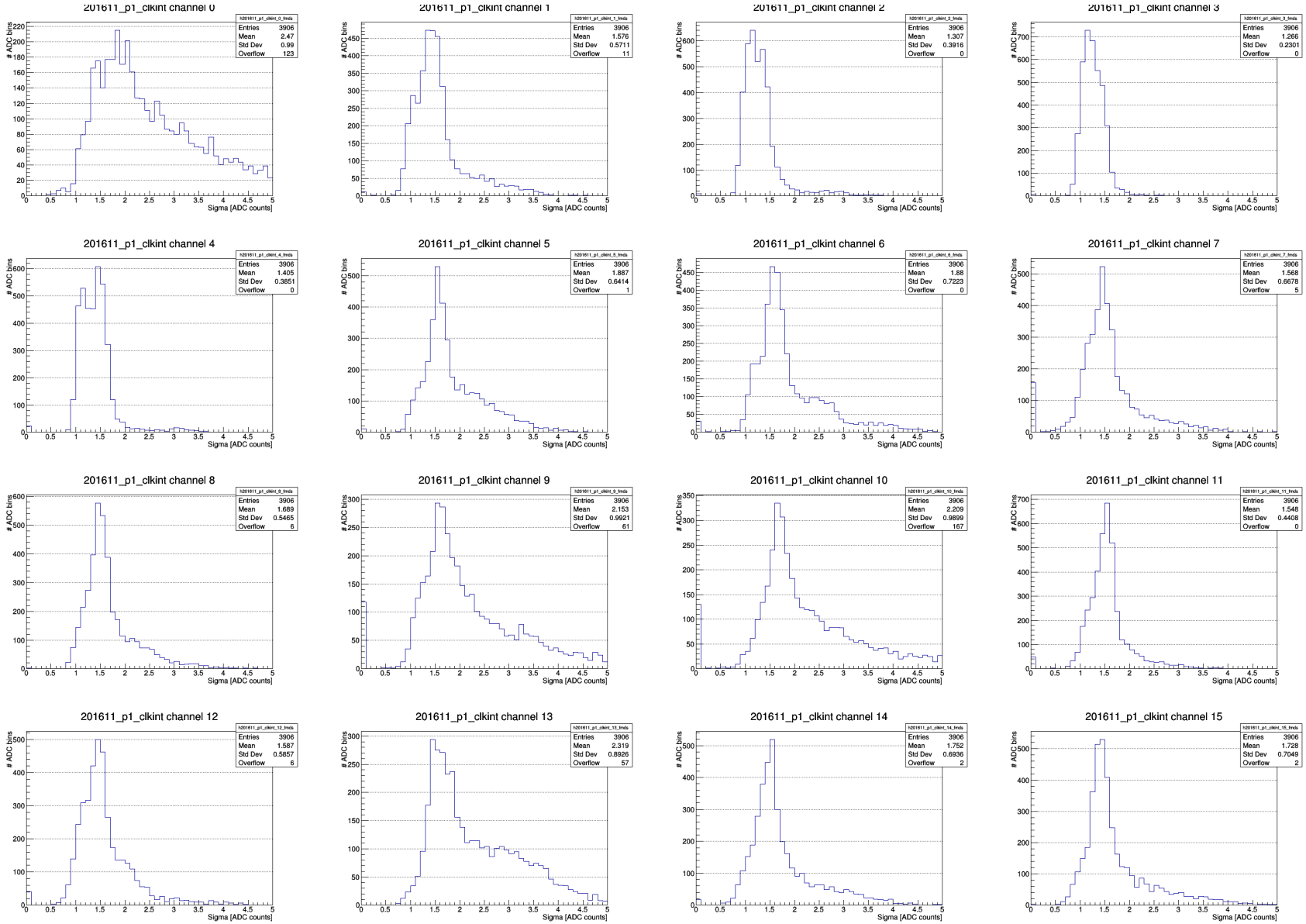
Nov VSTAR fit sigma



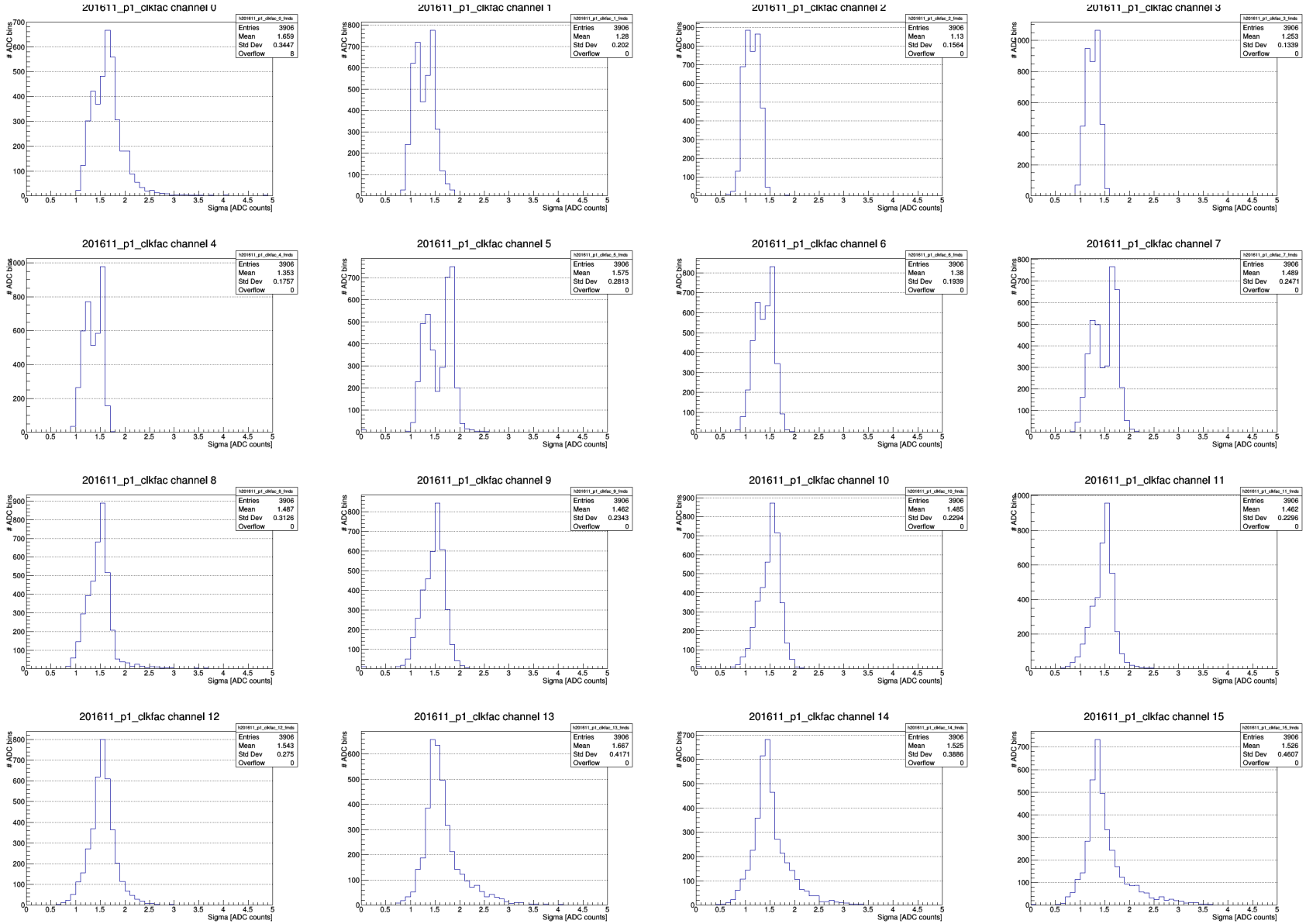
Oct P1 fit sigma



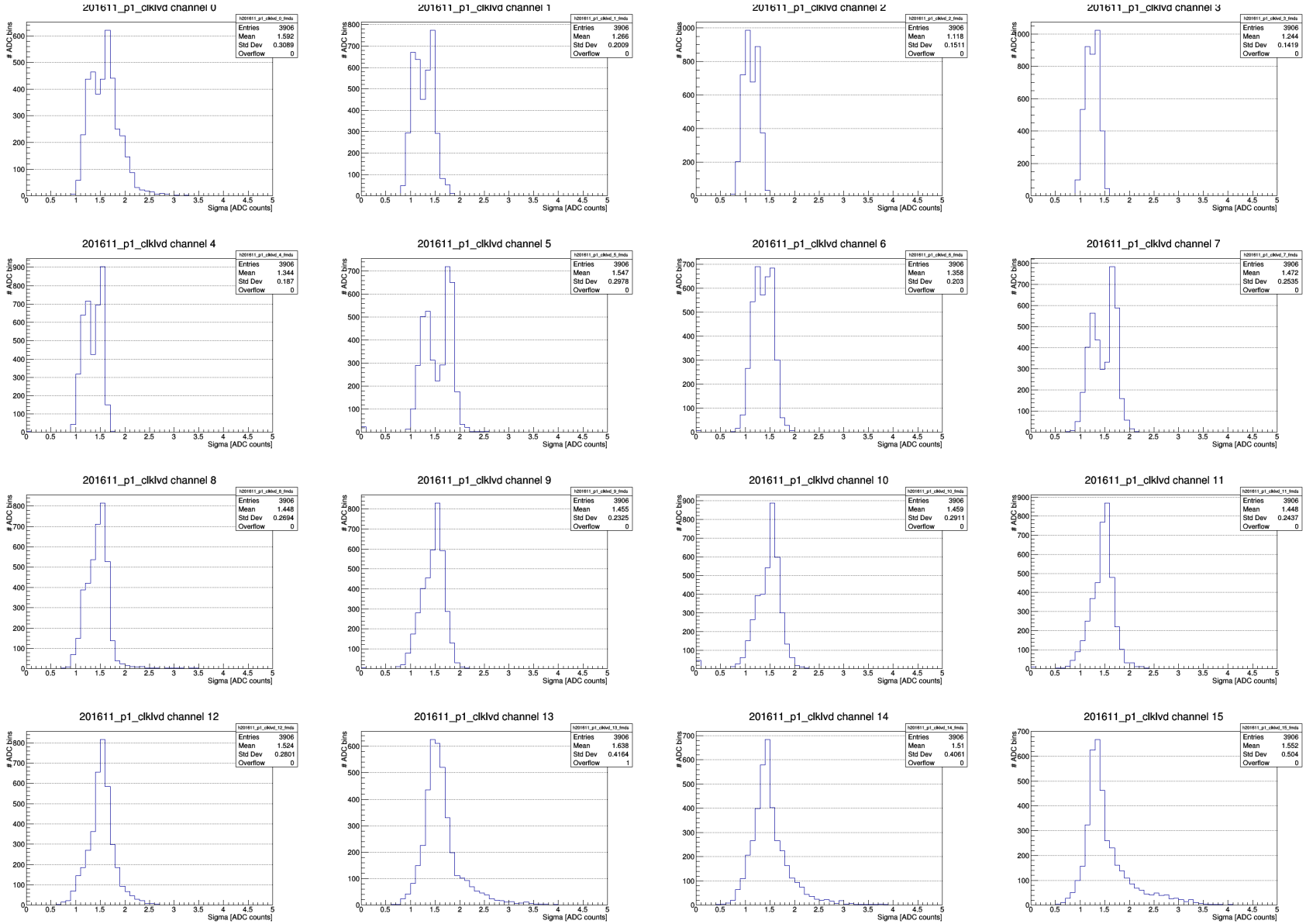
Nov P1 clkint fit sigma



Nov P1 clkfac fit sigma



Nov P1 clklvd fit sigma

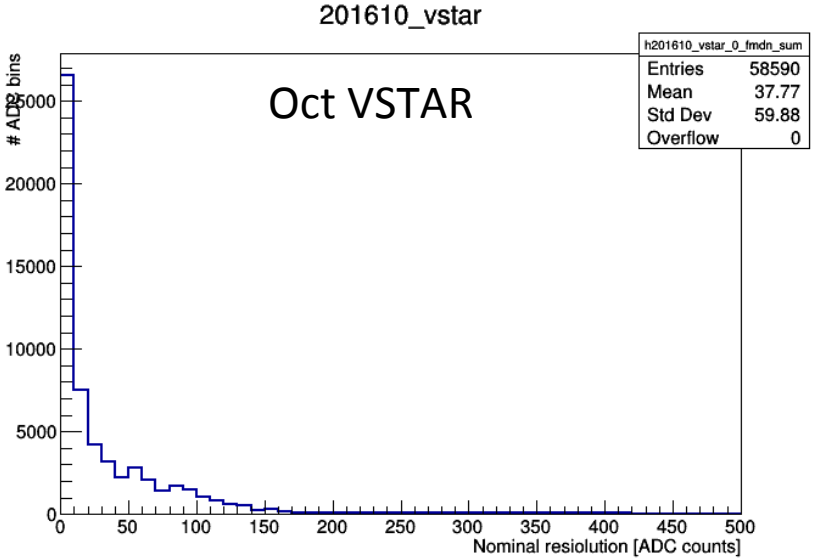


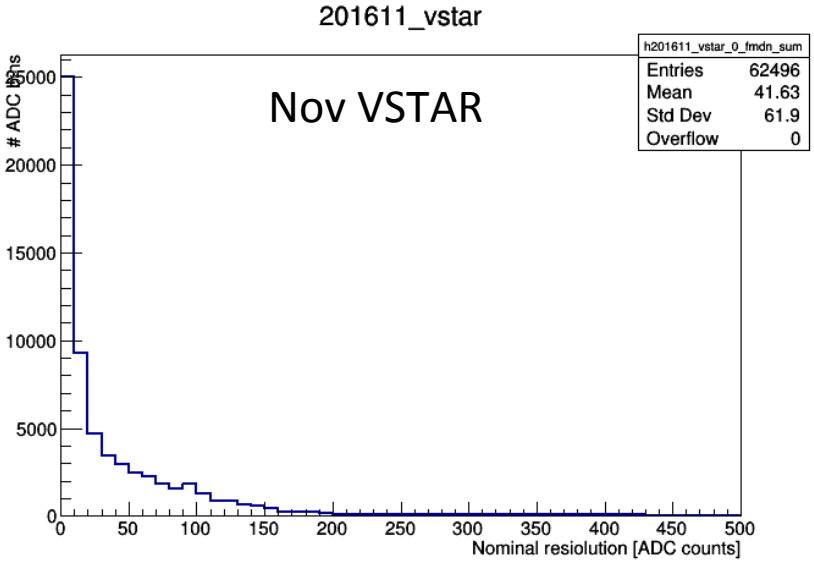
Resolution summary

Add channels from preceding plots

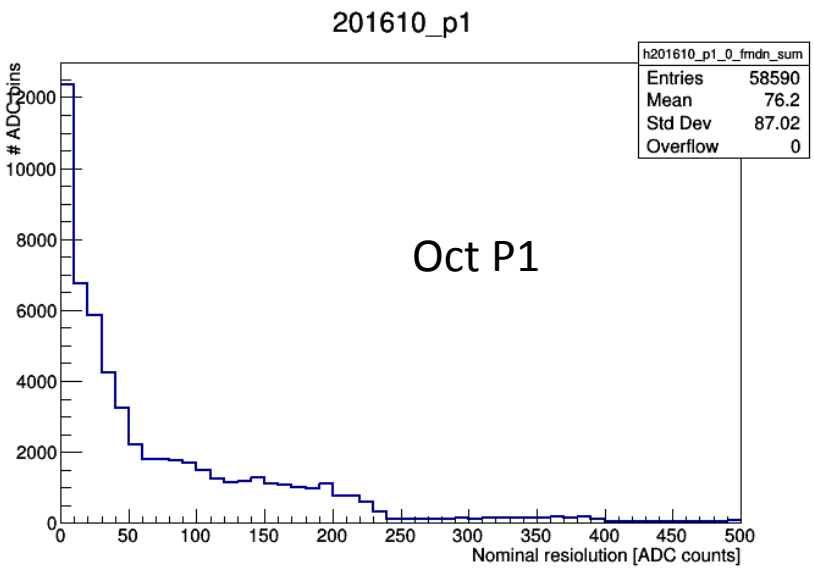
- Each plot includes all channels and bins for the indicates samples
- Except stuck bits and ADC < 64 are excluded
- Plots for stuck bits are also shown for the ultimate resolution

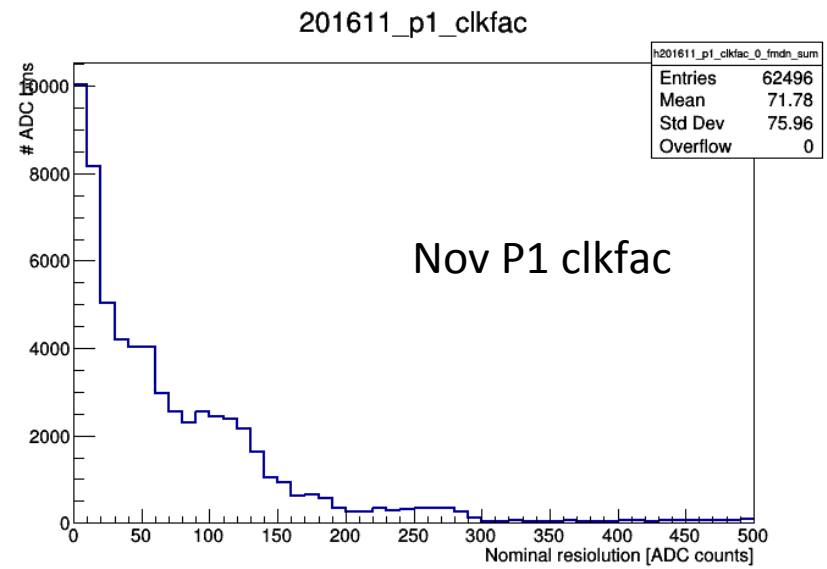
VSTAR nominal resolution

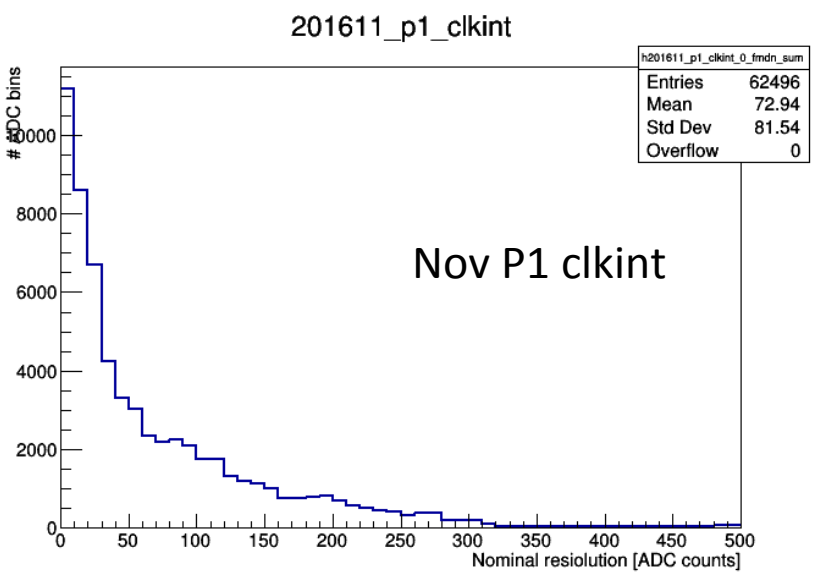


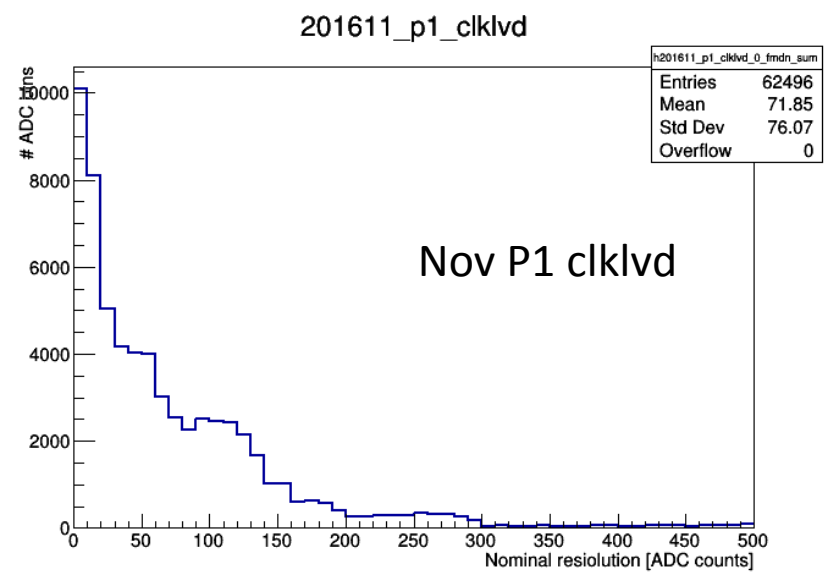


P1 nominal resolution

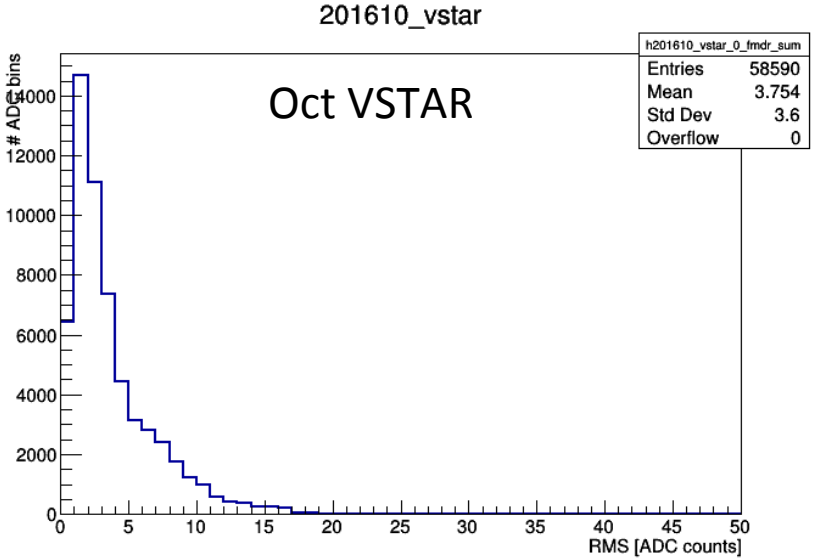


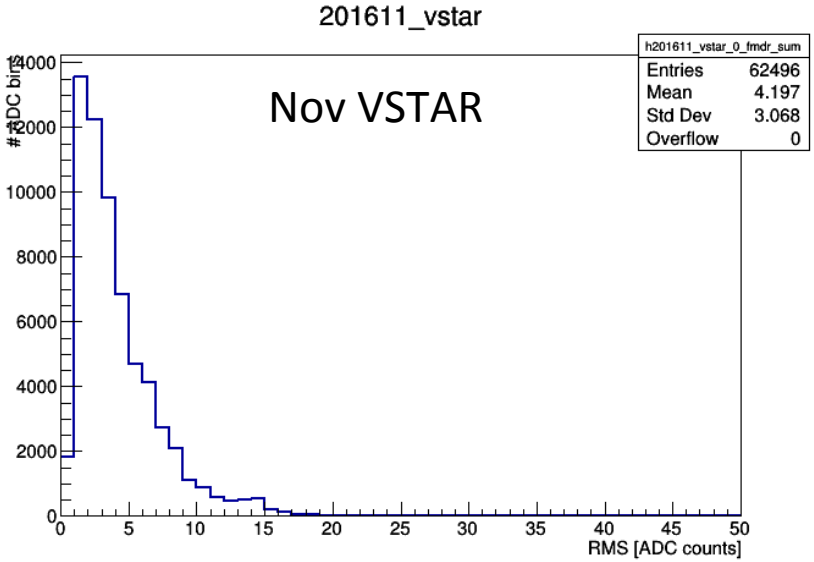




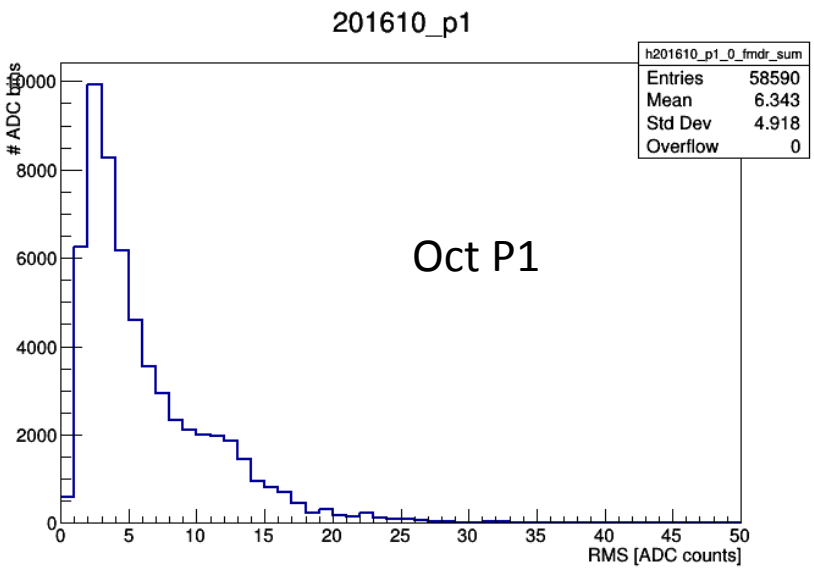


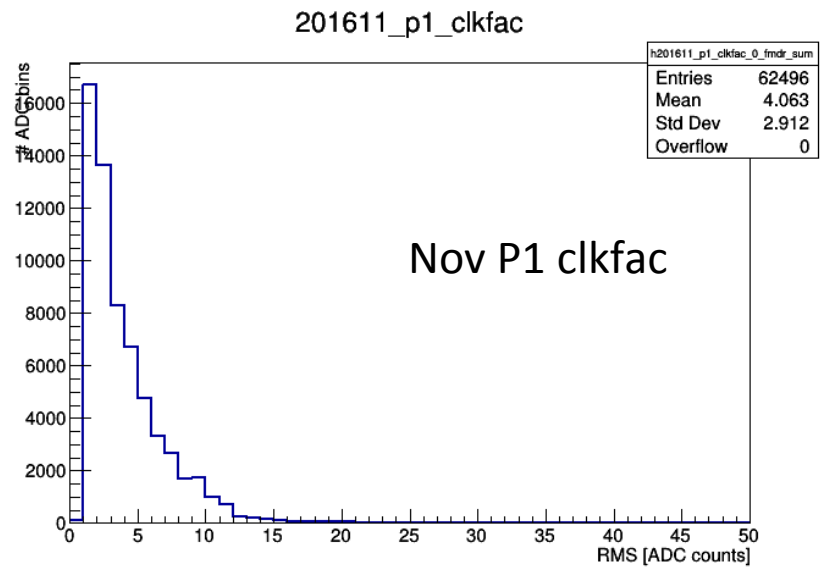
VSTAR fit resolution (RMS)

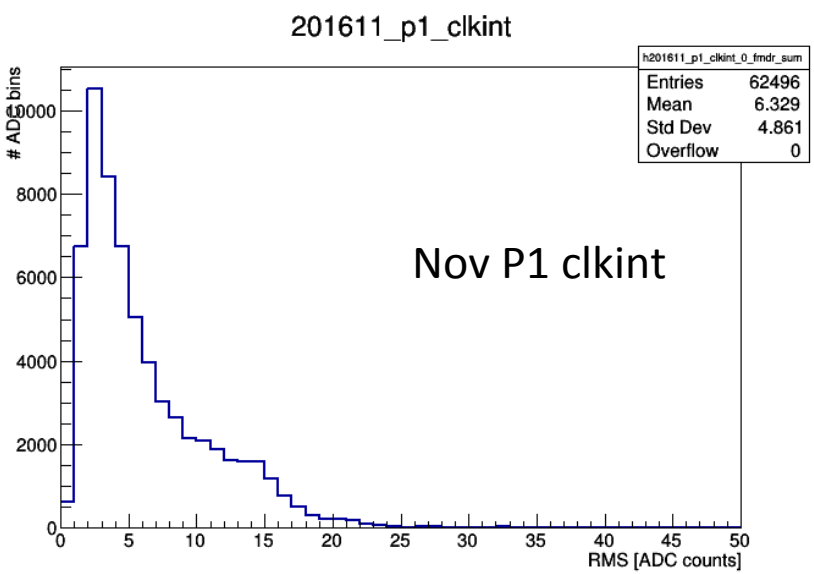


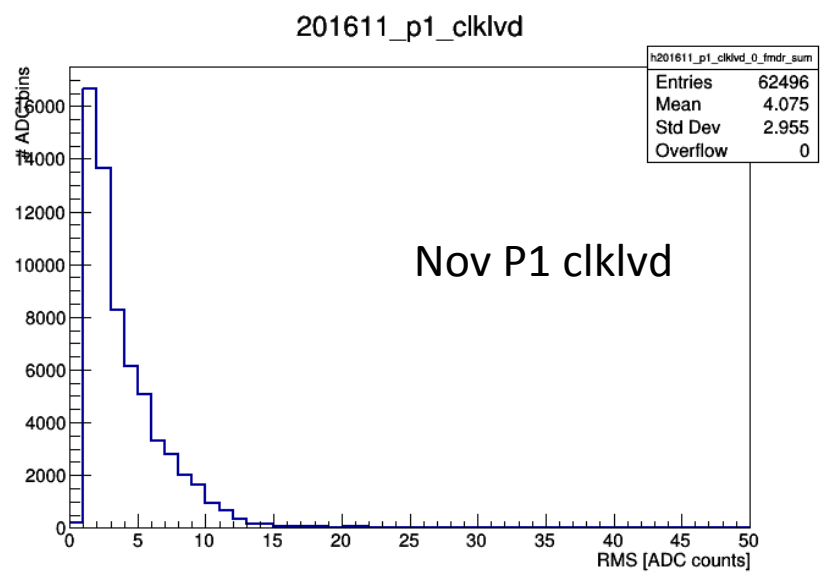


P1 fit resolution (RMS)

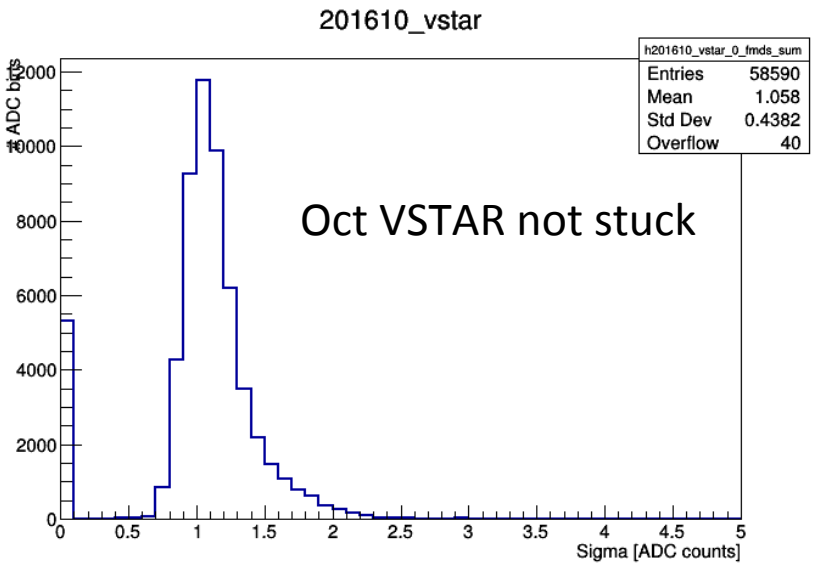


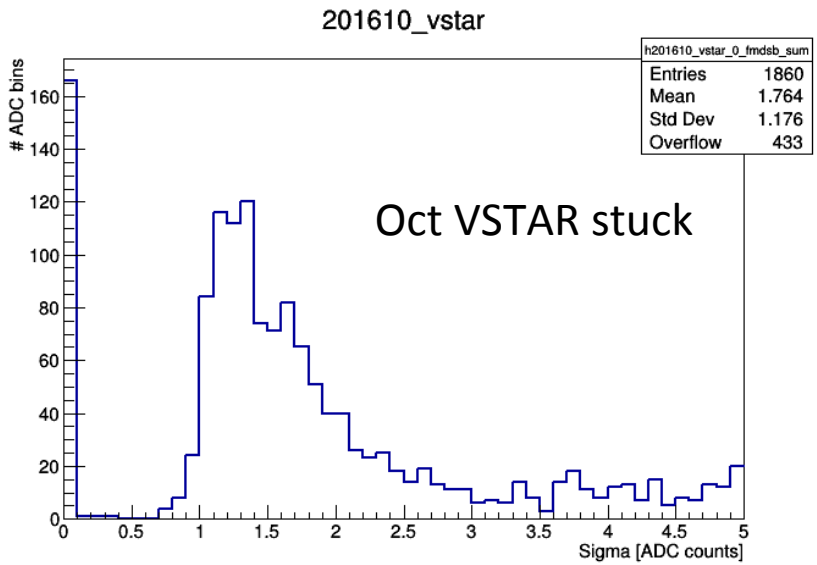


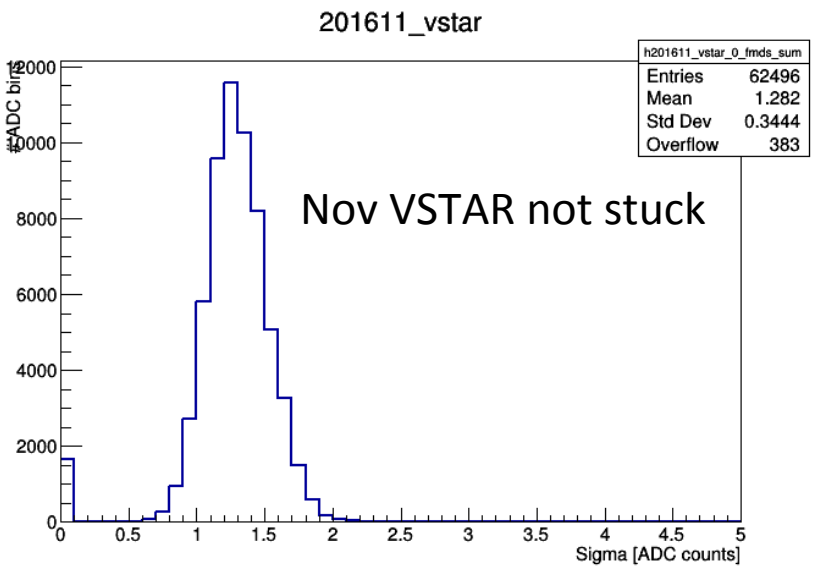


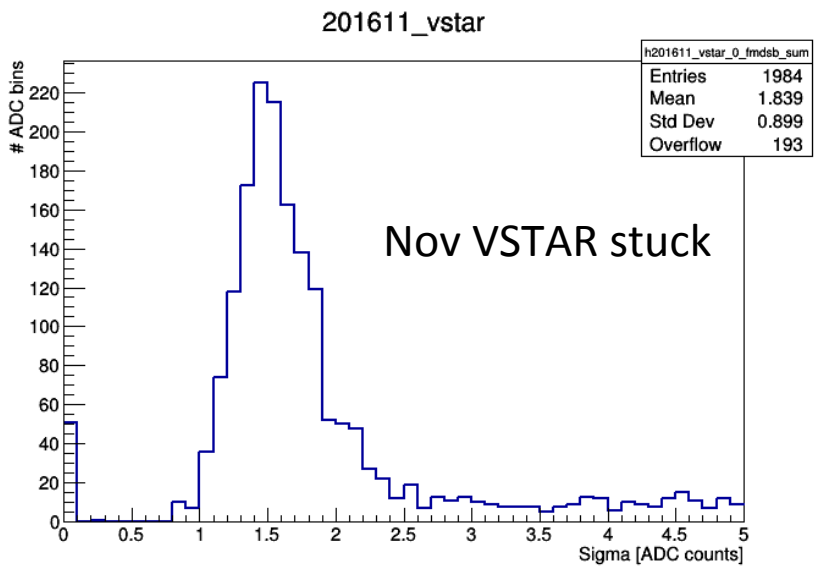


VSTAR ultimate resolution (sigma)

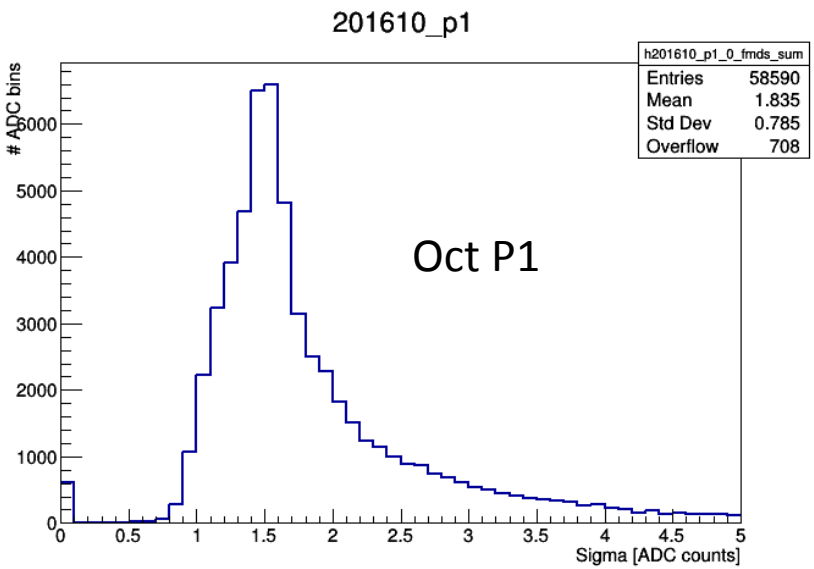


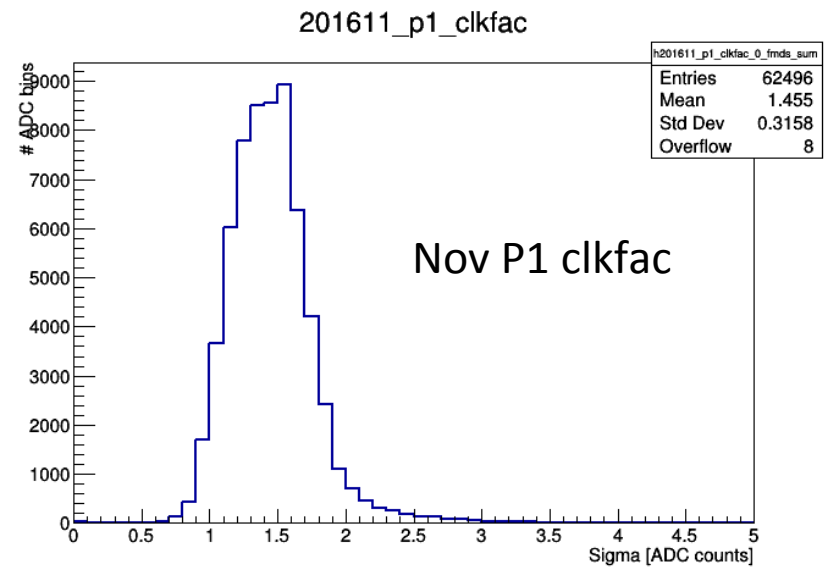


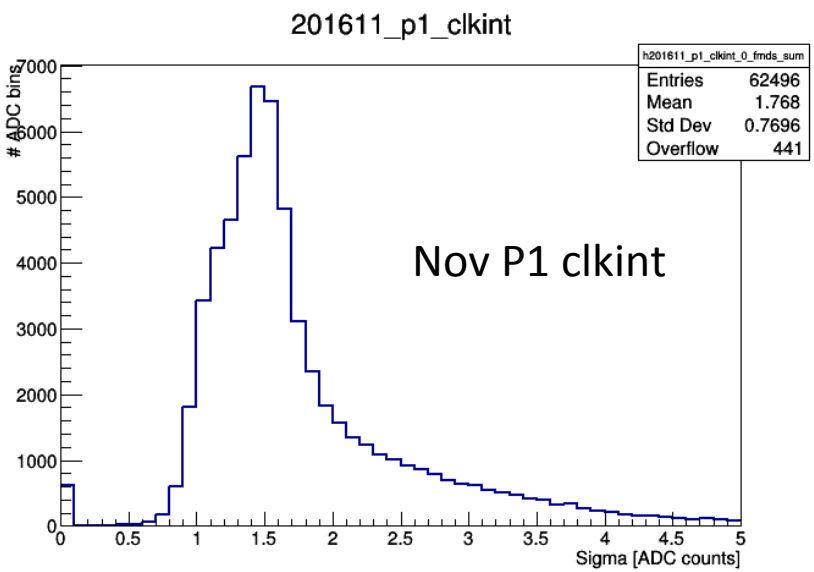


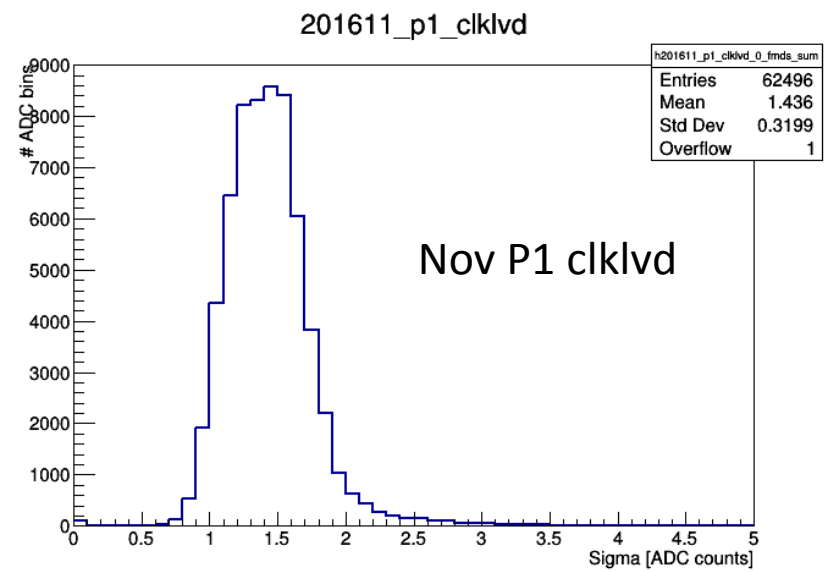


P1 ultimate resolution (sigma) for non-stuck bins

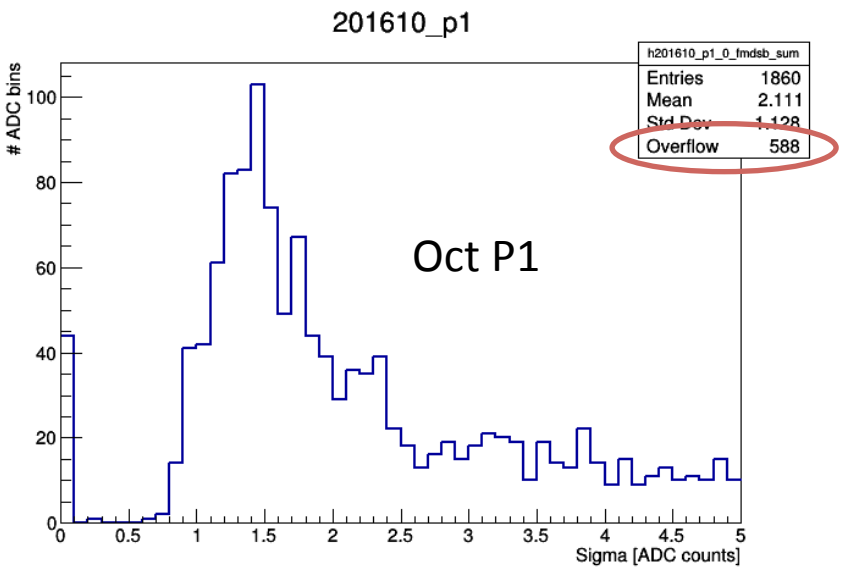


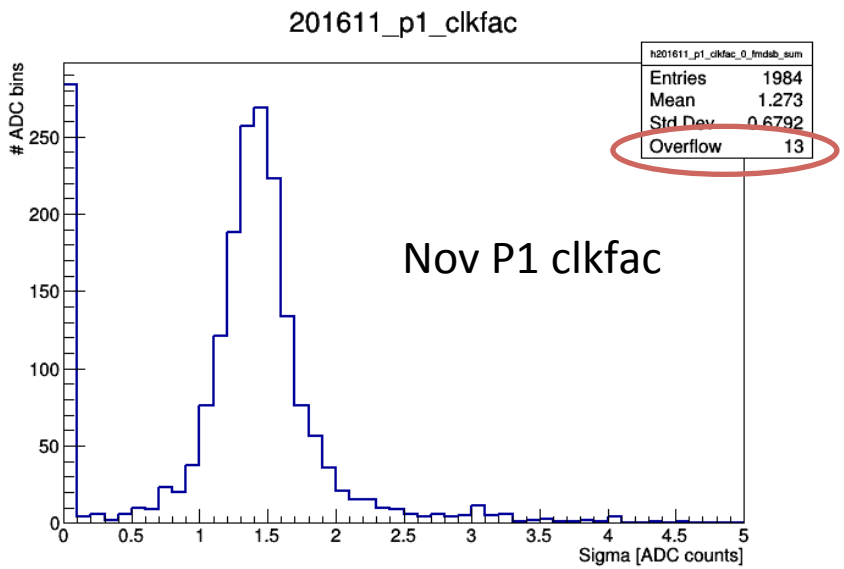


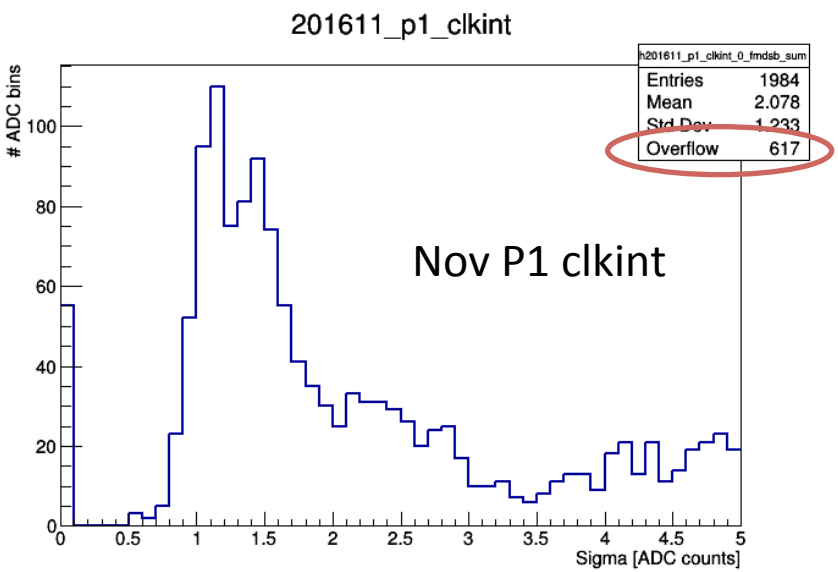


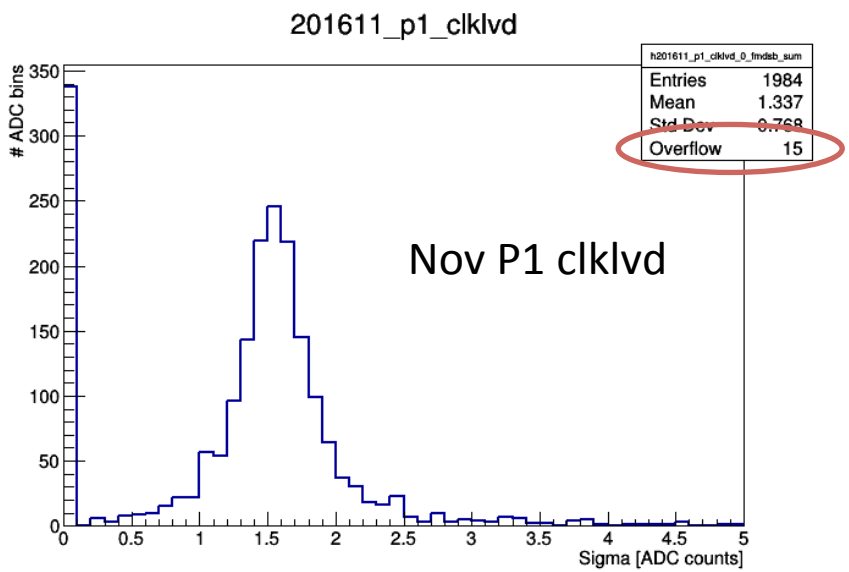


P1 ultimate resolution (sigma) for stuck bins









Comments and conclusions

Both VSTAR and P1 show significant gain variations

- Average resolutions are 42 and 72 ADC counts if not corrected
- Current offline does not correct for gain variations

Linear calibration helps a lot

- Resolutions around 4.2 and 4.1 ADC counts with linear calibration

Ultimate resolutions are better yet

- Average resolutions of 1.3 and 1.45 ADC counts for non-stuck bits
- Direct comparison is not fair because of different gains
  - Resolutions are 0.56 and 0.50 mV
- Significantly above digitization resolution of 0.29 ADC counts
- Not clear (to me) if this is ADC or measurement resolution

VSTAR response wraps around for large signals

- Probably want to avoid this (earlier-generation) device

P1 is significantly worse with internal clock

- Above results are all for the (similar) external clocks

Stuck bits mostly resolved for P1 with external clock

- Response still shows dependence on 6 LSB but many fewer stuck-bit bins are populated by a wide range of V_{in}