ADC performance

BNL DUNE

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April 12, 2017

Introduction

I have been looking at ADC test data taken at BNL

- I report here on data taken in March 2017
  - ADC samples are read out for input voltage steps with sawtooth envelope
  - 9M samples for each ADC channel
    - approximately 2k samples for each ADC bin
- Data is from new P1 chips for protoDUNE
- Data conditions
  - Cold (LN2)
    - There is warm data for one chip
  - 2 MHz sampling
  - All data taken with external clock
    - Earlier studies showed that correct choice of parameters gives better results than internal clock
    - Plan to vary parameters for each chip during testing

Data taking

Data taken by the following team

- Hucheng Chen, Shanshan Gao, Jack Fried, Feng Liu (BNL)
- Damian Goeldi (Univ. of Bern)

Thanks to them to making this data available to me

Data format

- ADC samples
- Input voltage ramp from –200 to 1600 mV at 400 mV/sec

Cold data taken for 76 ADC chips

- 16 channels each
  - I.e. a total of 1232 ADC channels
  - And a total of 5.0 M ADC bins (4096 bin/codes per channel)
- Chip packaging:
  - Chips D01-D40 in Quik-Pak packages
  - D41-D79 in MOSIS

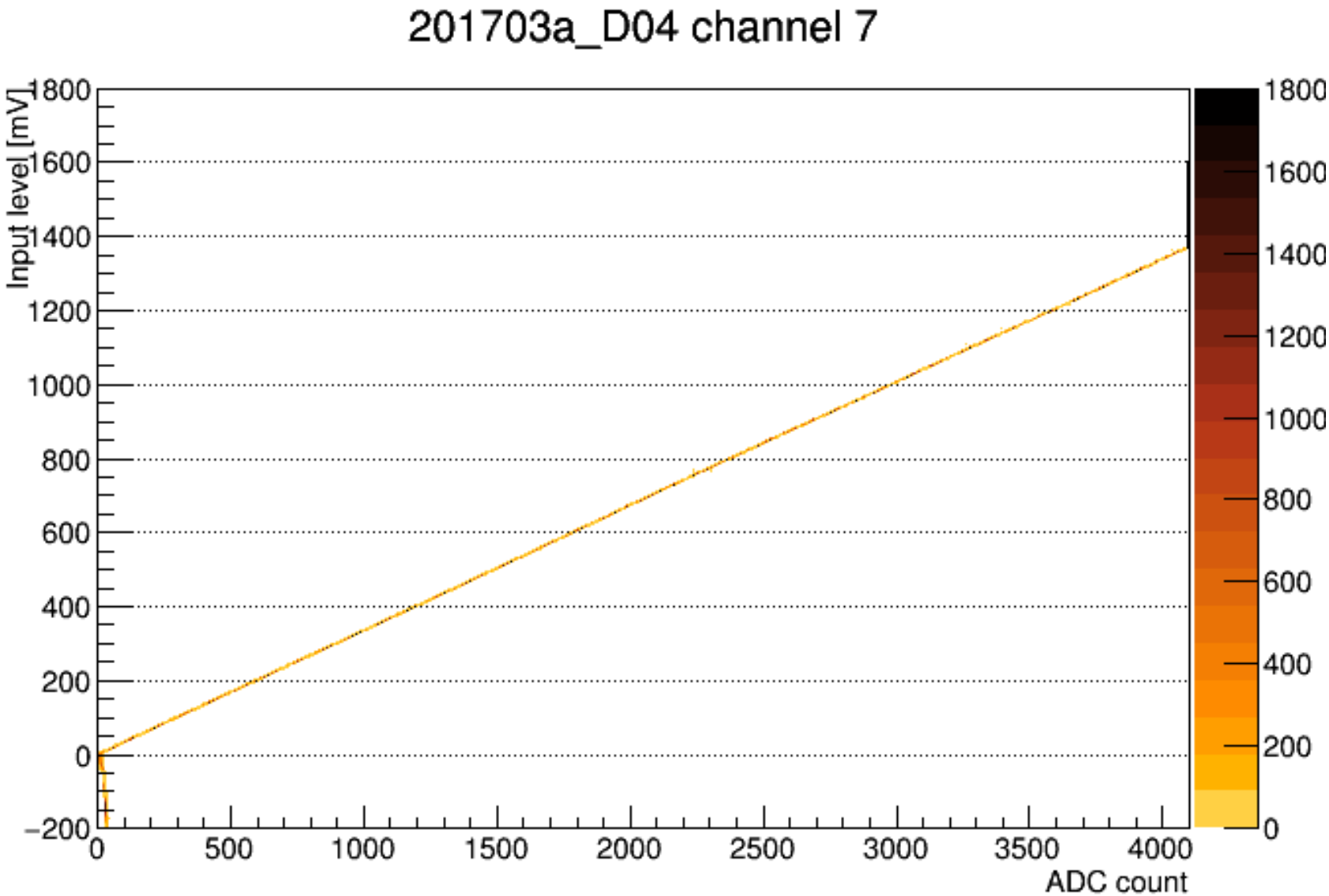
Data analysis 1: linear fit and residual

I process each channel separately

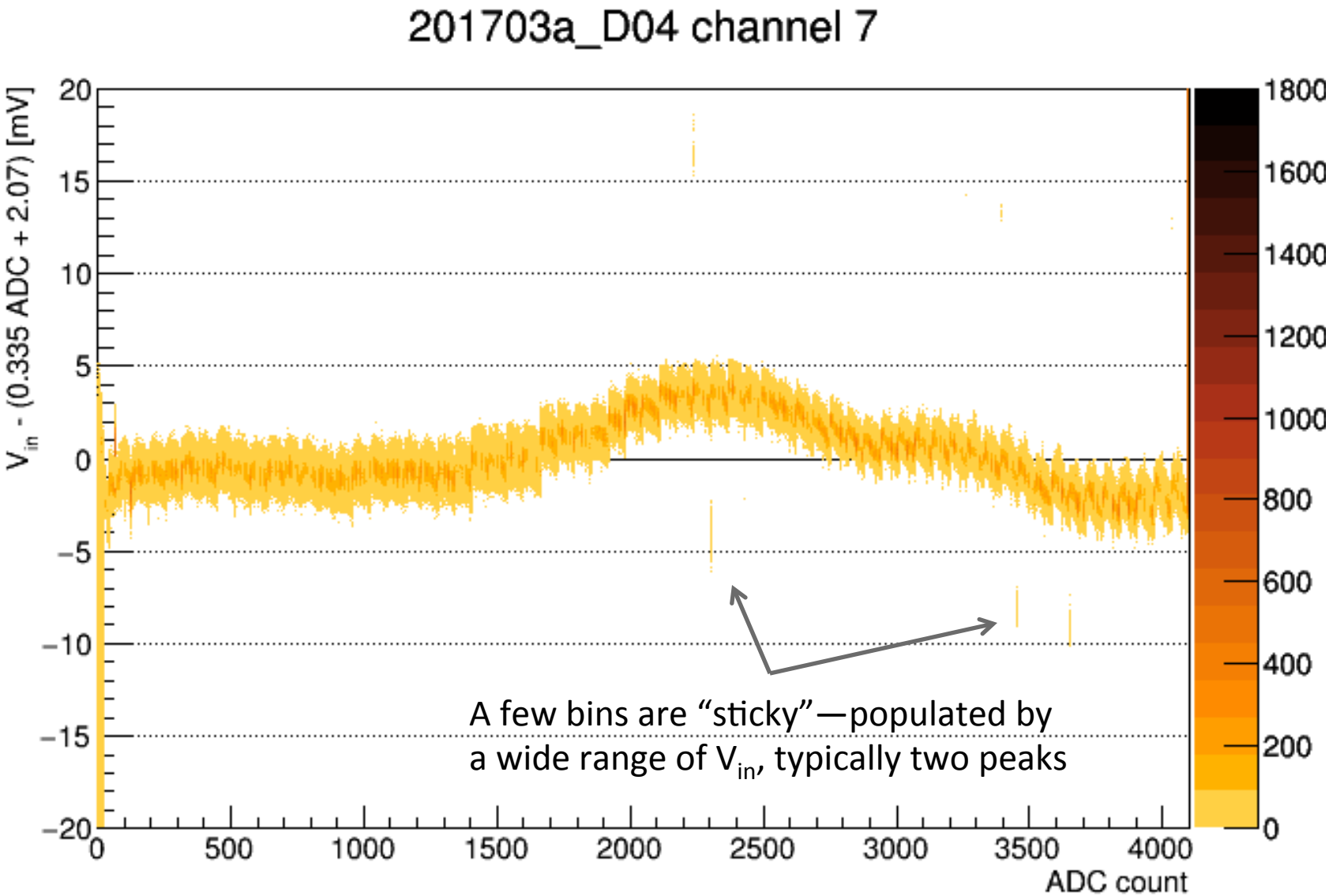
Initial data analysis

- Read samples from the provided file for the chip and channel
- Create 2D histograms of inverse response: V_{in} vs. bin
  - bin = ADC code and covers the range [0, 4095]
- I make a linear fit of the inverse response for each channel
  - V_{in} = gain×(ADC code) + offset
  - Require 64 < ADC < 4095
  - And 0 < V_{in} < 1600 mV
- I then plot the linear-fit residual
  - I.e. the difference between the measured V_{in} and the linear-fit value for each sample
- Examples for one channel follow
  - March data for chip D04 channel 7
  - This is a “good” channel

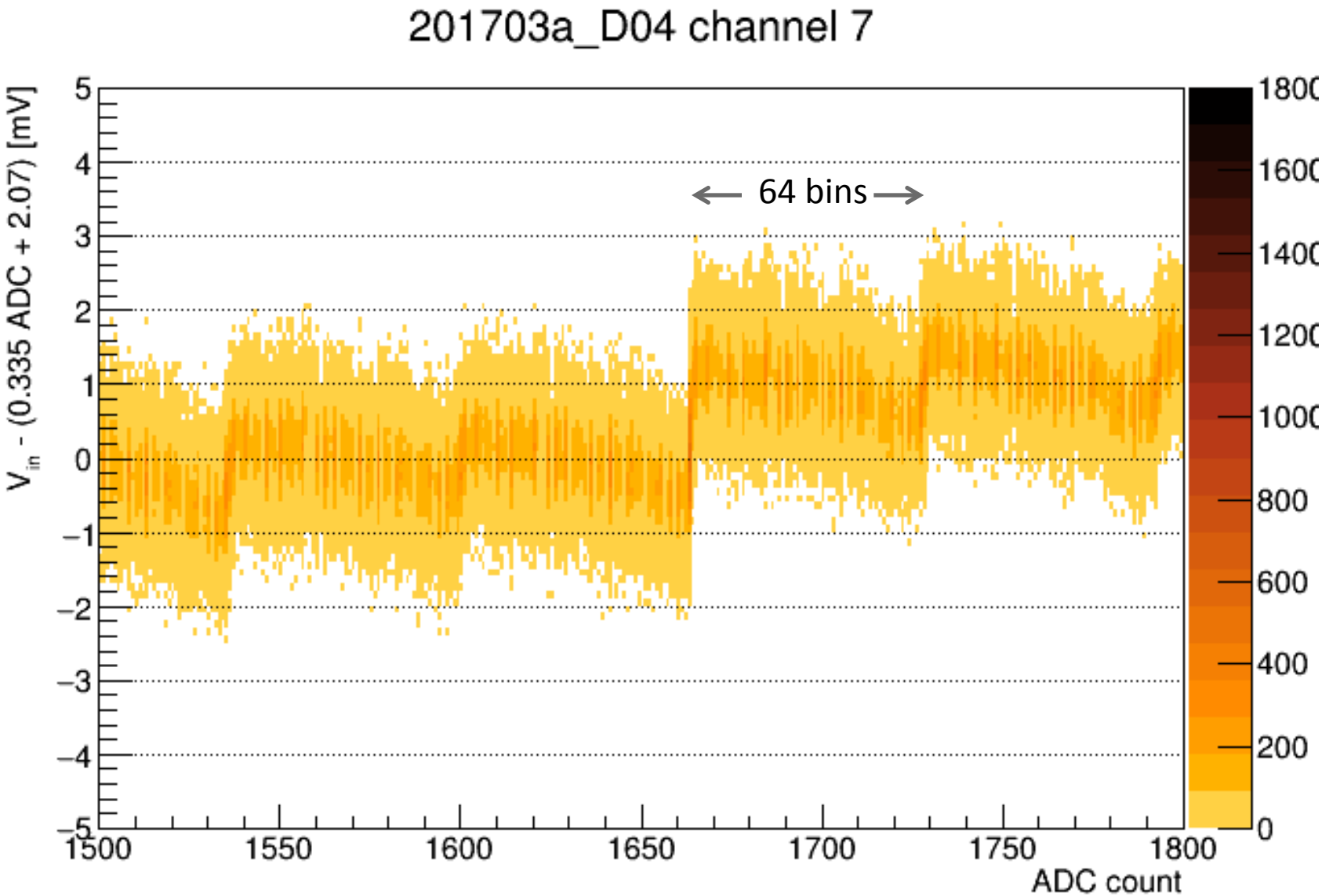
Inverse response



Linear fit residual



Linear fit residual zoomed



Data analysis 2: calibration and resolution

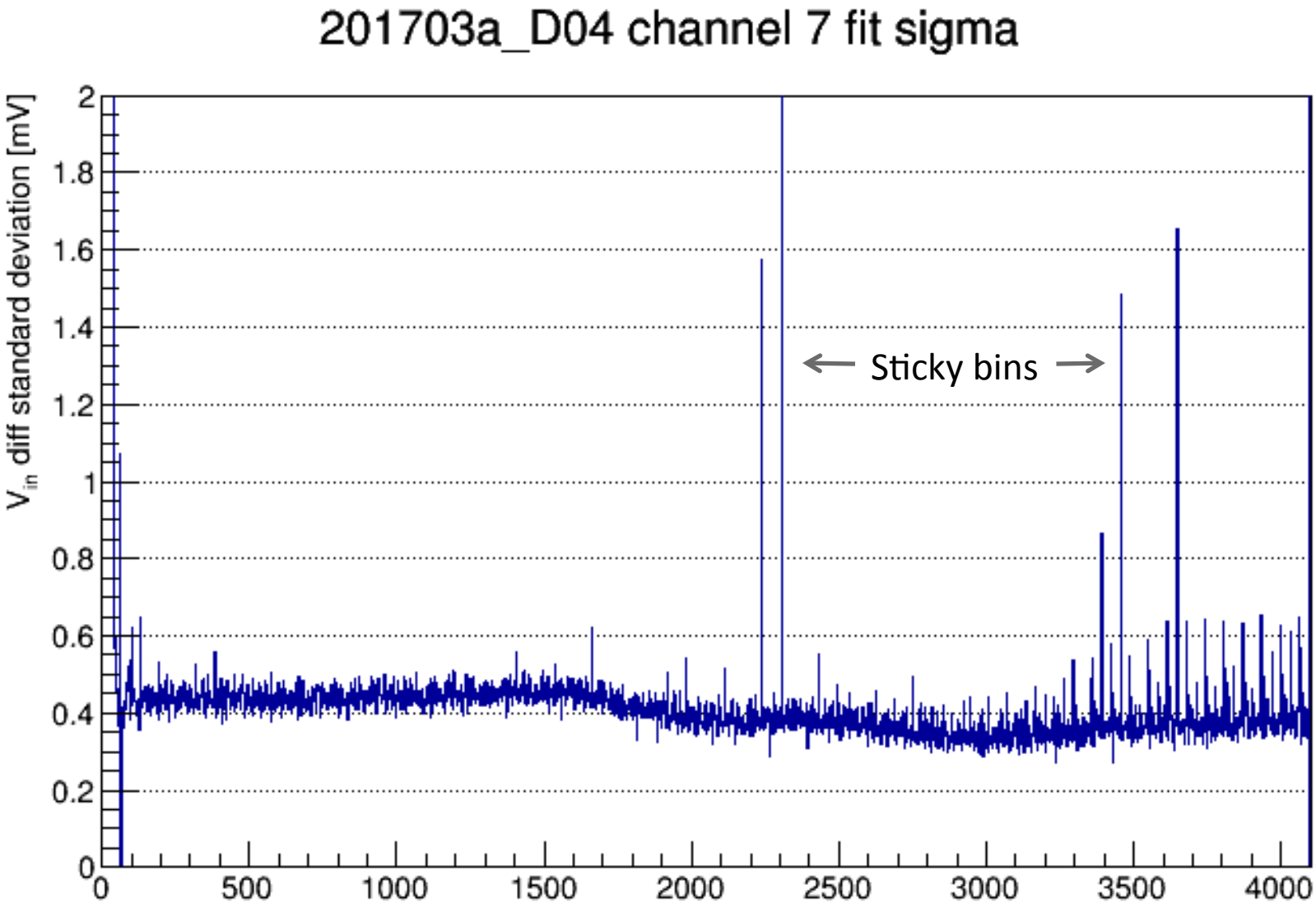
From fit and residual, define ultimate calibration for each bin

- Mean of the residual plus the linear fit is the calibrated value
- I.e. a lookup table for each channel with approximately 4000 entries
- May not be final calibration strategy but this is the best we can do

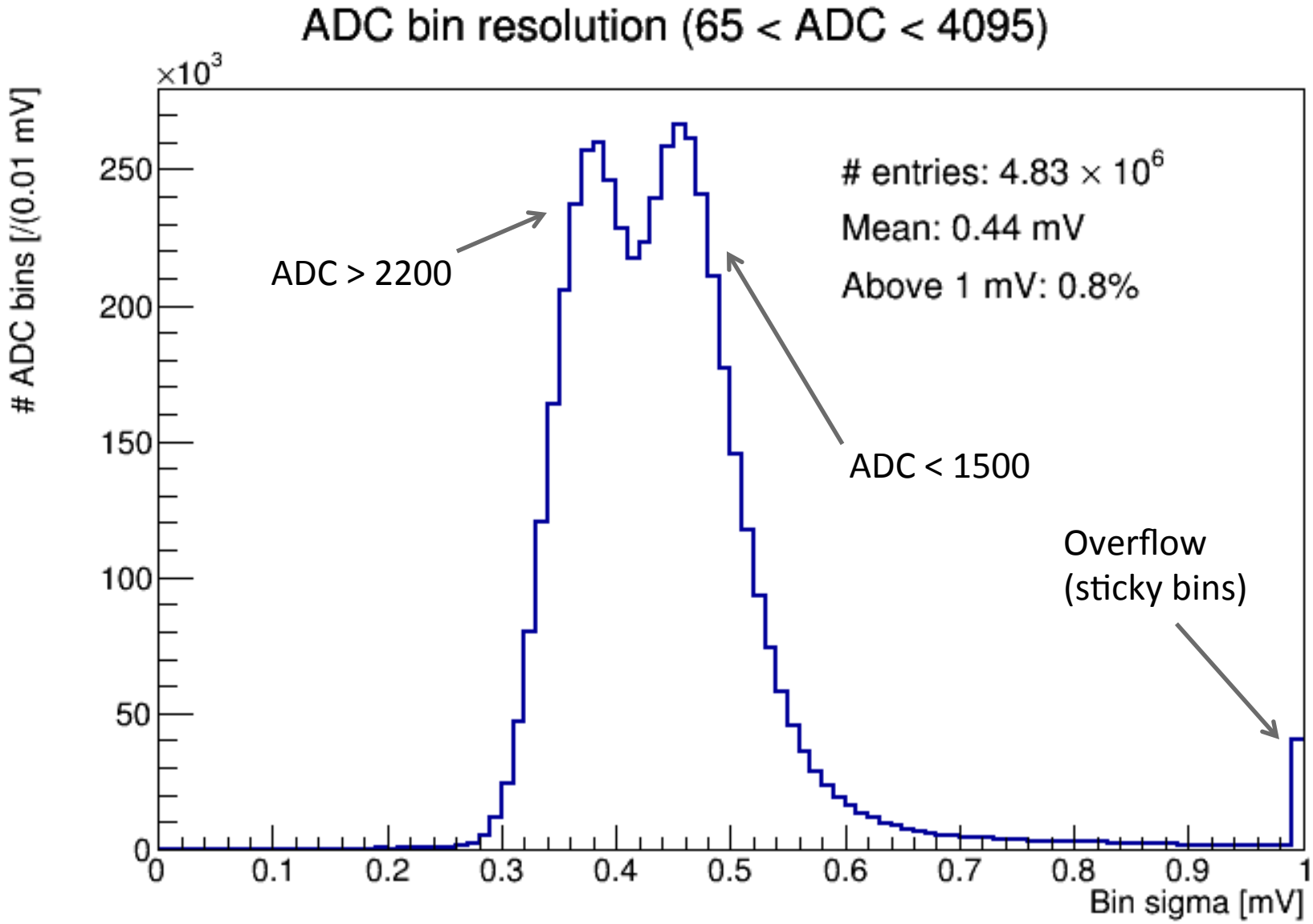
Ultimate resolution

- The spread in V_{in} provides a measure of the uncertainty in the voltage measurement for each bin
- Characterize this with the standard deviation, the RMS from the mean
- Typical example follows (again a "good" channel)
- Typically this is around 0.5 mV
  - Naïve expectation for perfect 12-bit ADC is 0.1 mV
- Following page shows the distribution for all chips

Ultimate resolution for one channel



Ultimate resolution for all chips



Data analysis 3: sticky bins

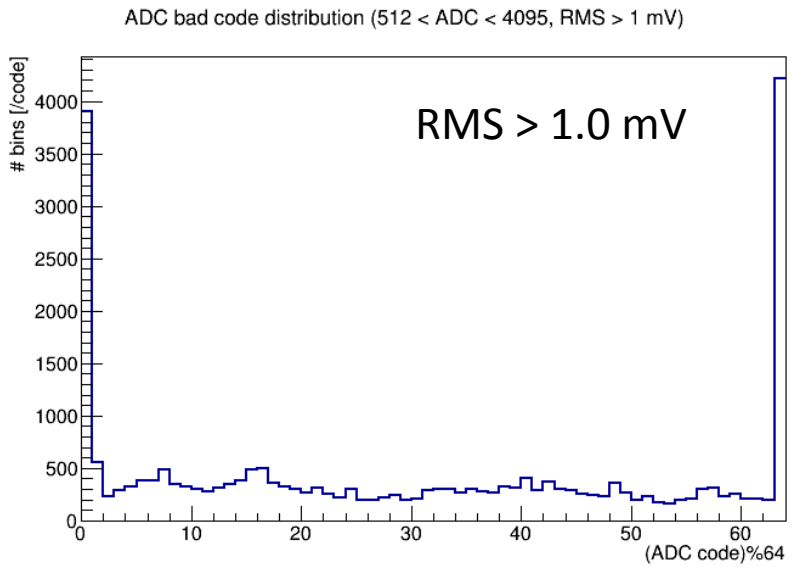
Sticky bins

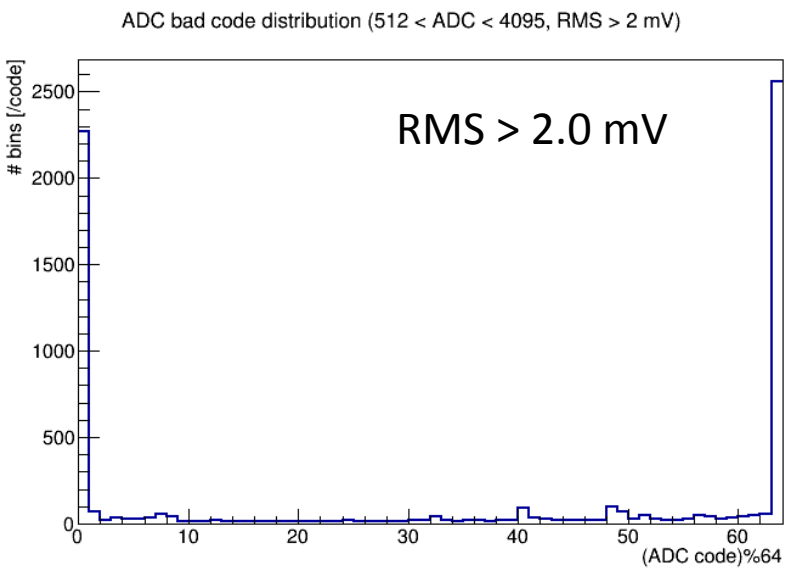
- There are always a few (sometimes many) bins populated by a wide range of input voltage
  - Can be identified by poor resolution i.e. large RMS
  - Often bins where LSB6 (lower six bits) are all 0 or all 1
  - Often a double peak where one peak is in the expected place
- Distribution for March 2017 data shown on following slide
  - 25 chips ➔ 400 channels ➔ 1.6M bins
- When resolution for a bin is too large, we can get better precision by discarding that measurement and interpolating between neighboring bins
- Plan to maintain a list of sticky bins for each channel so we know which bins to discard
  - Use the resolution (RMS from mean) to identify sticky bins
  - Here define sticky as RMS > 1.0 mV
    - This is equivalent to an input noise of 450 e for preamp gain 14 mV/fC

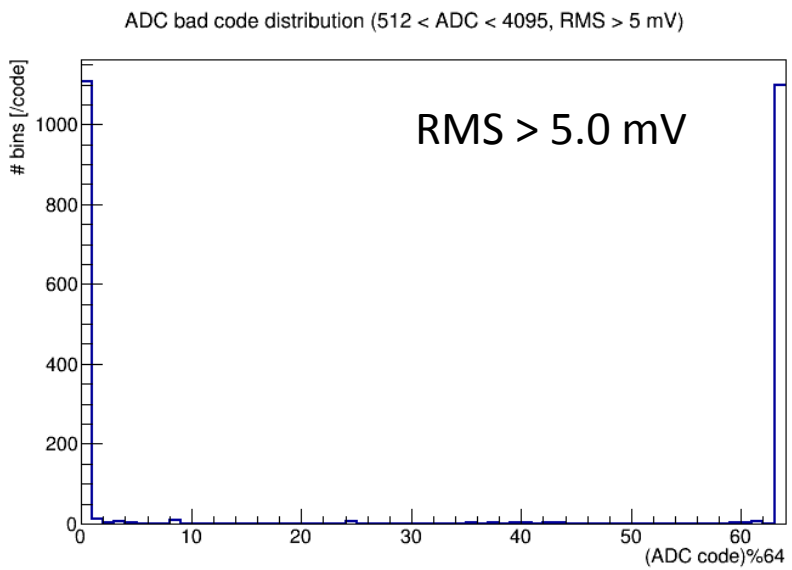
Sticky bins: LSB6 distributions

Plots show LSB6 for bad bins

- LSB6 = six least significant bits
  - I.e. bin%64
- For different RMS thresholds
- Classic values of 0 and 63 are enhanced for all thresholds
  - Dominate for high threshold







Data analysis 4: ADC quality

Voltage response

- We evaluate ADC quality as a function of voltage
  - No ADC channel covers the full range of interest (0, 1600) mV
- Evaluate three metrics: efficiency, resolution and tails
- All evaluated as functions of V_{in} in bins of 20 mV
- Results presented in "performance summary plots" (PSPs)
  - Example plot for an ADC bin follows
  - Not the bin used in earlier example plots—instead one with issues

ADC efficiency

- Define efficiency to be fraction of samples that land in good ADC bins
  - For each range of input voltage
  - Good means RMS(V_{in} residual) < 1.0 mV
- Performance summary plots show efficiency vs. V_{in} (blue histogram)
  - Following example is the same "good" channel as in earlier plots
  - Plots for all 76 chips in appendix

Data analysis 4: ADC quality (2)

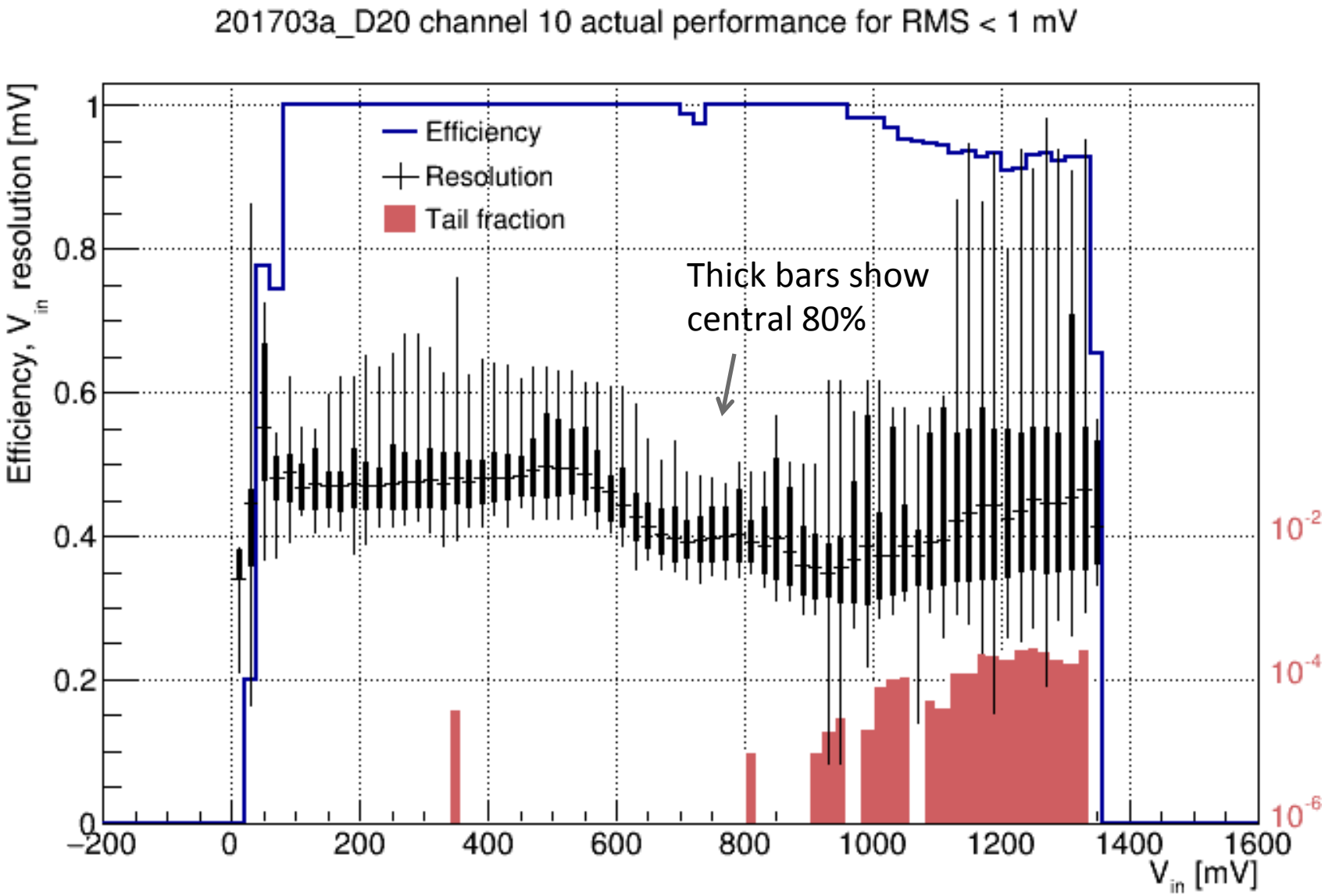
Resolution

- Resolution vs. V_{in} is shown on the same plot (black markers)
  - Evaluated as the RMS difference between the measured and true V_{in} for each sample in the voltage bin
    - Measured V_{in} is obtained by applying the calibration to the ADC count
  - Horizontal bars indicate the mean of this RMS for each bin
  - Error bars show the extent of the distribution of assigned uncertainties
    - Using all ADC bins populated by the samples in the voltage bin
    - Full range (earlier plots only showed central 80%)
    - Assigned uncertainty for and ADC bin is RMS(V_{in} residual)

Tail fraction

- The tail fraction is also shown (filled red histogram)
  - Fraction of samples in the voltage bin less than 5 mV from the true V_{in}
    - Previously used 5σ to define tail but this seems too tight
    - Because uncertainty at input to ADC is 1.3 mV
      - » 600 e with a gain of 14 mV/fC

Example performance summary plot

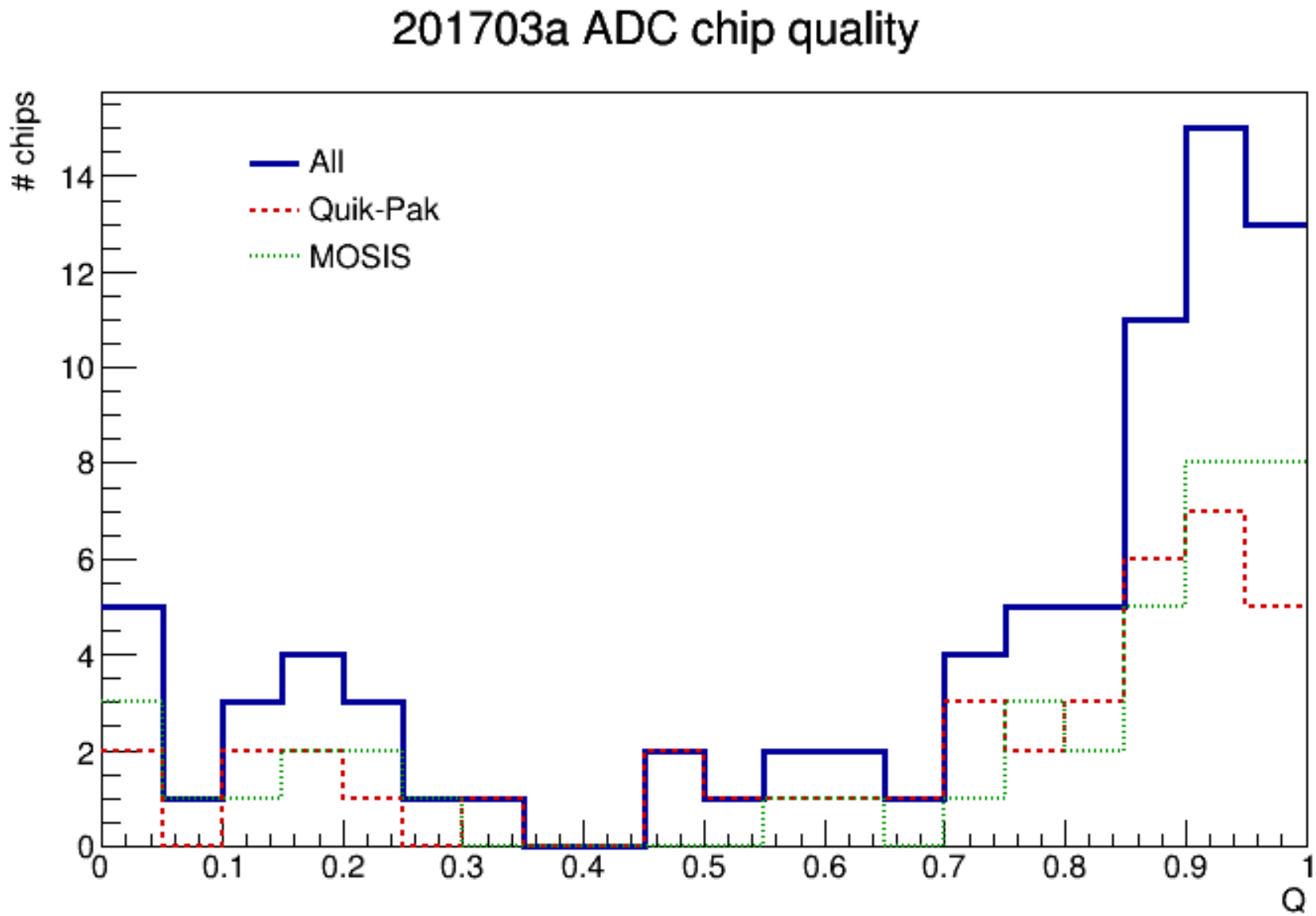


Ranking chips

We would like to rank the ADC chips

- Choose the best/acceptable ones for use in protoDUNE
- Desired yield is around 1/3 or 27 of the 78 candidate chips
  - Two failed warm test, one put in FEMB w/o cold testing
- I start from the performance plots and define a metric
- Keep things simple for now:
  - Channel metric is the average efficiency for V_{in} in (200, 1200) mV
    - Like greater voltage range but many channels don't have it
  - Chip metric Q is the product of these efficiencies for all 16 channels
- This metric and the rank (1 is the best chip) are included on the plots
  - Distribution shown on following page
- May want to change quality criteria
  - Account for core resolution, tails or remaining voltage range
  - But current definition seems roughly OK by eye
  - Open to suggestions
  - Easy to add subclasses with alternatives

Ranking chips: Quality distribution



Results

Performance plots are in appendix

- For all 76 ADC chips
- Readout at 2 MHz with external clock
- Chips are grouped and ordered by quality Q (see previous page)
  - Categories based on thresholds on this variable
    - good ($Q > 0.95$) - are mostly OK
    - fair ($0.85 < Q < 0.95$) - show some problems but some must be used
    - poor ($0.70 < Q < 0.85$) - more problems; prefer not to use these
    - bad ($Q < 0.70$) - typically have one or more very bad channels
  - Need to keep good and many of fair to get the desired yield
    - $Q > 0.90$ gives desired yield (28/78)

Residual plots are also in appendix

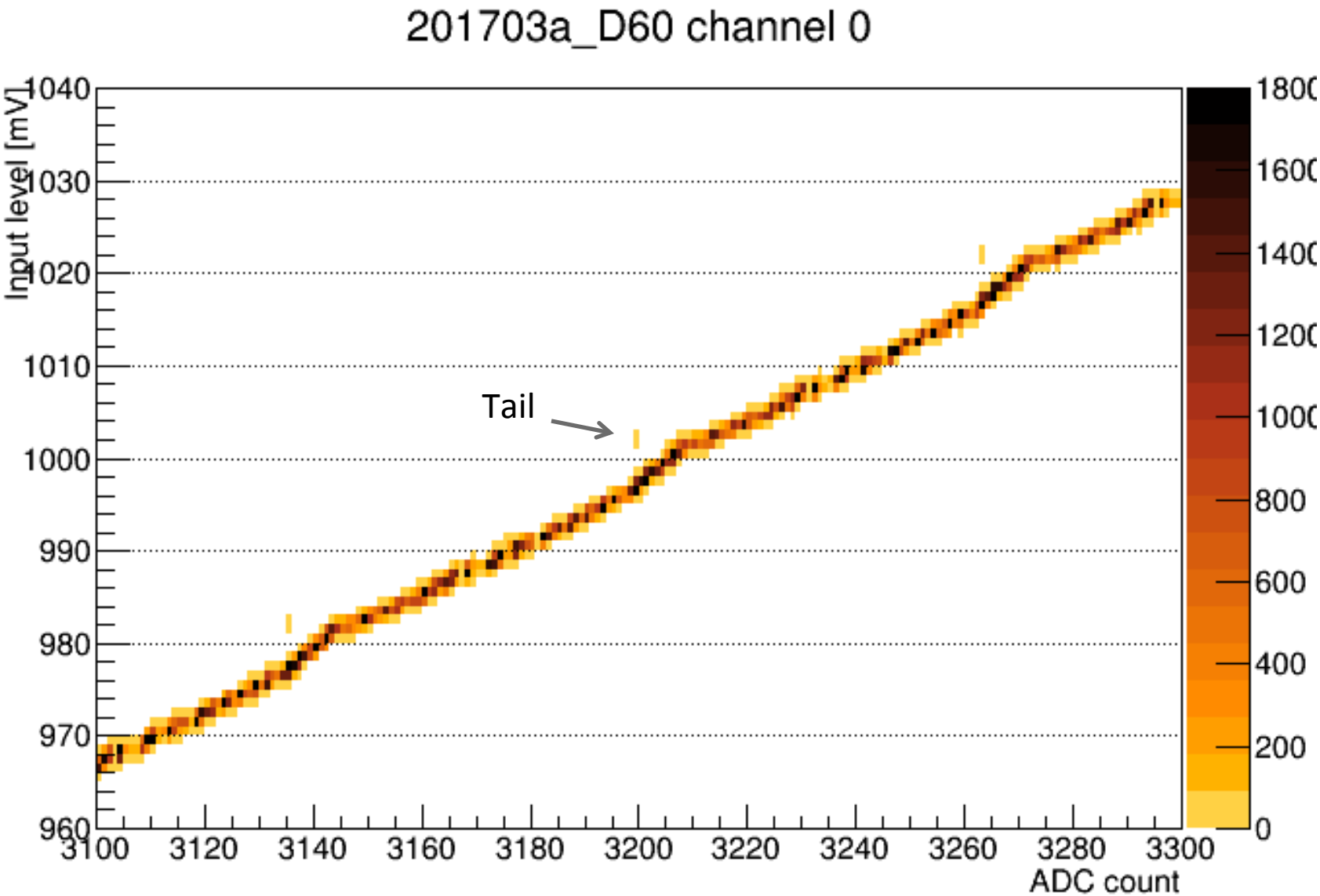
- Residual from linear fit—shows non-linearity
- Same grouping

Tails

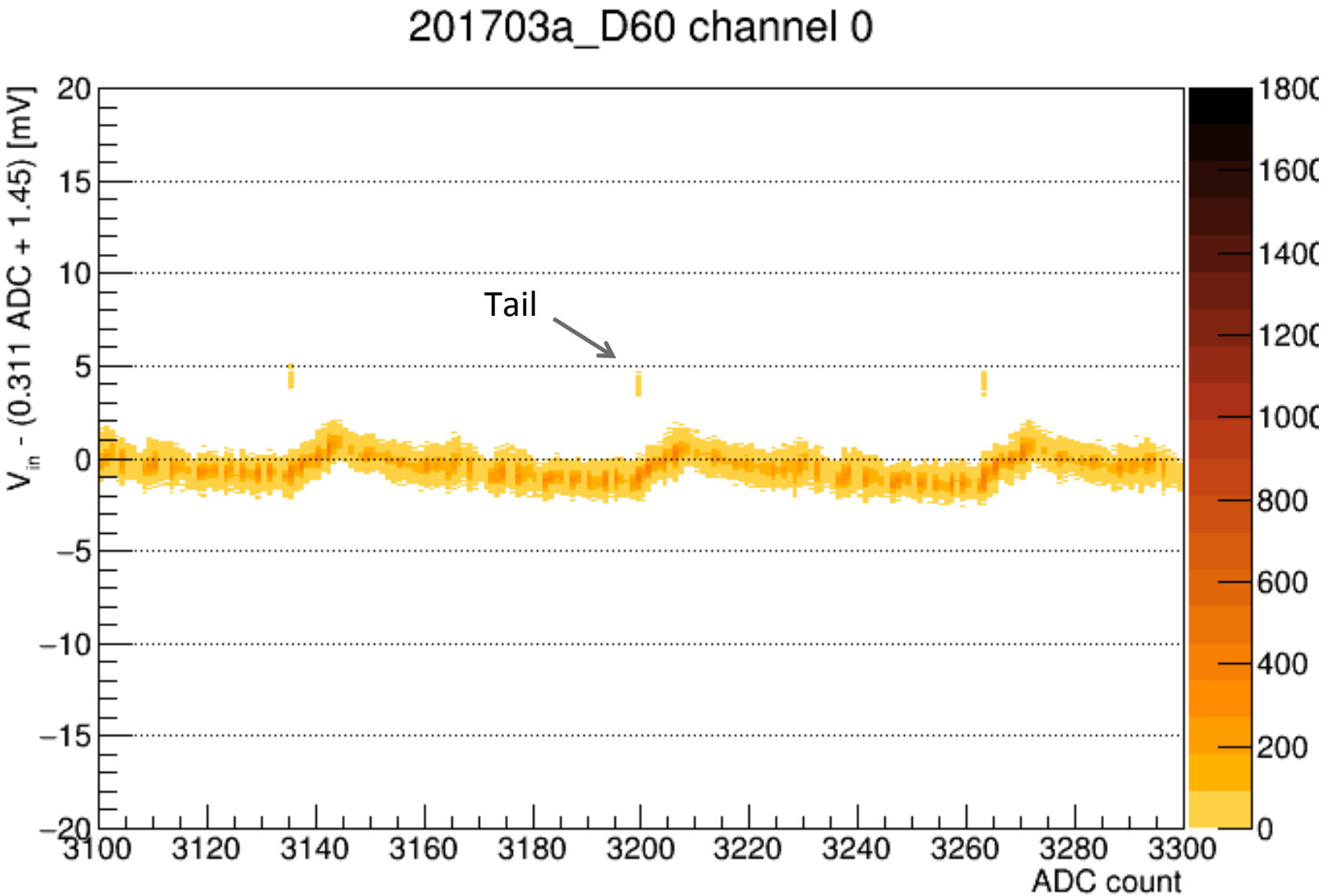
We now define tail to be fraction beyond 5 mV

- Still see some tails though much less than definition using 5σ
- Maximum allowed ADC bin uncertainty is 1.0 mV
  - For Gaussian, the tail fraction is < 10^{-6} at this value
- Presumably still large here because distribution has two distinct peaks many mV apart with most samples in one of the peaks
  - If peaks have similar population, the tail fraction is small but σ is large
  - Following pages show an example: bin 3199 in chip 60 channel 0
    - This chip was ranked #1 using efficiency product metric

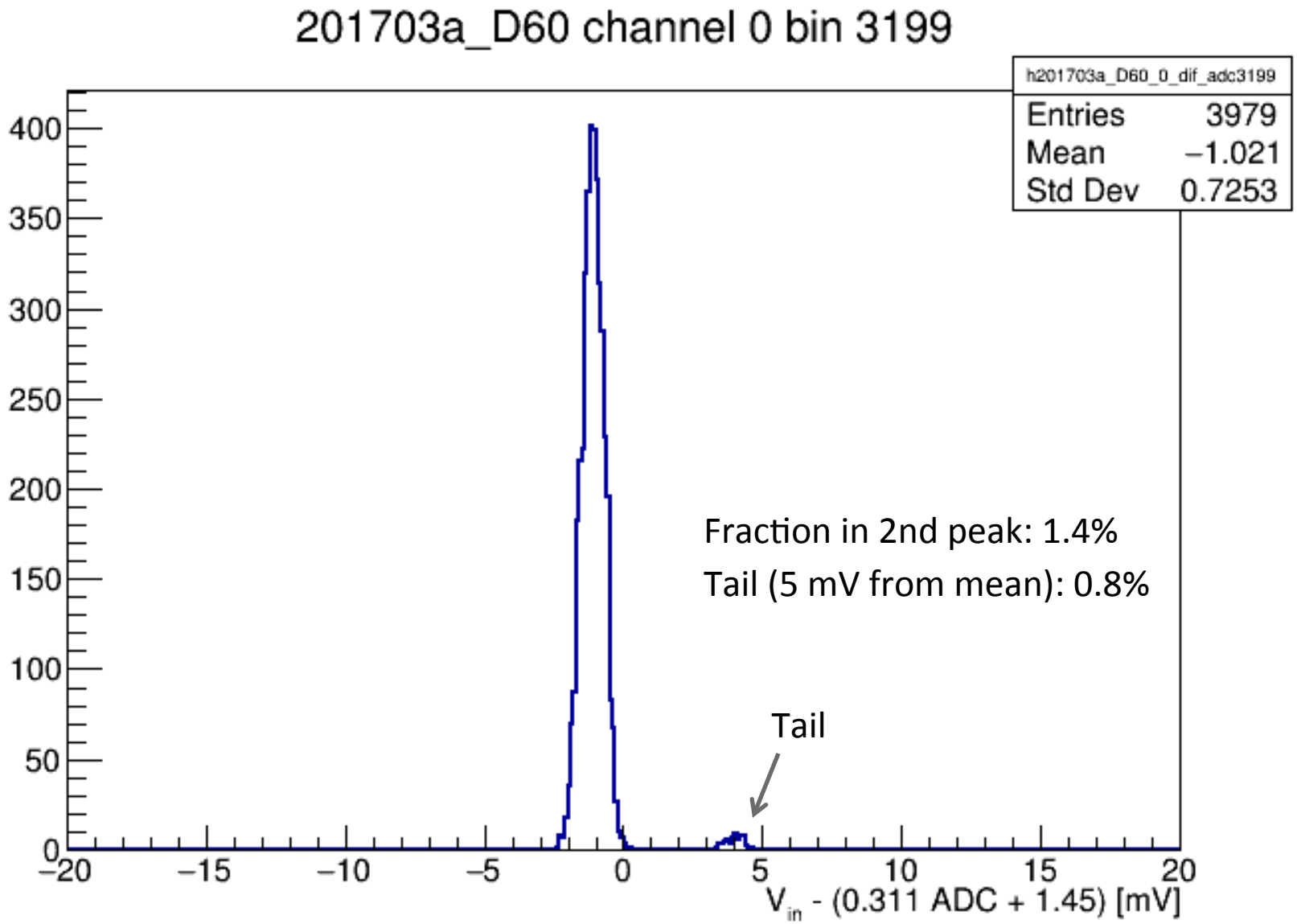
Tails: chip D6 channel 0 response



Tails: chip D6 channel 0 residual



Tails: chip D6 channel 0 bin 3199 residual



Tails: Comments

Declare bins bad if tail fraction is above some threshold?

- Could have different thresholds for multiple tail definitions
  - E.g. bin is bad if
    - any samples are 10 mV from mean or
    - 1% are 5 mV from mean

Include tails when assigning quality and ranking chips?

- Current metric only uses efficiency

Efficiency

Voltage bin efficiency is the fraction of samples that are good

- A sample is good if it lands in an ADC bin with RMS(V_{in}) < 1.0 mV
  - The RMS is evaluated with a flat input distribution (linear ramp)
- Threshold set at 1 mV because nominal preamp noise is 1.2 mV
  - 1.2 mV = 600 e at gain 14 mV/fC
- Expect that bad samples will be mitigated by interpolating between neighboring time samples

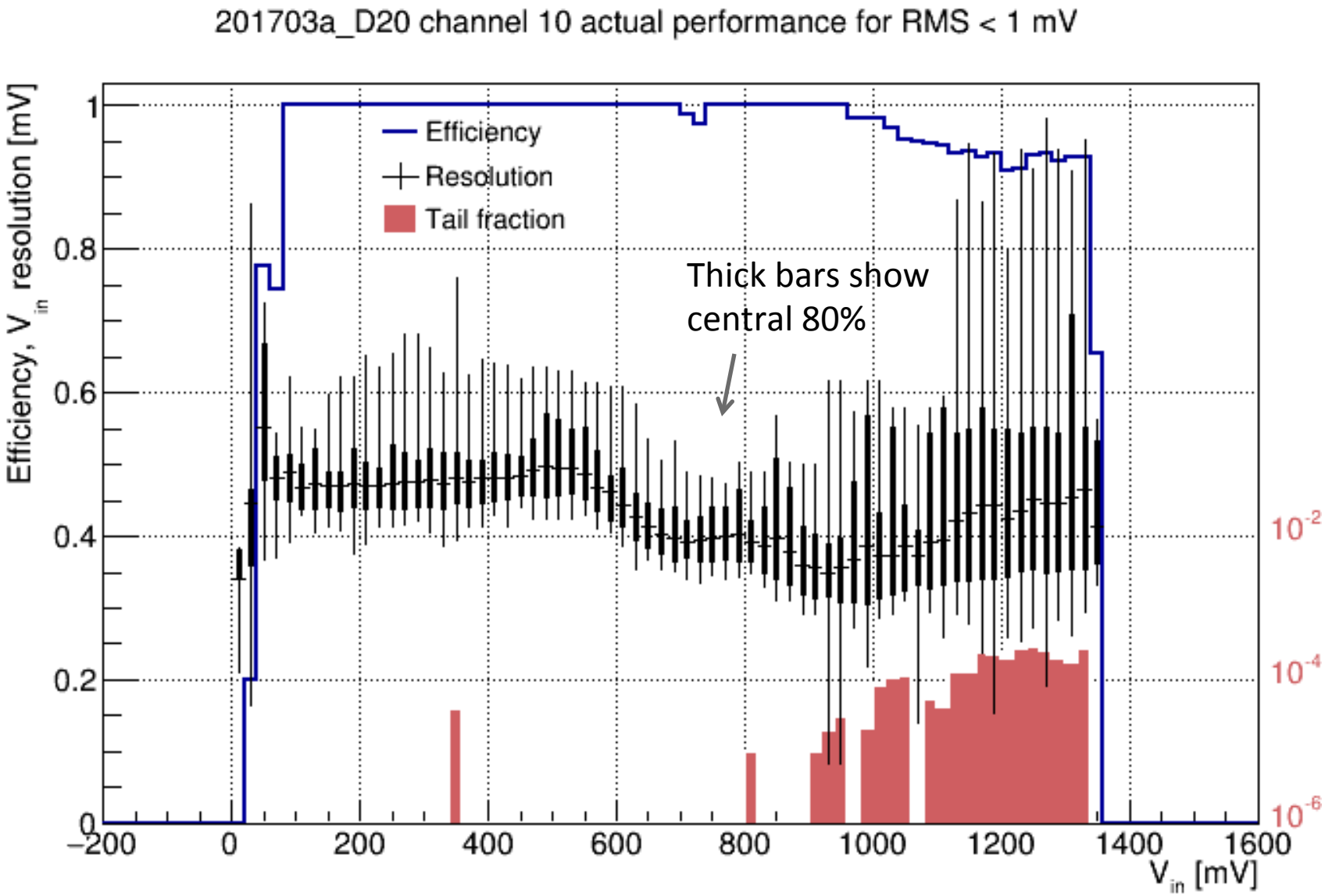
May want to consider other definitions

- Change the RMS threshold
- Flag bins as bad if they have tails

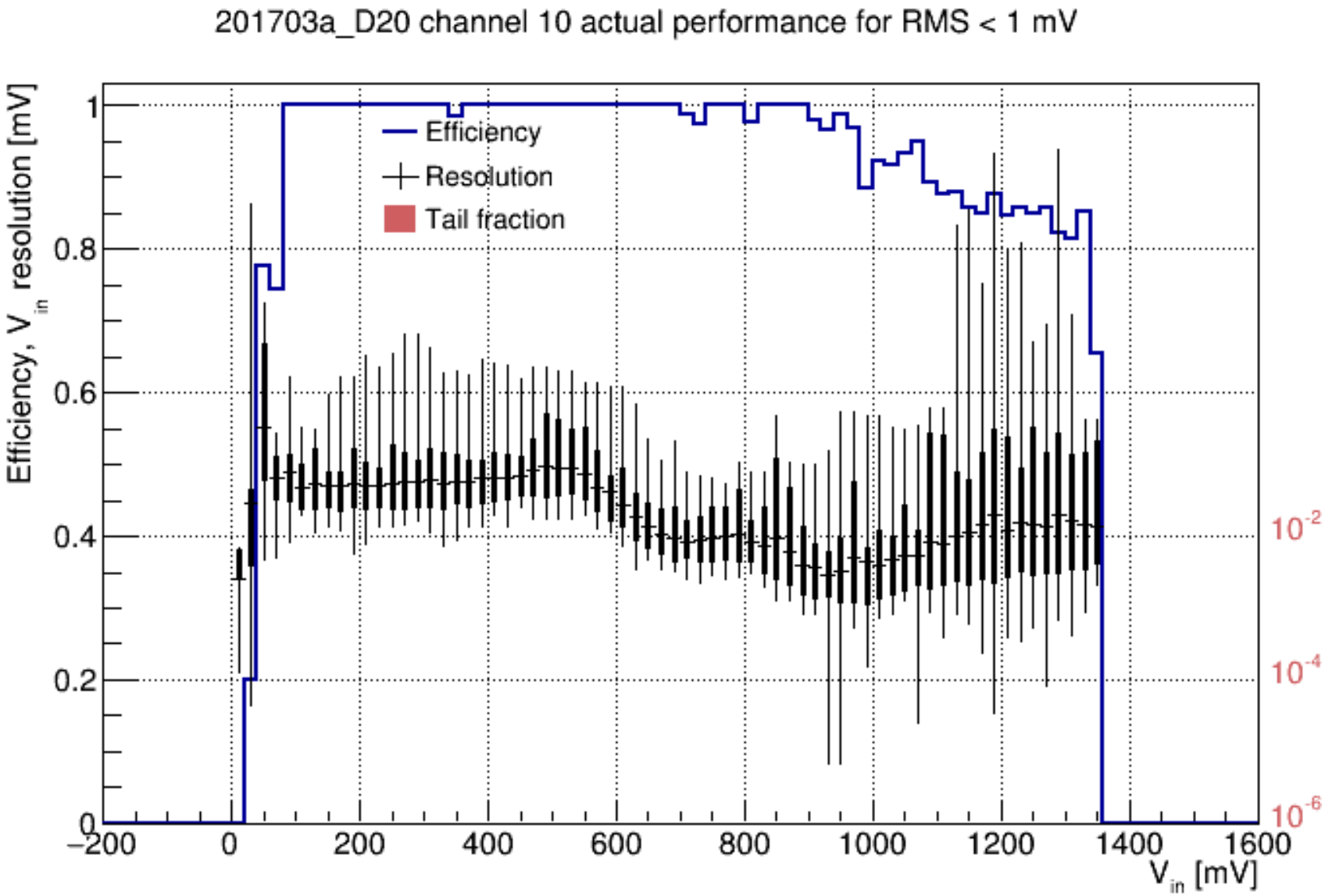
Following 4 pages show the effect of making these changes

- For a bad channel from the last accepted chip (rank = 26)
- RMS threshold at 1.0 and 2.0 mV
- Keeping and discarding bins with tails
  - Tail = any sample more than 5.0 mV from the mean

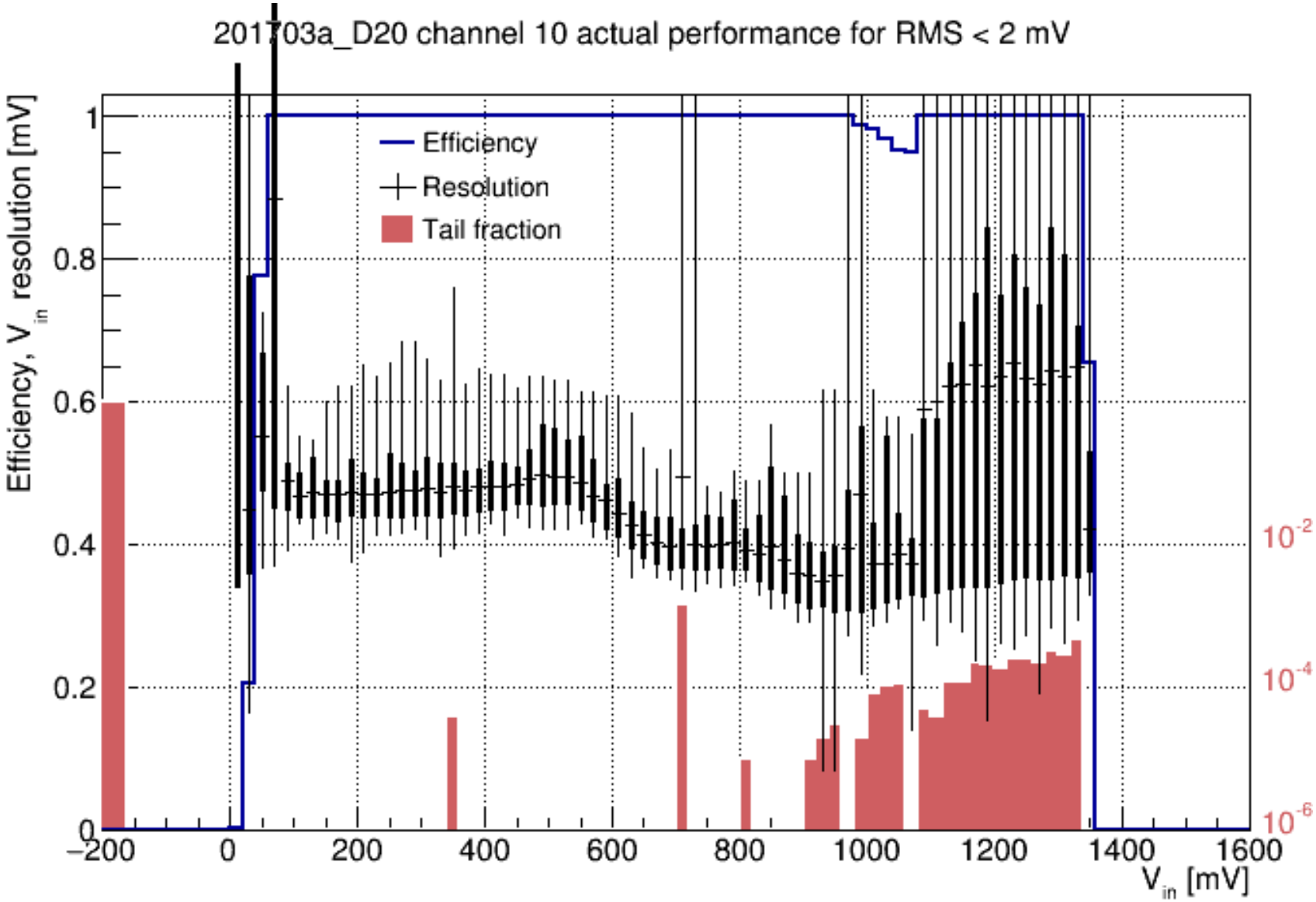
Example perf. with default cuts



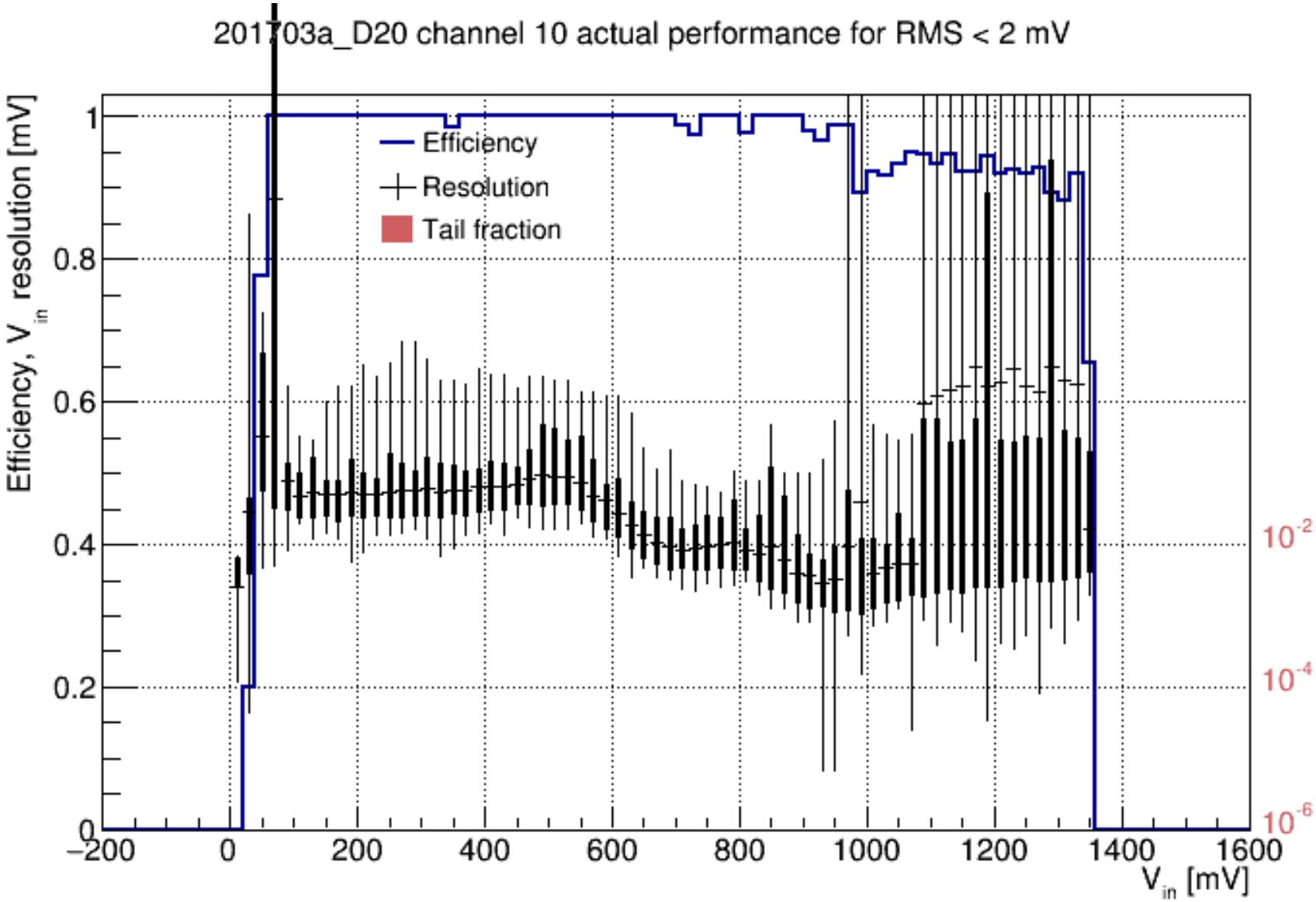
Example perf with higher excluding tails



Example perf with higher RMS threshold



Example perf with higher RMS and no tails



Selecting chips

I discussed ADC chip selection with Matt

- Schedule does not allow the luxury of testing all chips and then selecting the best 1/3
- He needs criterion to identify good chips as they are tested so they can then be soldered into FEMBs
- Do we want to use the definition here?
  - Q = product of channel efficiencies
  - Channel efficiency is fraction of samples in bins with RMS(V_{in}) < 1.0 mV
  - Measured over the range (0.2, 1.2) mV
  - Keep Q > 0.90

Comments/Conclusions

ADC can be used but does have issues

- Do not cover the full 0-1.6 V of preamp
  - Most channels cover (200, 1200) mV
- Some inefficiency (samples in sticky bins)
- Tails (measurements > 5 mV from true value)

Calibration

- Need channel-specific calibration of non-linearity
- Need to keep list of bad bins for each channel

New ADCs

- The performance of the new 76 ADCs is similar to the earlier 26
- Selecting the best 1/3 the worst efficiencies (0.2 < Vin < 1.2) V are
  - 0.993 for a chip and
  - 0.936 for channel

Tails

- Still have tails with new definition (measured – true > 5 mV)
- Should we flag bins bad when they have tails? ➔Lose more efficiency.

Still need to look at time dependence

Appendix

Performance plots

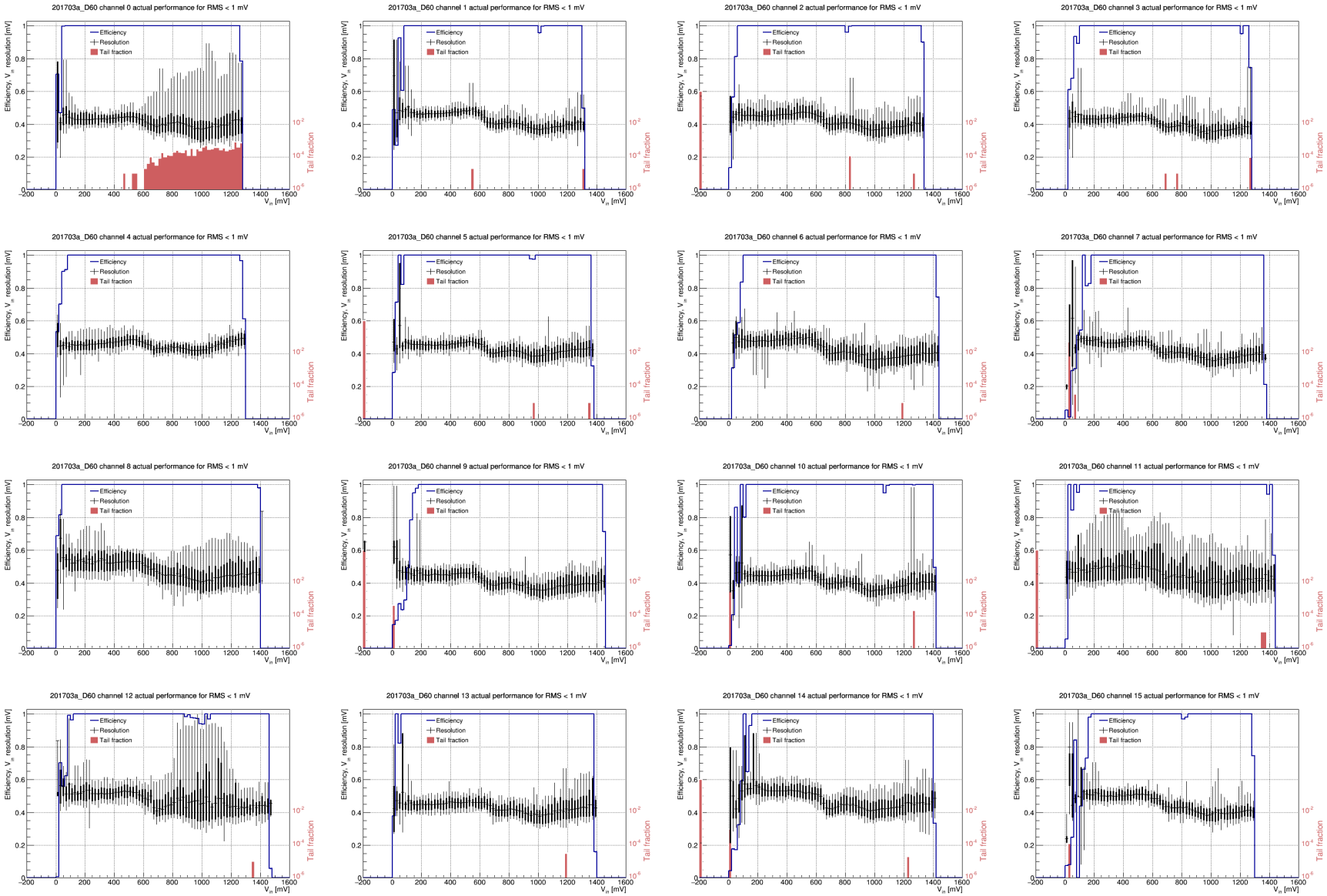
Residual plots

Note: Plot titles include

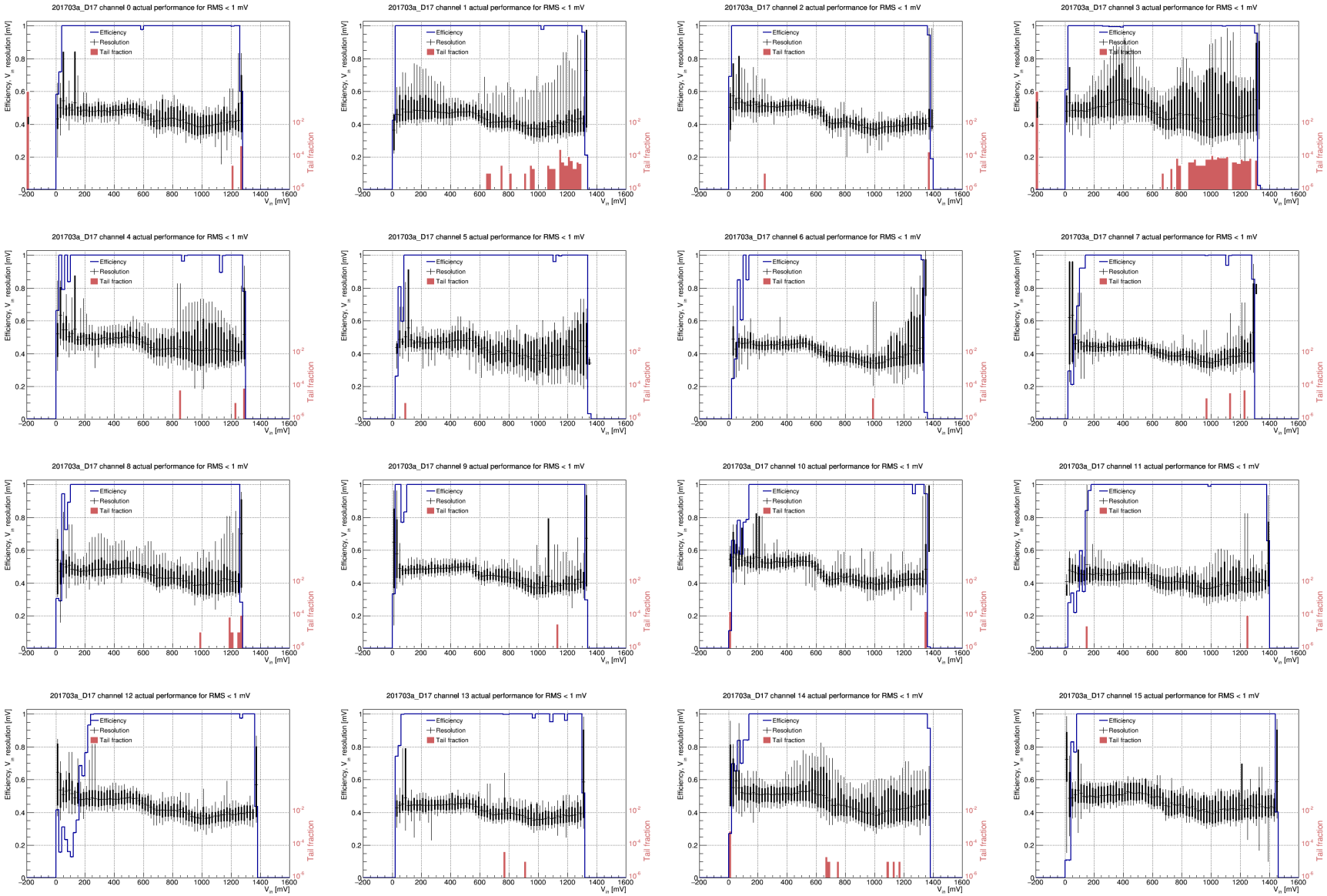
- rank – Order in quality (1 is best)
- Q – Quality metric (product of channel efficiencies)
- a – Average efficiency for the chip
- m – Lowest channel efficiency for the chip
- All evaluated for V_{in} in the range (200, 1200) mV

Good chips

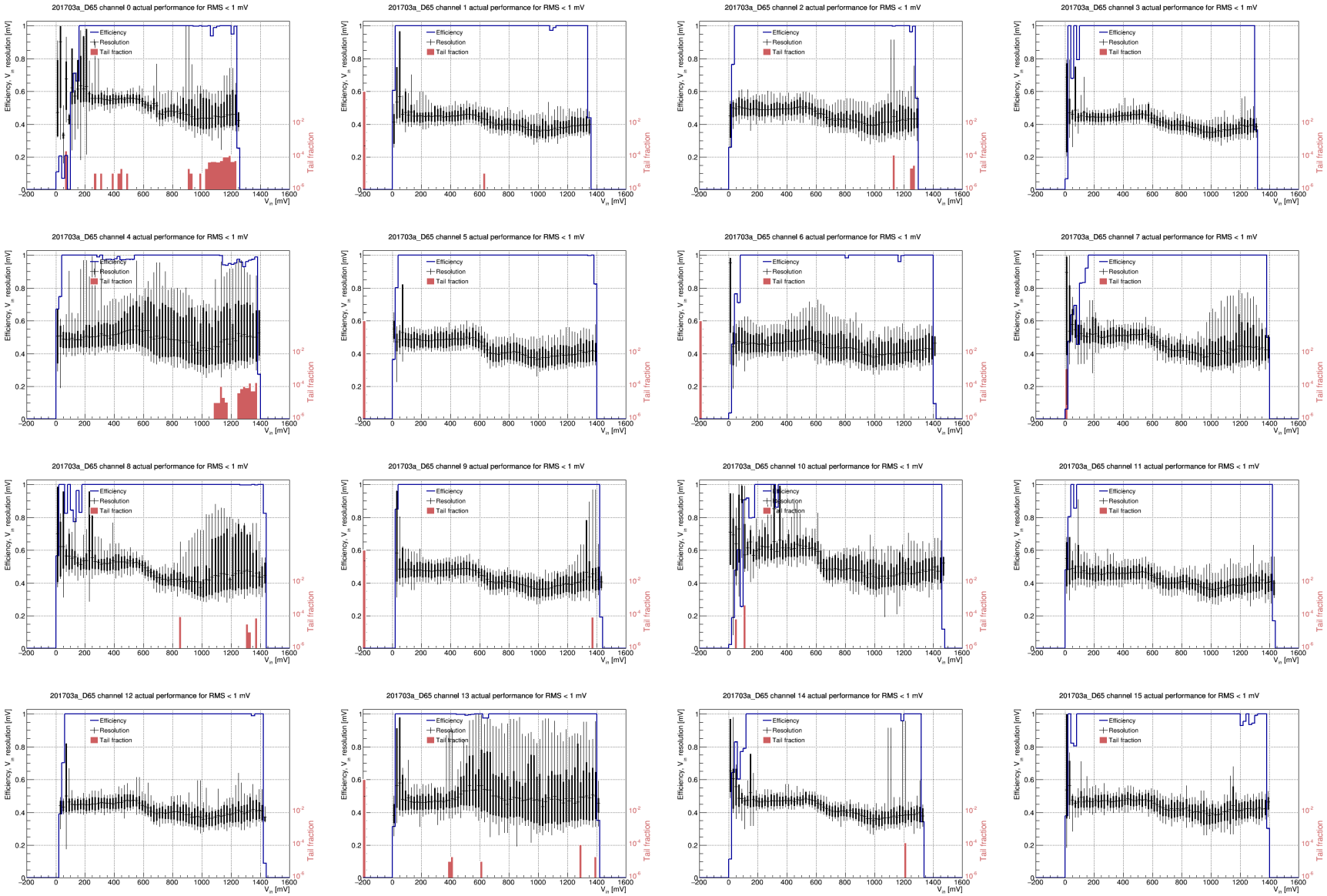
Chip D60 (rank=1, Q=0.990, a=0.999, m=0.995)



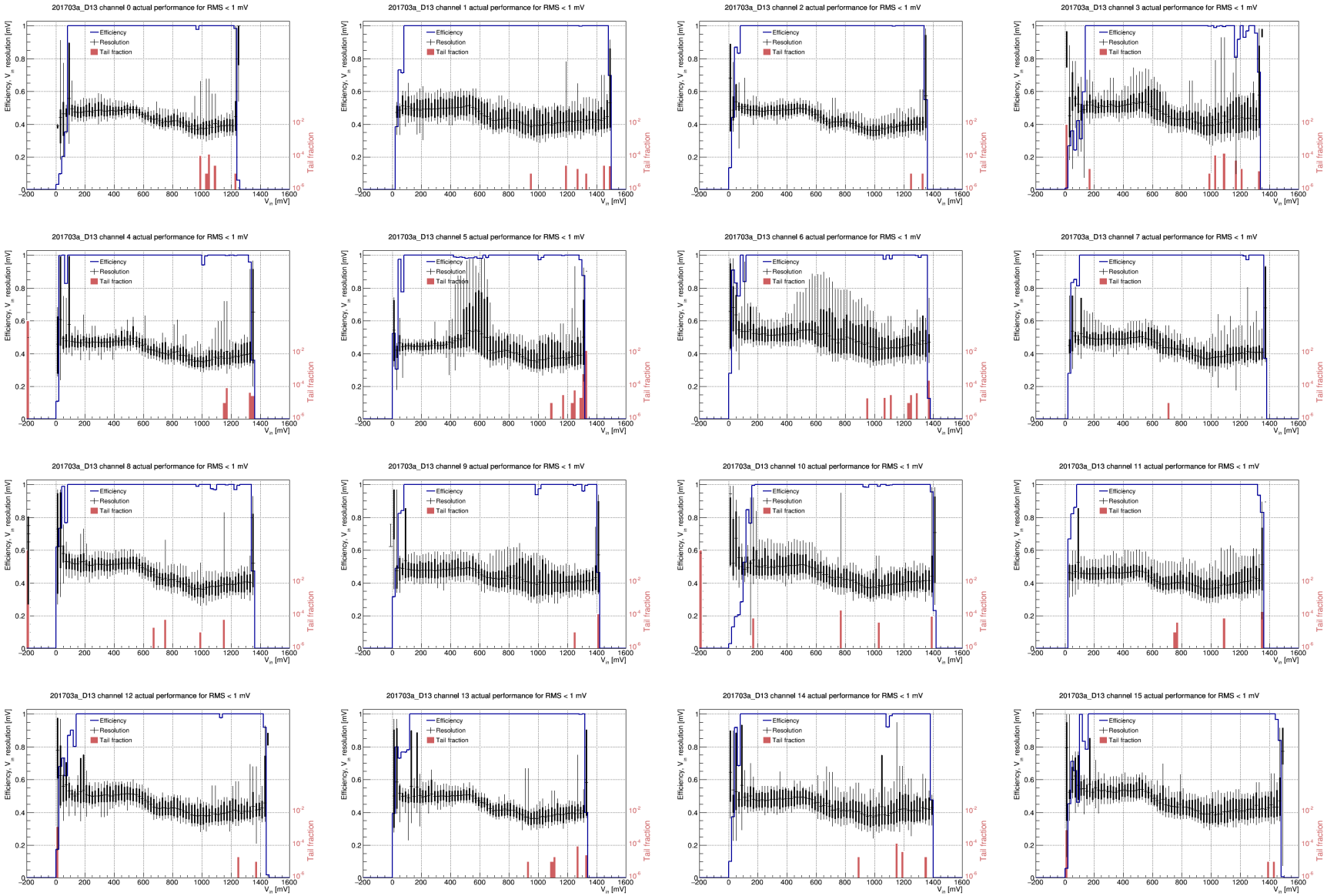
Chip D17 (rank=2, Q=0.984, a=0.999, m=0.993)



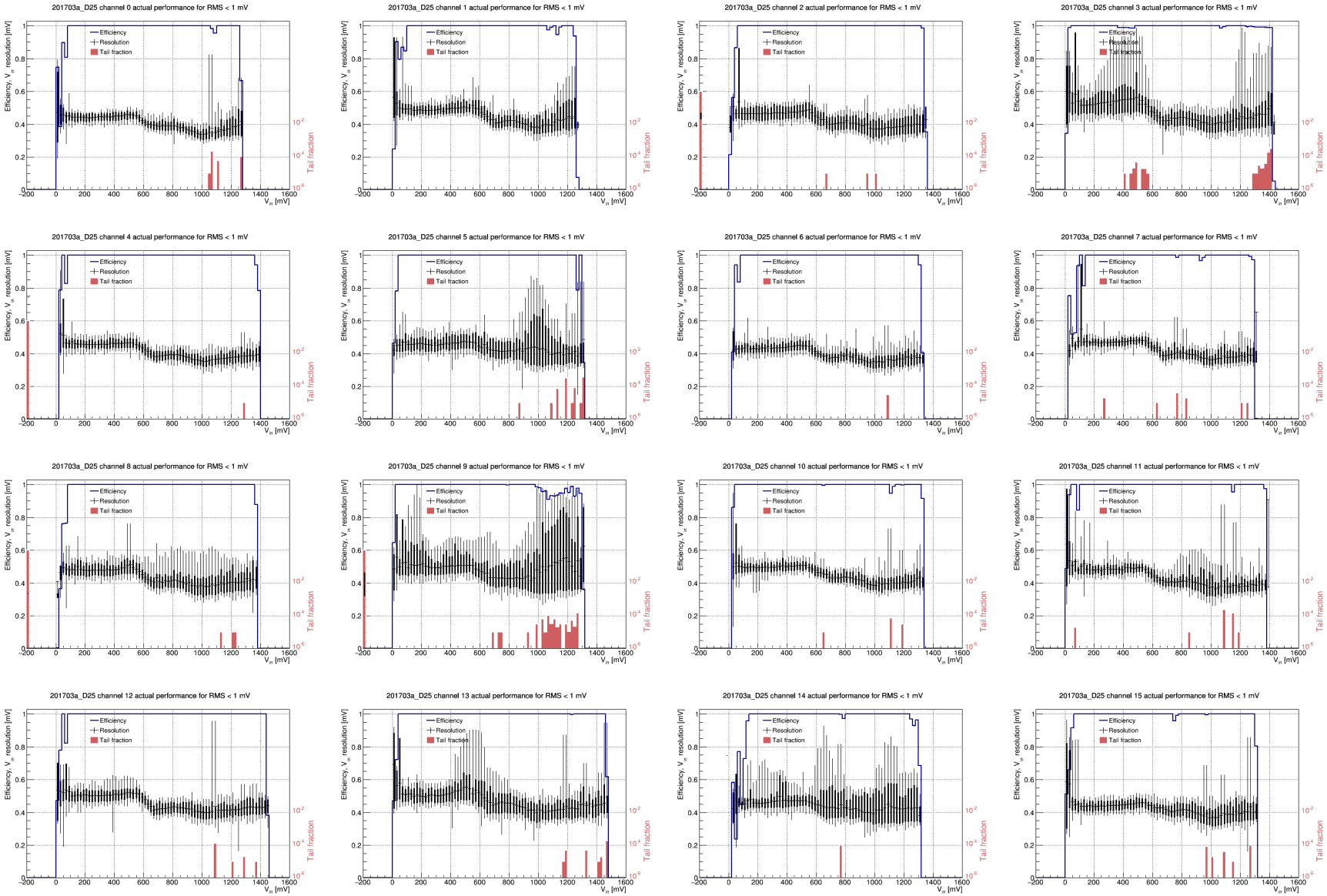
Chip D65 (rank=3, Q=0.982, a=0.998, m=0.990)



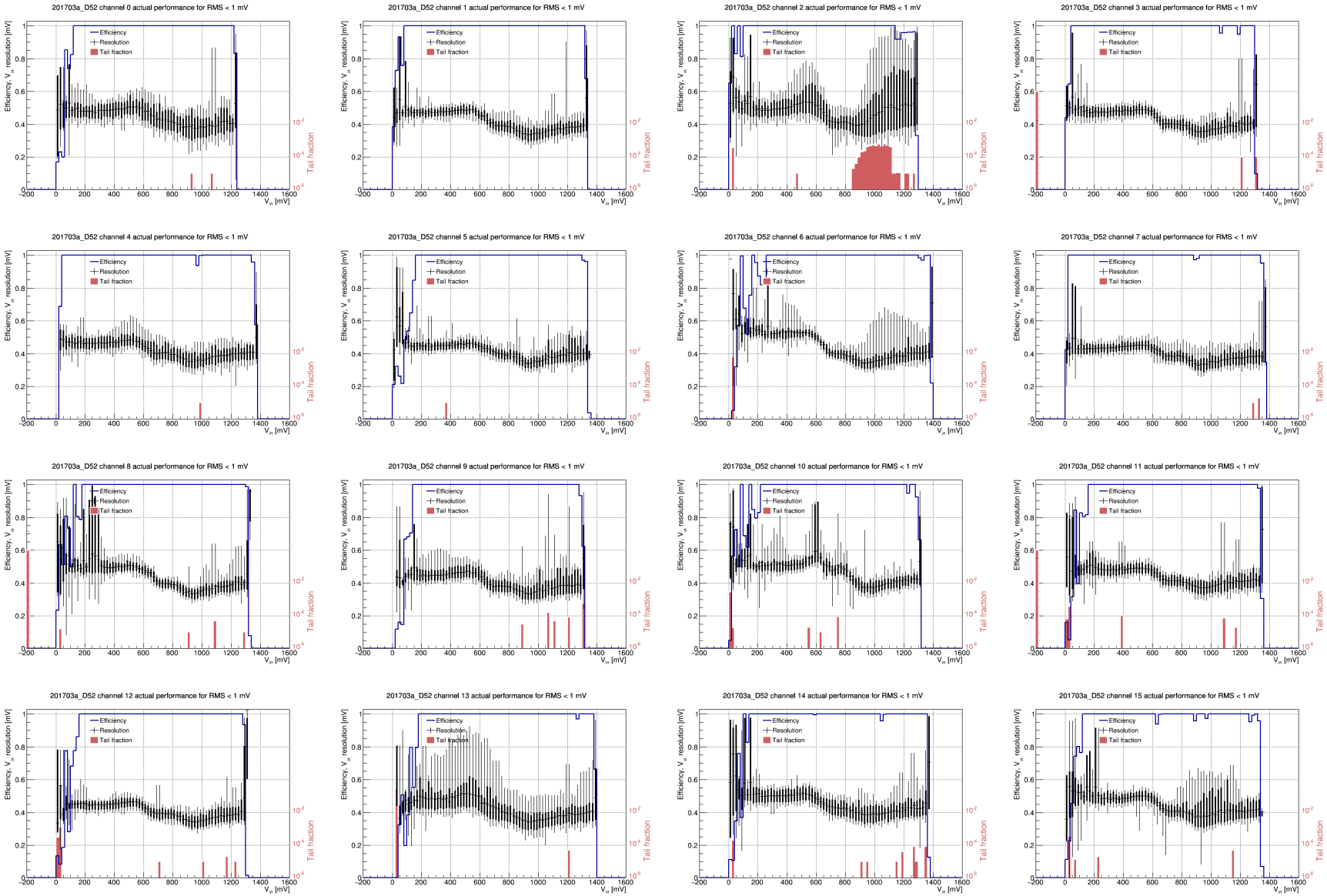
Chip D13 (rank=4, Q=0.980, a=0.998, m=0.994)



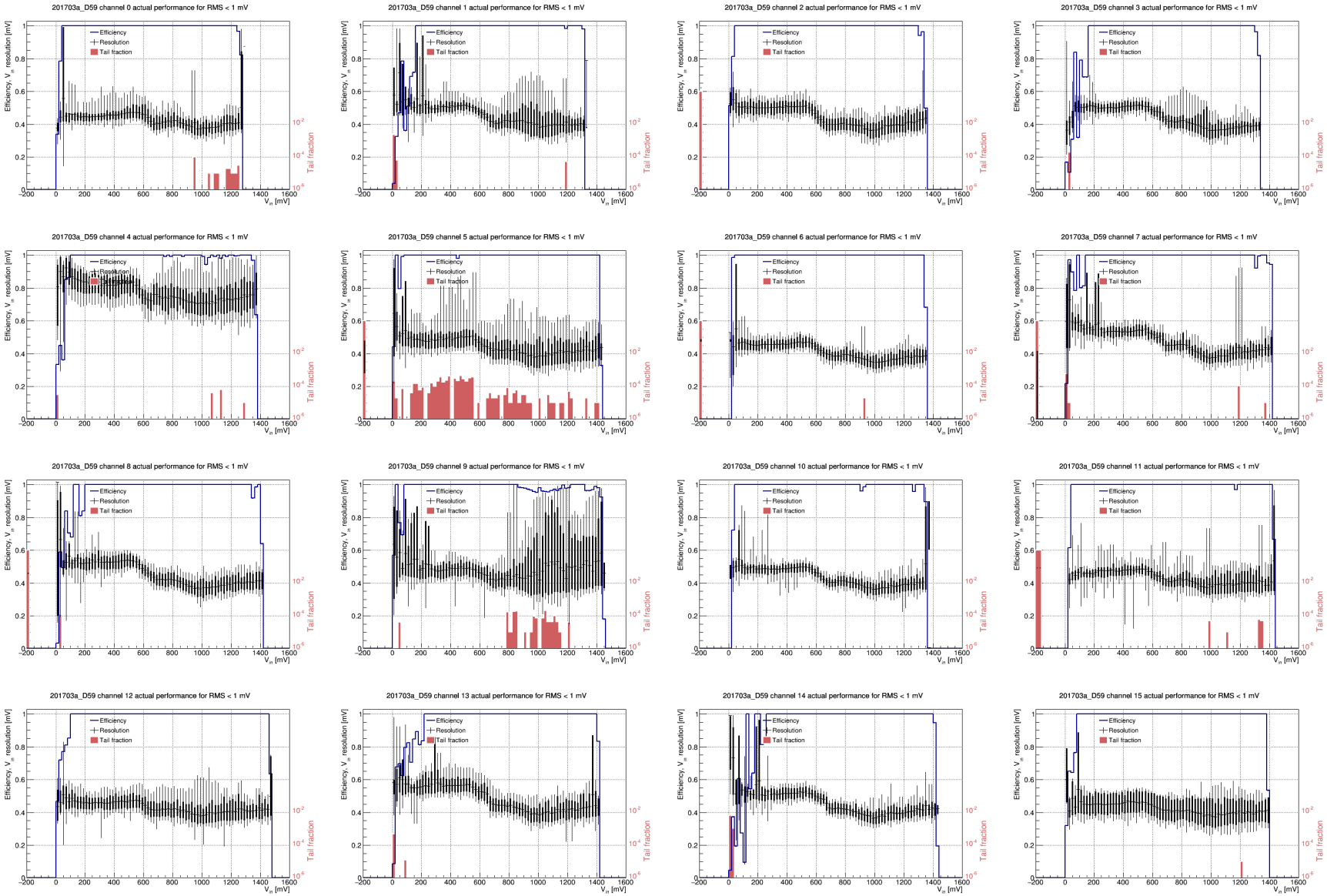
Chip D25 (rank=5, Q=0.979, a=0.998, m=0.989)



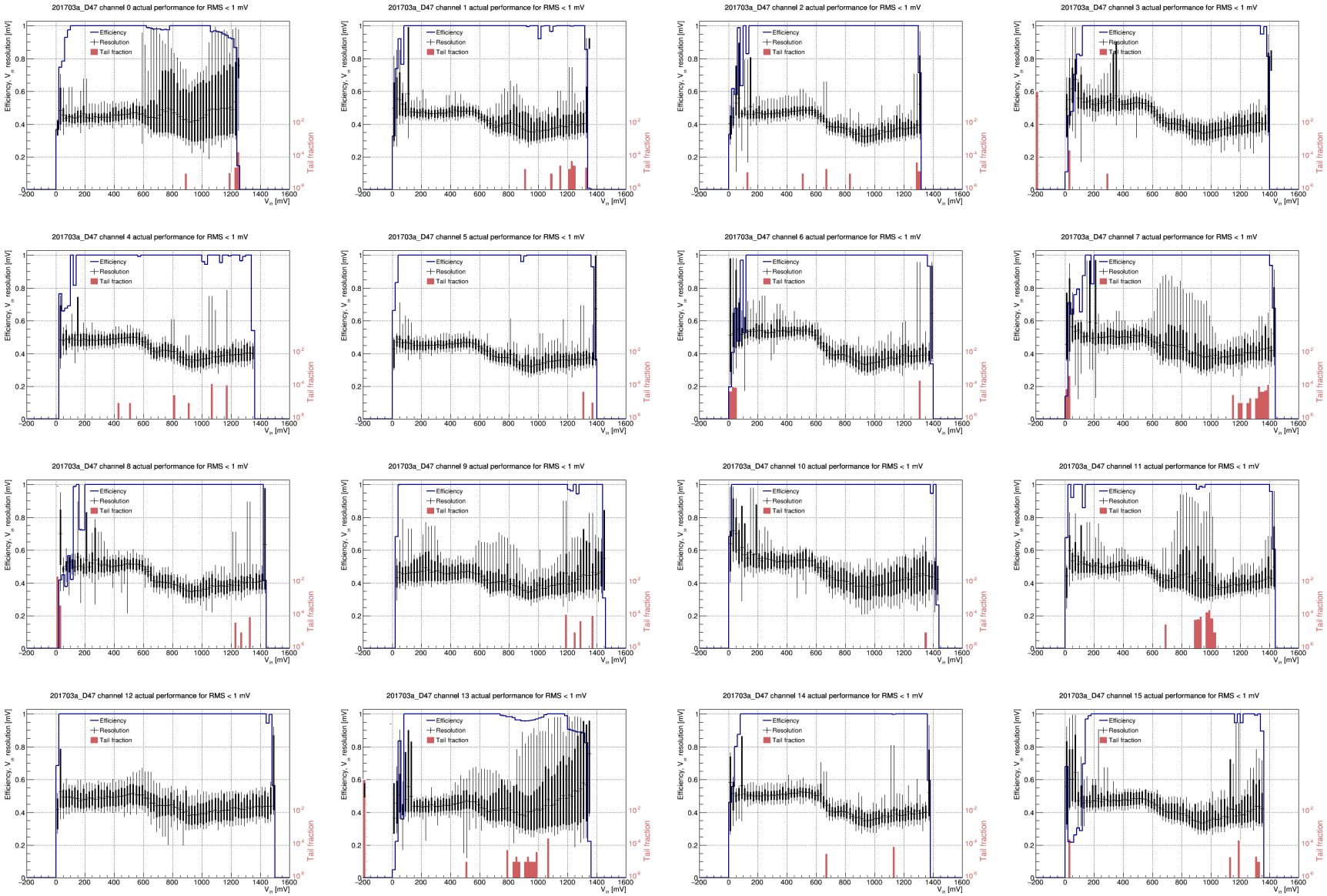
Chip D52 (rank=6, Q=0.975, a=0.998, m=0.990)



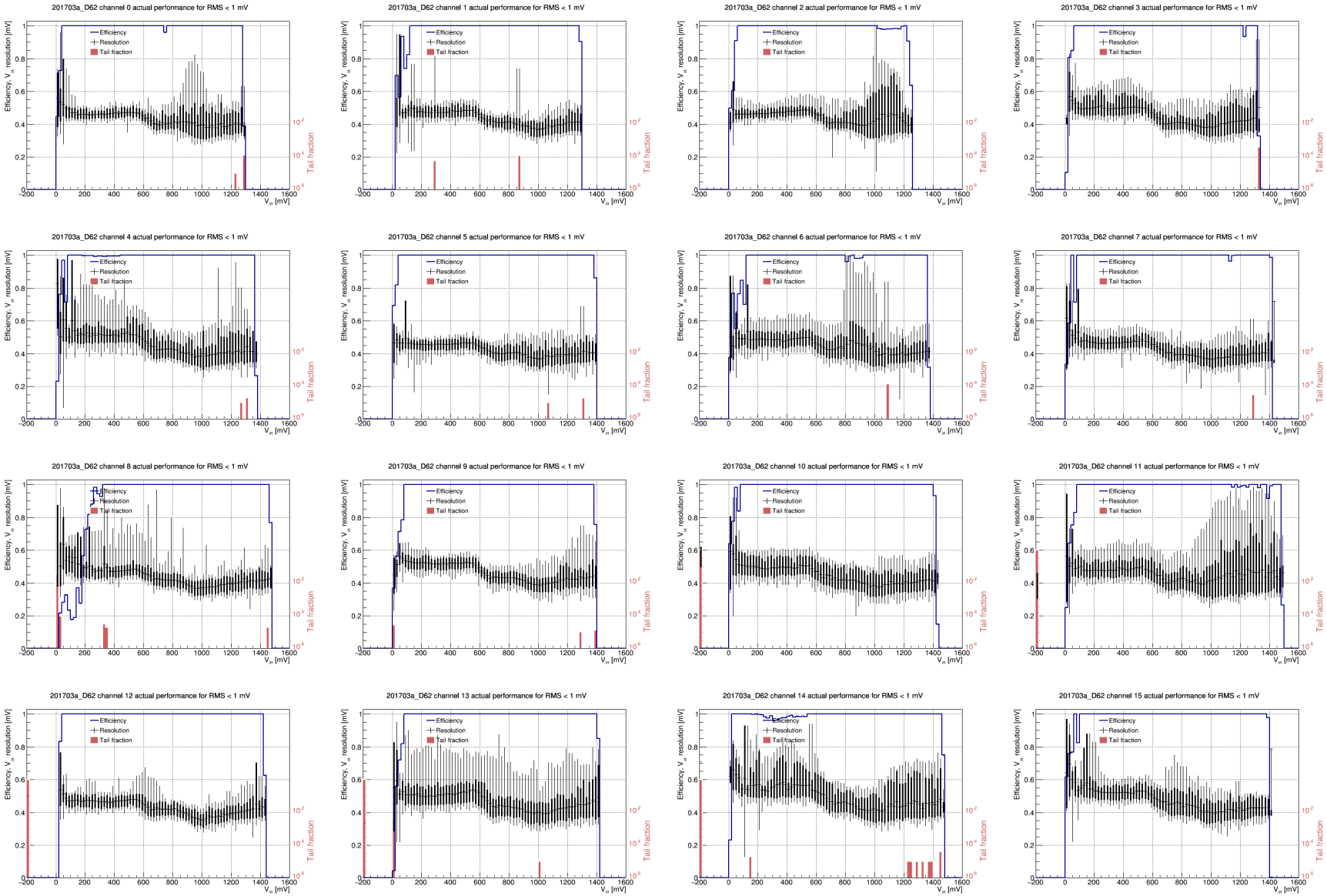
Chip D59 (rank=7, Q=0.974, a=0.998, m=0.989)



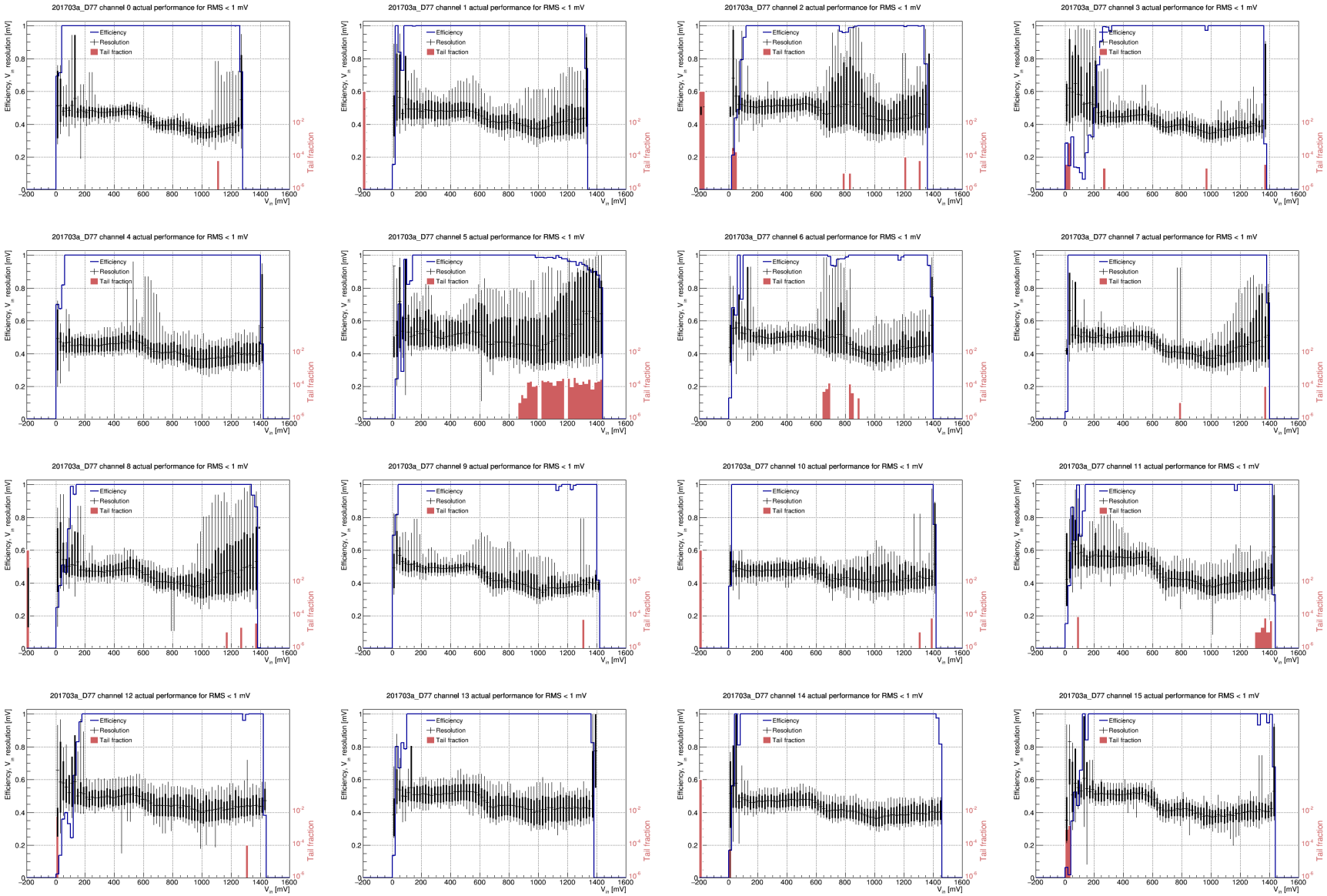
Chip D47 (rank=8, Q=0.973, a=0.998, m=0.990)



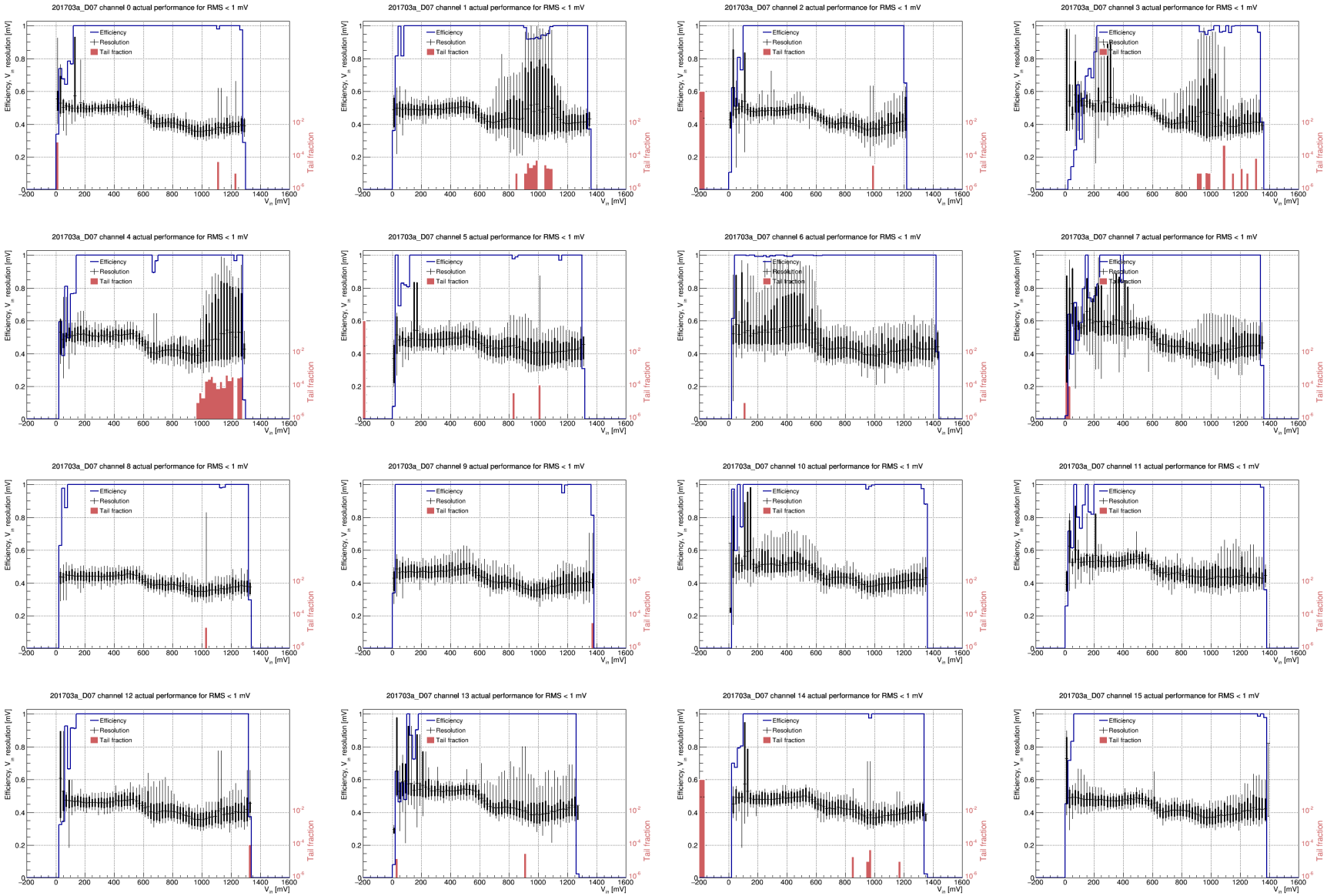
Chip D62 (rank=9, Q=0.970, a=0.998, m=0.985)



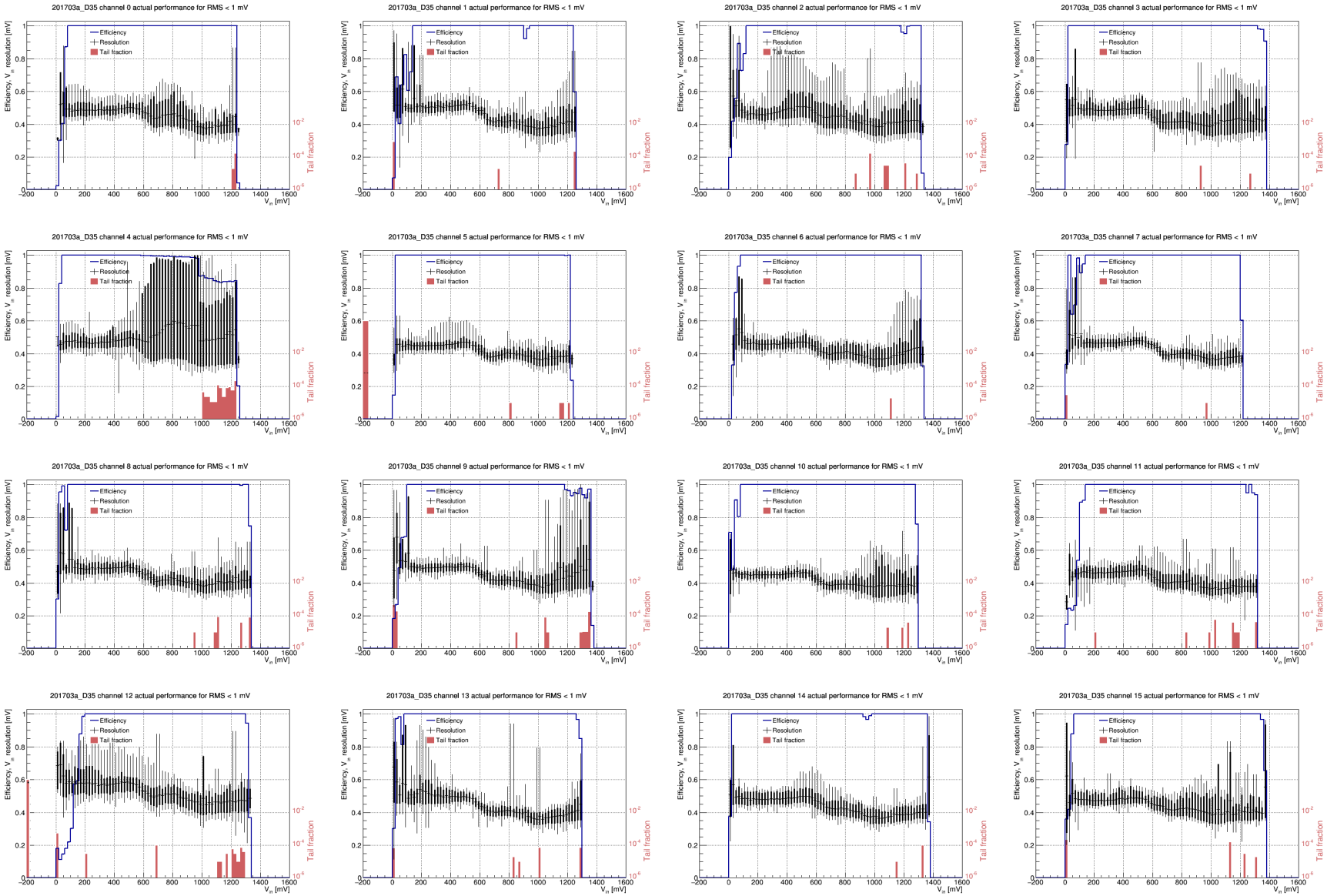
Chip D77 (rank=10, Q=0.969, a=0.998, m=0.981)



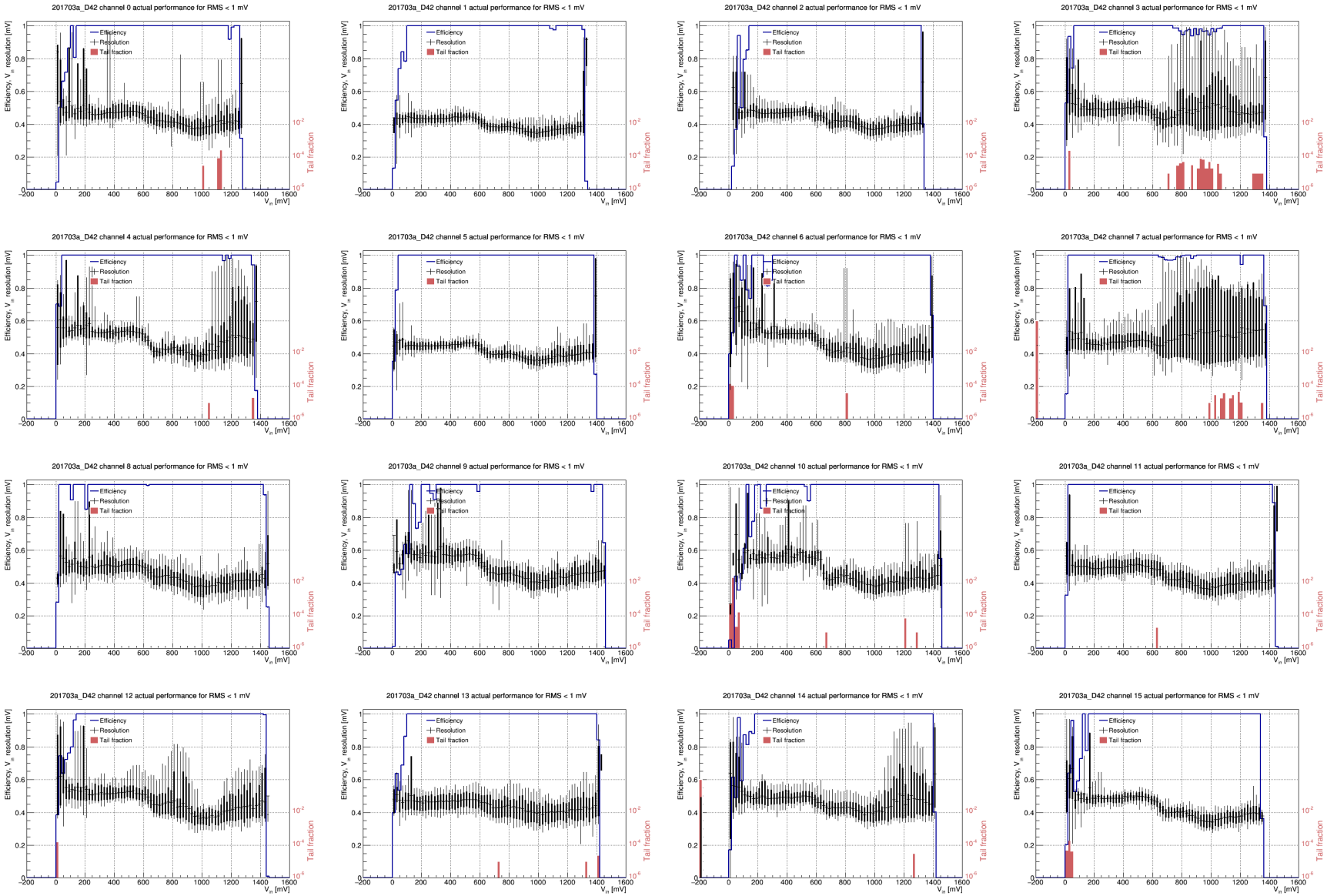
Chip D07 (rank=11, Q=0.959, a=0.997, m=0.988)



Chip D35 (rank=12, Q=0.959, a=0.997, m=0.964)

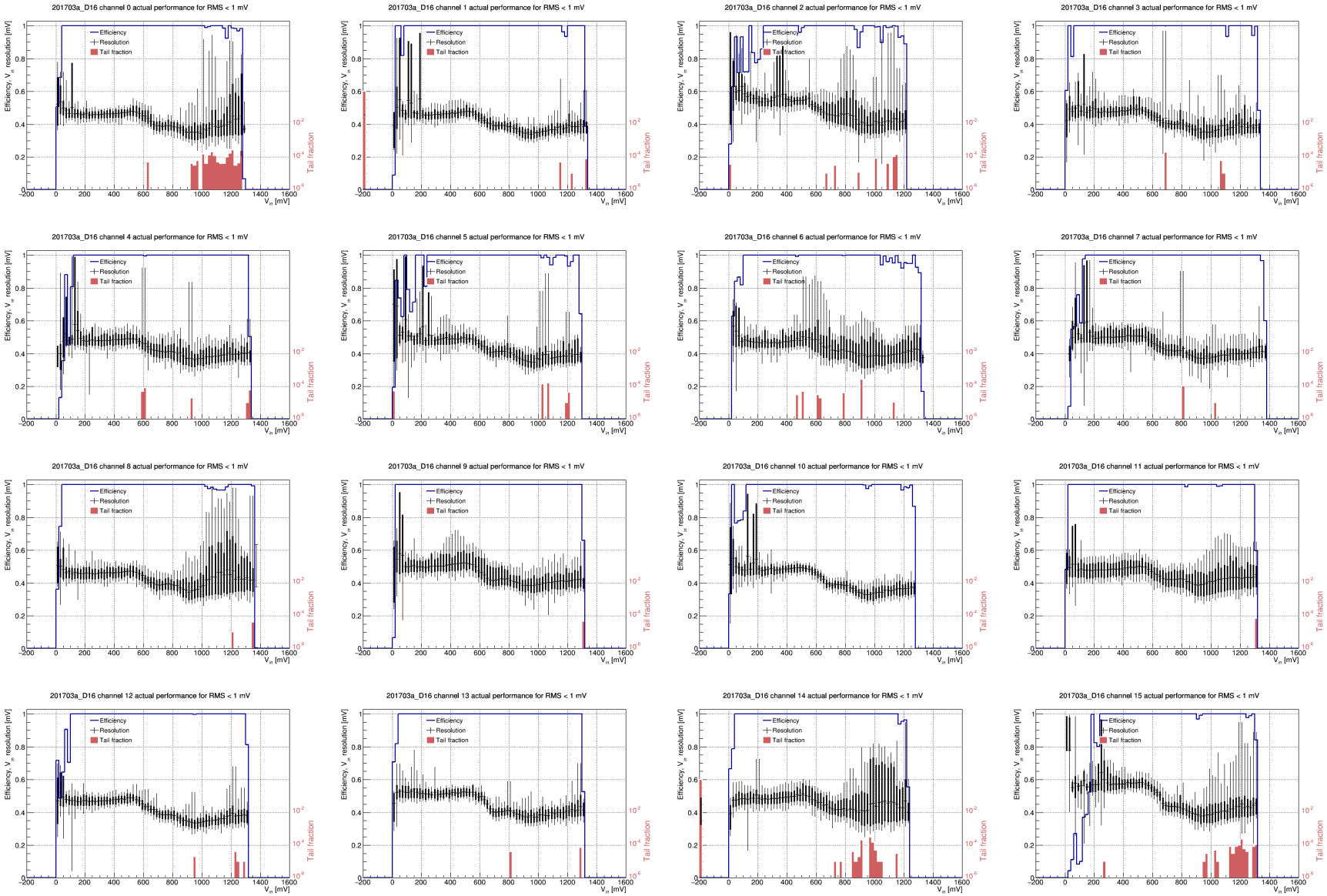


Chip D42 (rank=13, Q=0.957, a=0.997, m=0.989)

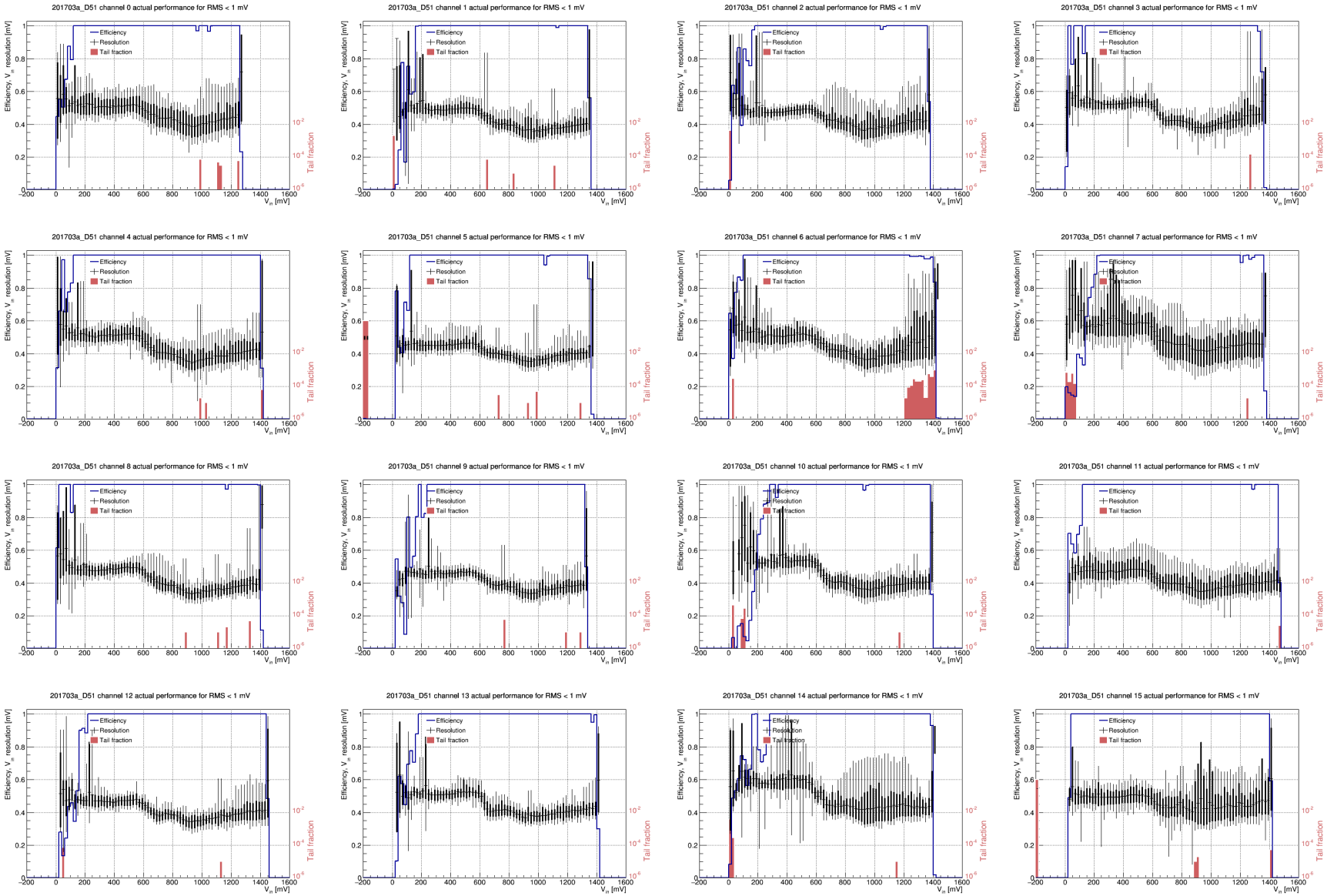


Fair chips

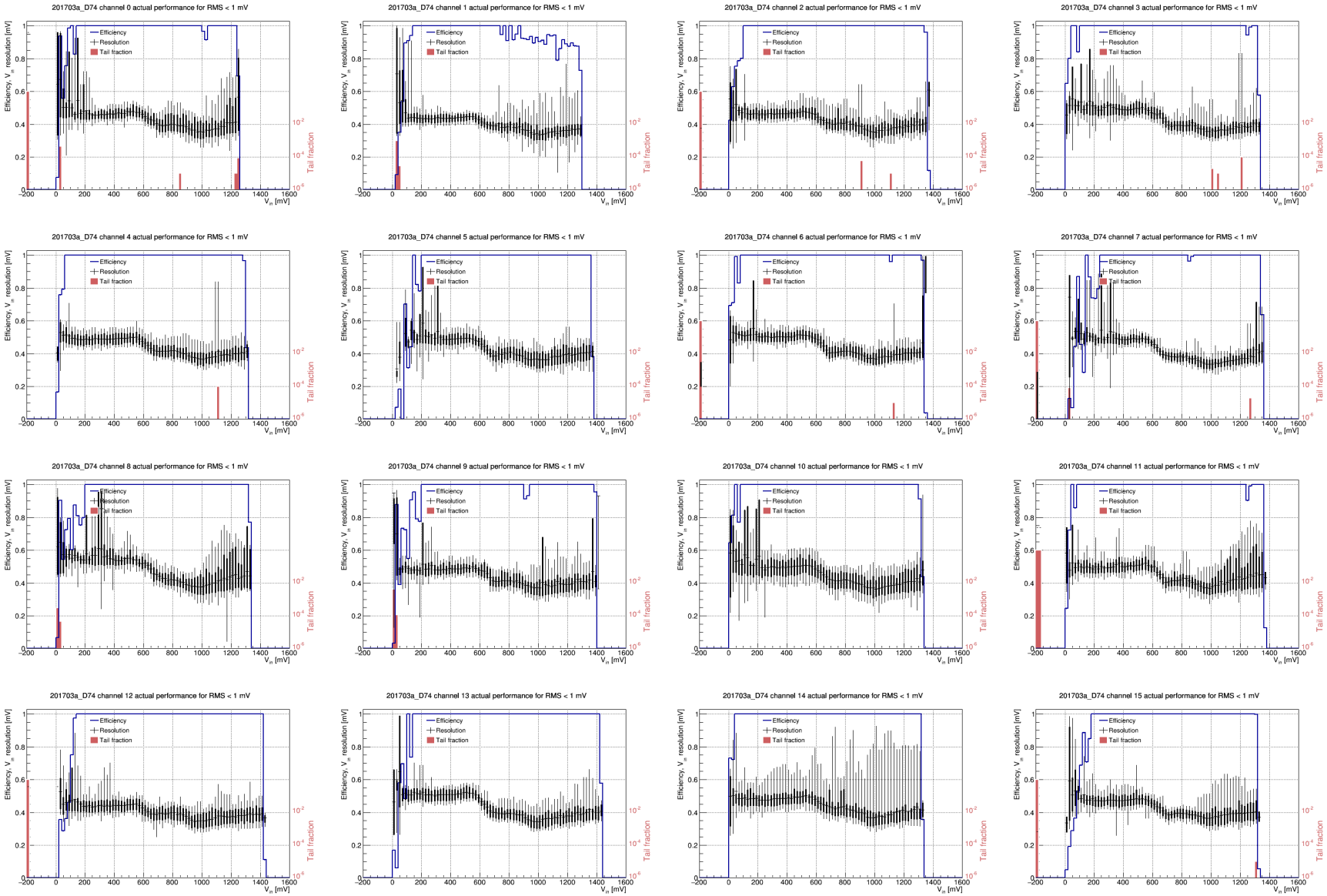
Chip D16 (rank=14, Q=0.949, a=0.996, m=0.982)



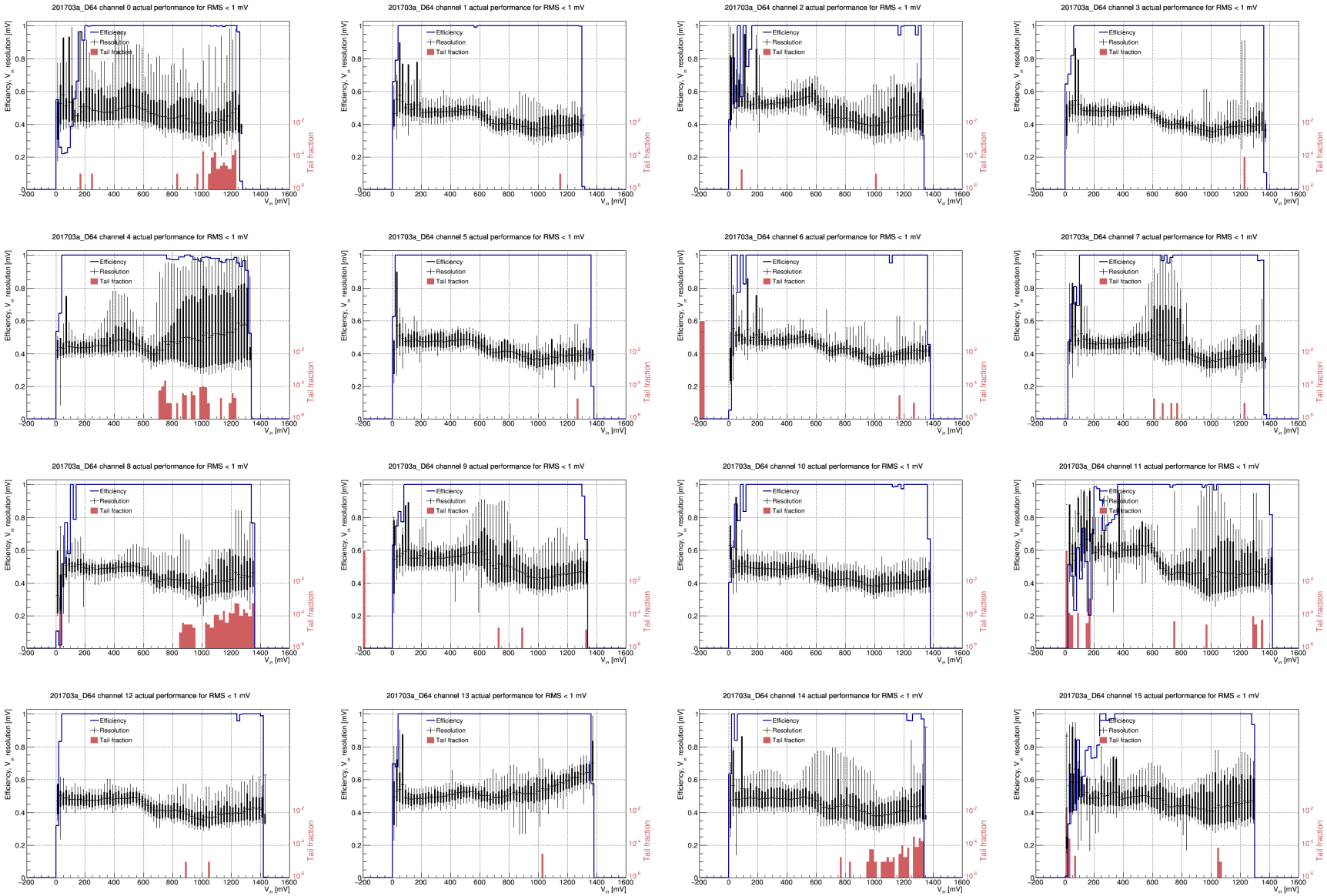
Chip D51 (rank=15, Q=0.948, a=0.996, m=0.981)



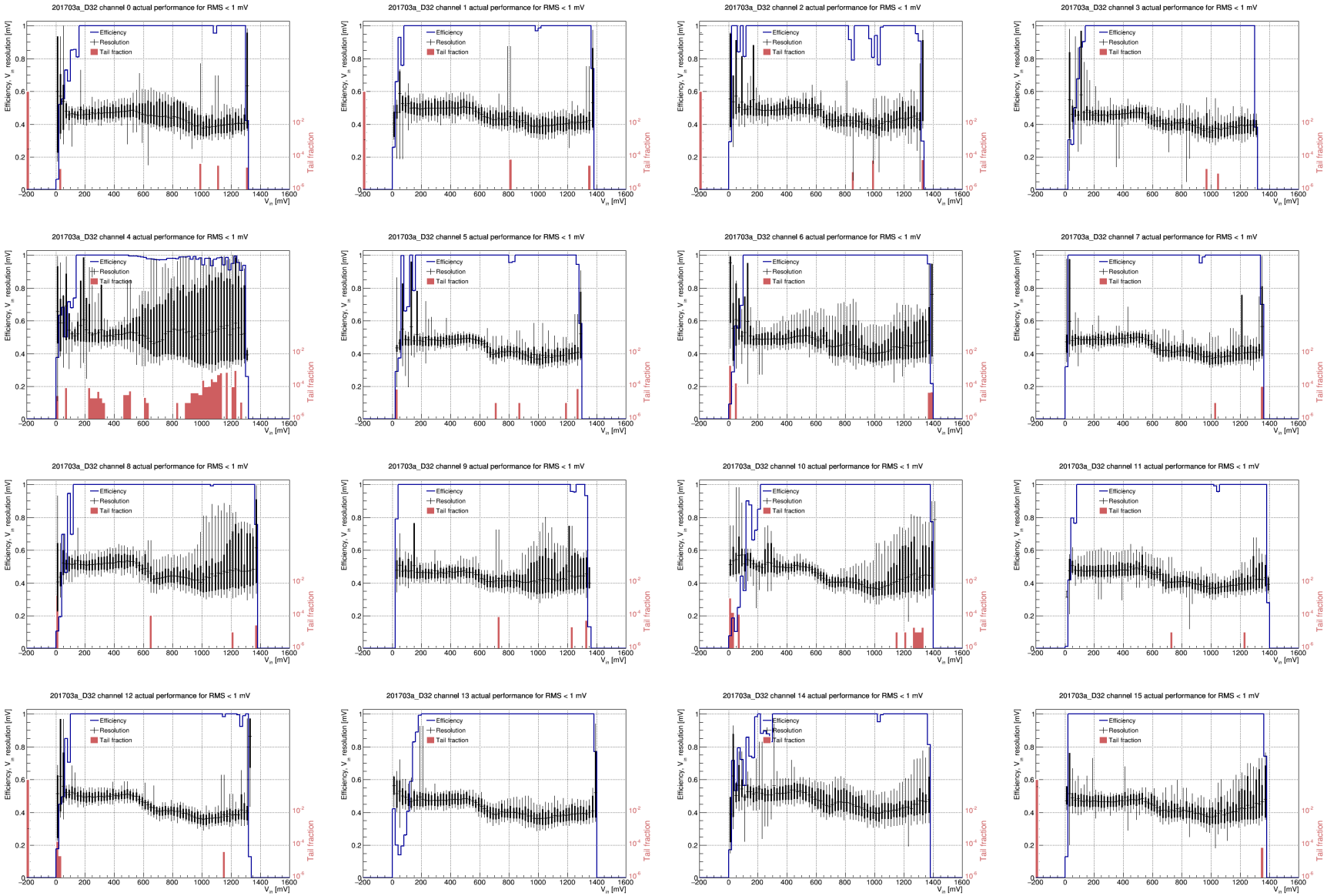
Chip D74 (rank=16, Q=0.948, a=0.996, m=0.964)



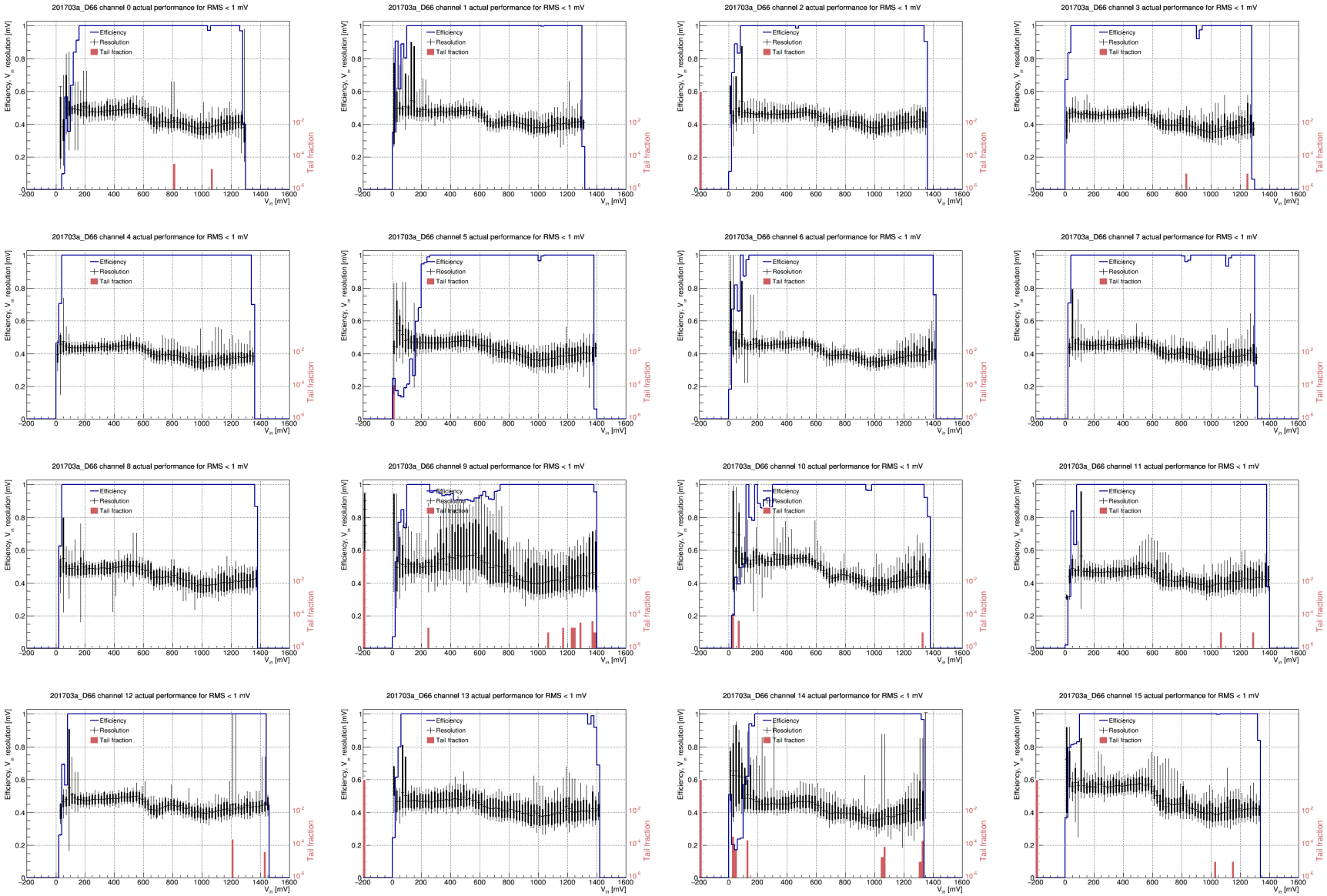
Chip D64 (rank=17, Q=0.947, a=0.996, m=0.972)



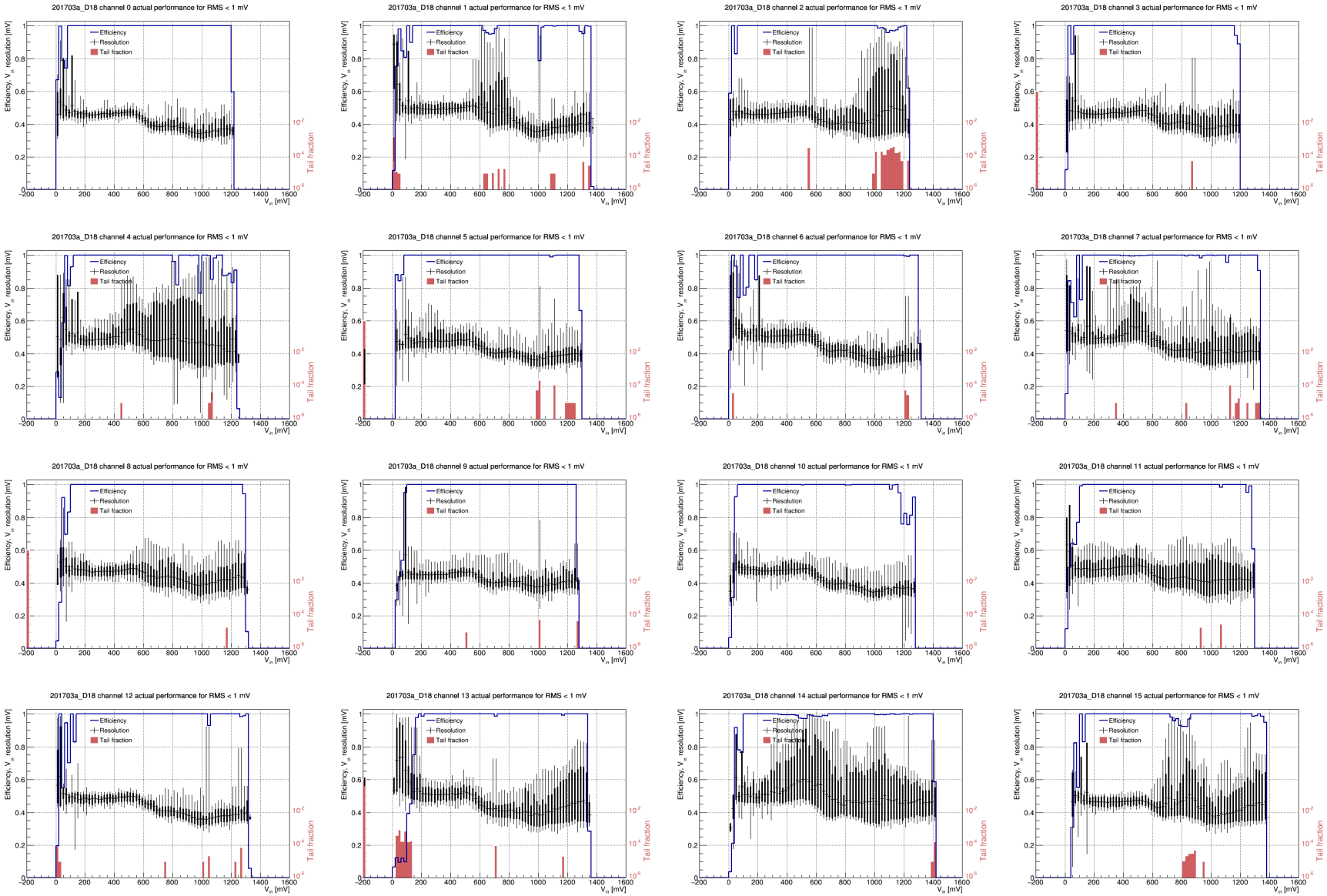
Chip D32 (rank=18, Q=0.946, a=0.996, m=0.982)



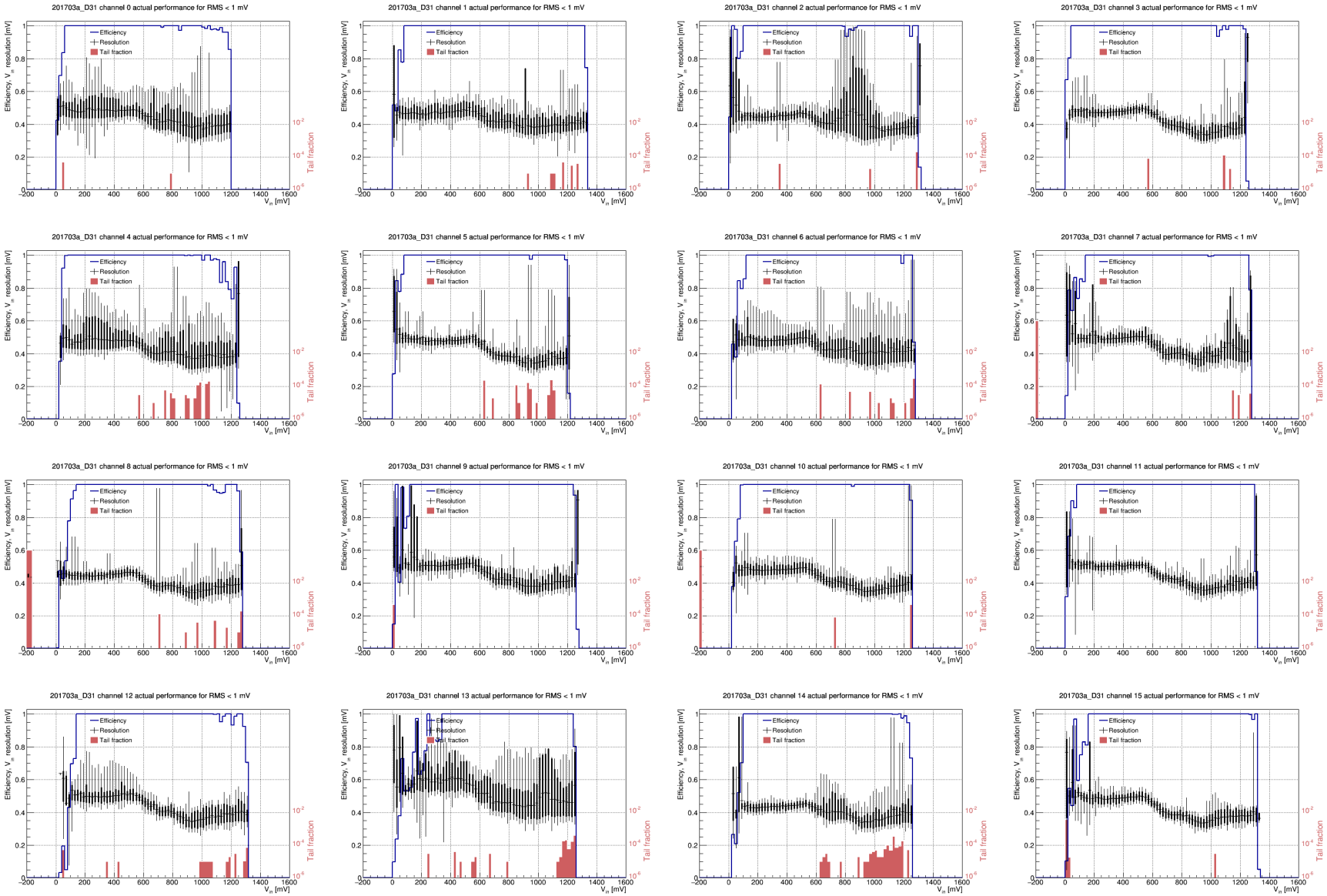
Chip D66 (rank=19, Q=0.945, a=0.996, m=0.966)



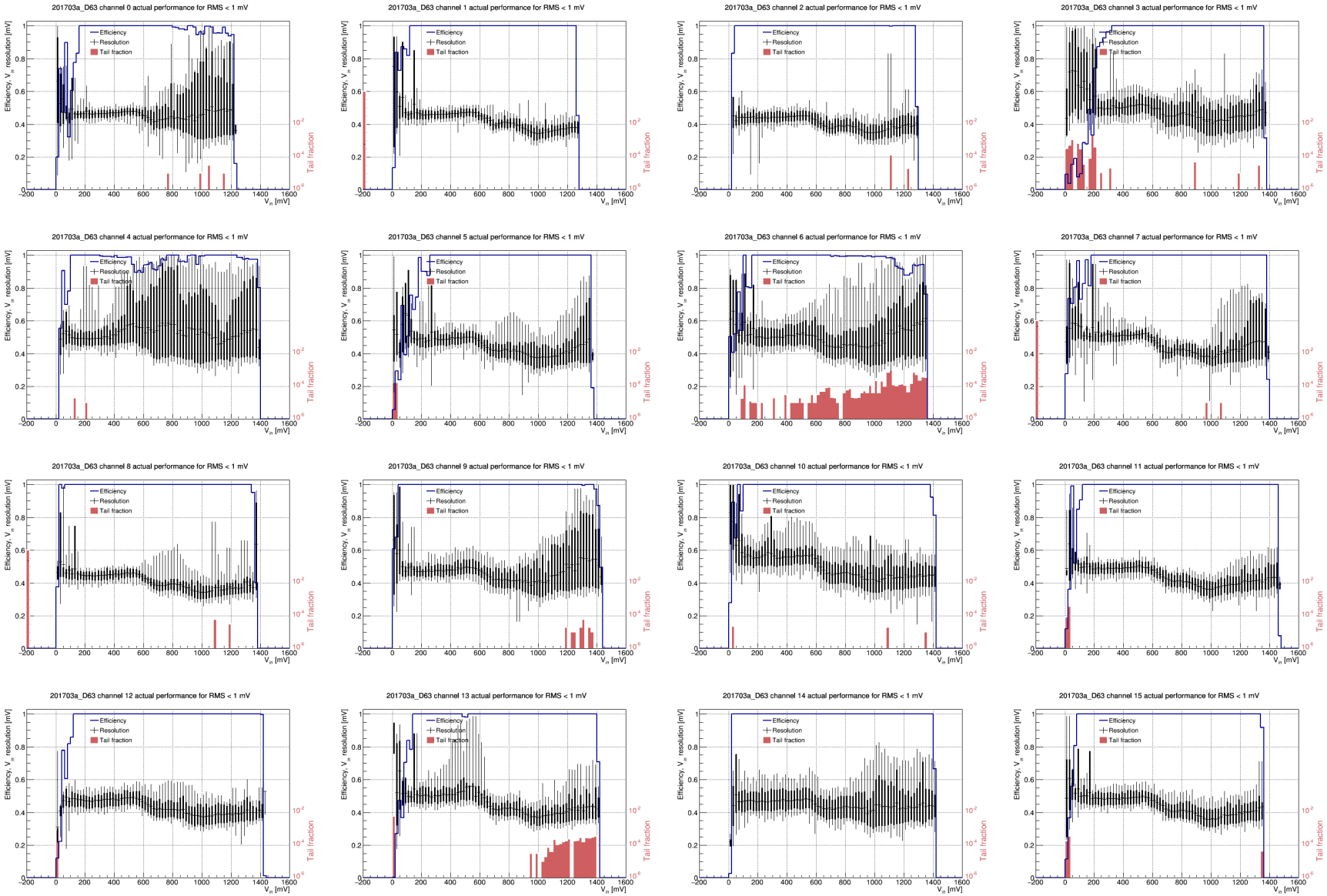
Chip D18 (rank=20, Q=0.943, a=0.996, m=0.980)



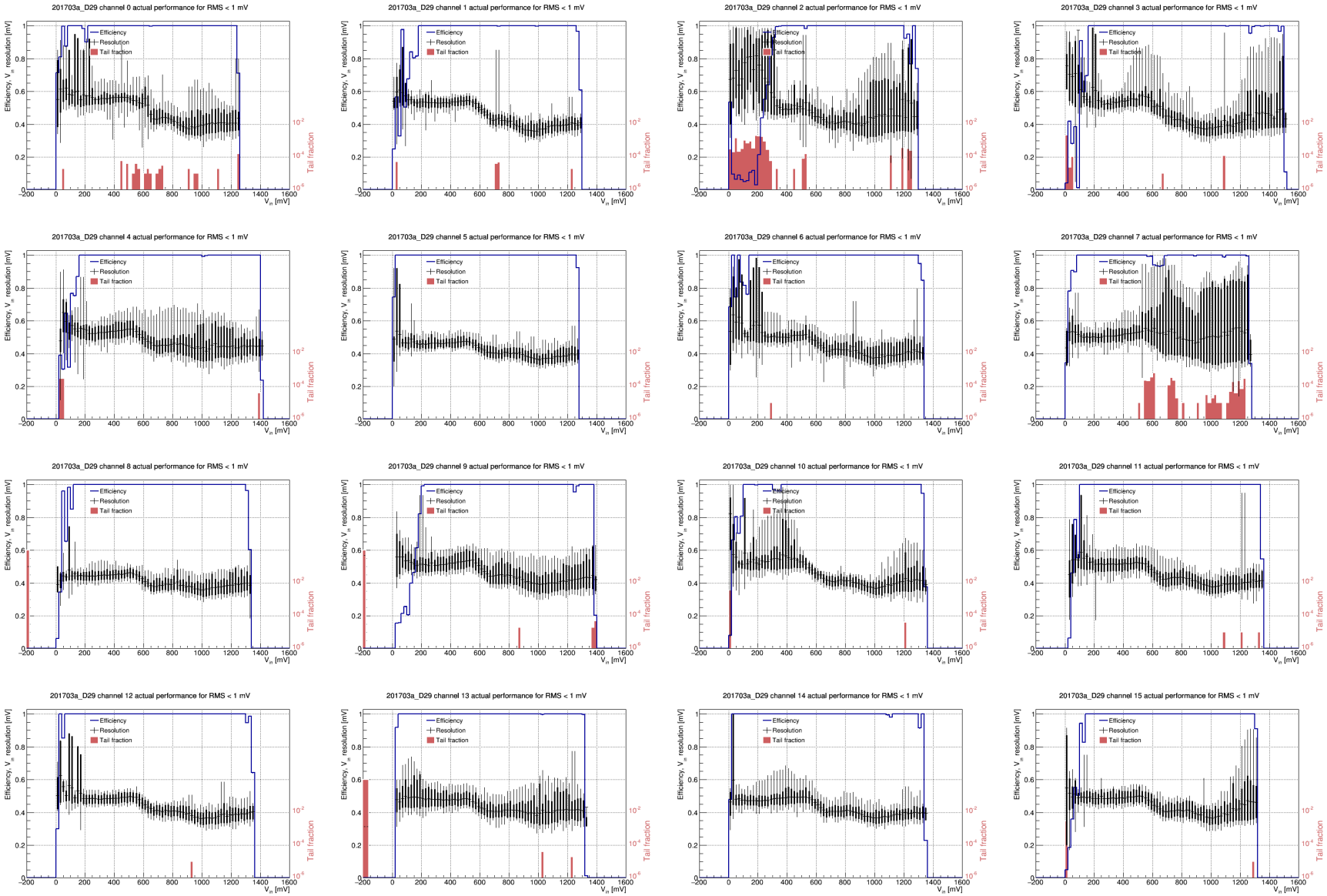
Chip D31 (rank=21, Q=0.942, a=0.996, m=0.975)



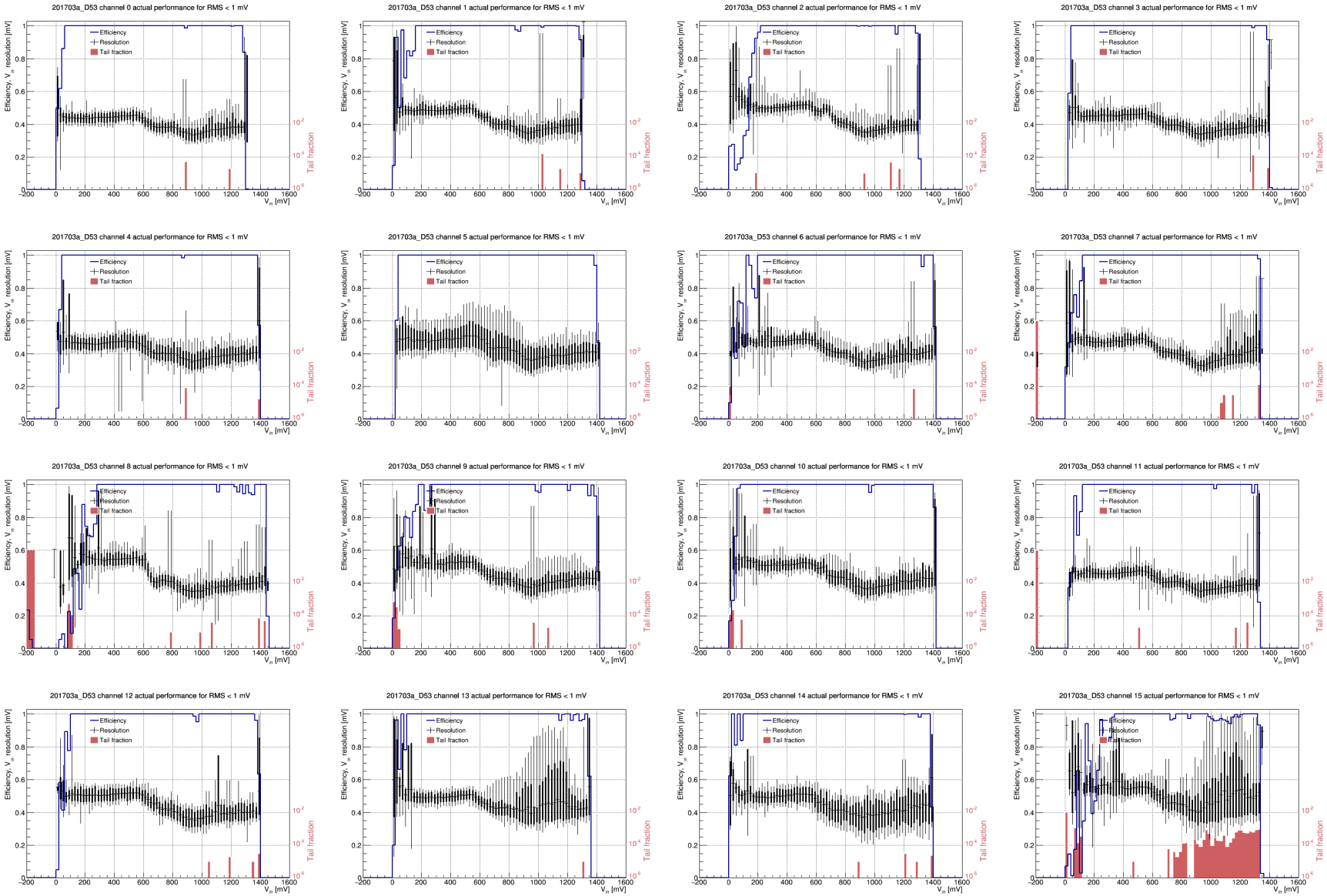
Chip D63 (rank=22, Q=0.941, a=0.996, m=0.978)



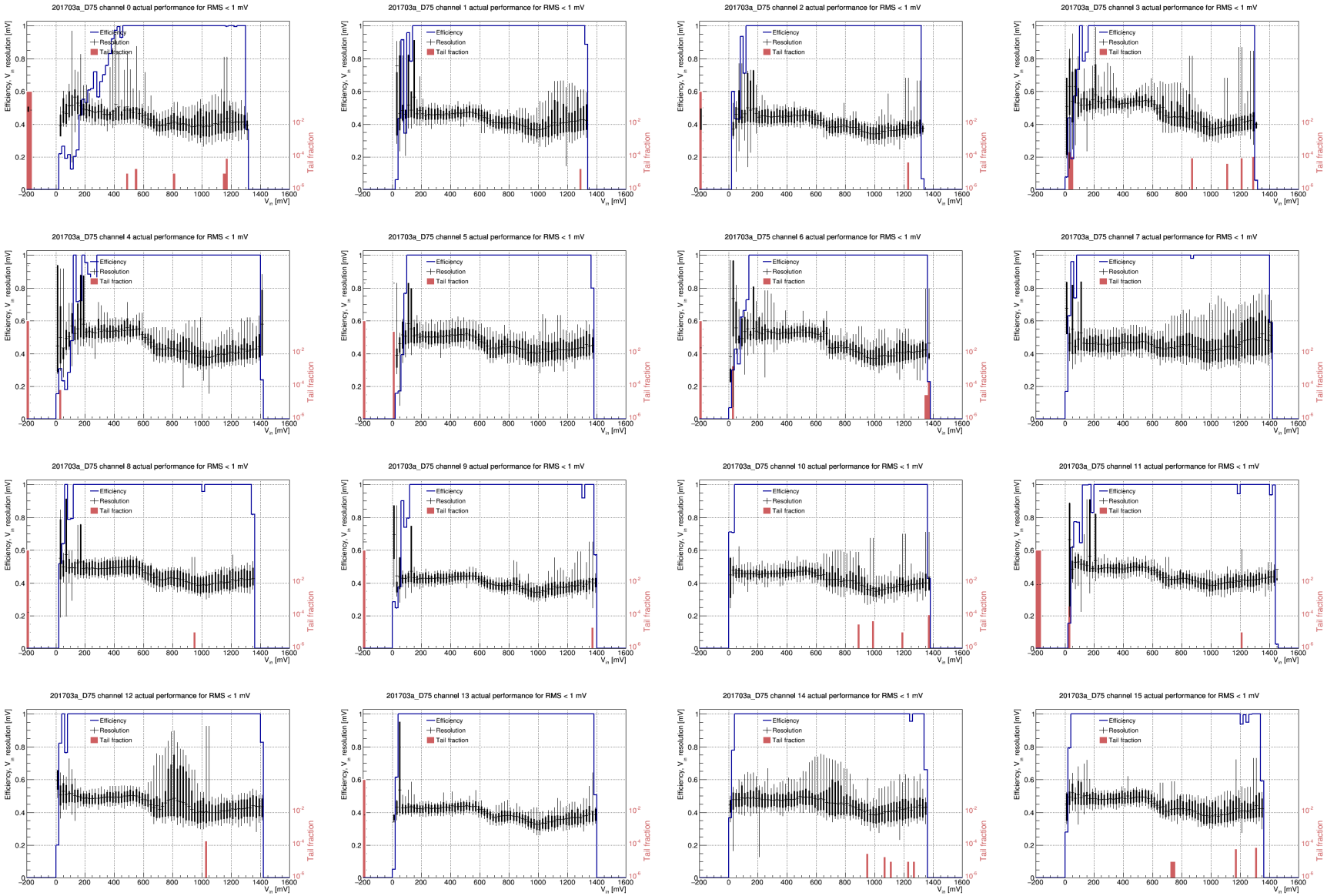
Chip D29 (rank=23, Q=0.940, a=0.996, m=0.951)



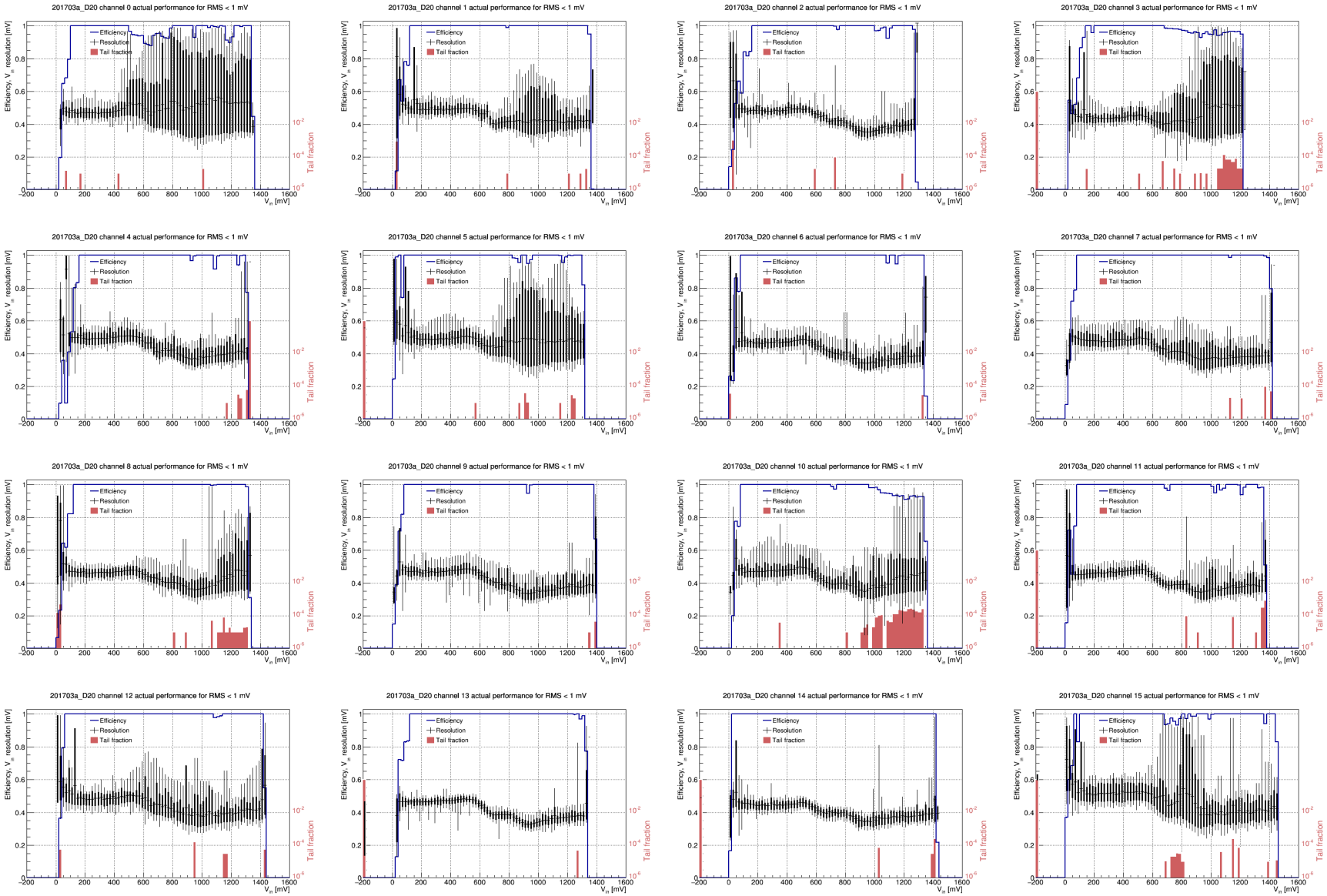
Chip D53 (rank=24, Q=0.926, a=0.995, m=0.963)



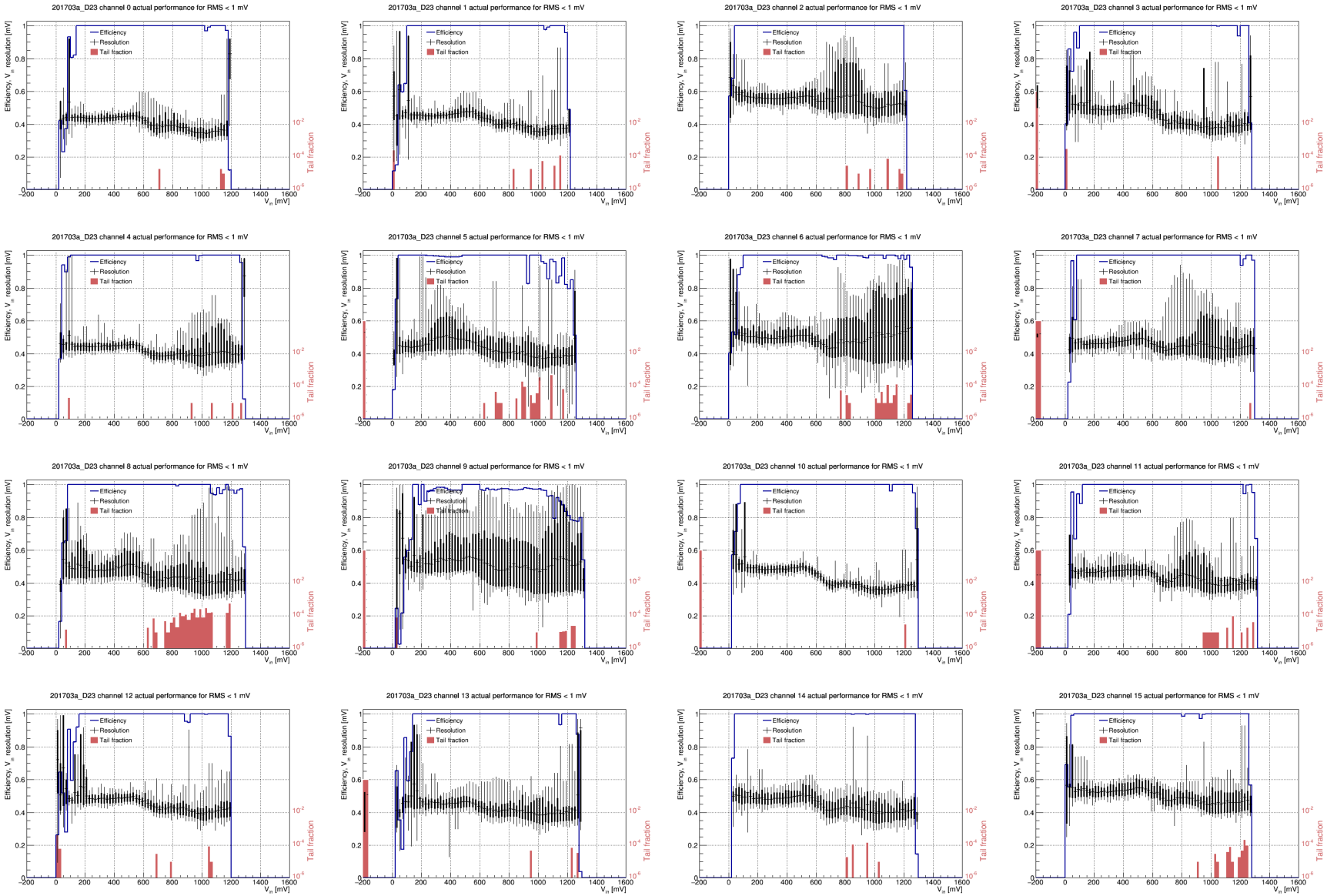
Chip D75 (rank=25, Q=0.924, a=0.995, m=0.936)



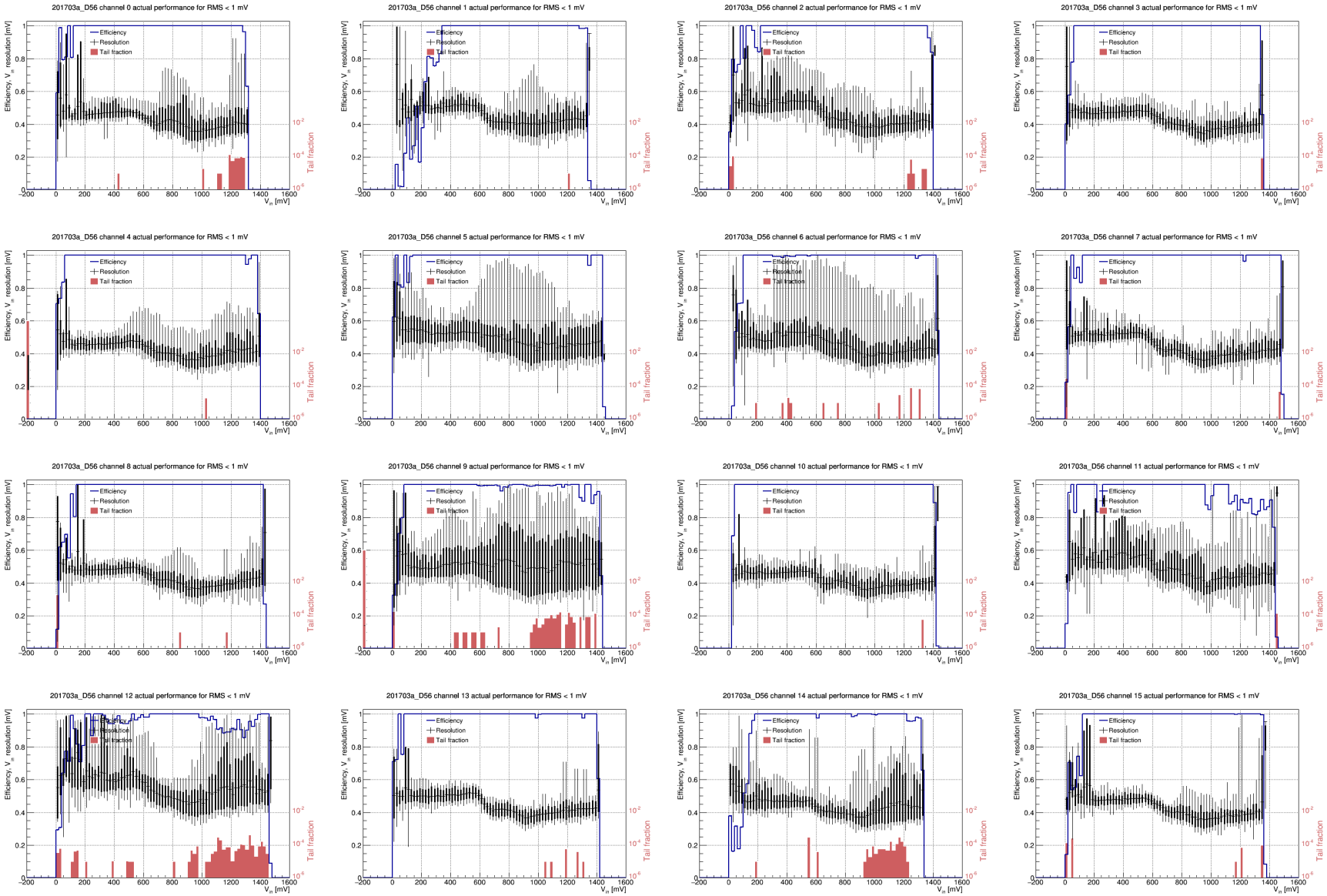
Chip D20 (rank=26, Q=0.919, a=0.994, m=0.974)



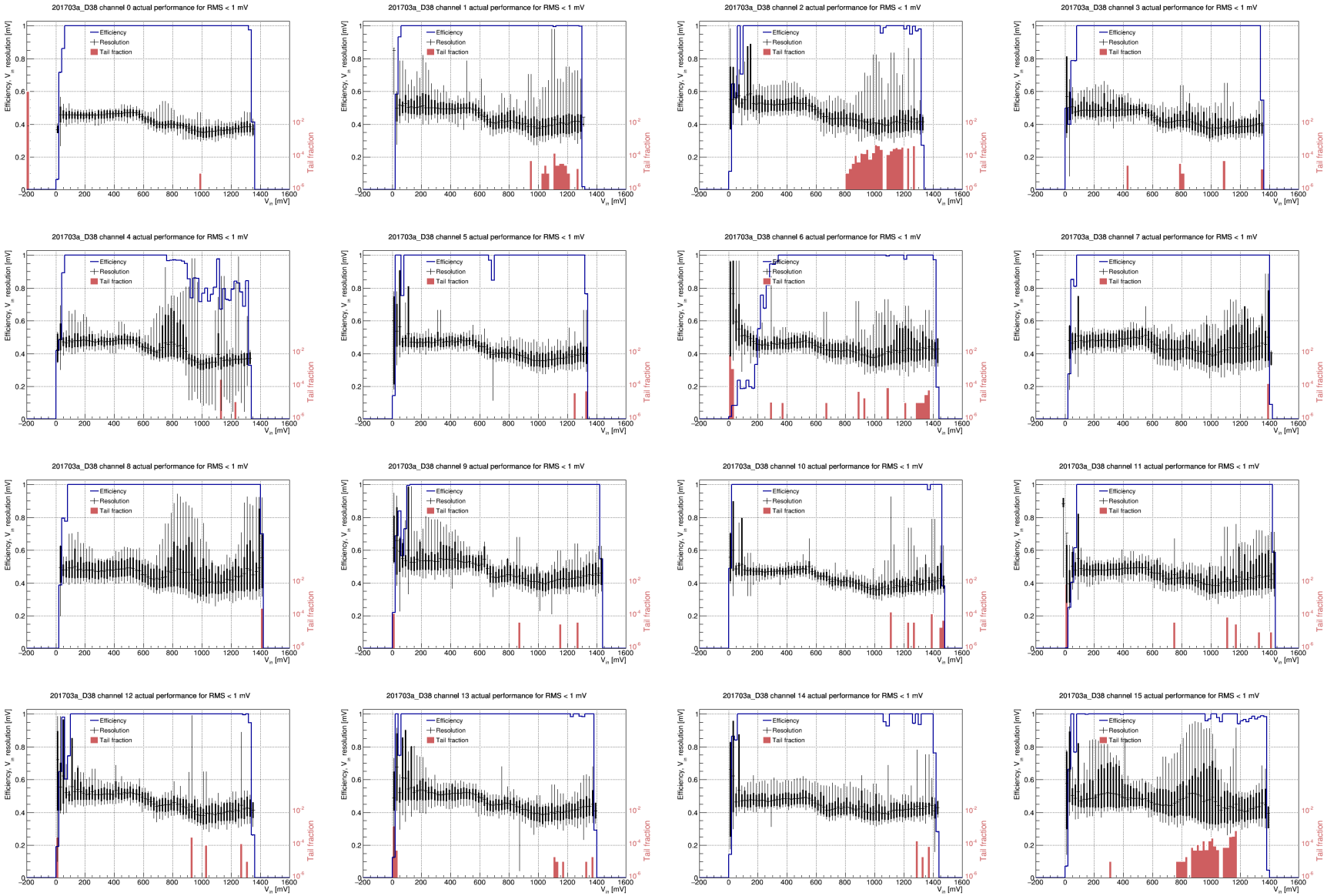
Chip D23 (rank=27, Q=0.905, a=0.993, m=0.961)



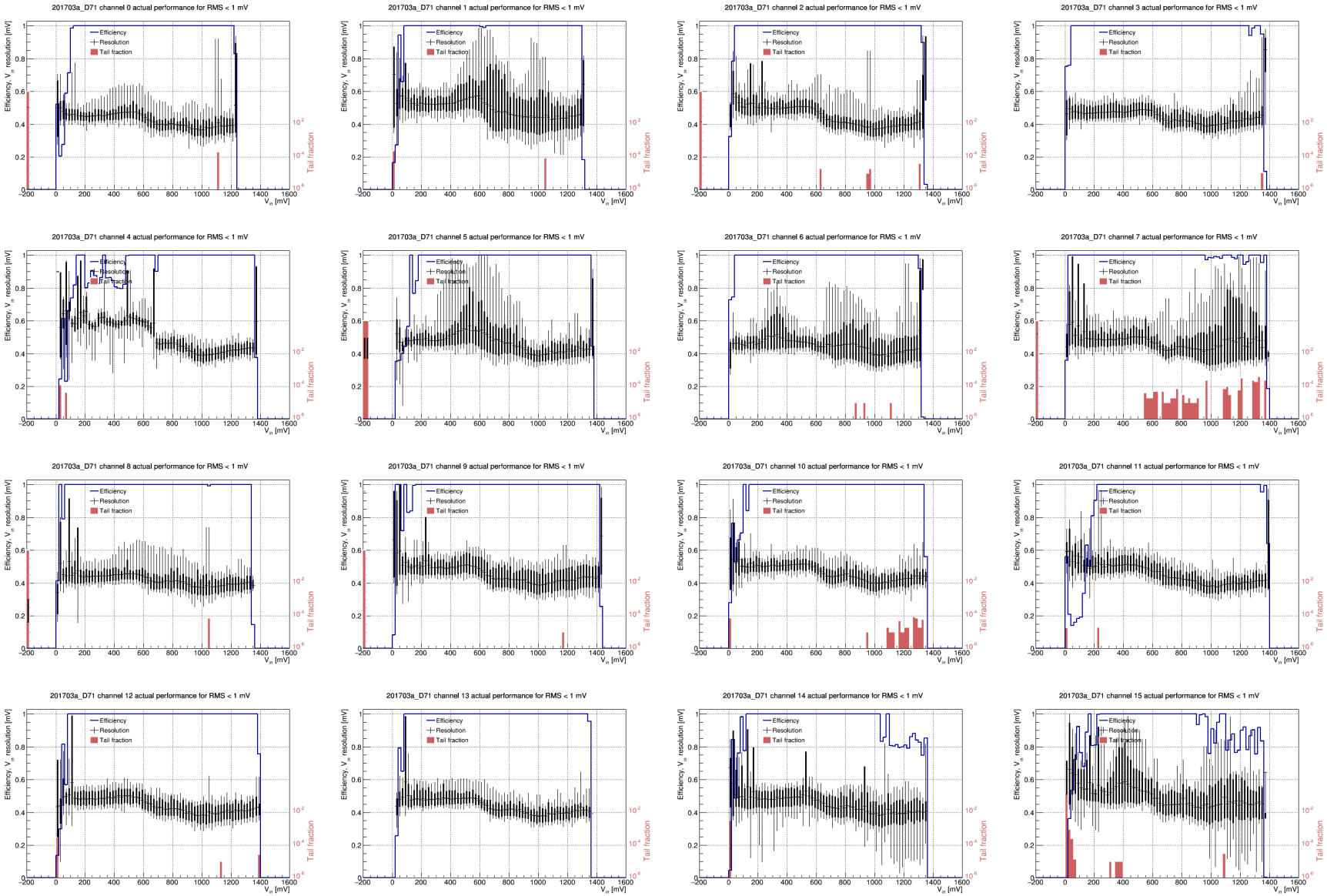
Chip D56 (rank=28, Q=0.904, a=0.993, m=0.960)



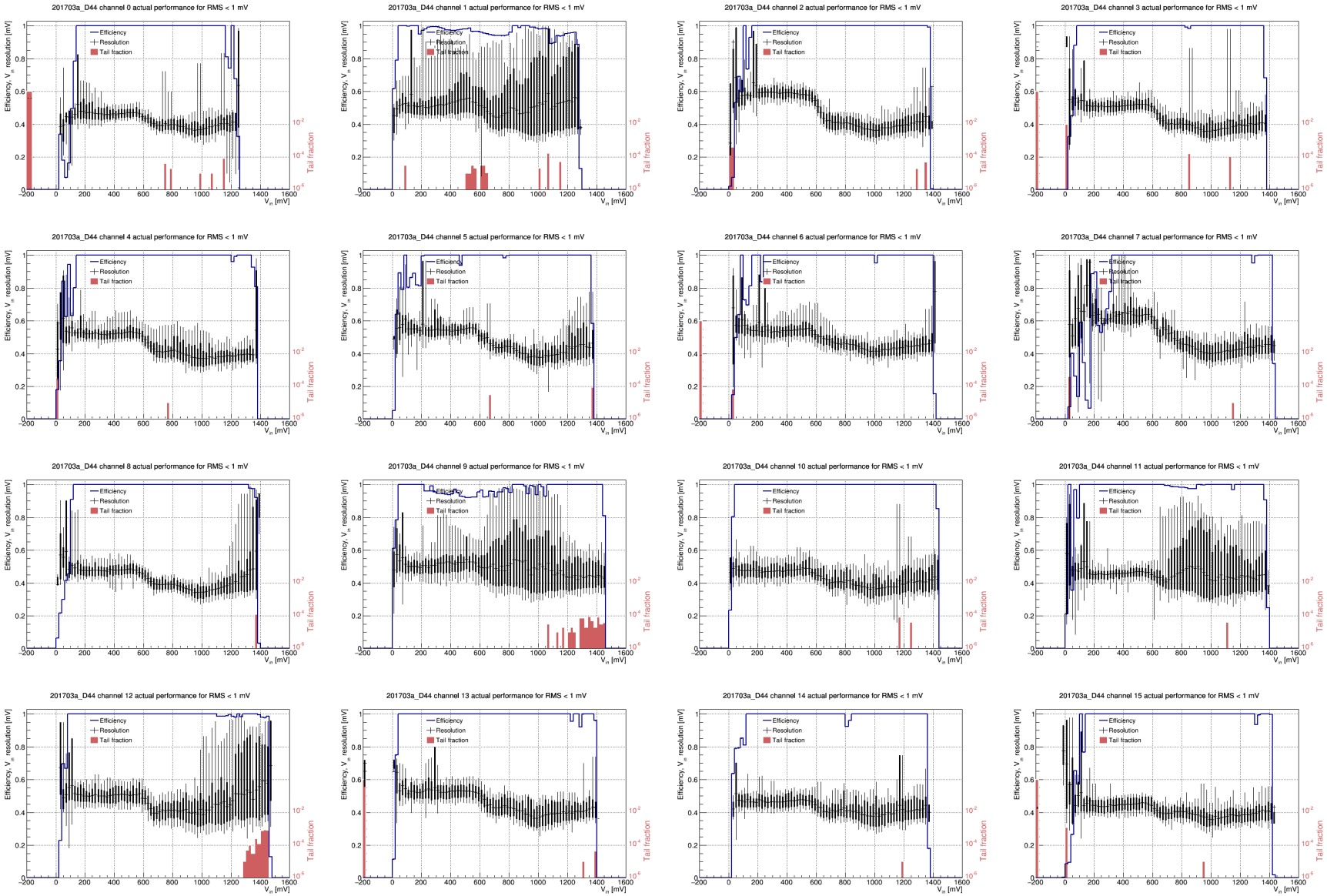
Chip D38 (rank=29, Q=0.895, a=0.993, m=0.930)



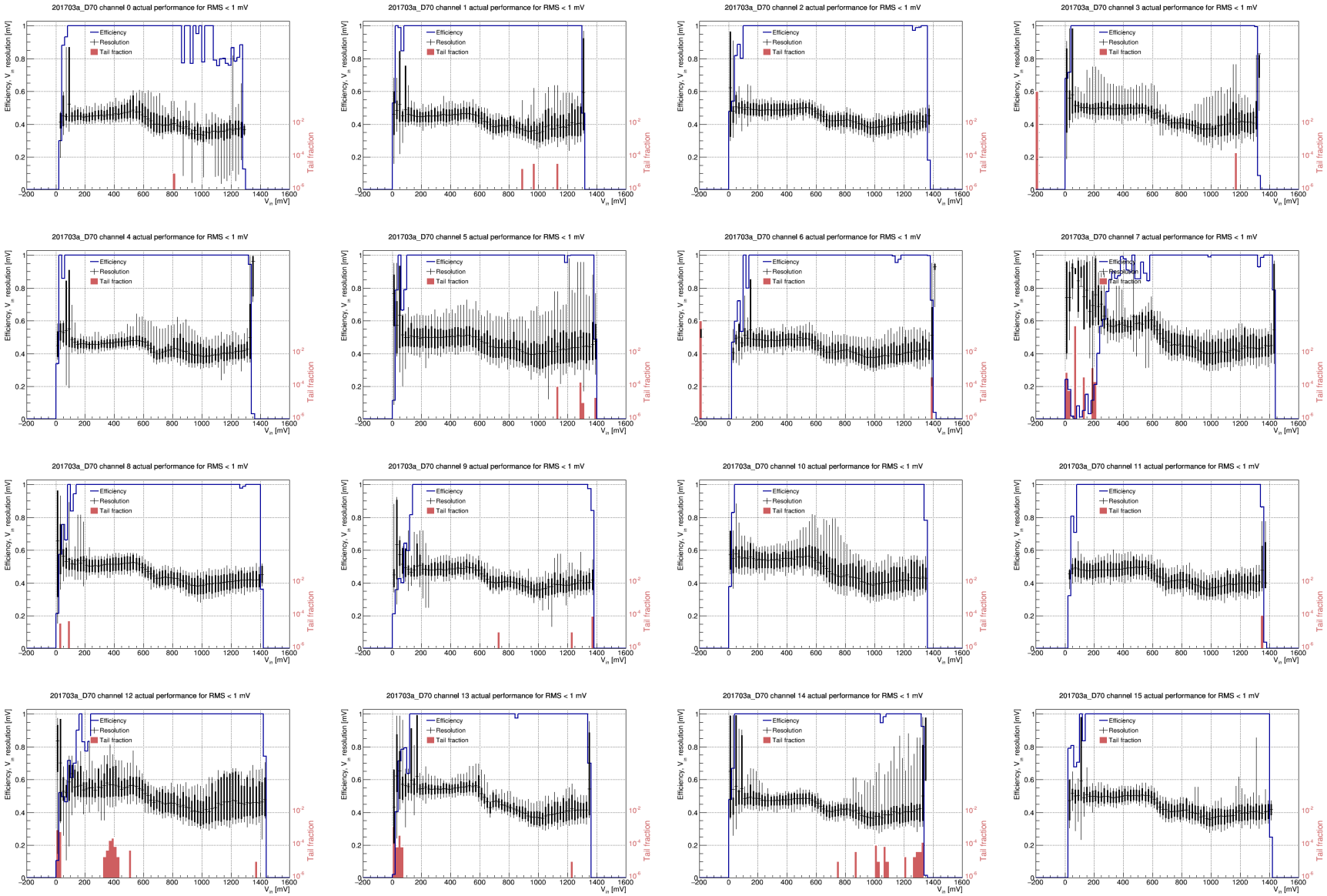
Chip D71 (rank=30, Q=0.893, a=0.993, m=0.956)



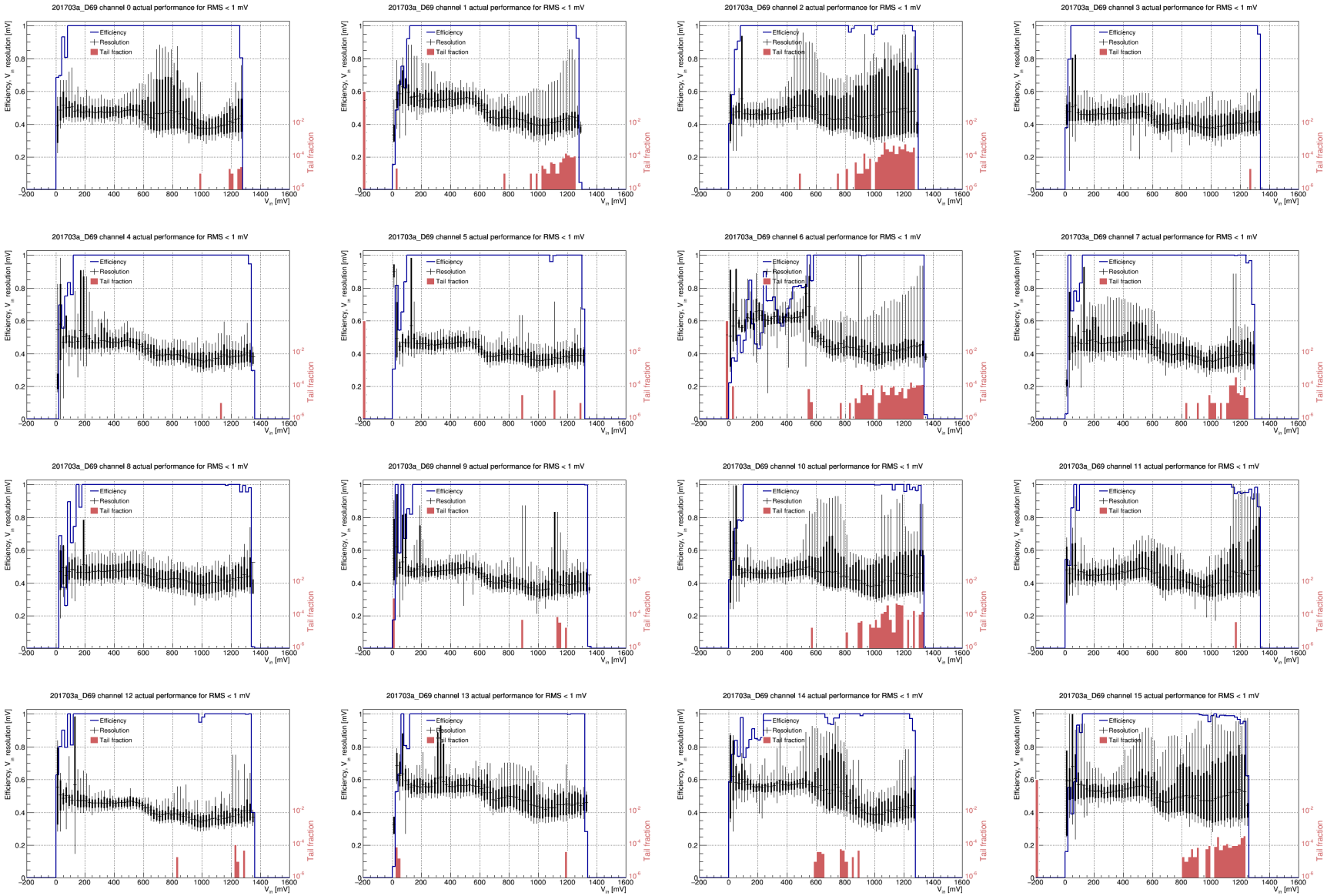
Chip D44 (rank=31, Q=0.877, a=0.991, m=0.960)



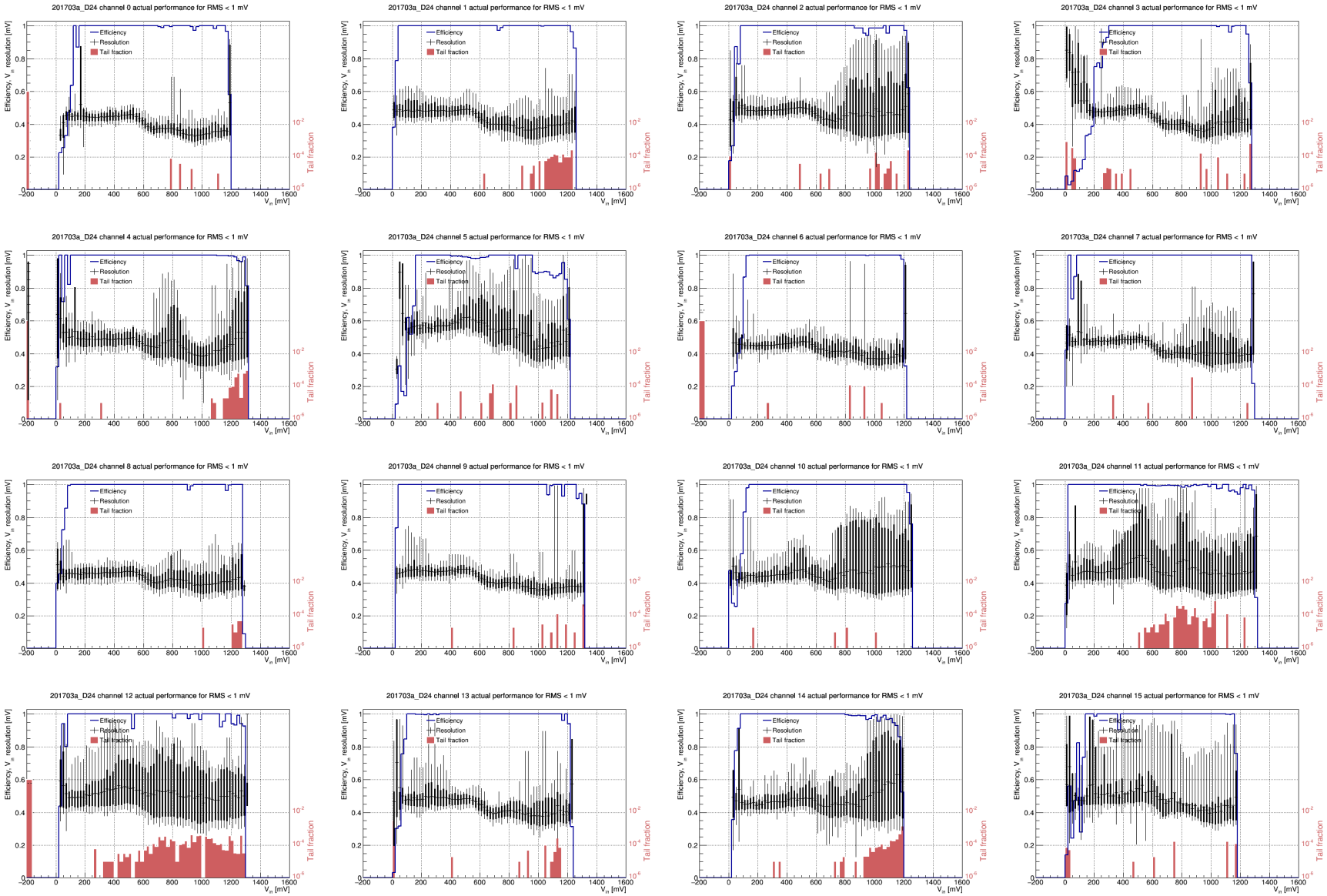
Chip D70 (rank=32, Q=0.875, a=0.991, m=0.924)



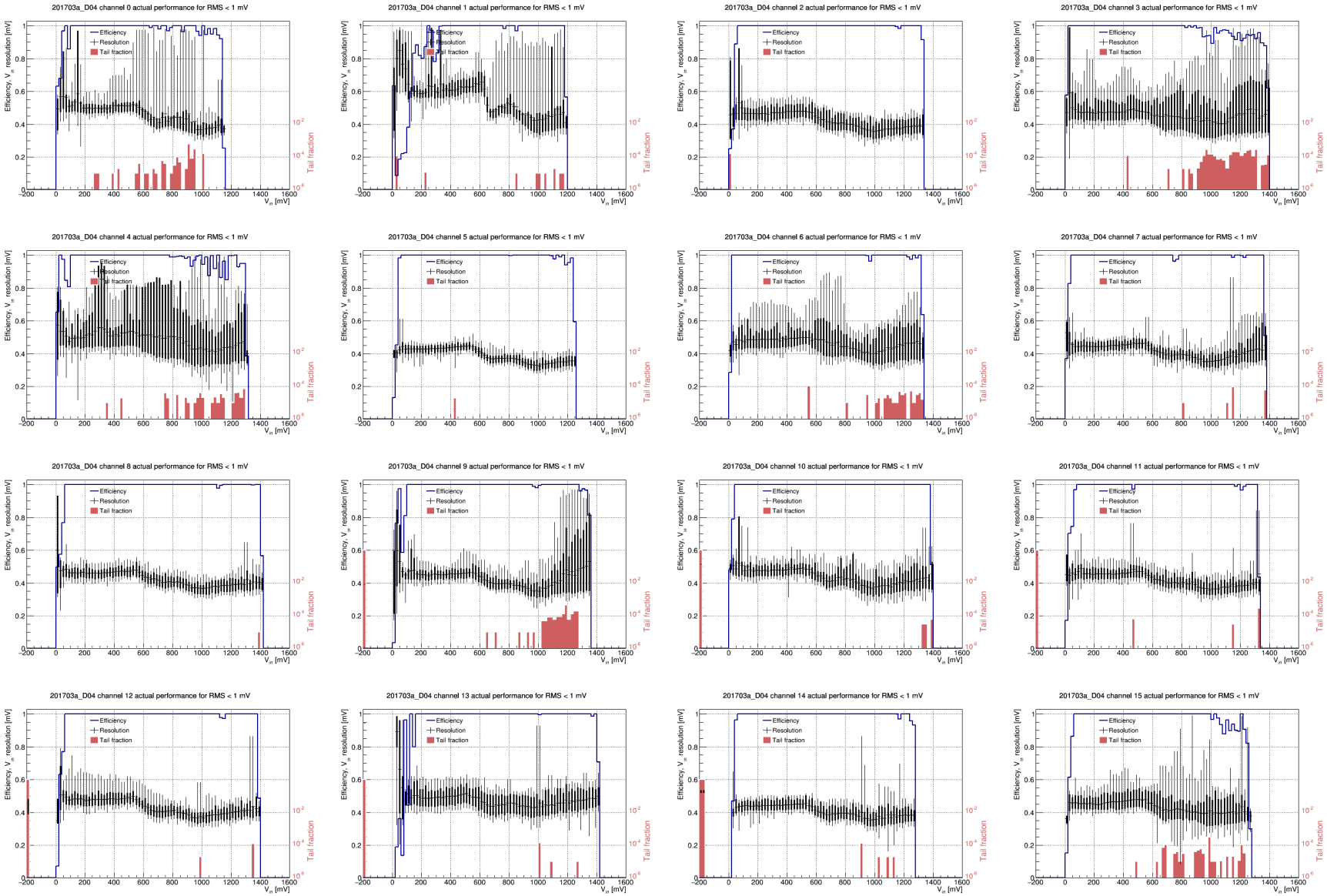
Chip D69 (rank=33, Q=0.875, a=0.992, m=0.895)



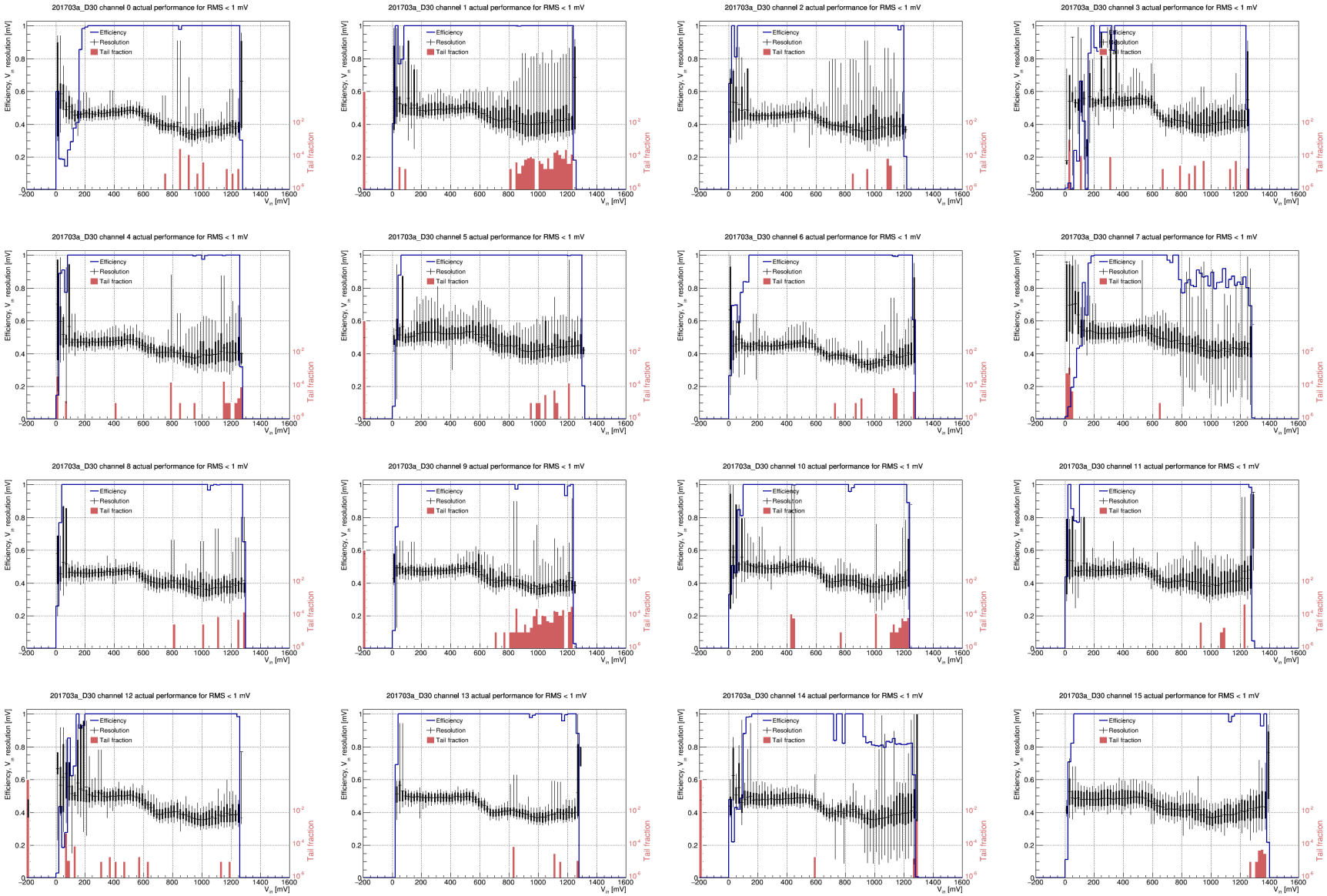
Chip D24 (rank=34, Q=0.873, a=0.991, m=0.968)



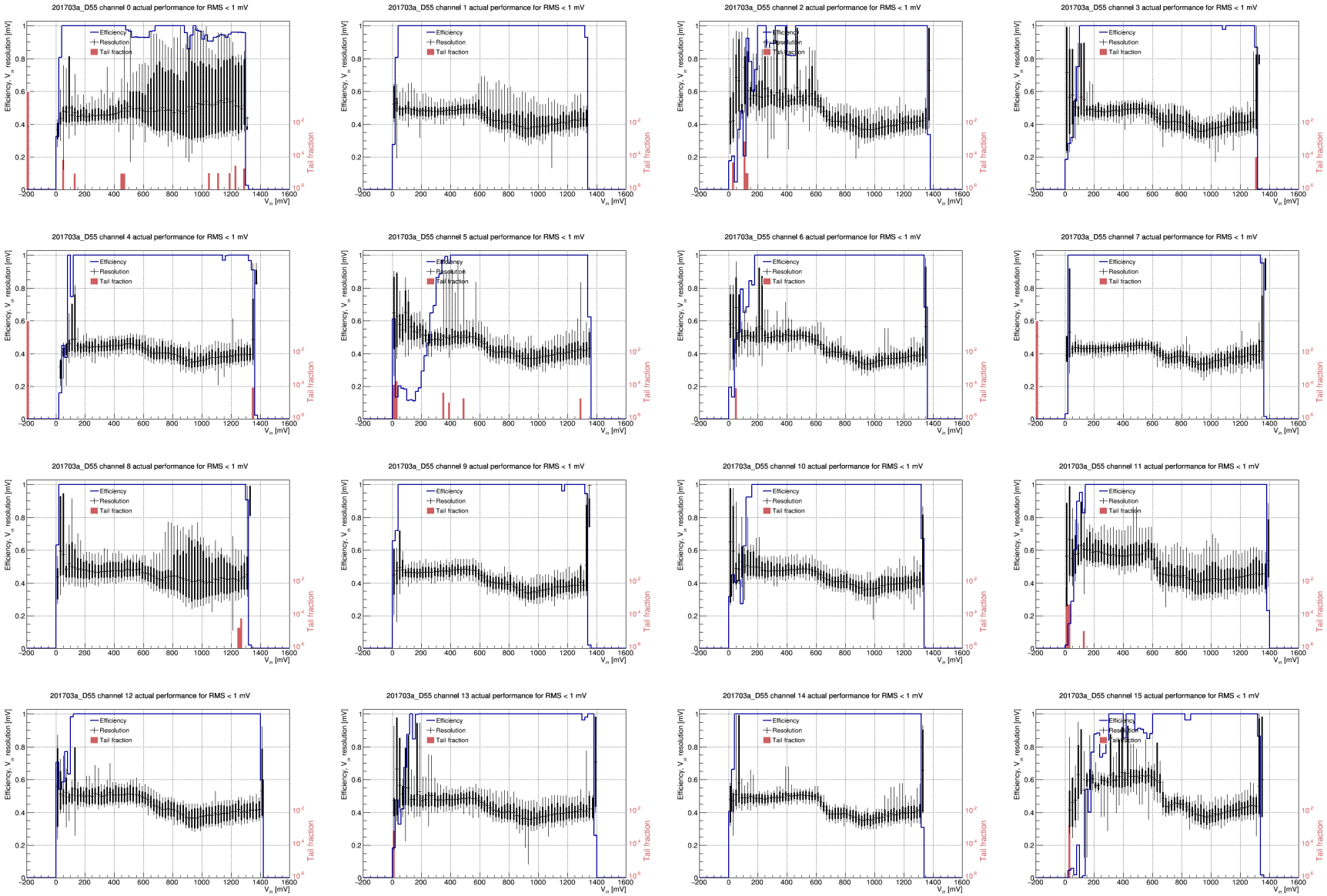
Chip D04 (rank=35, Q=0.867, a=0.991, m=0.935)



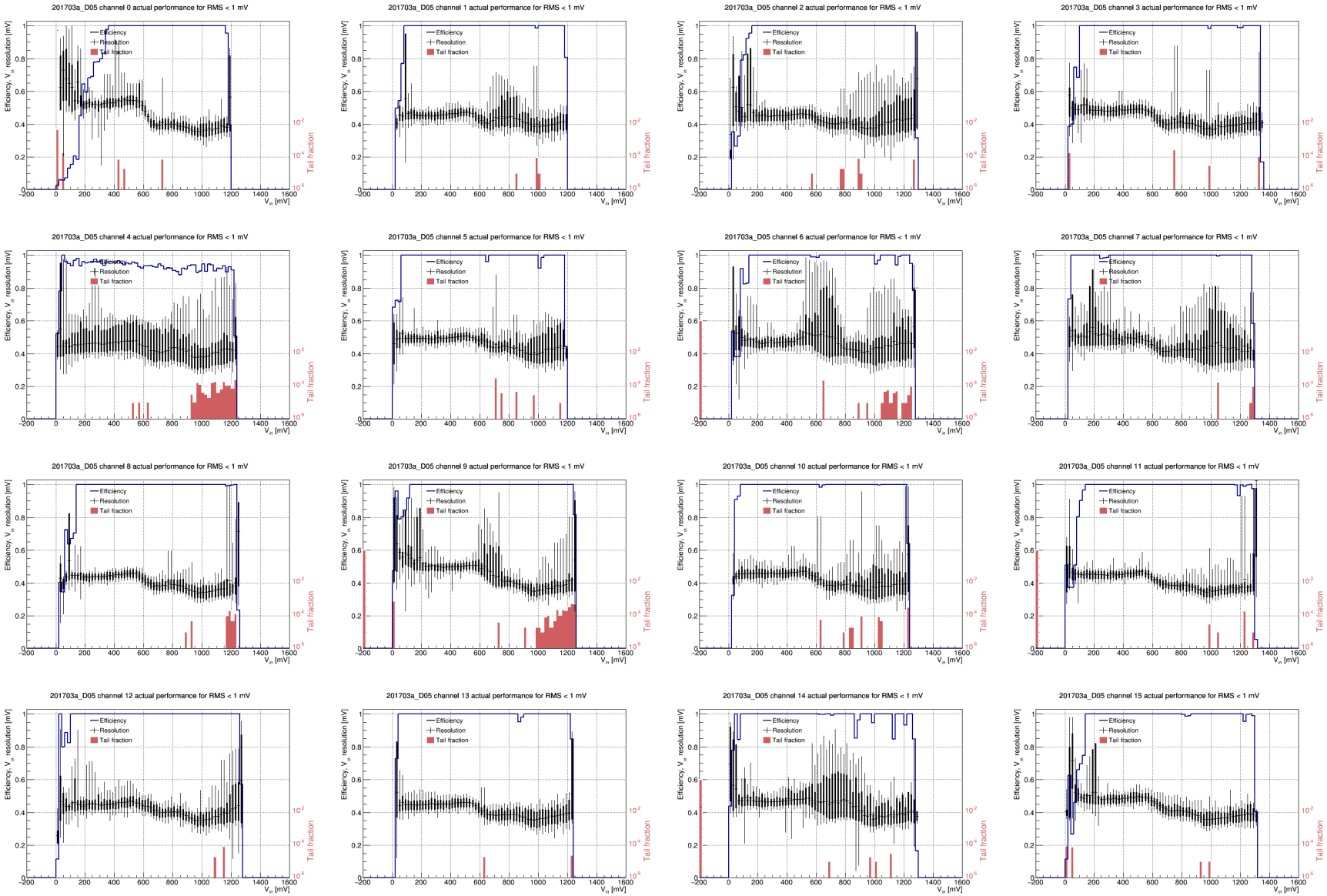
Chip D30 (rank=36, Q=0.864, a=0.991, m=0.933)



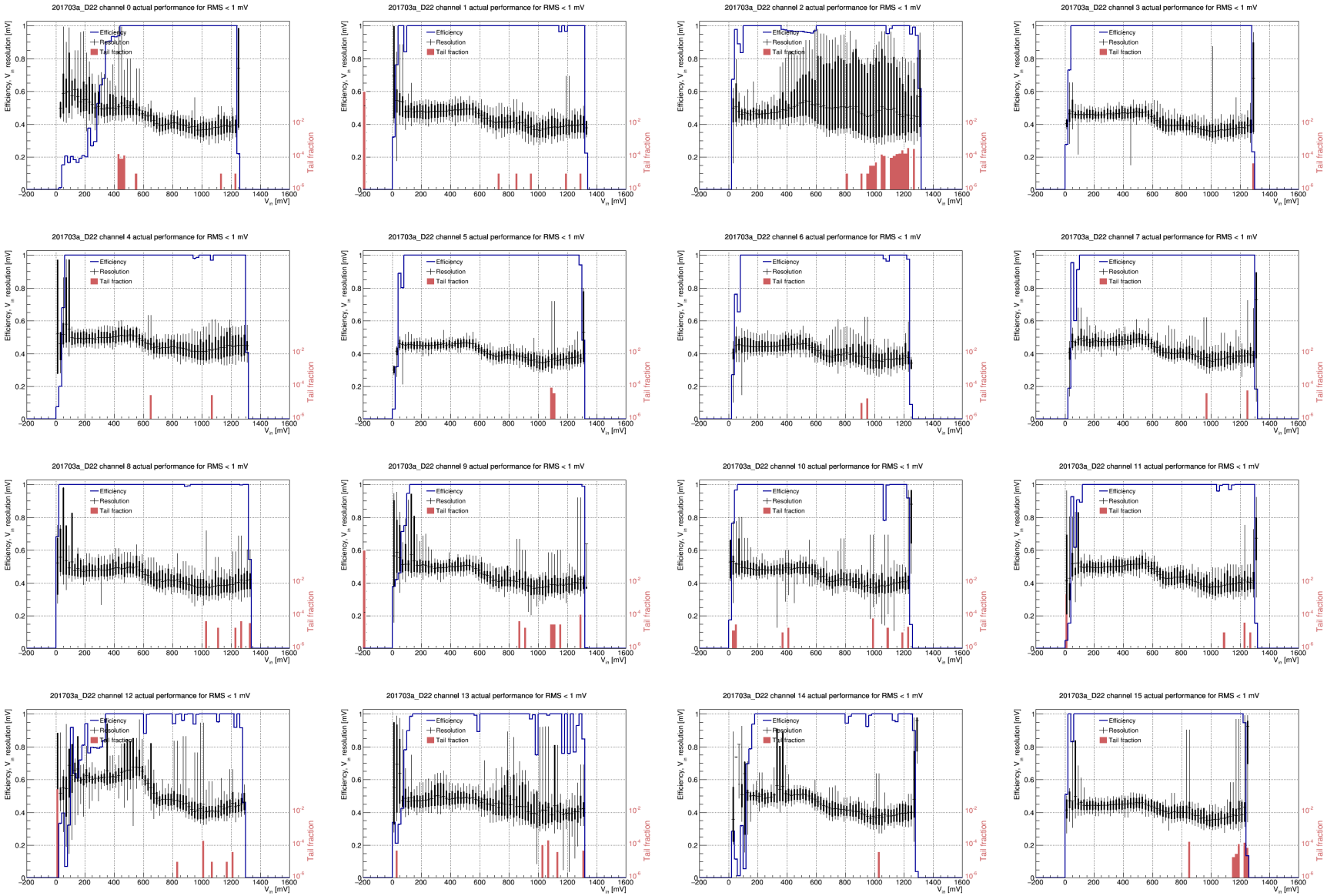
Chip D55 (rank=37, Q=0.863, a=0.991, m=0.942)



Chip D05 (rank=38, Q=0.857, a=0.990, m=0.934)

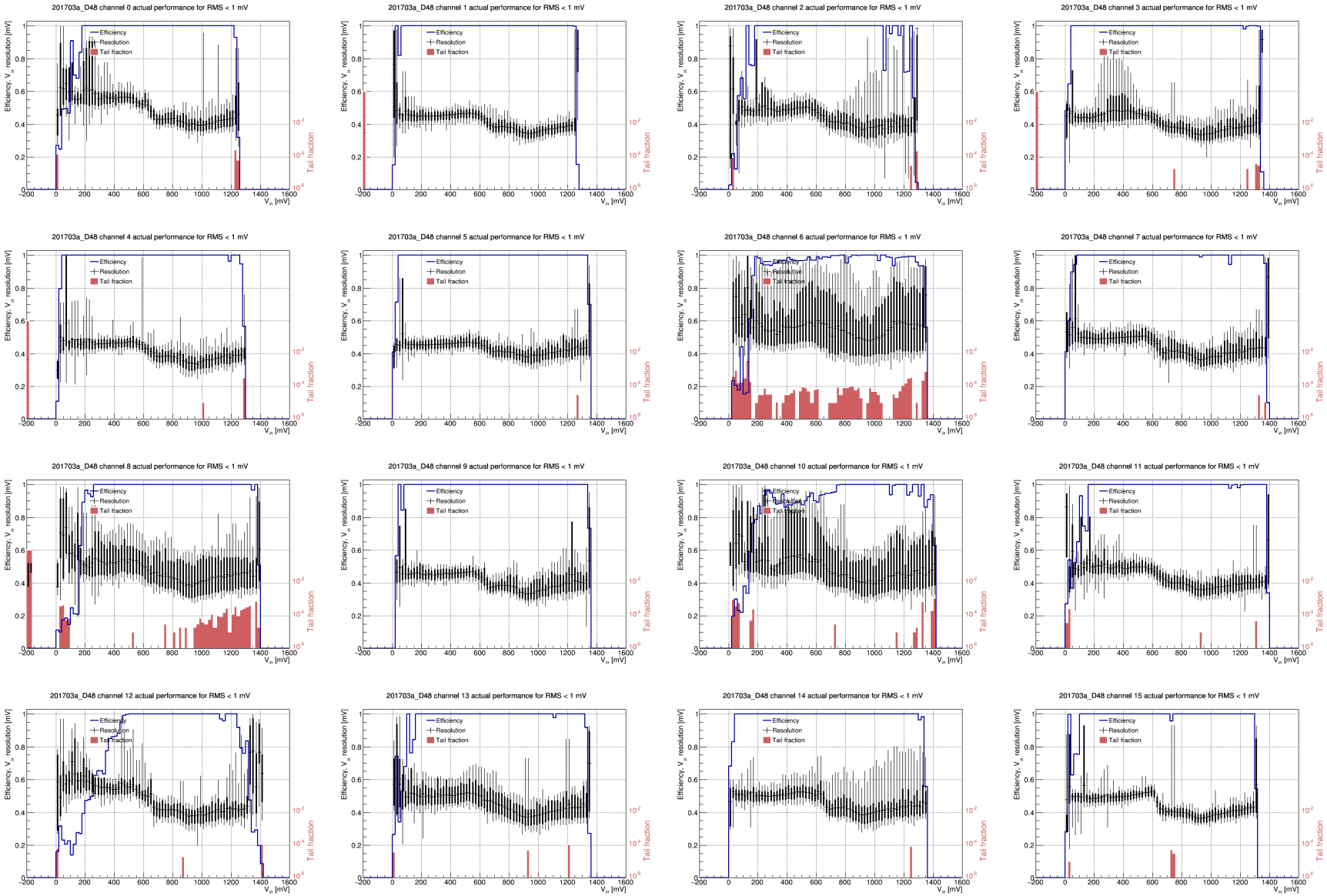


Chip D22 (rank=39, Q=0.850, a=0.990, m=0.912)

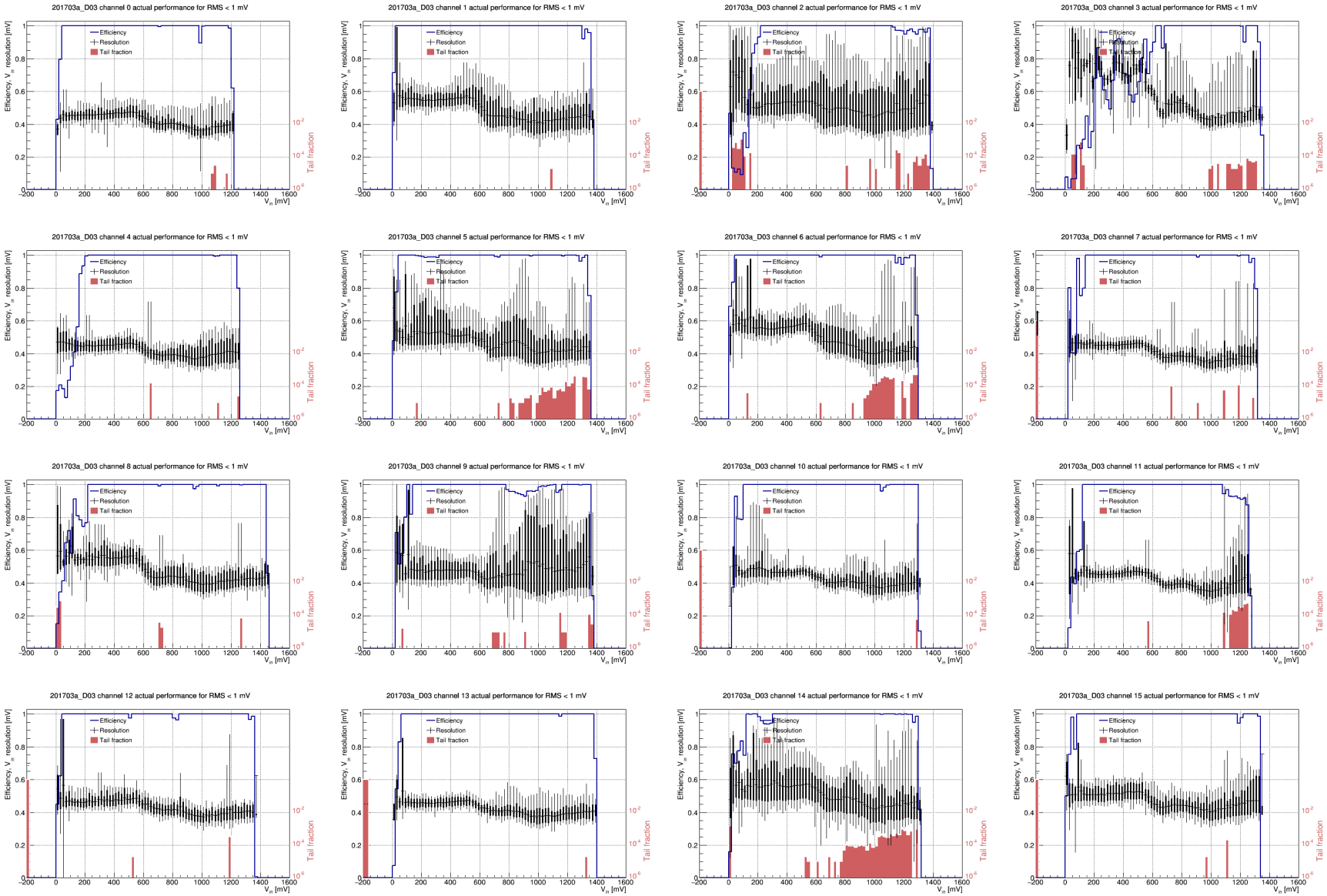


Poor chips

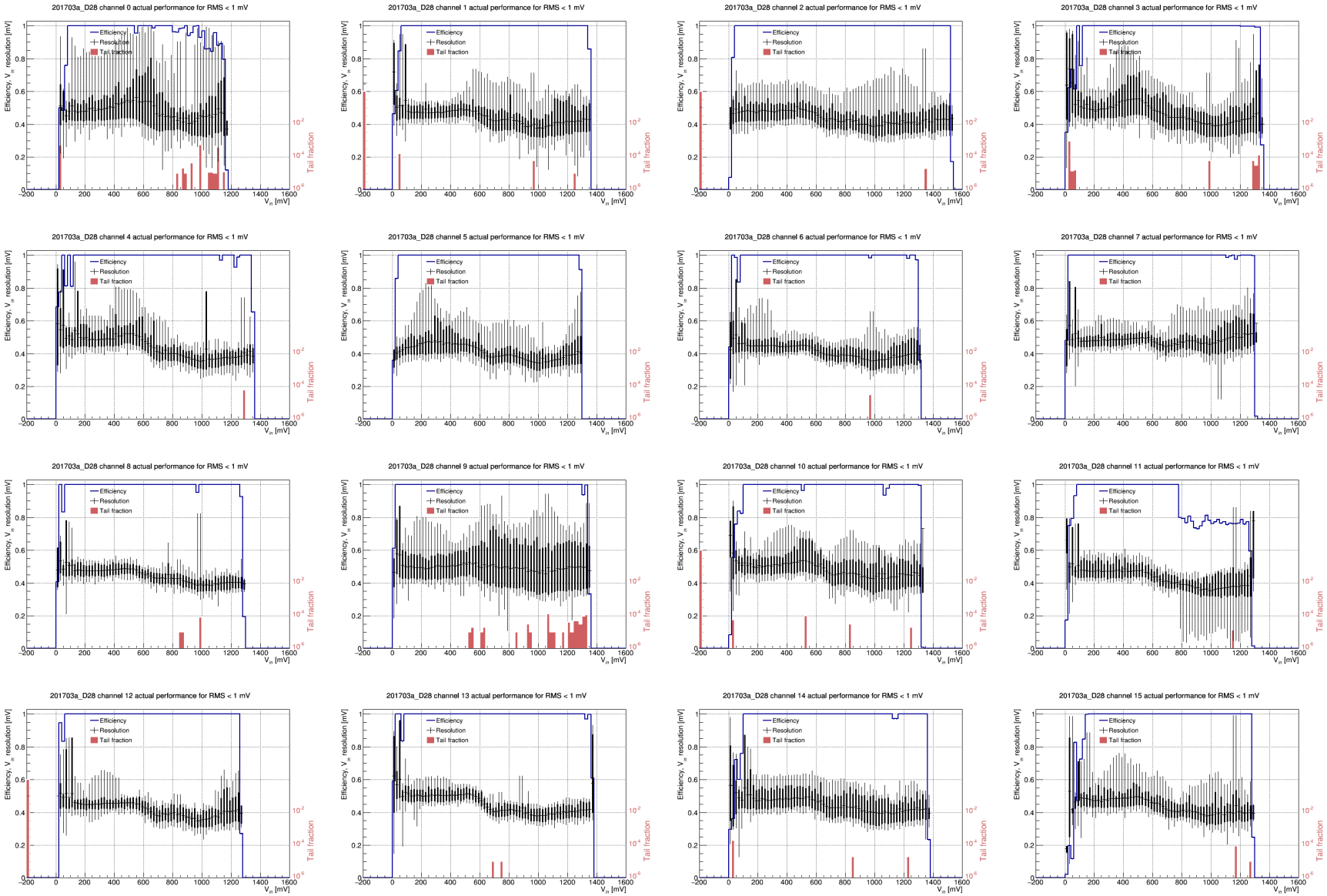
Chip D48 (rank=40, Q=0.845, a=0.989, m=0.922)



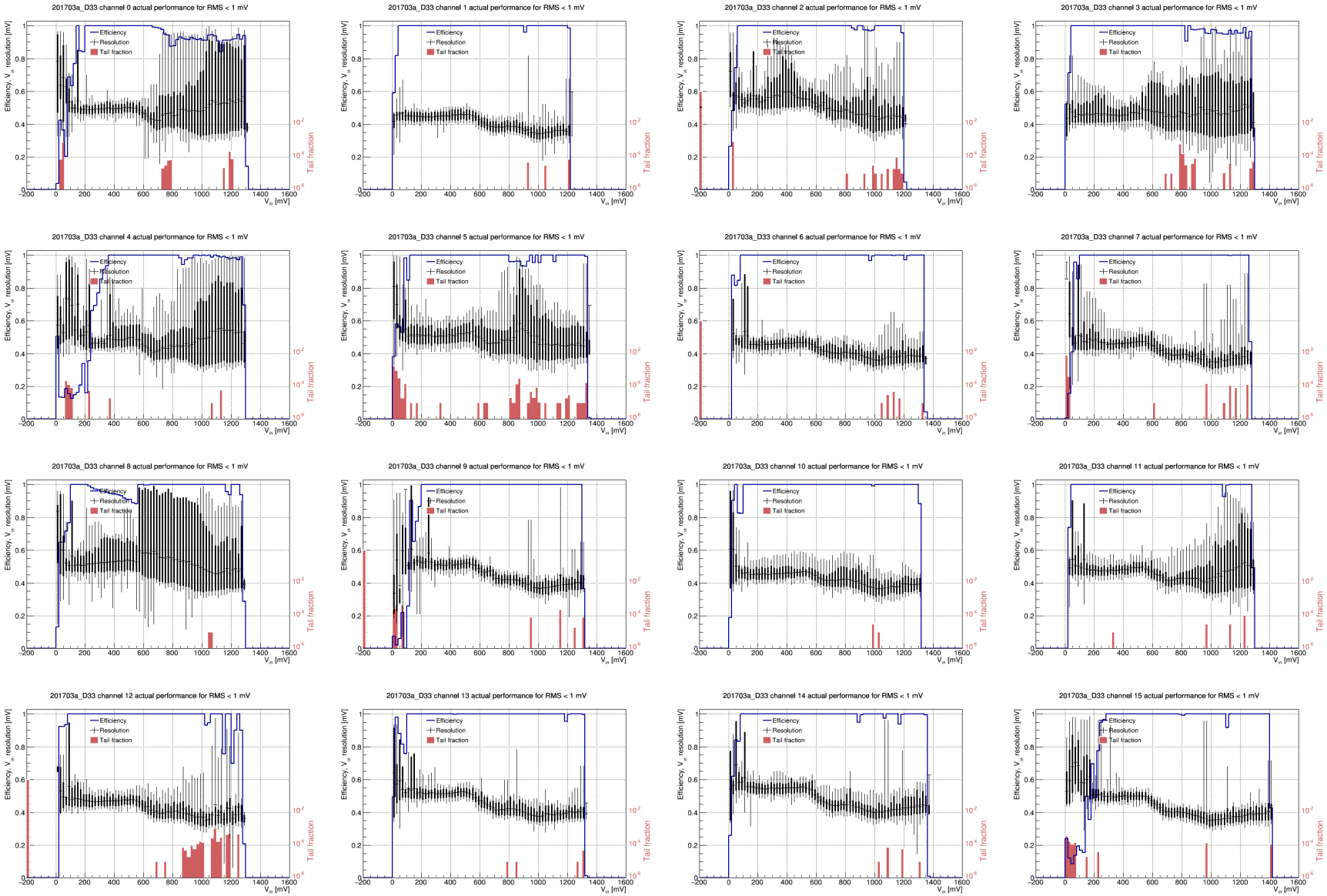
Chip D03 (rank=41, Q=0.841, a=0.989, m=0.881)



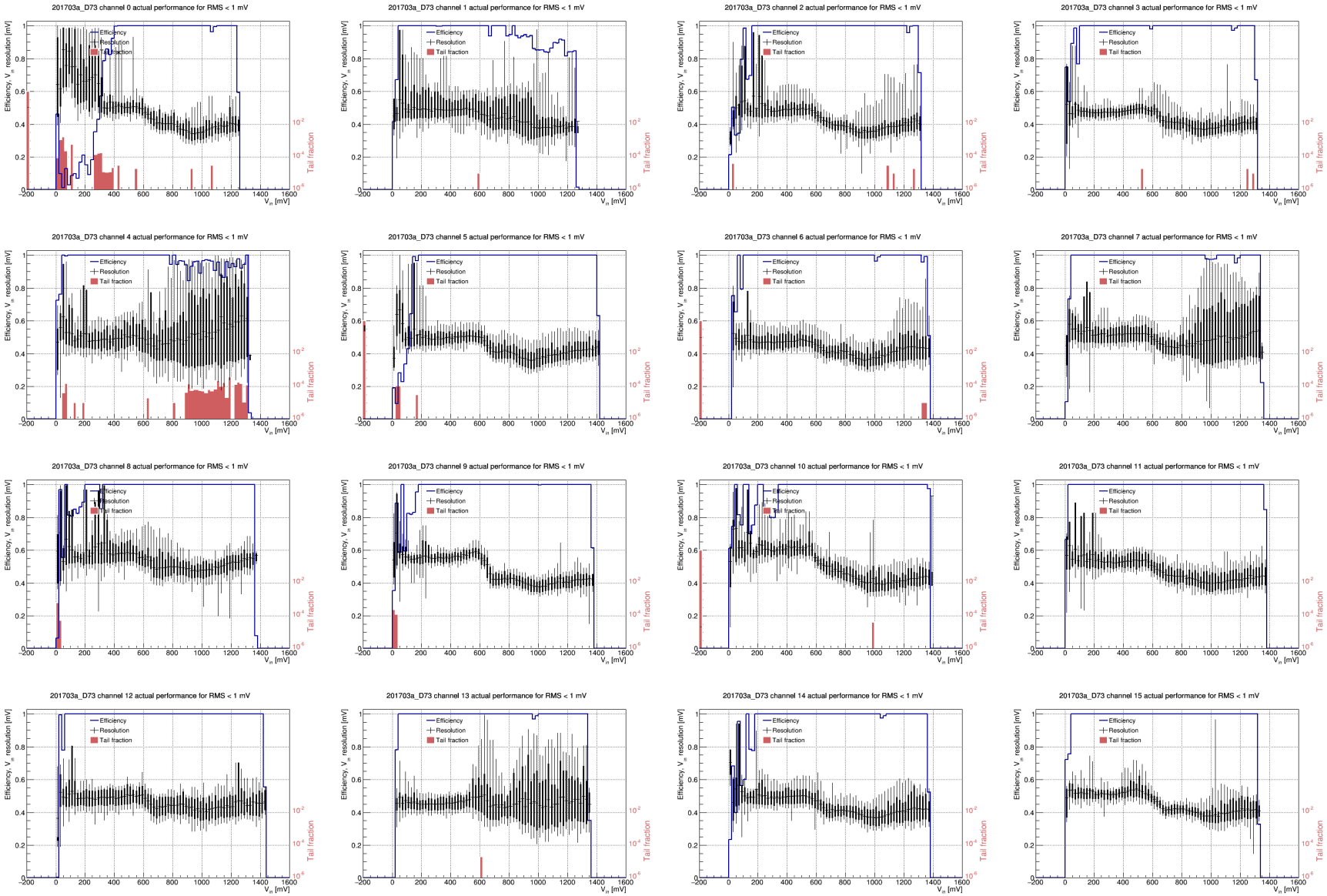
Chip D28 (rank=42, Q=0.841, a=0.989, m=0.903)



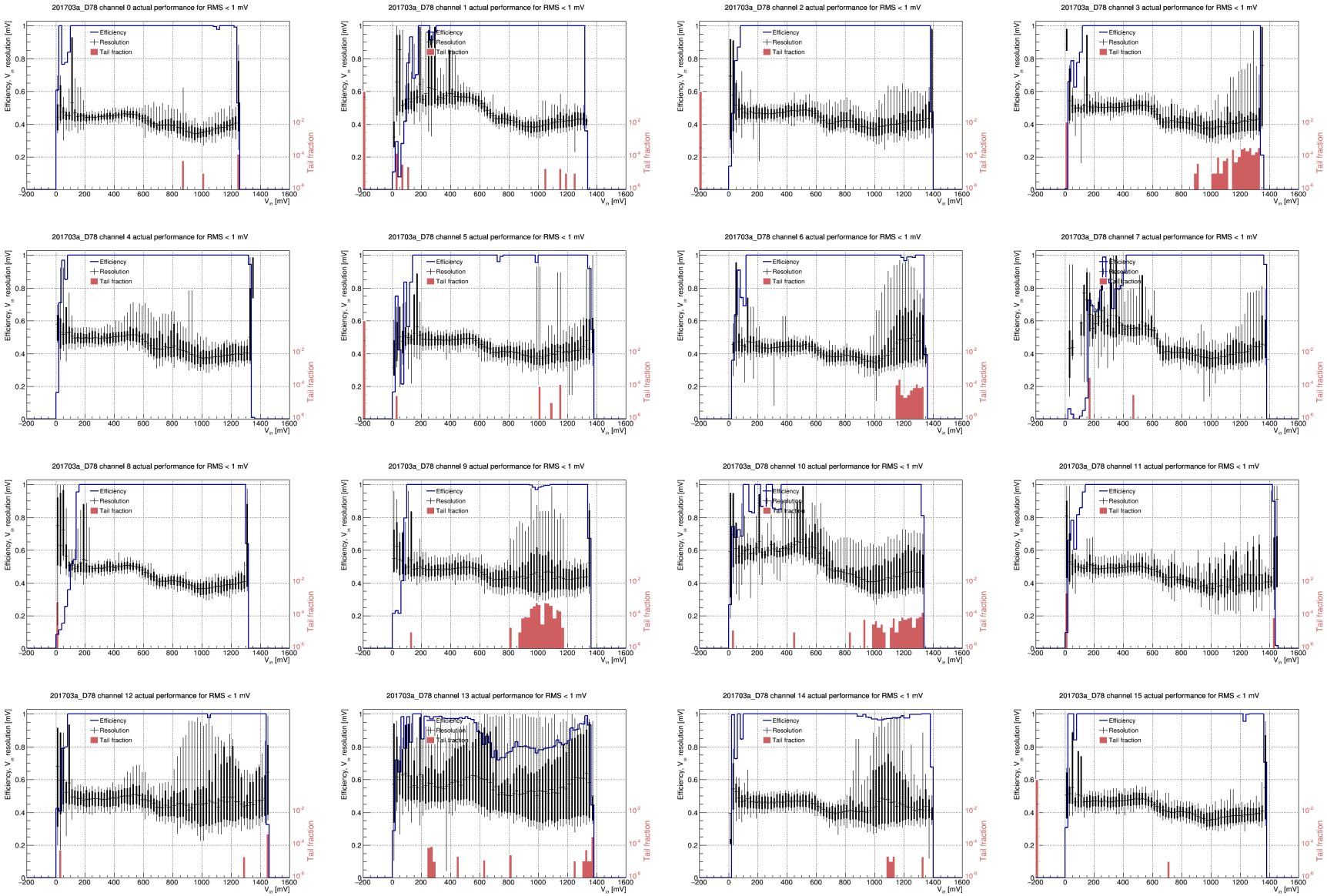
Chip D33 (rank=43, Q=0.833, a=0.988, m=0.942)



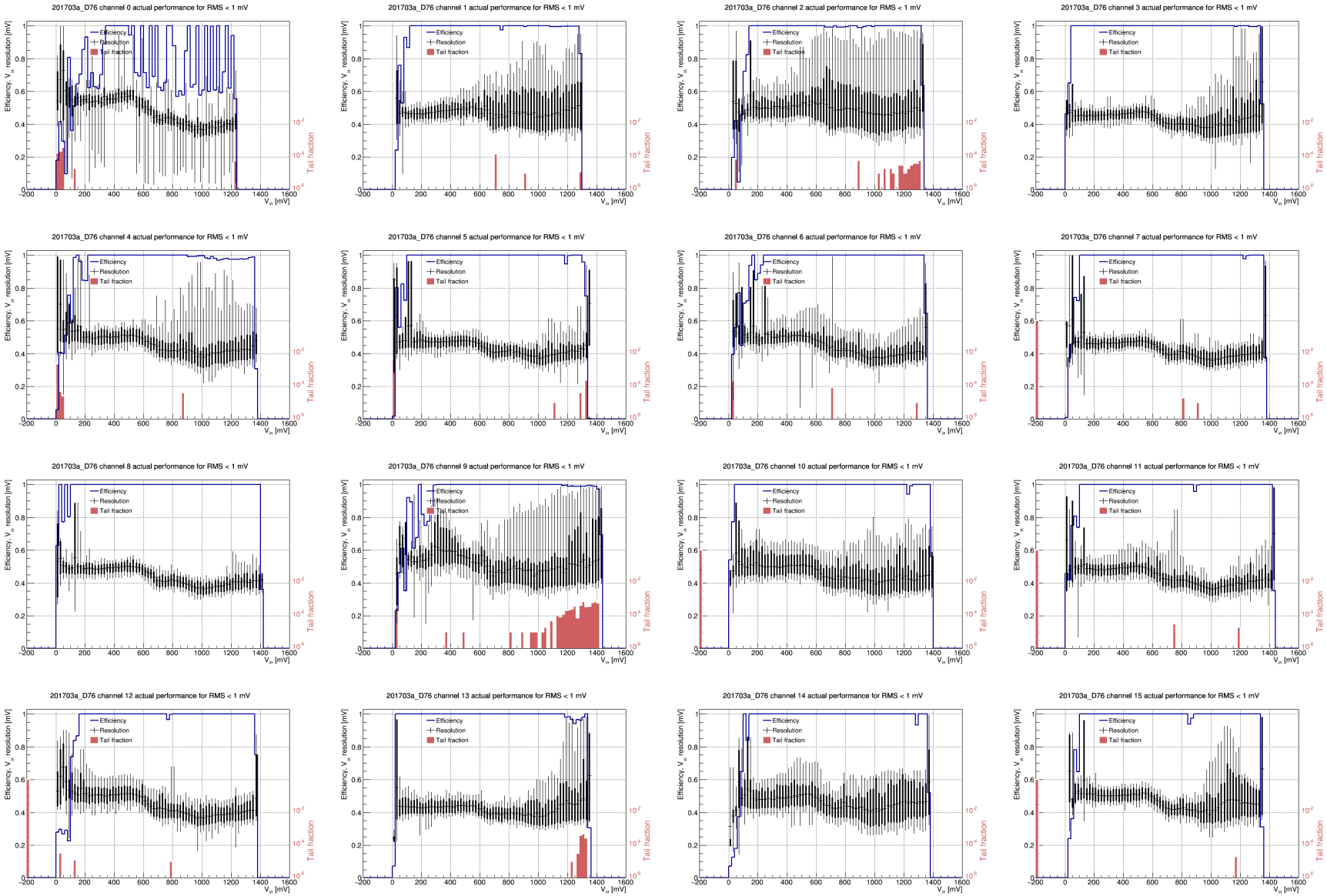
Chip D73 (rank=44, Q=0.818, a=0.987, m=0.902)



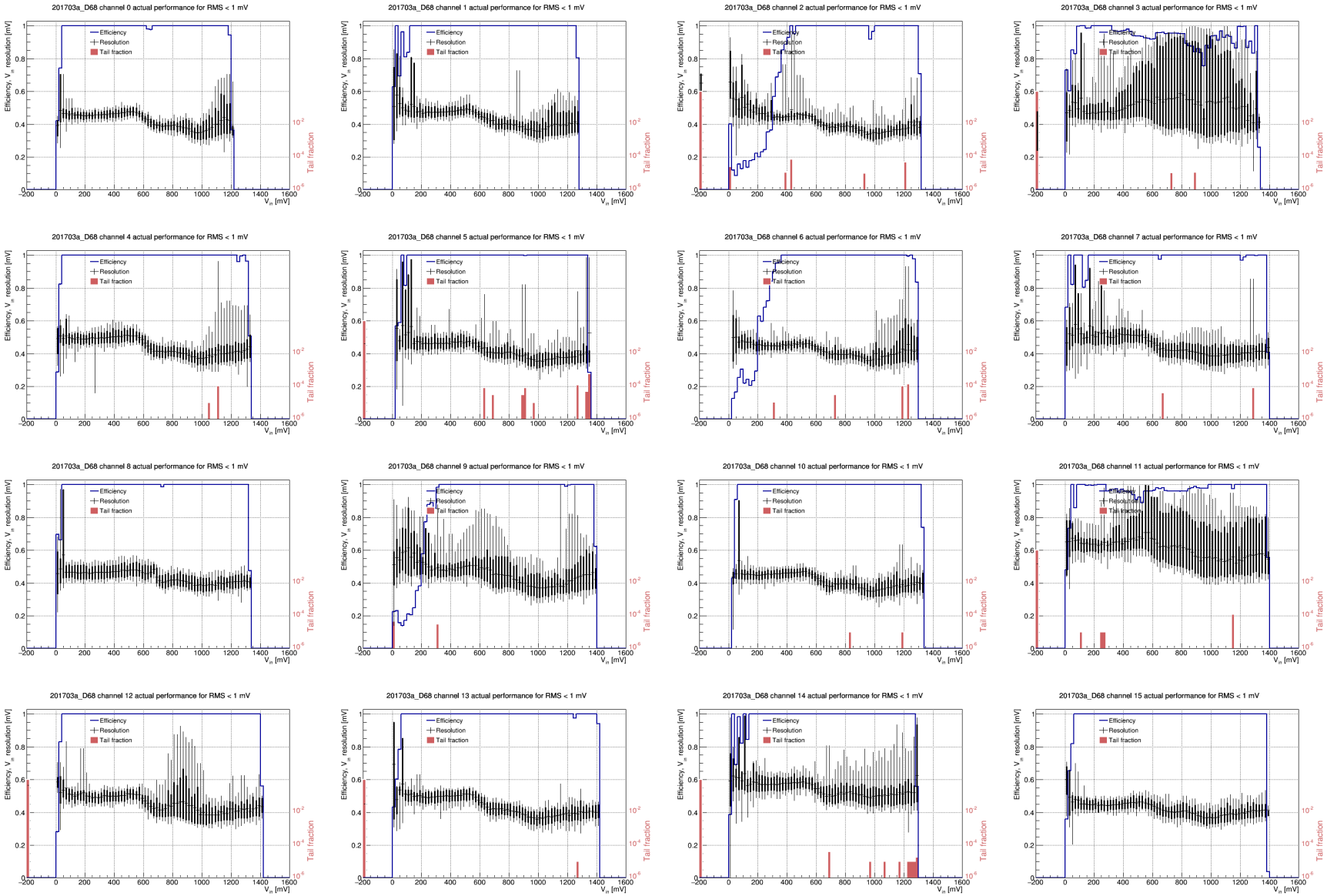
Chip D78 (rank=45, Q=0.799, a=0.986, m=0.862)



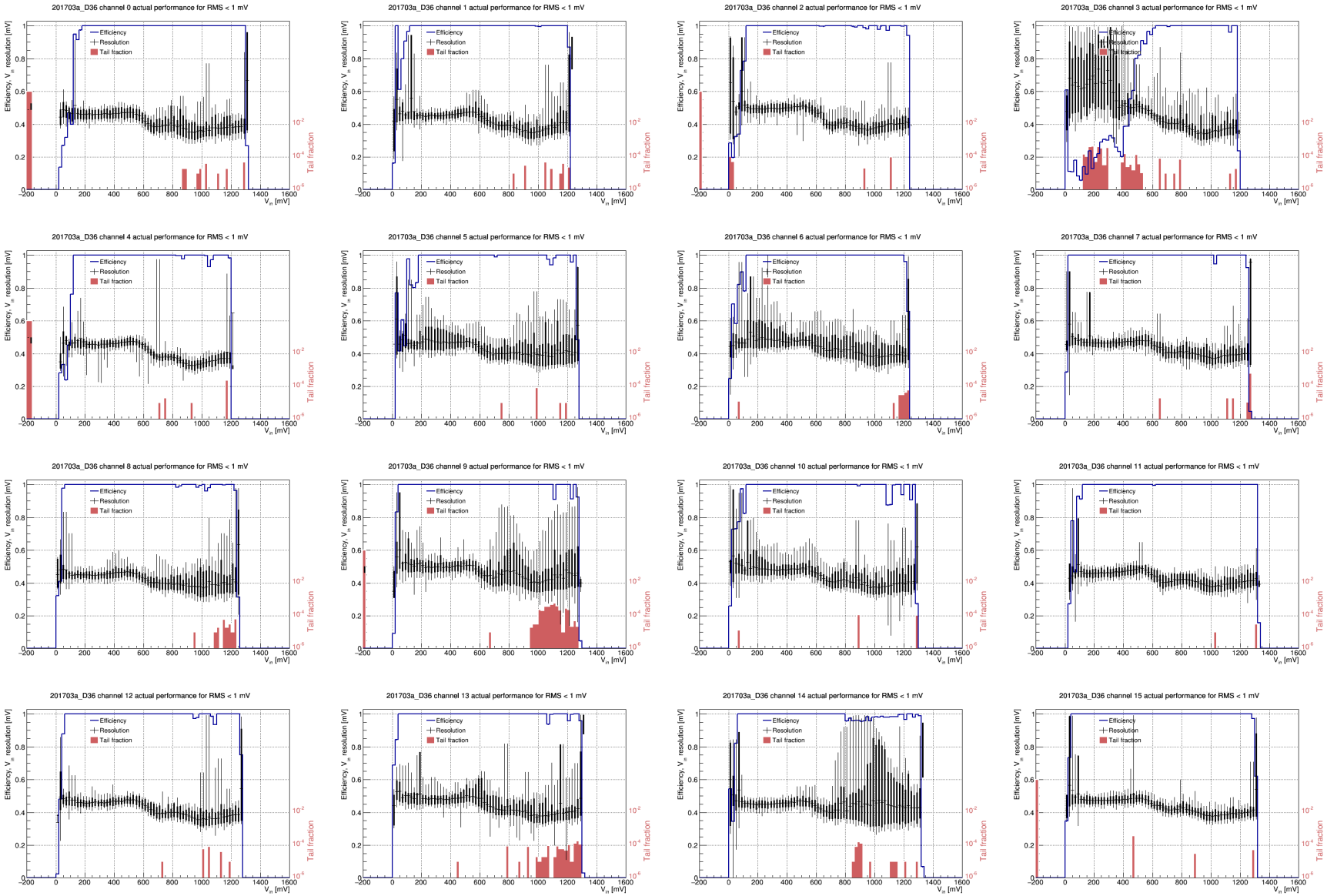
Chip D76 (rank=46, Q=0.780, a=0.985, m=0.808)



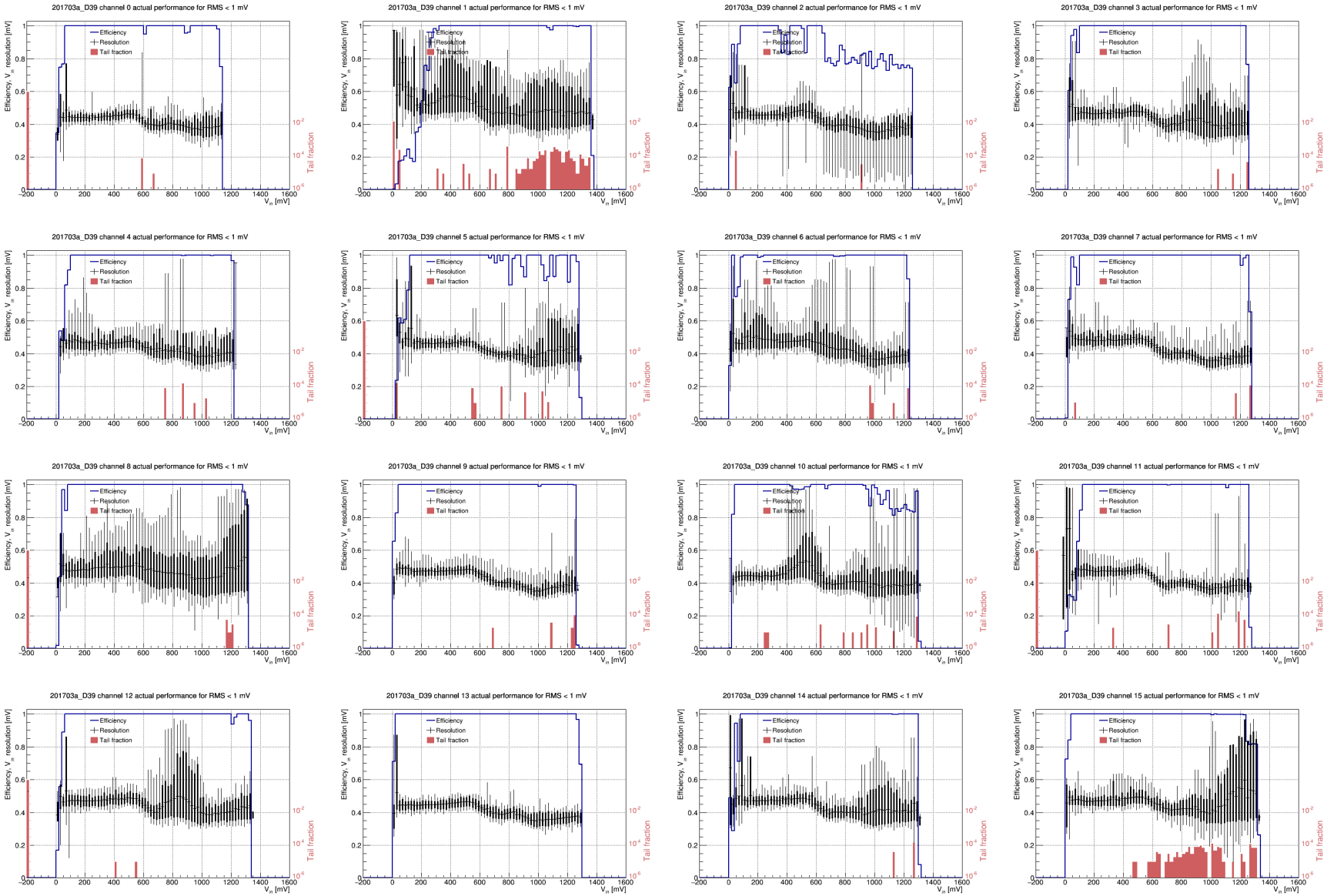
Chip D68 (rank=47, Q=0.770, a=0.984, m=0.897)



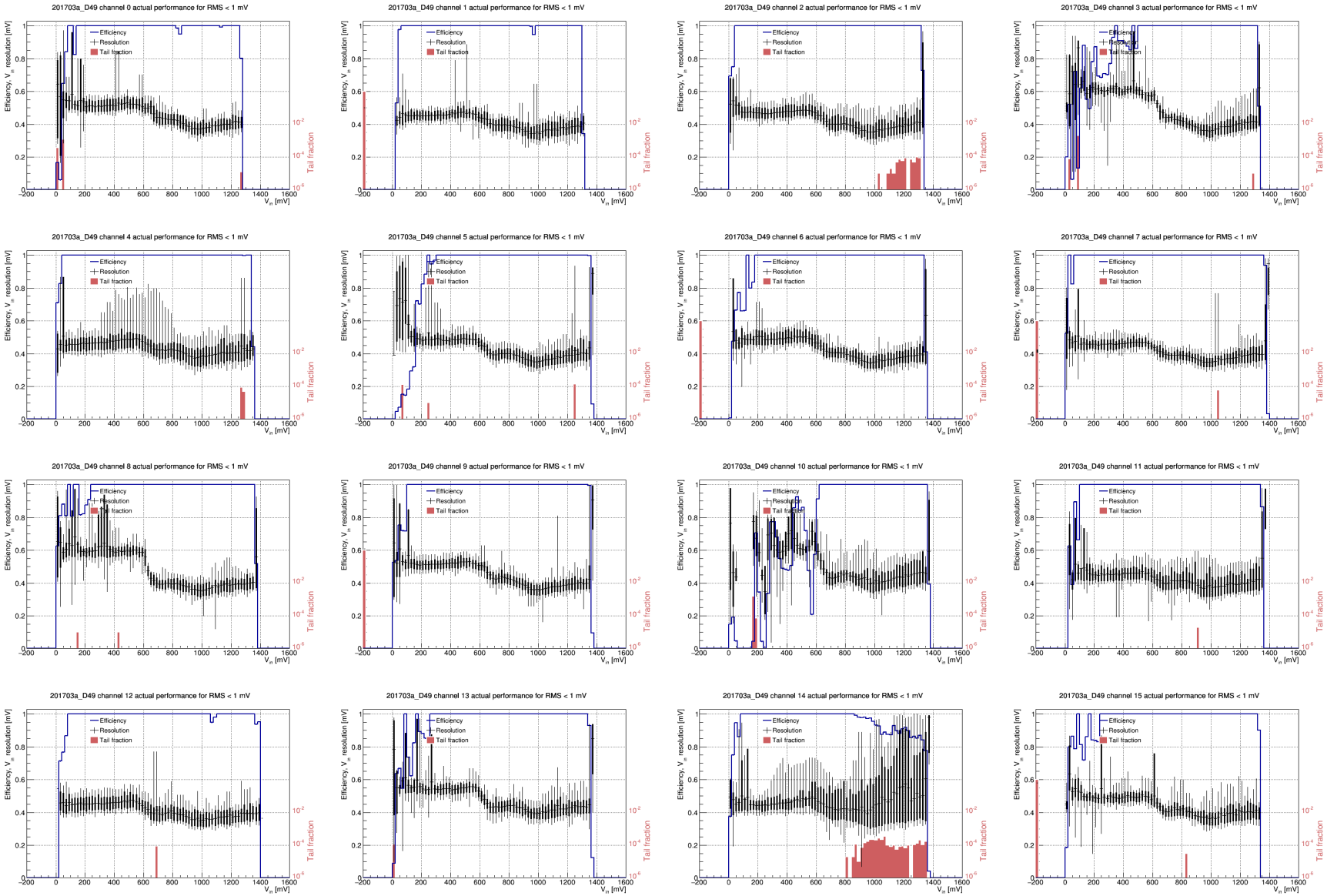
Chip D36 (rank=48, Q=0.757, a=0.984, m=0.782)



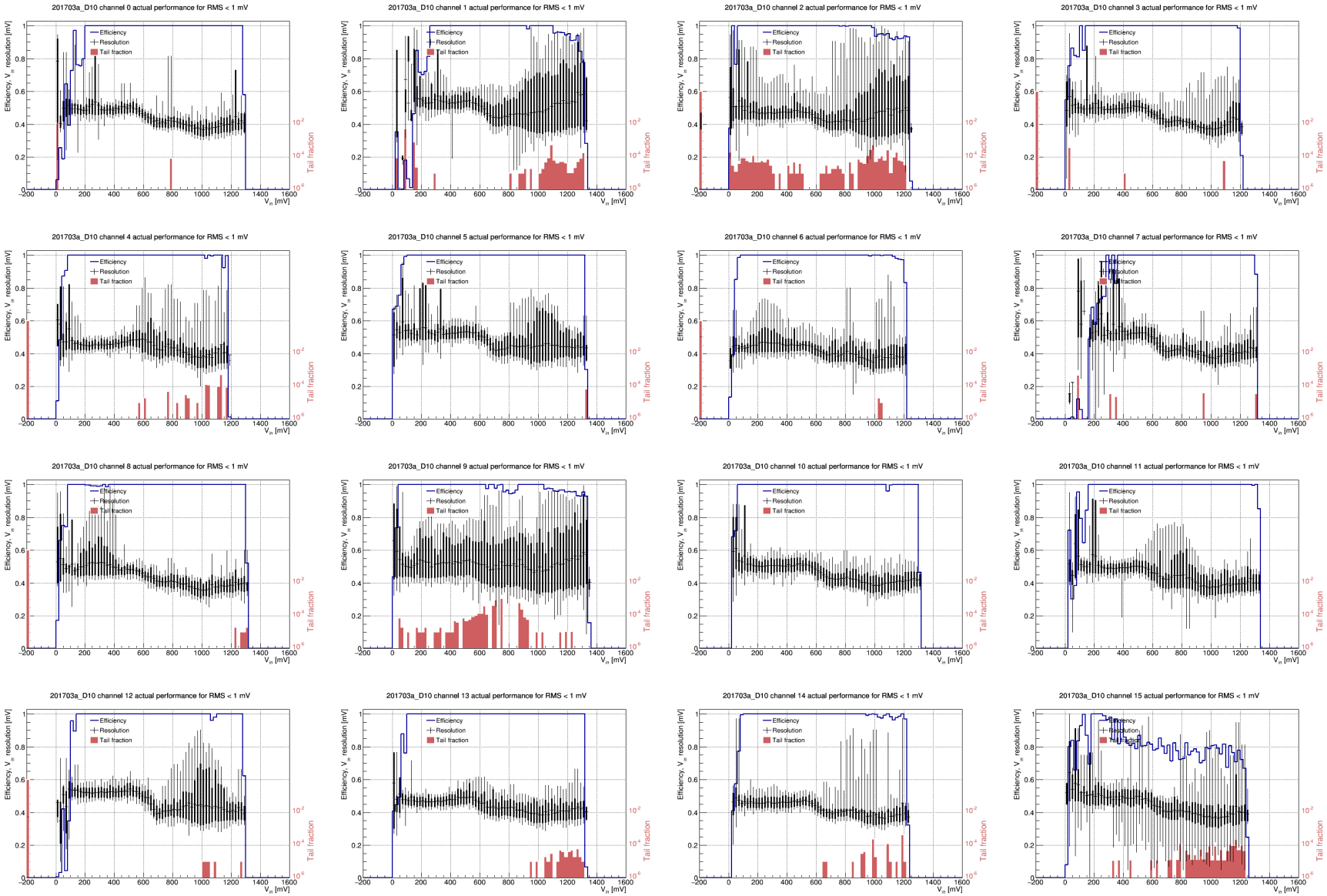
Chip D39 (rank=49, Q=0.754, a=0.983, m=0.872)



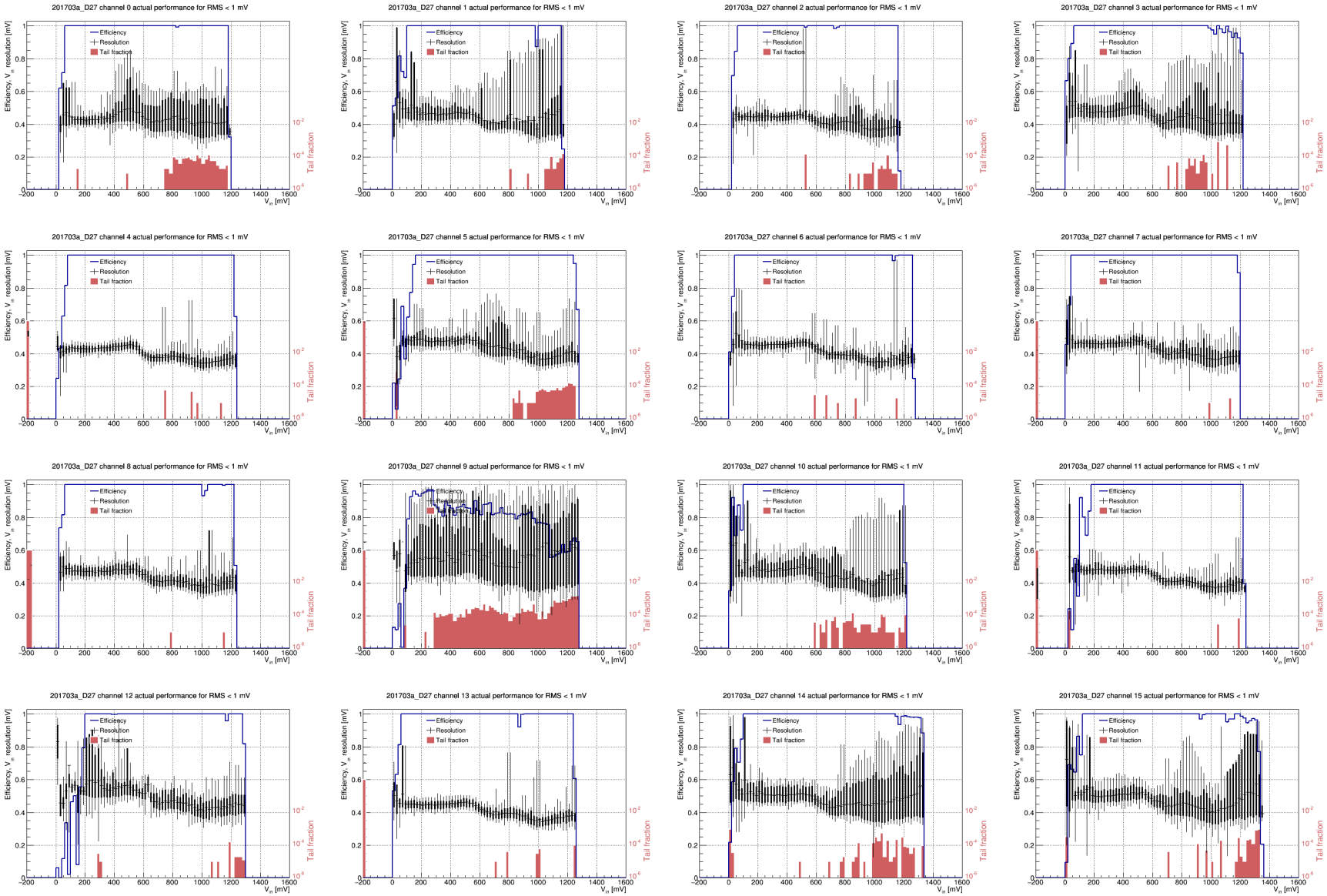
Chip D49 (rank=50, Q=0.736, a=0.982, m=0.816)



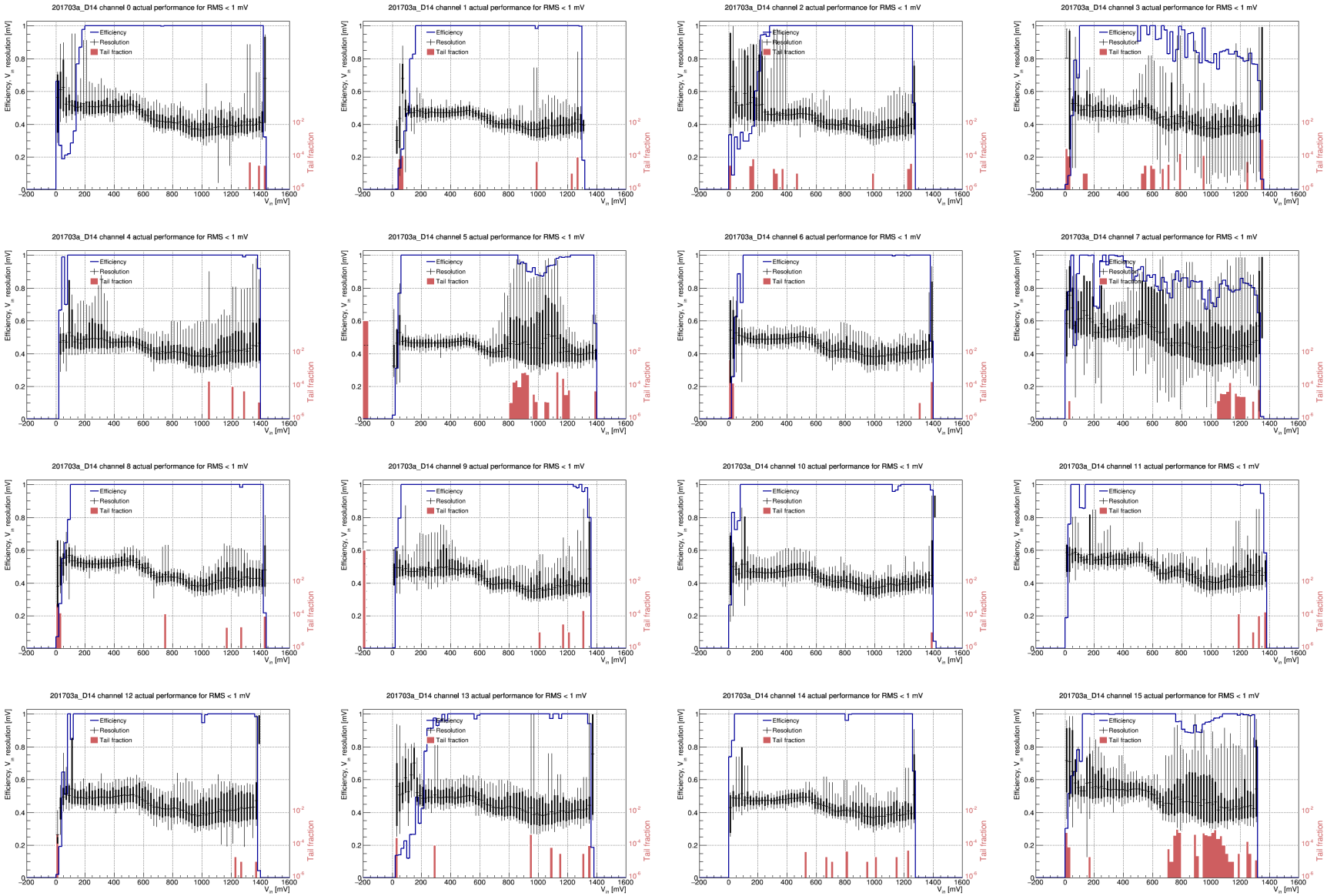
Chip D10 (rank=51, Q=0.735, a=0.982, m=0.818)



Chip D27 (rank=52, Q=0.726, a=0.981, m=0.812)

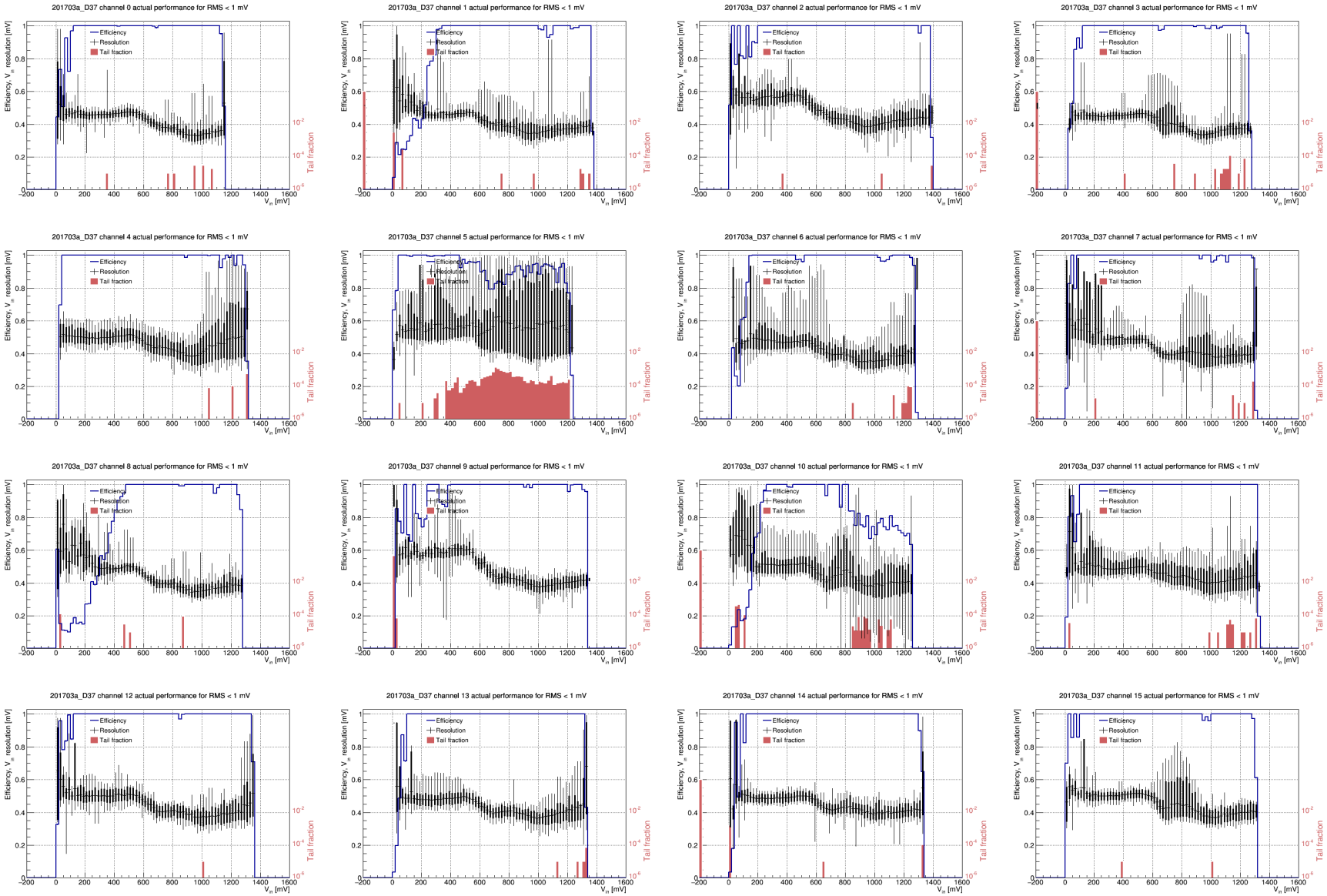


Chip D14 (rank=53, Q=0.715, a=0.980, m=0.846)

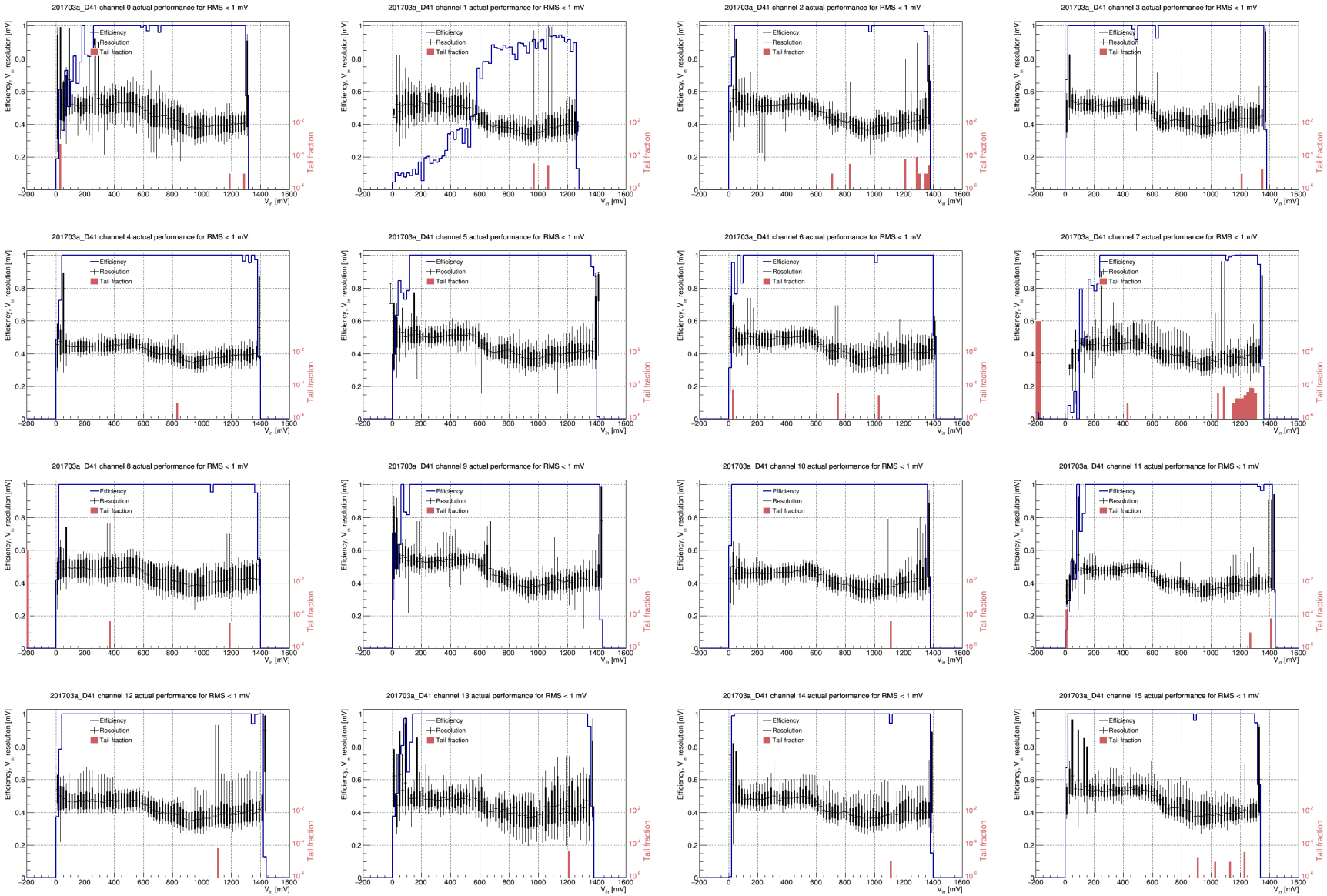


Bad chips

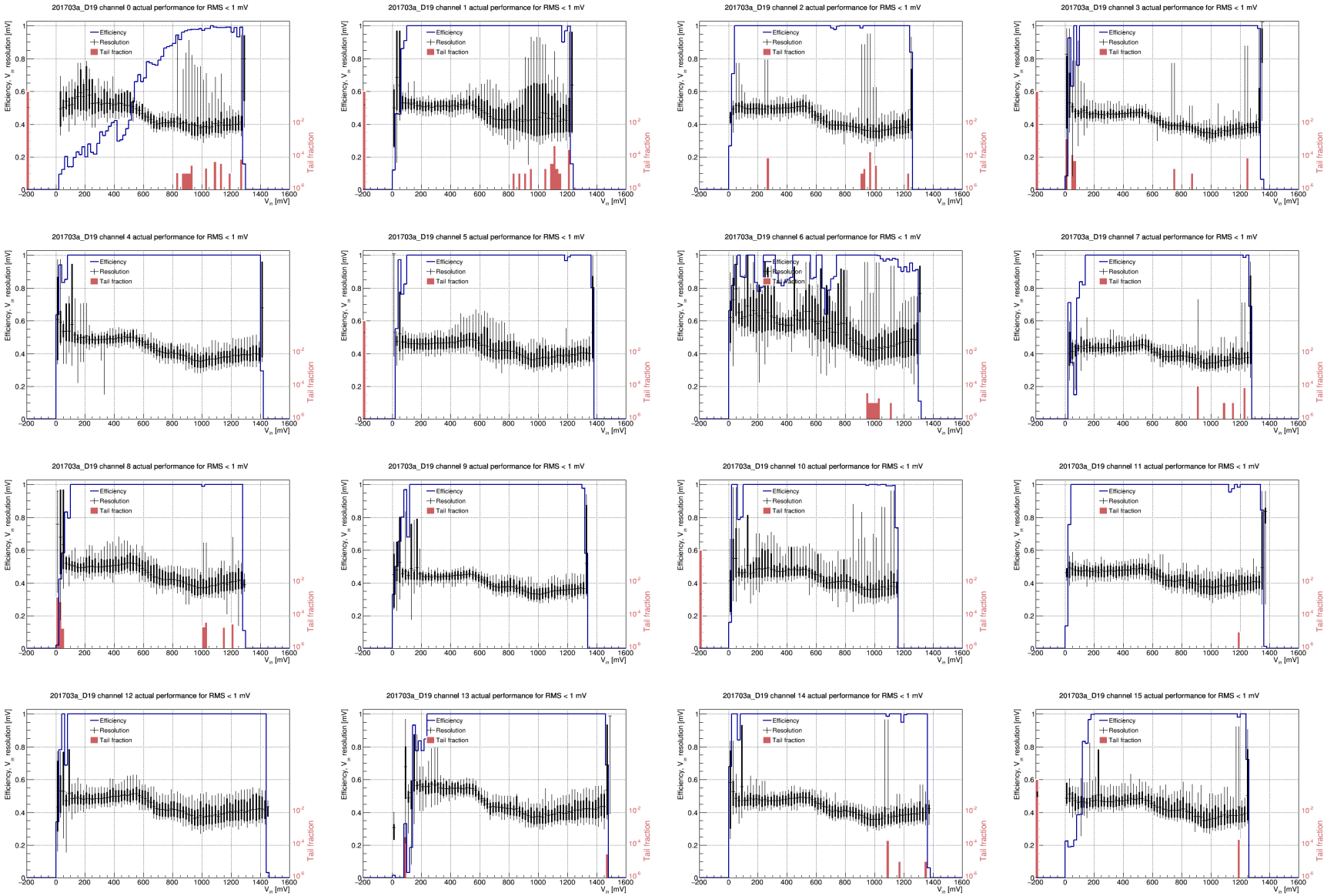
Chip D37 (rank=54, Q=0.652, a=0.974, m=0.890)



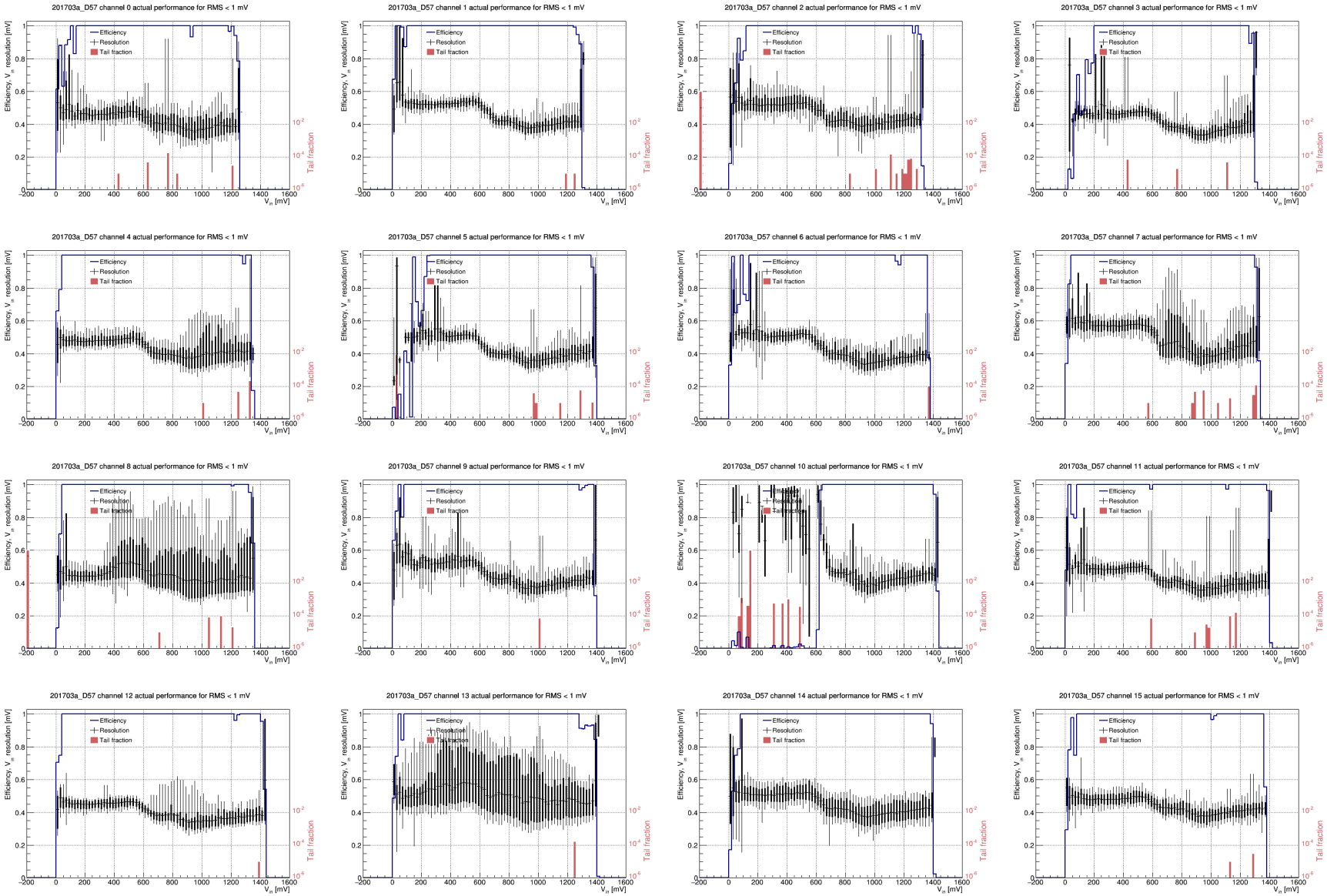
Chip D41 (rank=55, Q=0.621, a=0.975, m=0.640)



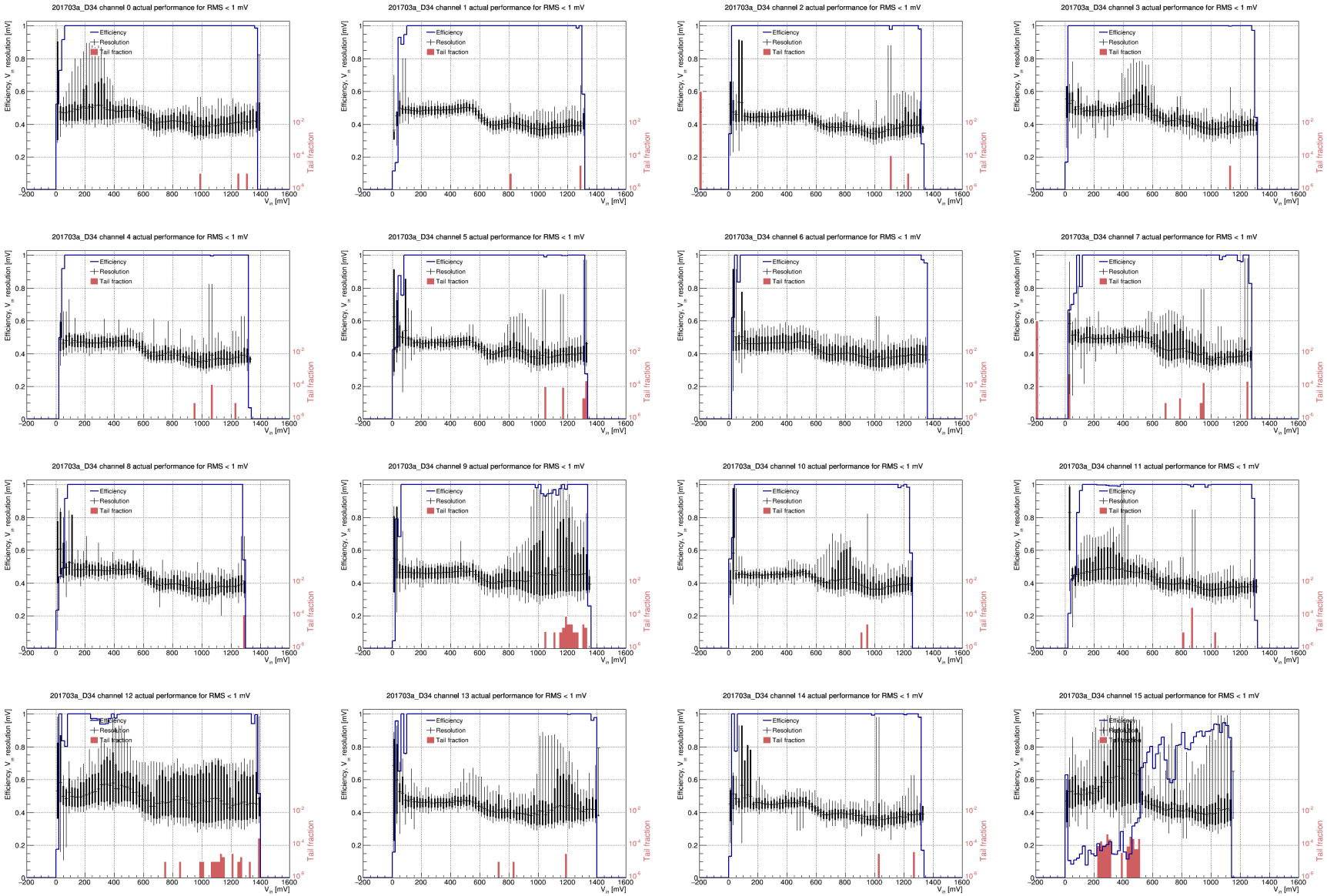
Chip D19 (rank=56, Q=0.621, a=0.973, m=0.703)



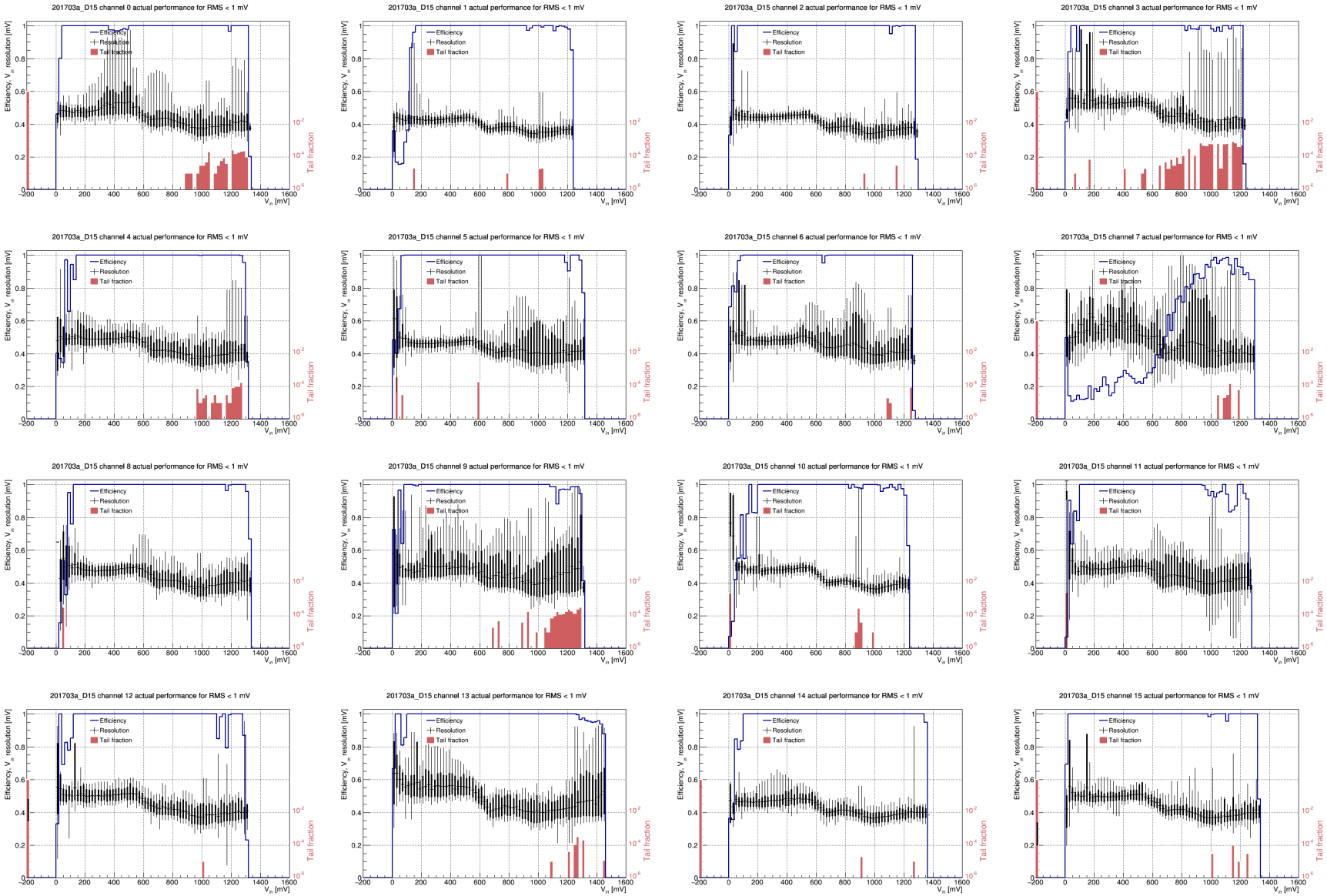
Chip D57 (rank=57, Q=0.575, a=0.973, m=0.584)



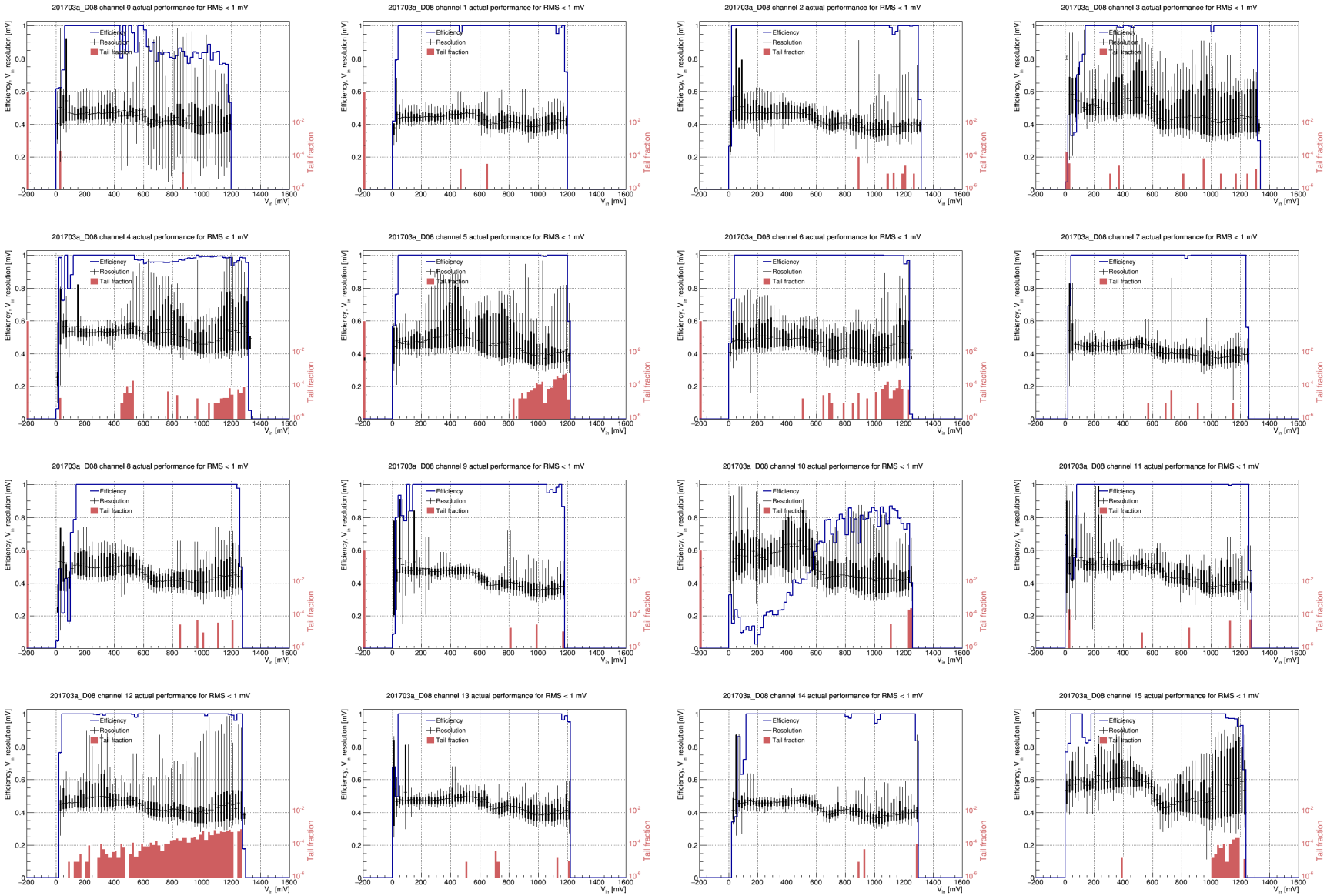
Chip D34 (rank=58, Q=0.557, a=0.971, m=0.568)



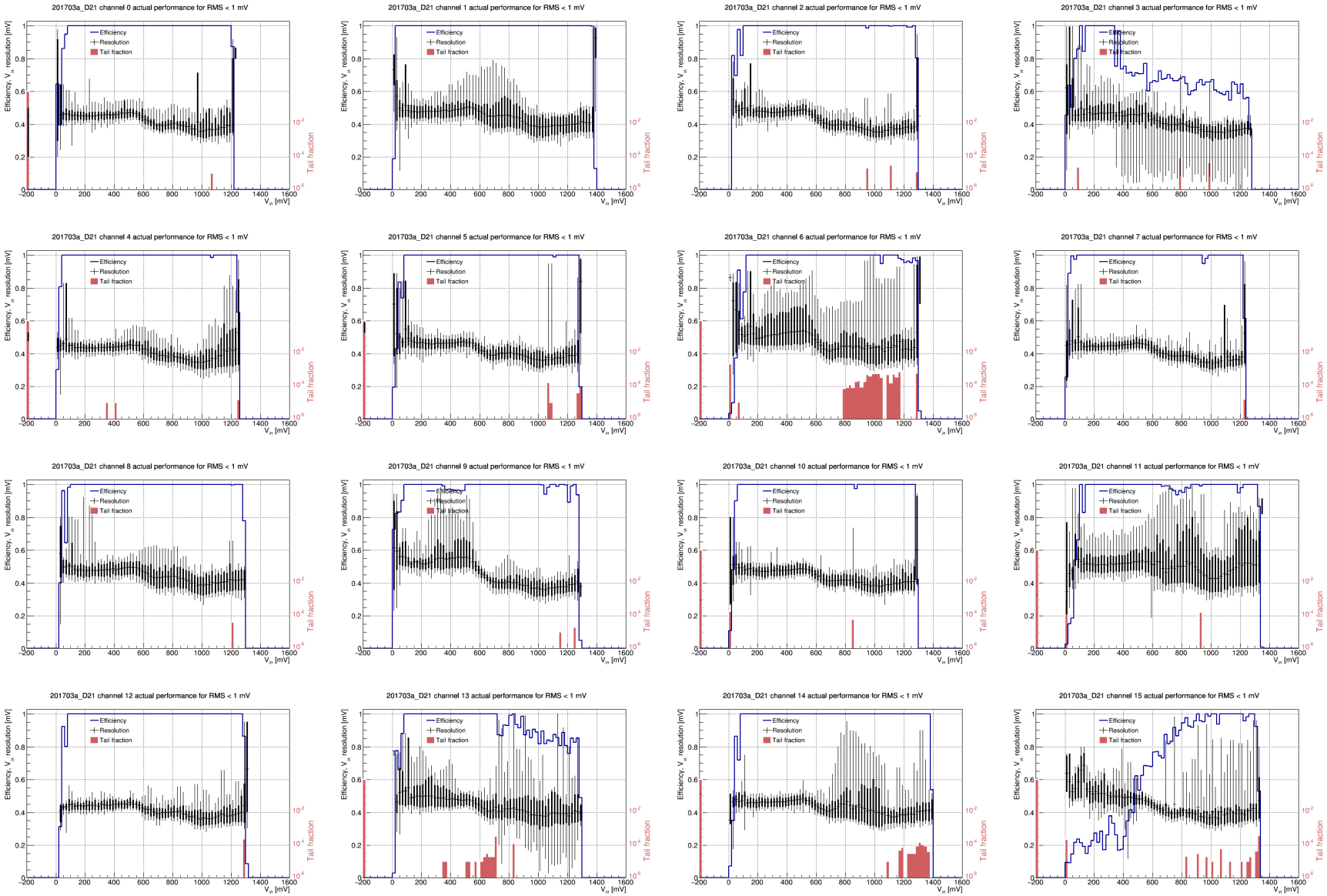
Chip D15 (rank=59, Q=0.533, a=0.969, m=0.560)



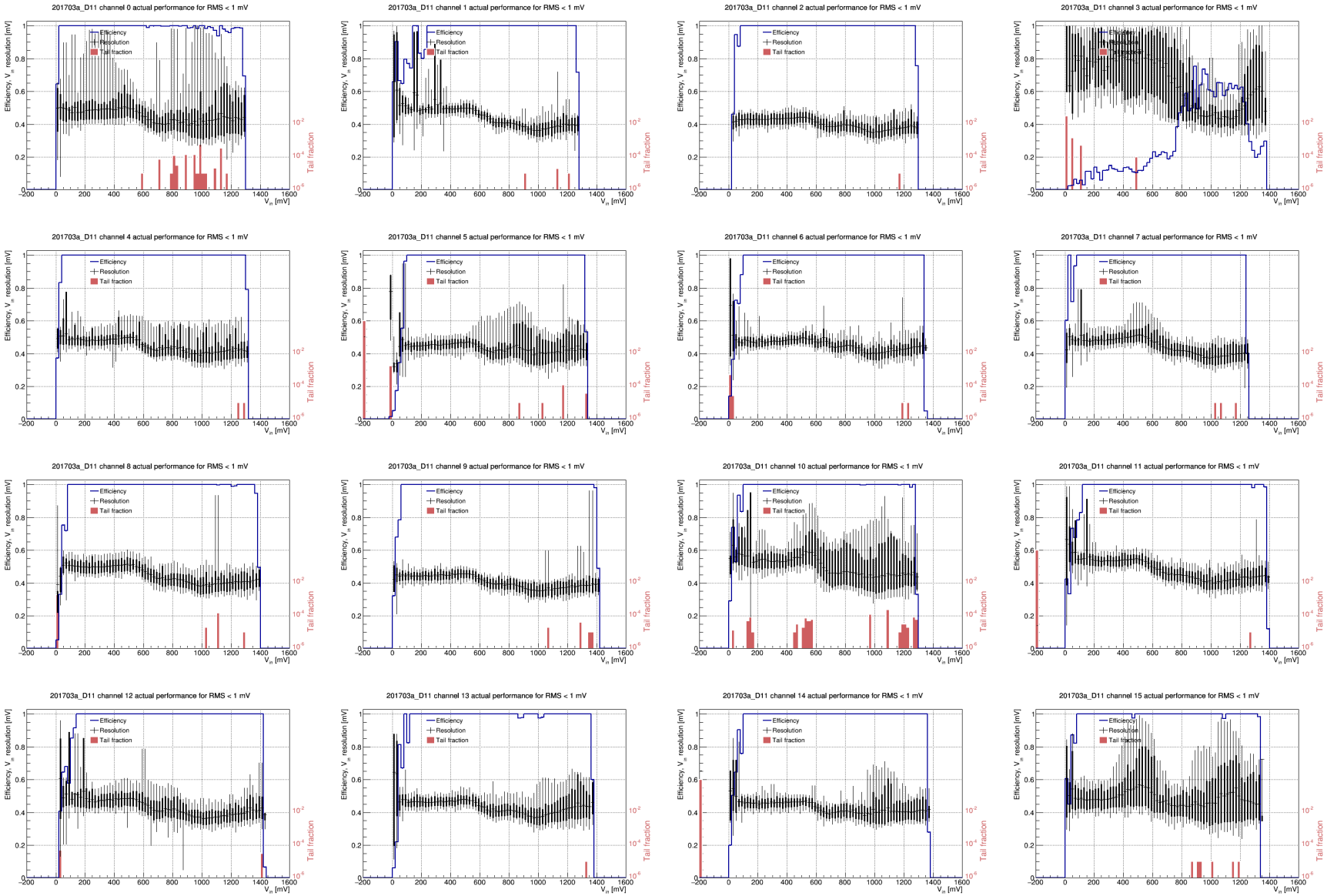
Chip D08 (rank=60, Q=0.486, a=0.962, m=0.589)



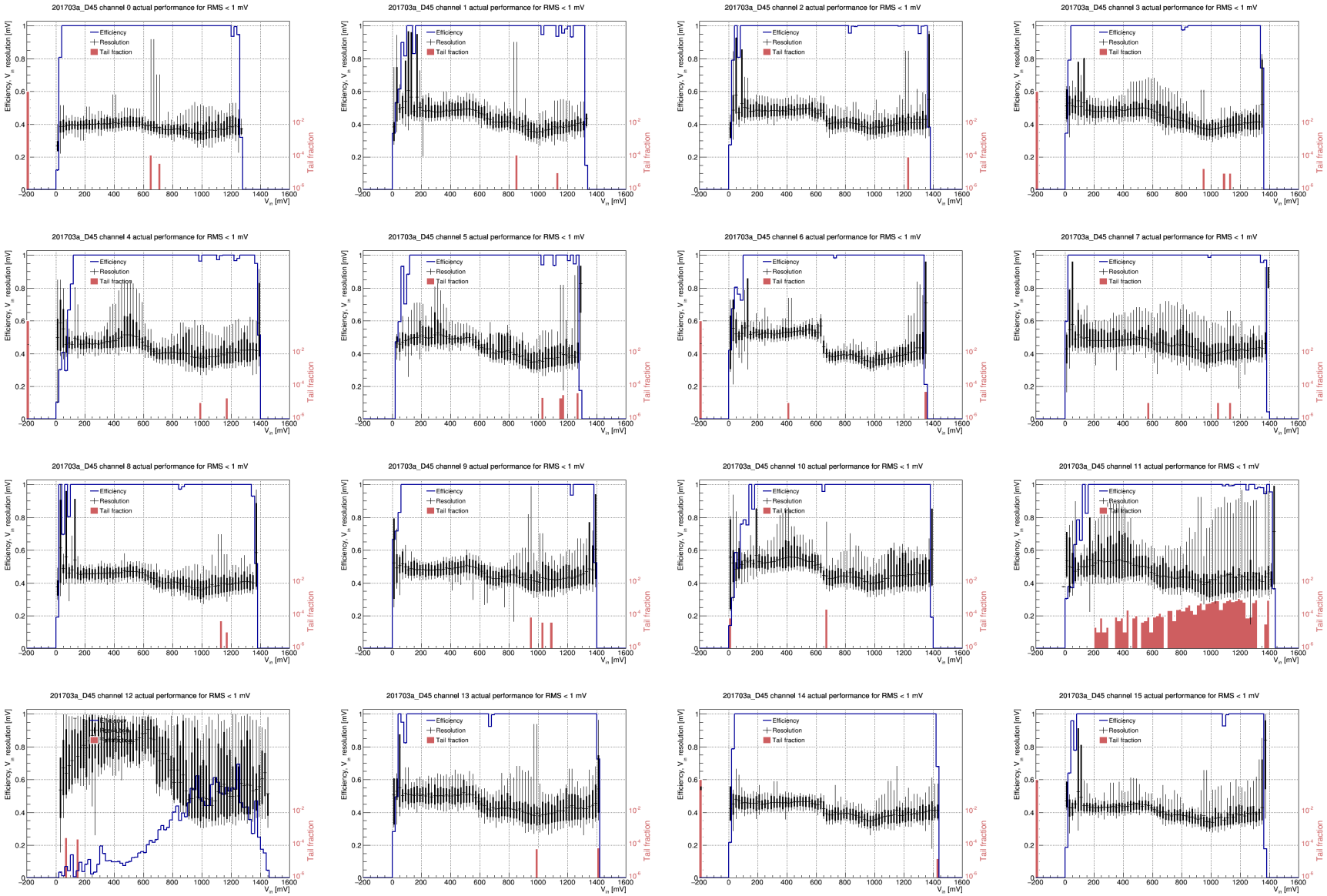
Chip D21 (rank=61, Q=0.472, a=0.959, m=0.711)



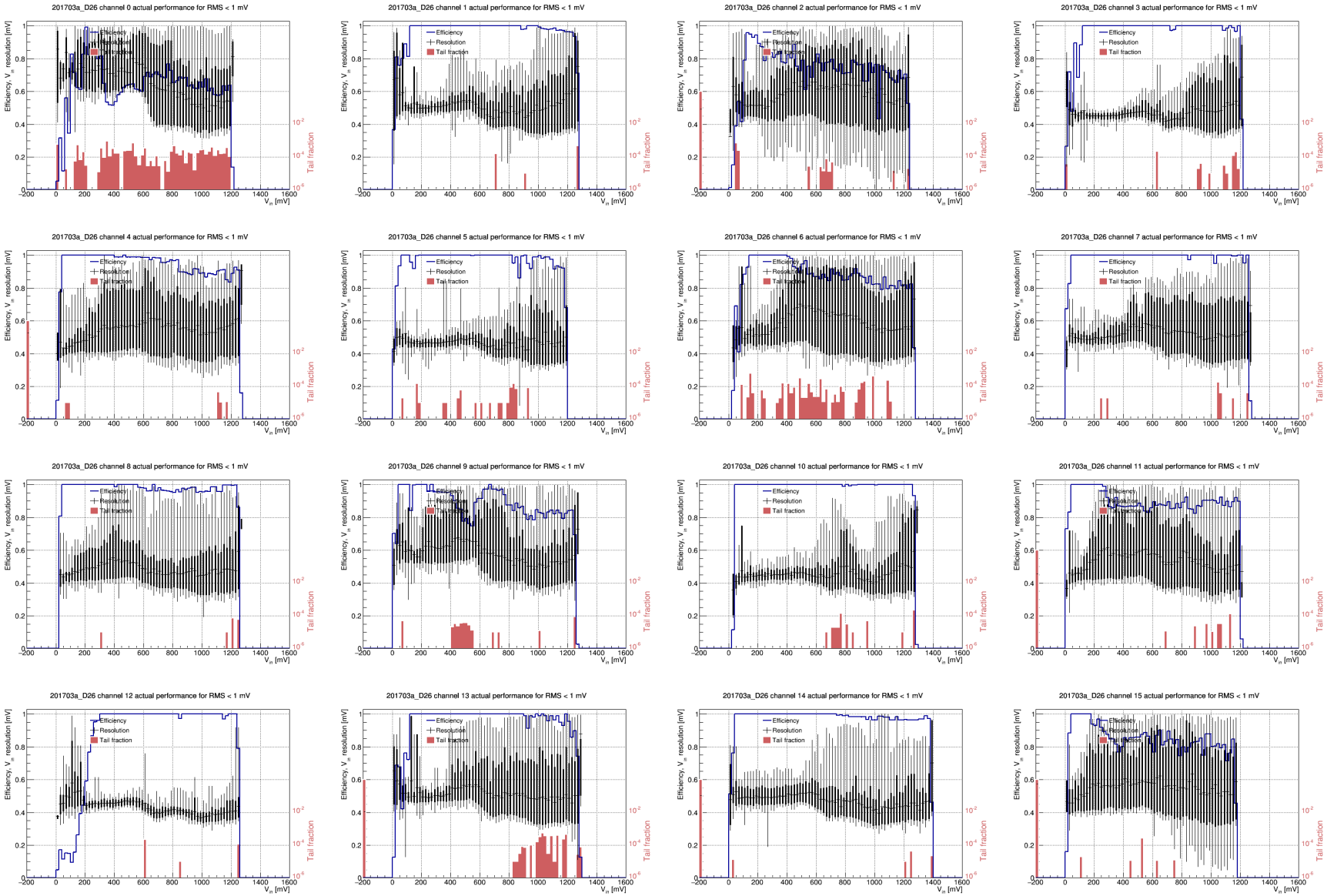
Chip D11 (rank=62, Q=0.340, a=0.958, m=0.345)



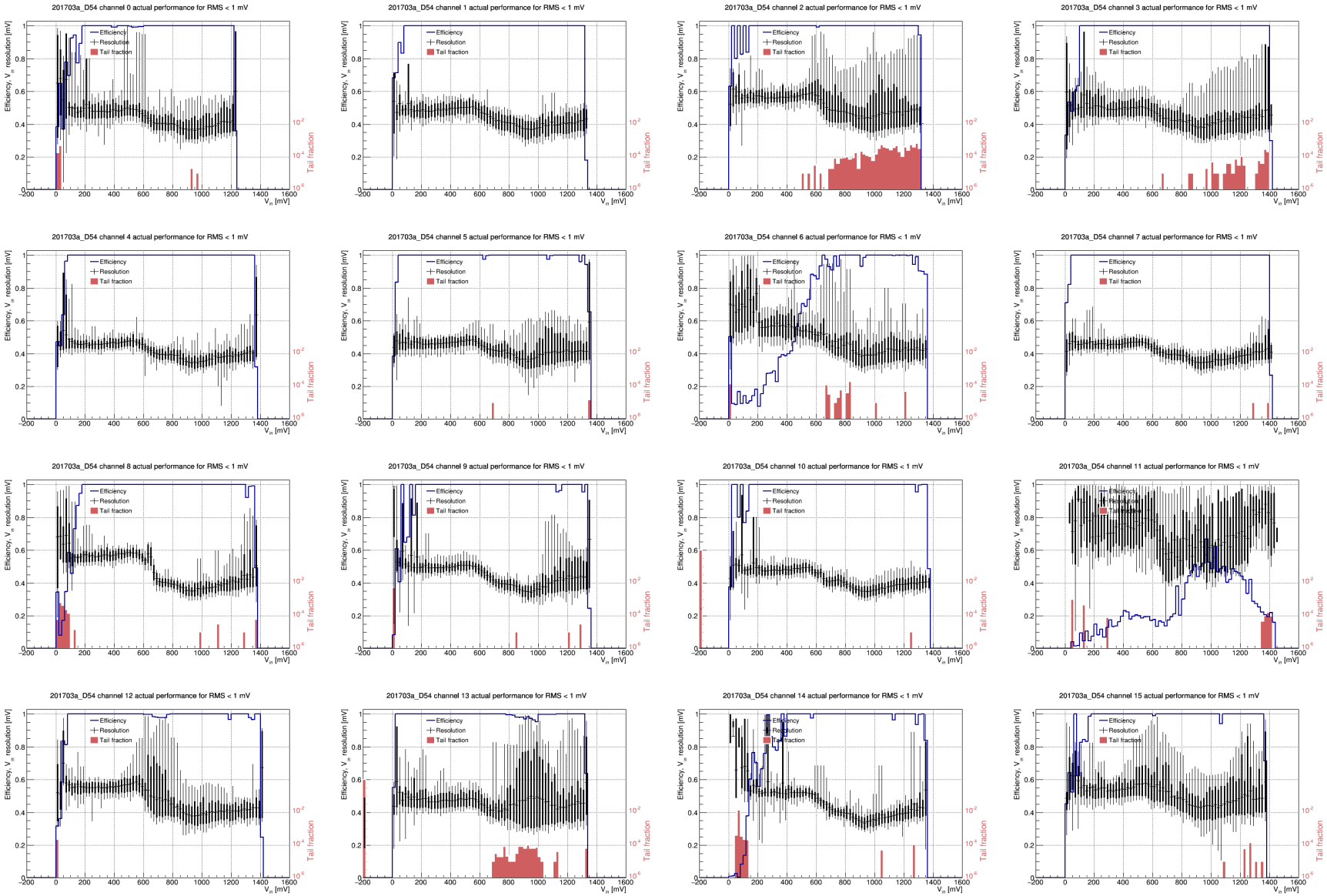
Chip D45 (rank=63, Q=0.286, a=0.954, m=0.290)



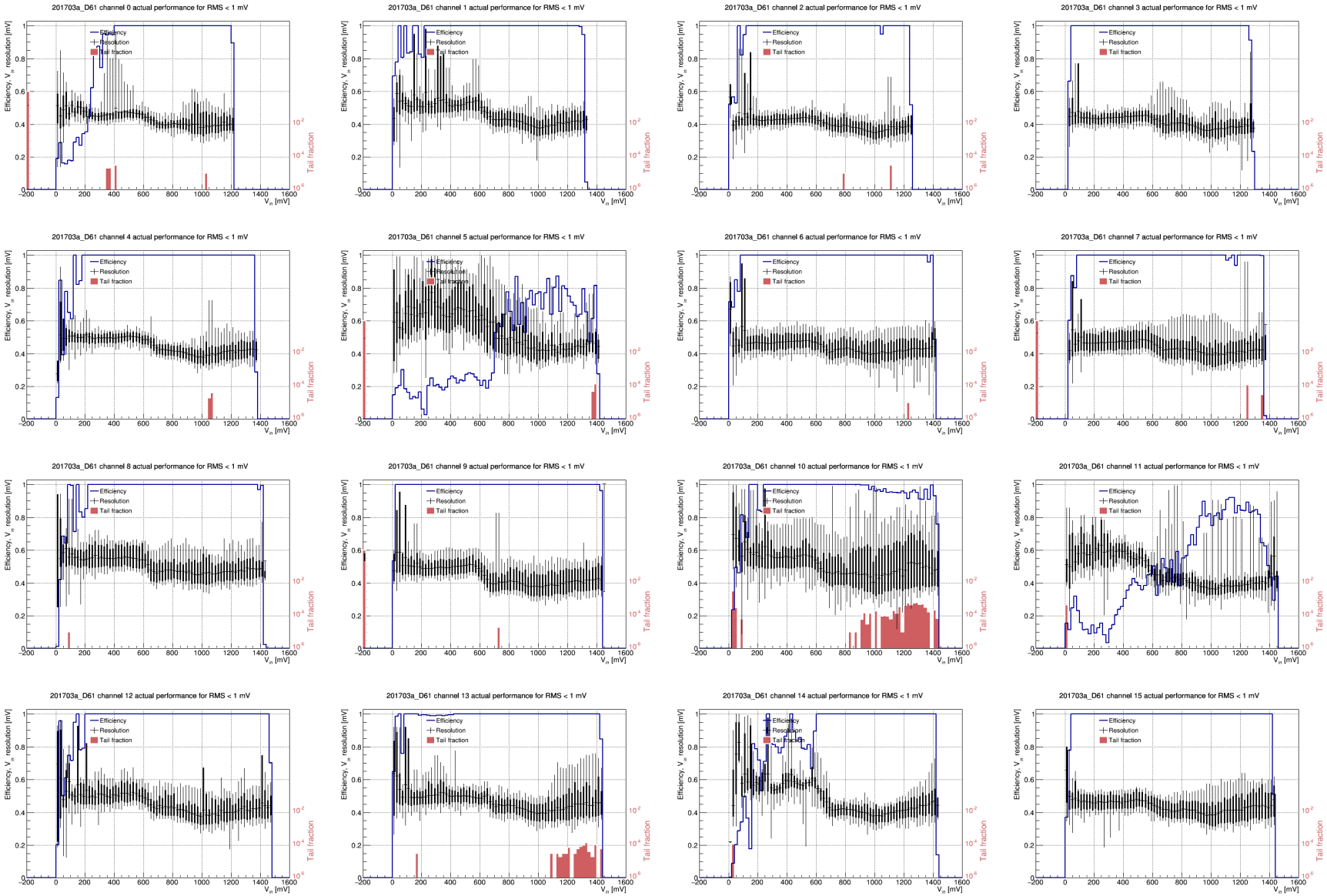
Chip D26 (rank=64, Q=0.249, a=0.922, m=0.663)



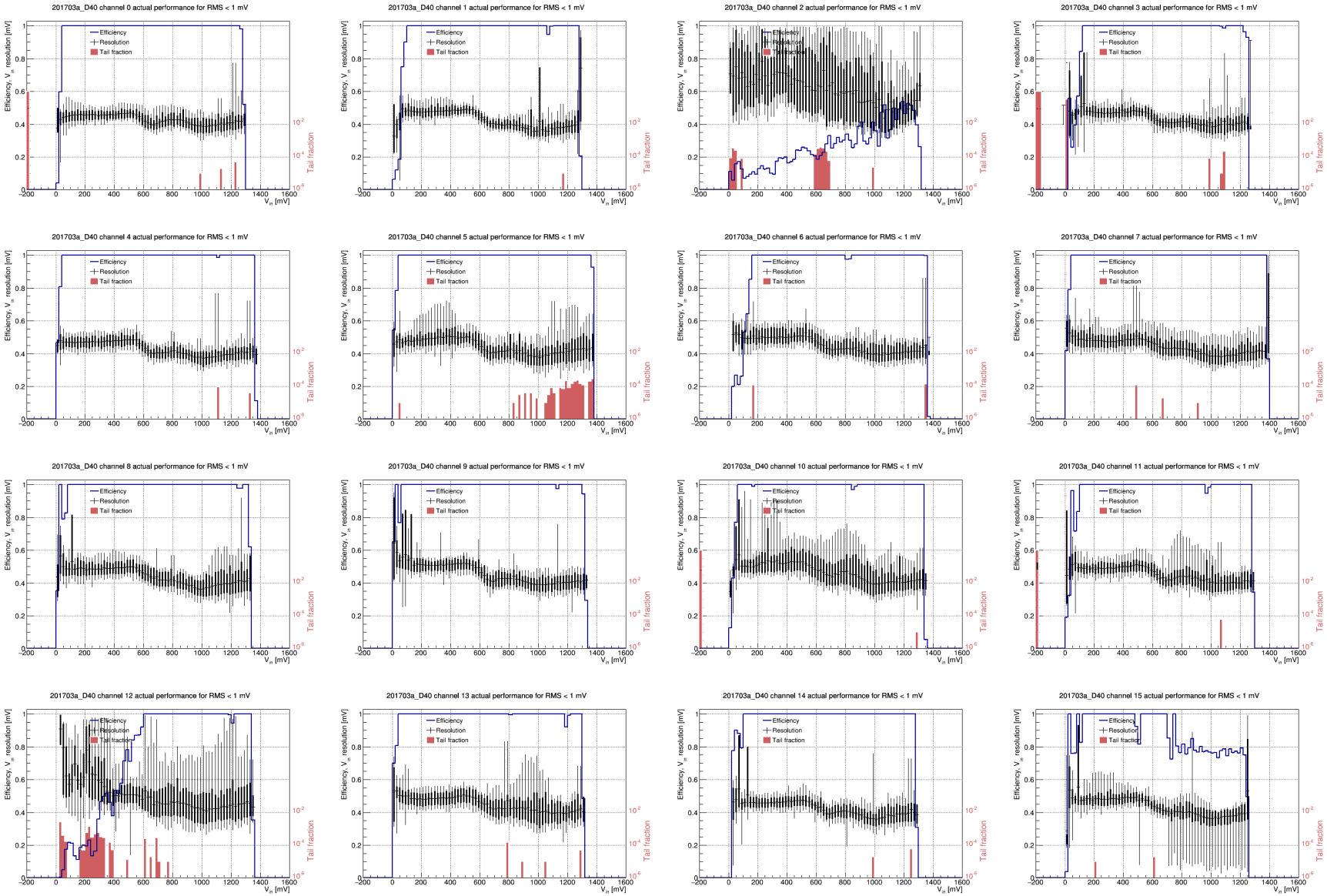
Chip D54 (rank=65, Q=0.217, a=0.938, m=0.297)



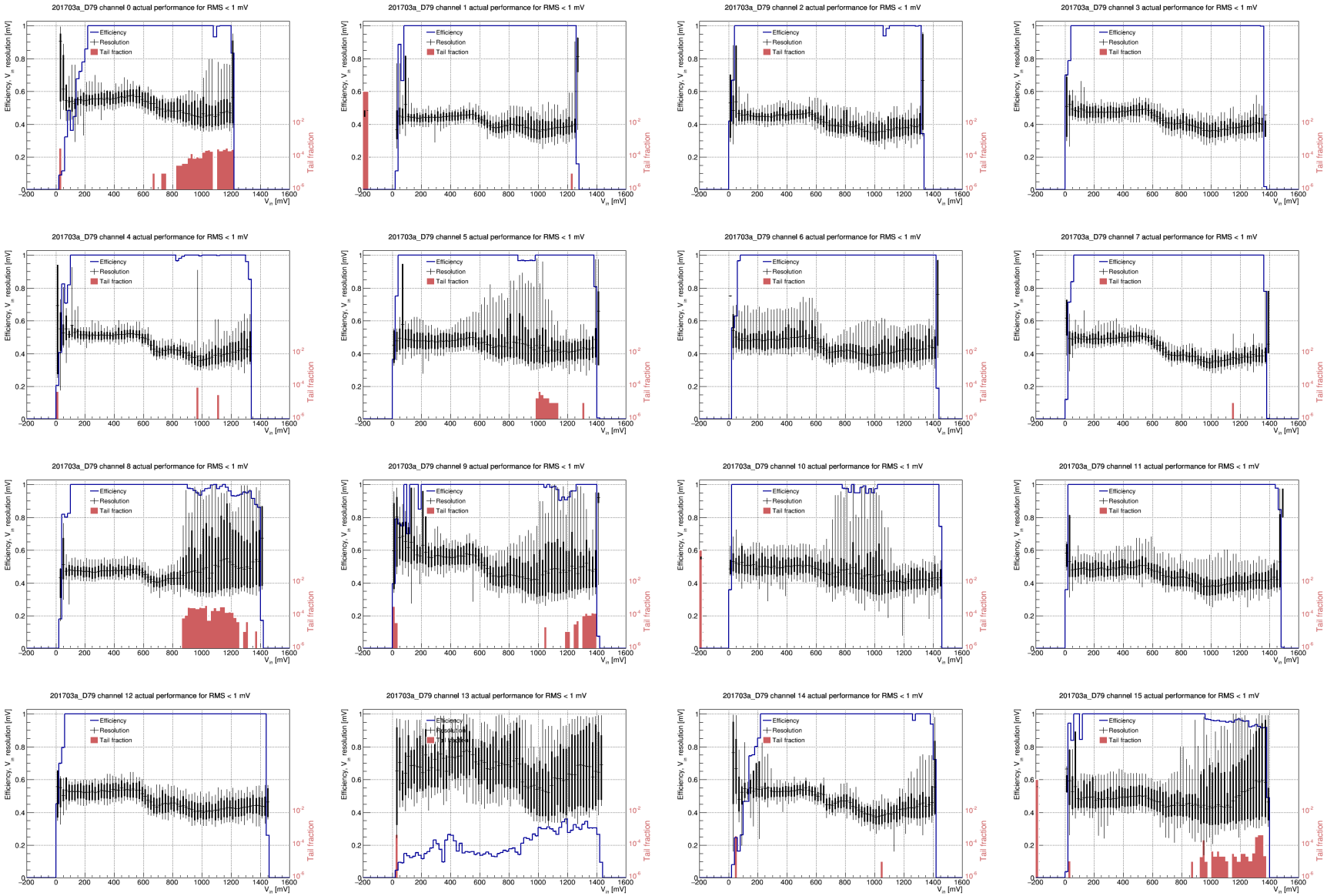
Chip D61 (rank=66, Q=0.202, a=0.926, m=0.461)



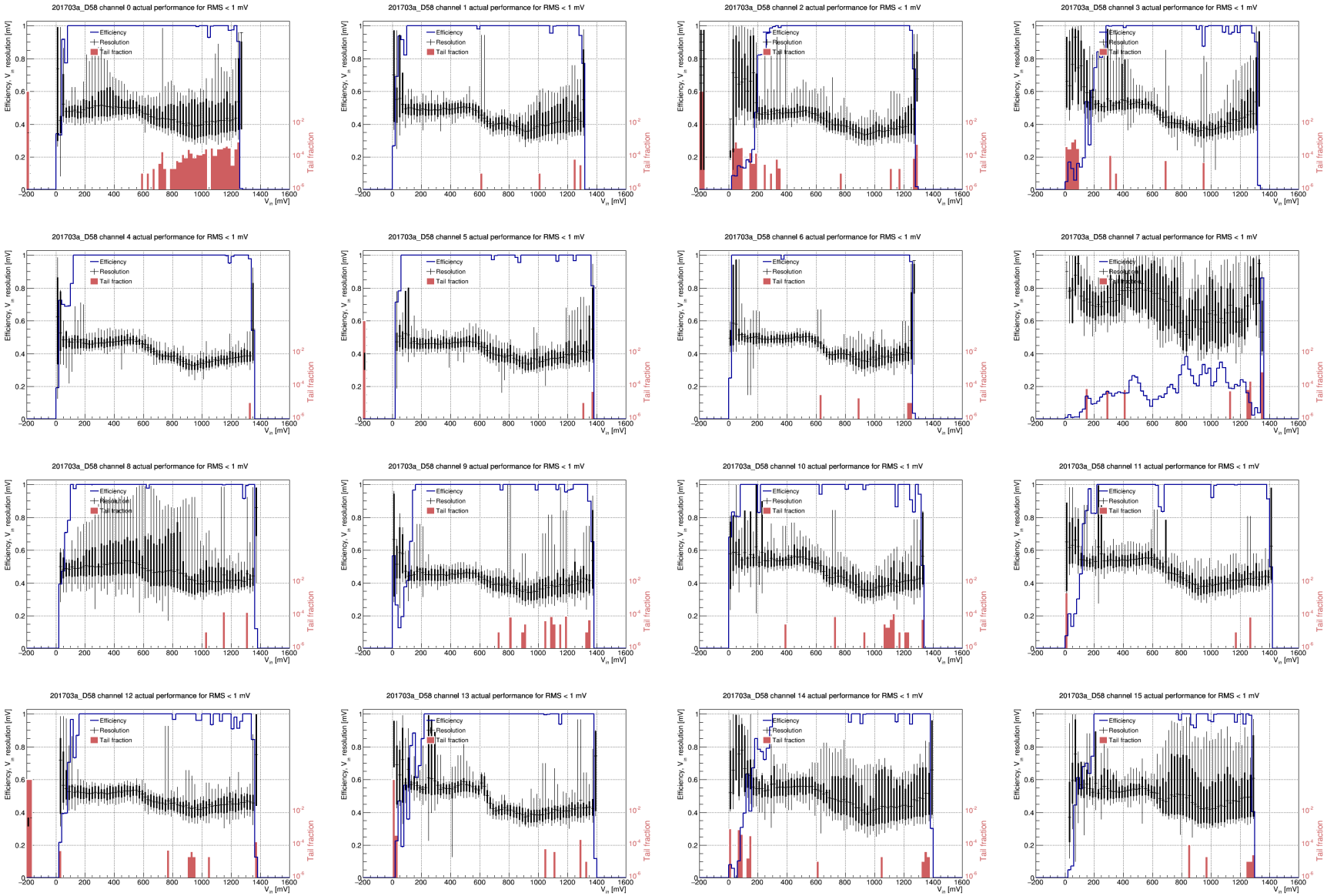
Chip D40 (rank=67, Q=0.199, a=0.935, m=0.277)



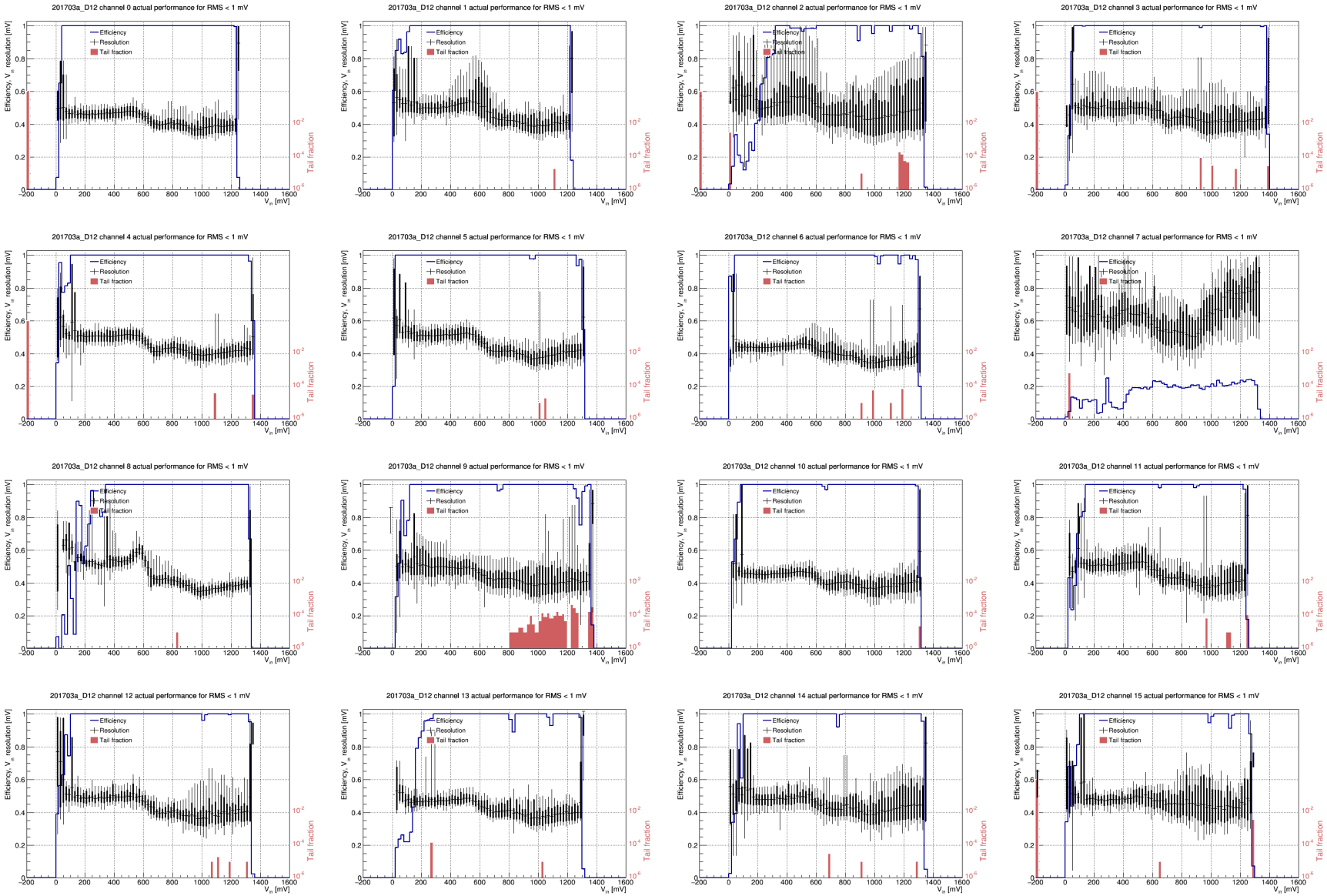
Chip D79 (rank=68, Q=0.196, a=0.947, m=0.205)



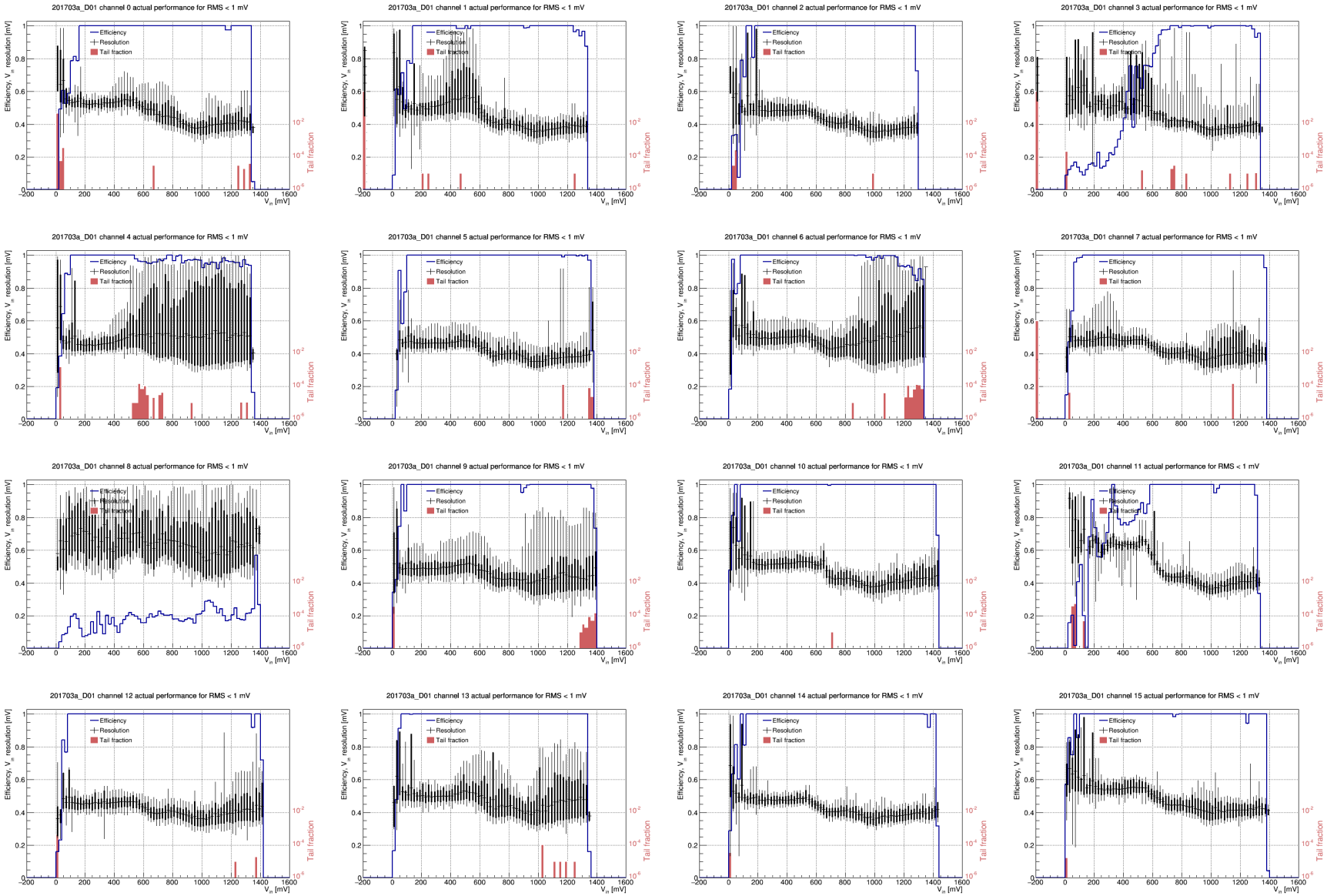
Chip D58 (rank=69, Q=0.184, a=0.943, m=0.204)



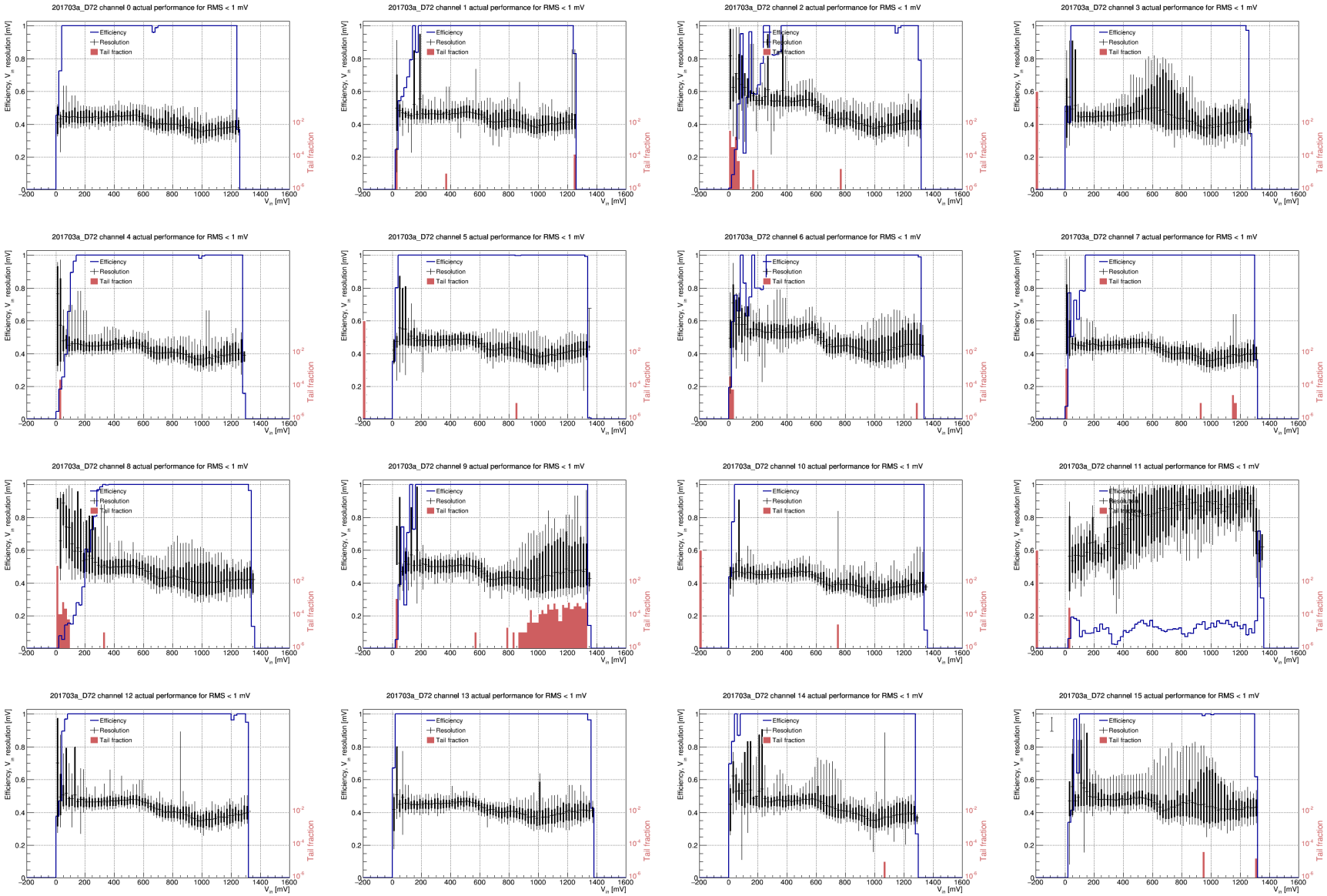
Chip D12 (rank=70, Q=0.162, a=0.942, m=0.177)



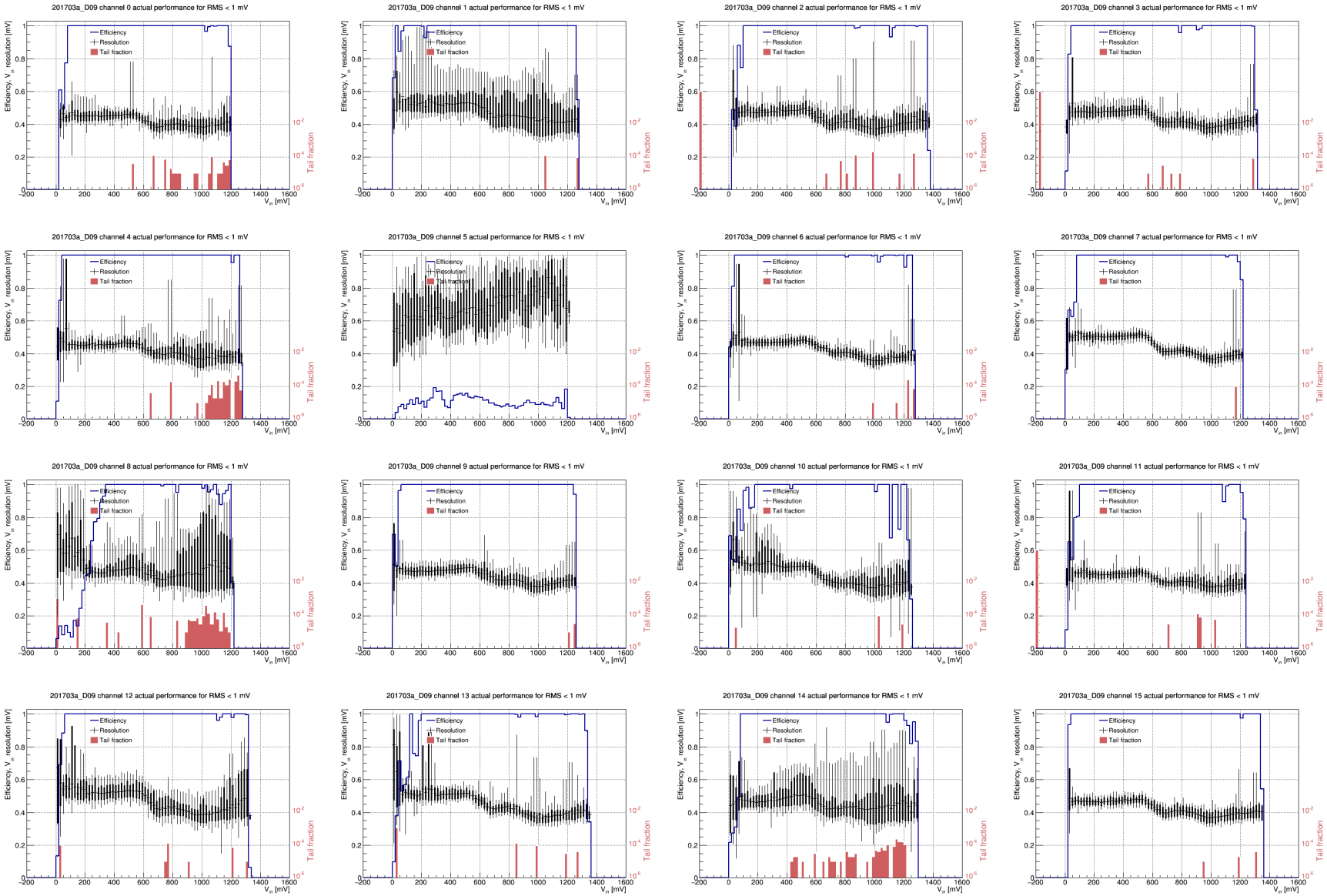
Chip D01 (rank=71, Q=0.125, a=0.927, m=0.186)



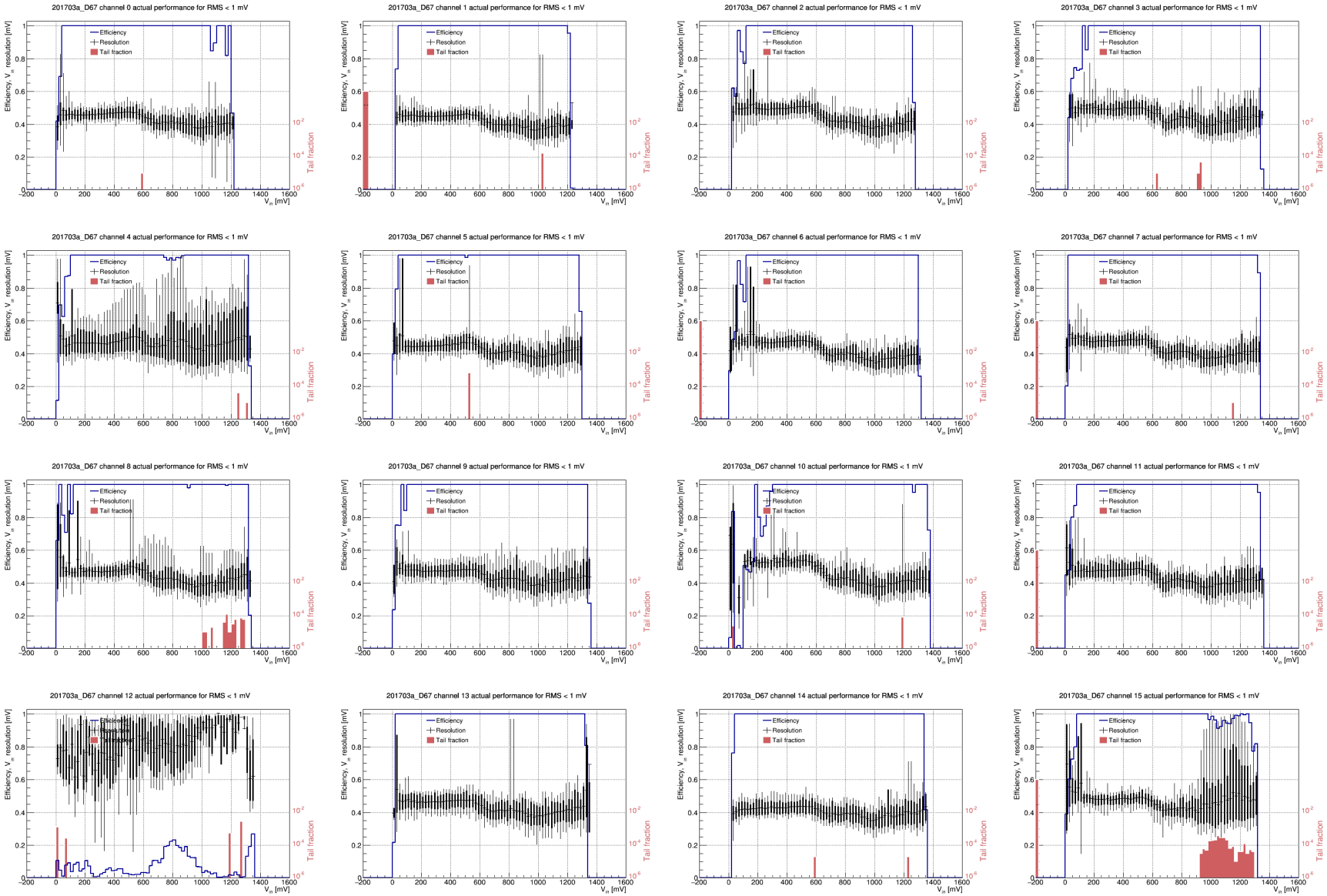
Chip D72 (rank=72, Q=0.114, a=0.941, m=0.122)



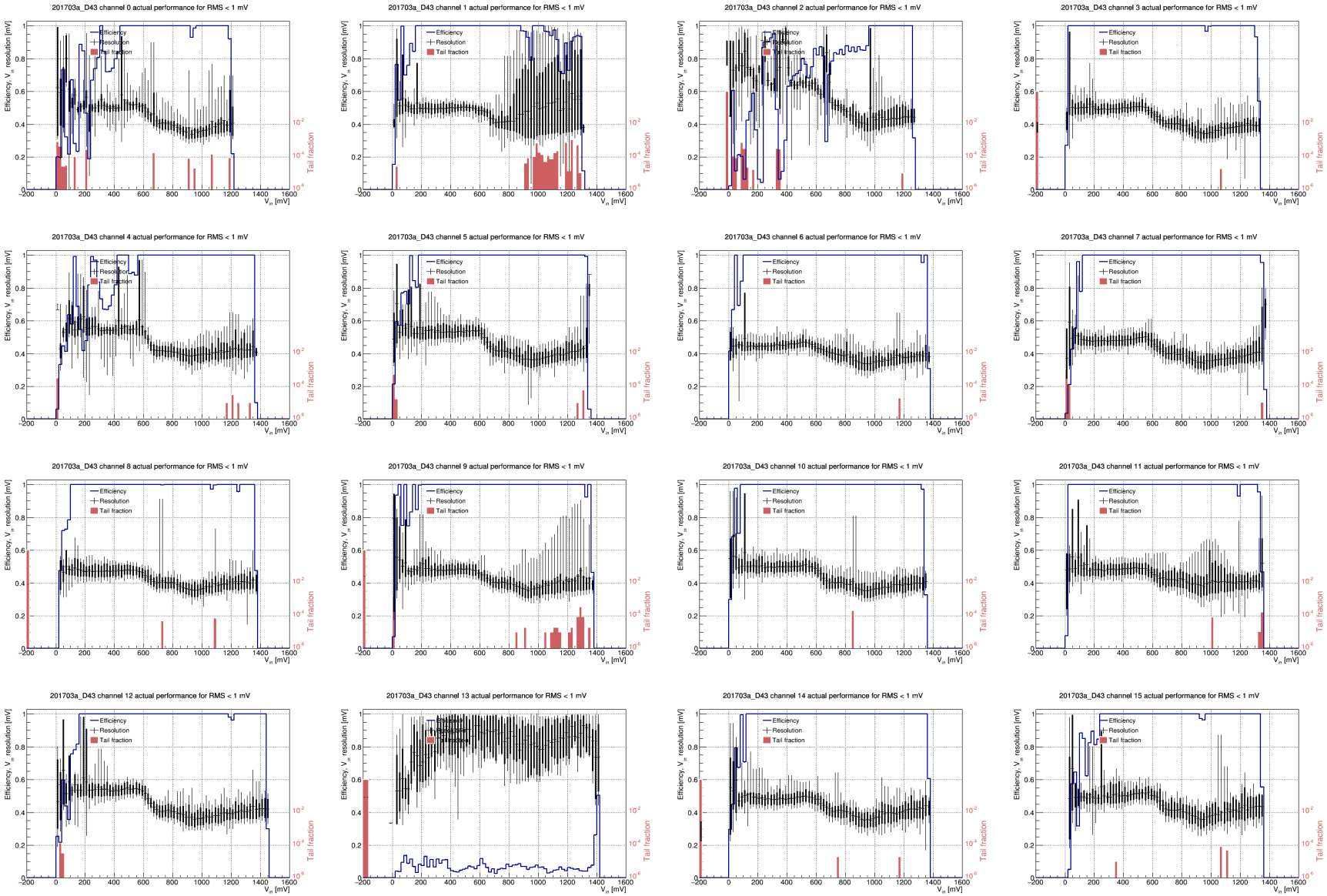
Chip D09 (rank=73, Q=0.102, a=0.939, m=0.110)



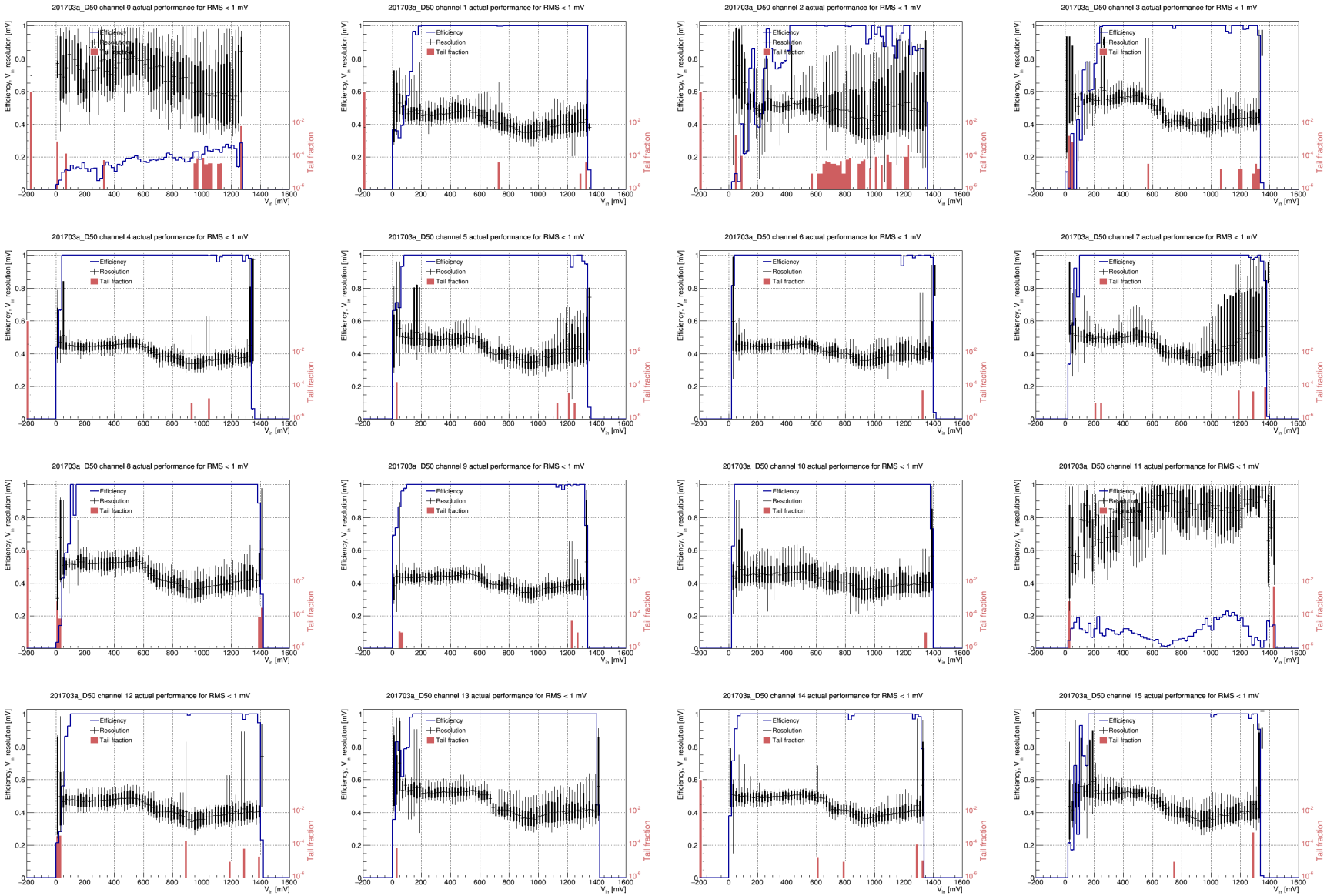
Chip D67 (rank=74, Q=0.069, a=0.939, m=0.072)



Chip D43 (rank=75, Q=0.043, a=0.916, m=0.066)

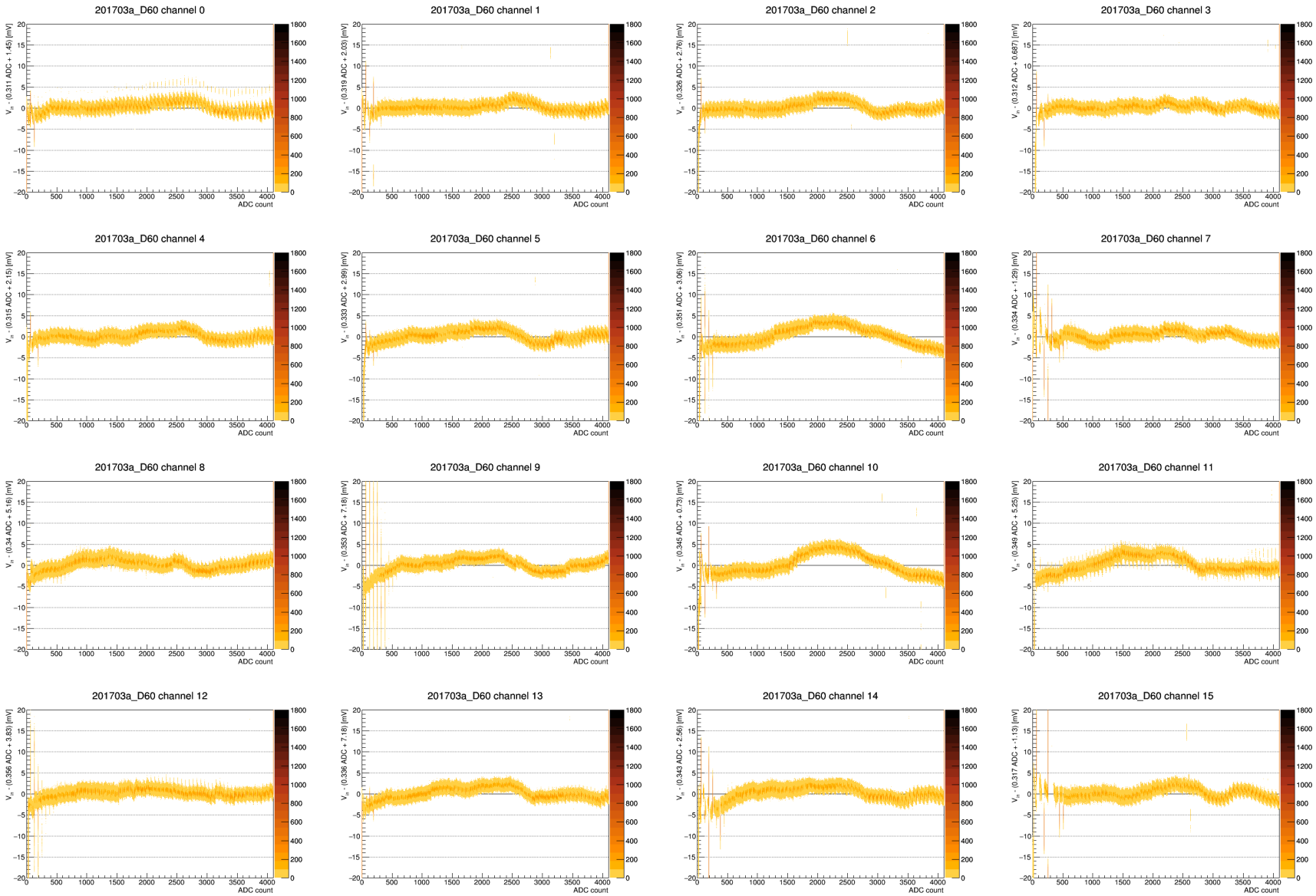


Chip D50 (rank=76, Q=0.017, a=0.887, m=0.105)

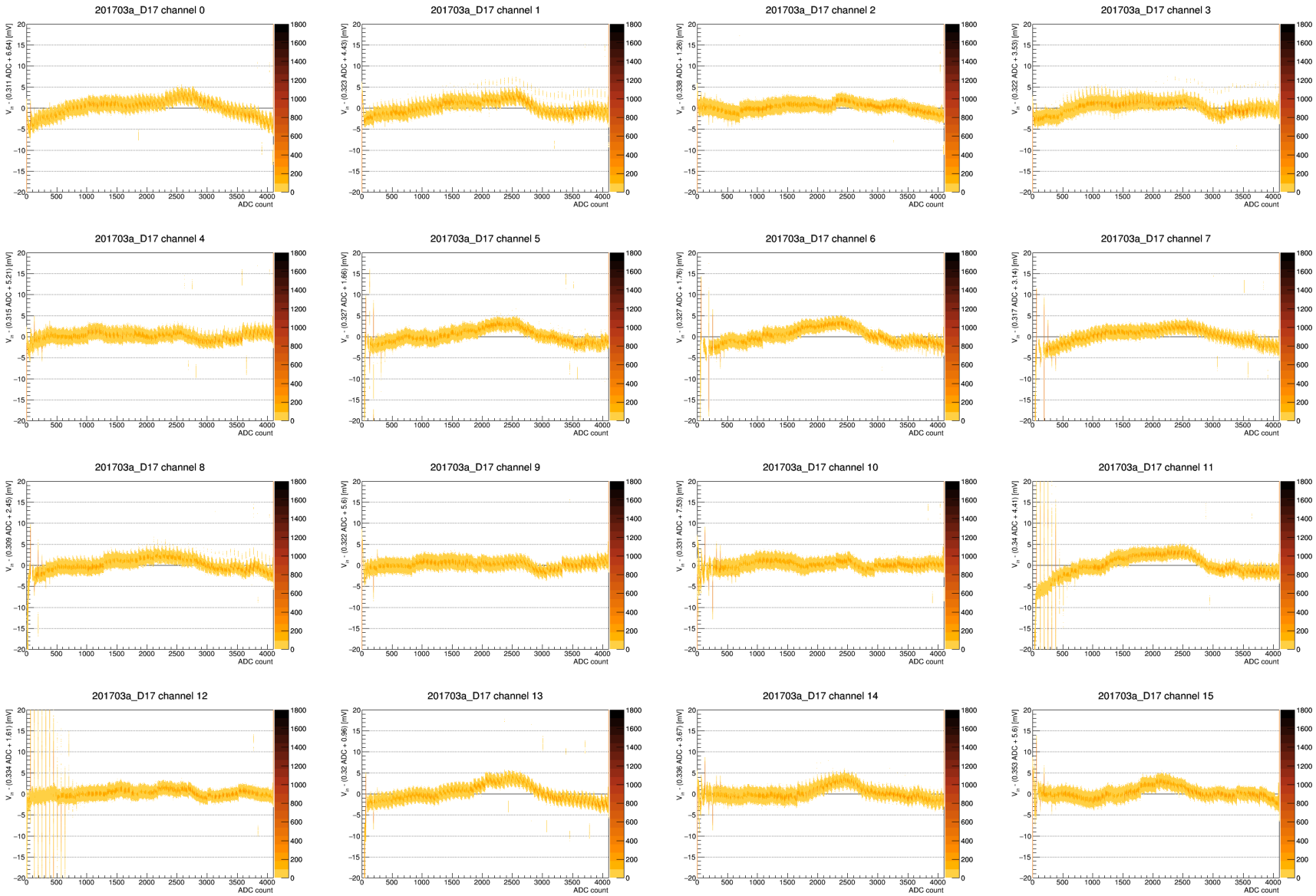


Good chips

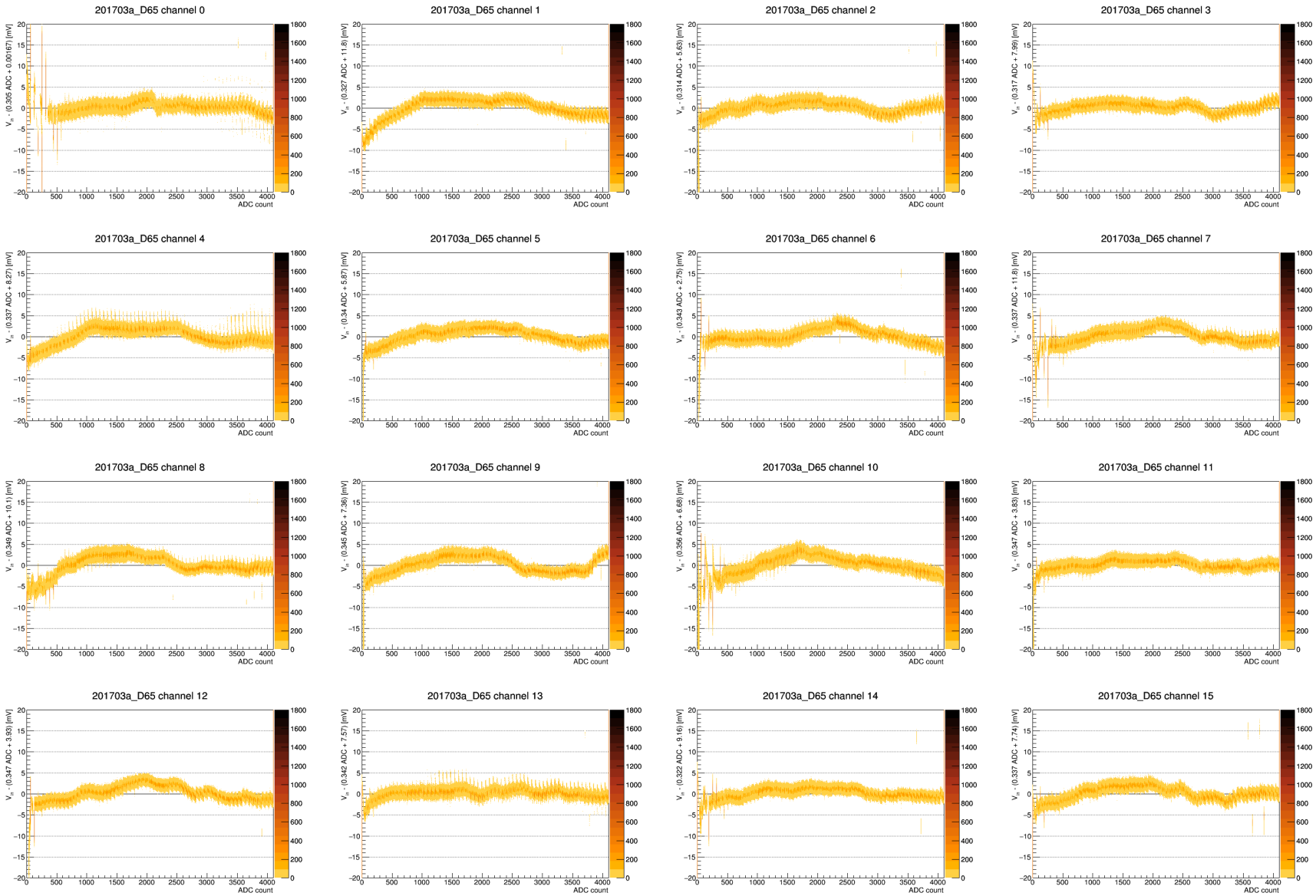
Chip D60 (rank=1, Q=0.990, a=0.999, m=0.995)



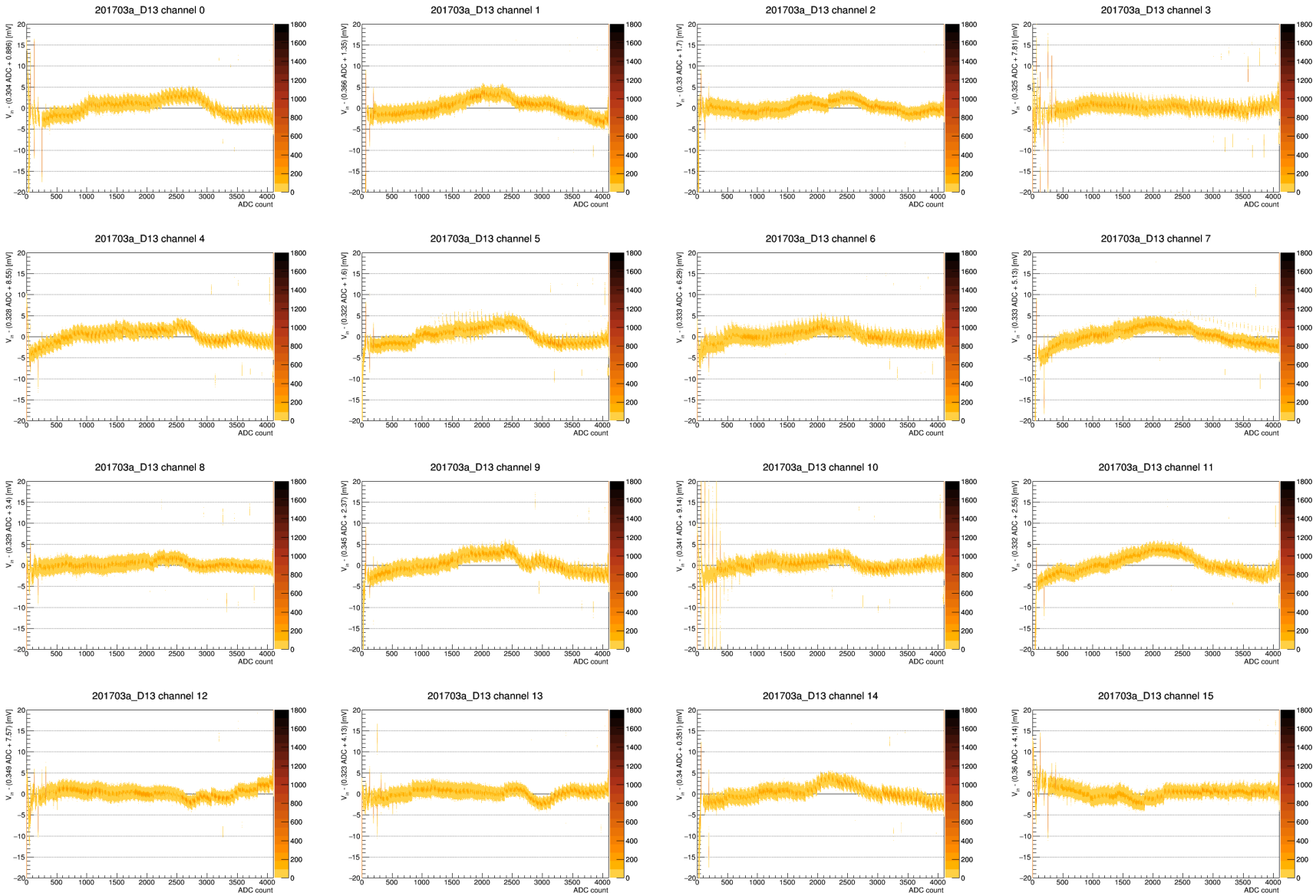
Chip D17 (rank=2, Q=0.984, a=0.999, m=0.993)



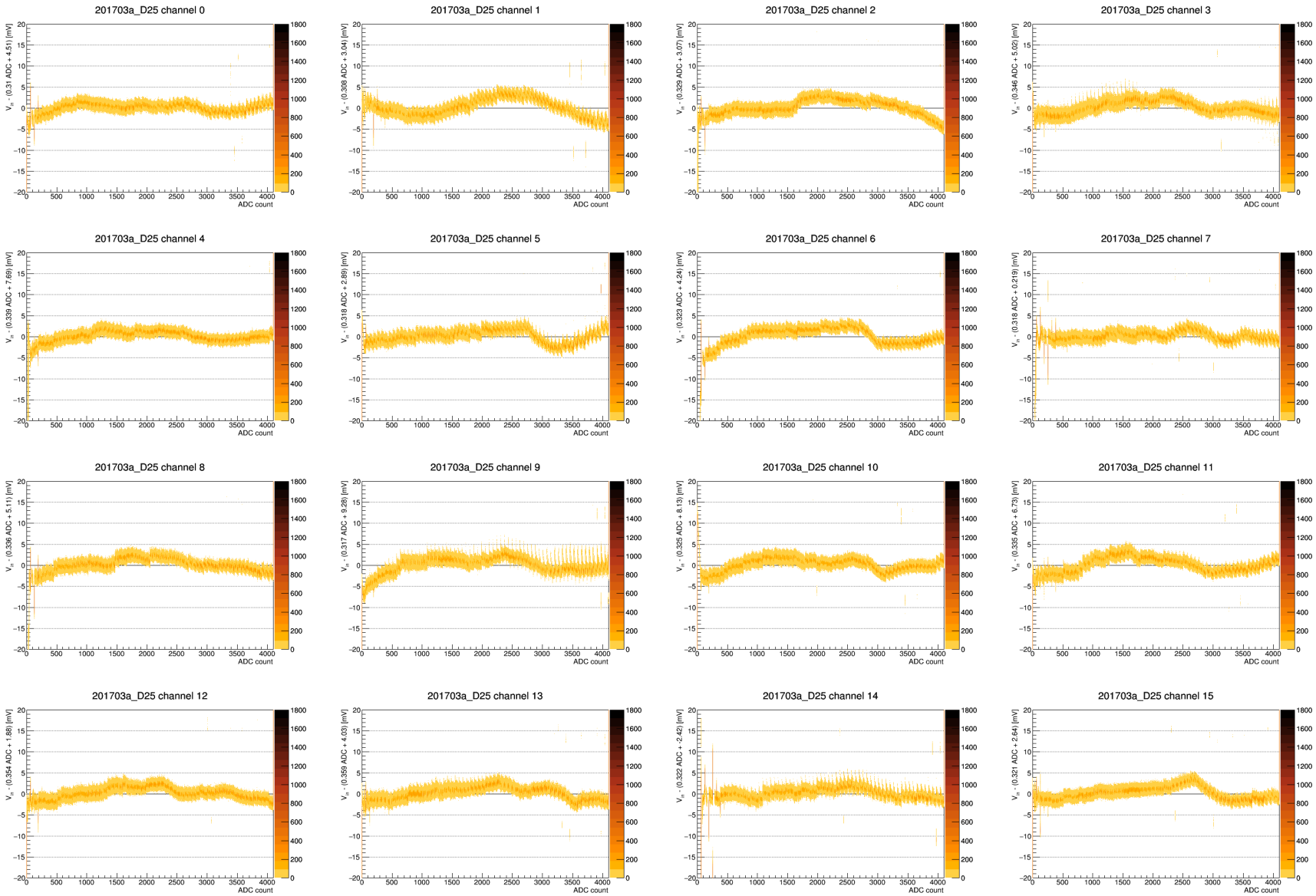
Chip D65 (rank=3, Q=0.982, a=0.998, m=0.990)



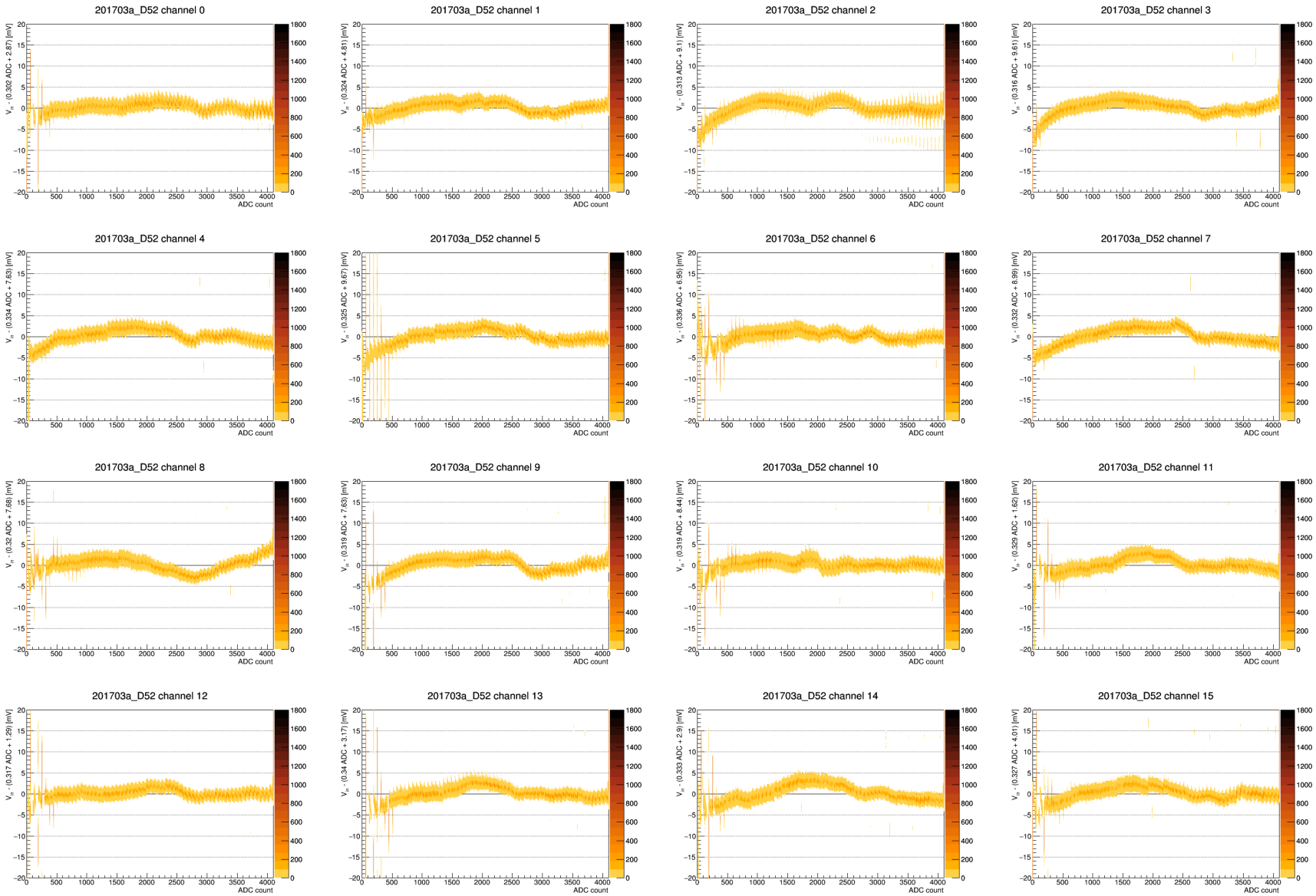
Chip D13 (rank=4, Q=0.980, a=0.998, m=0.994)



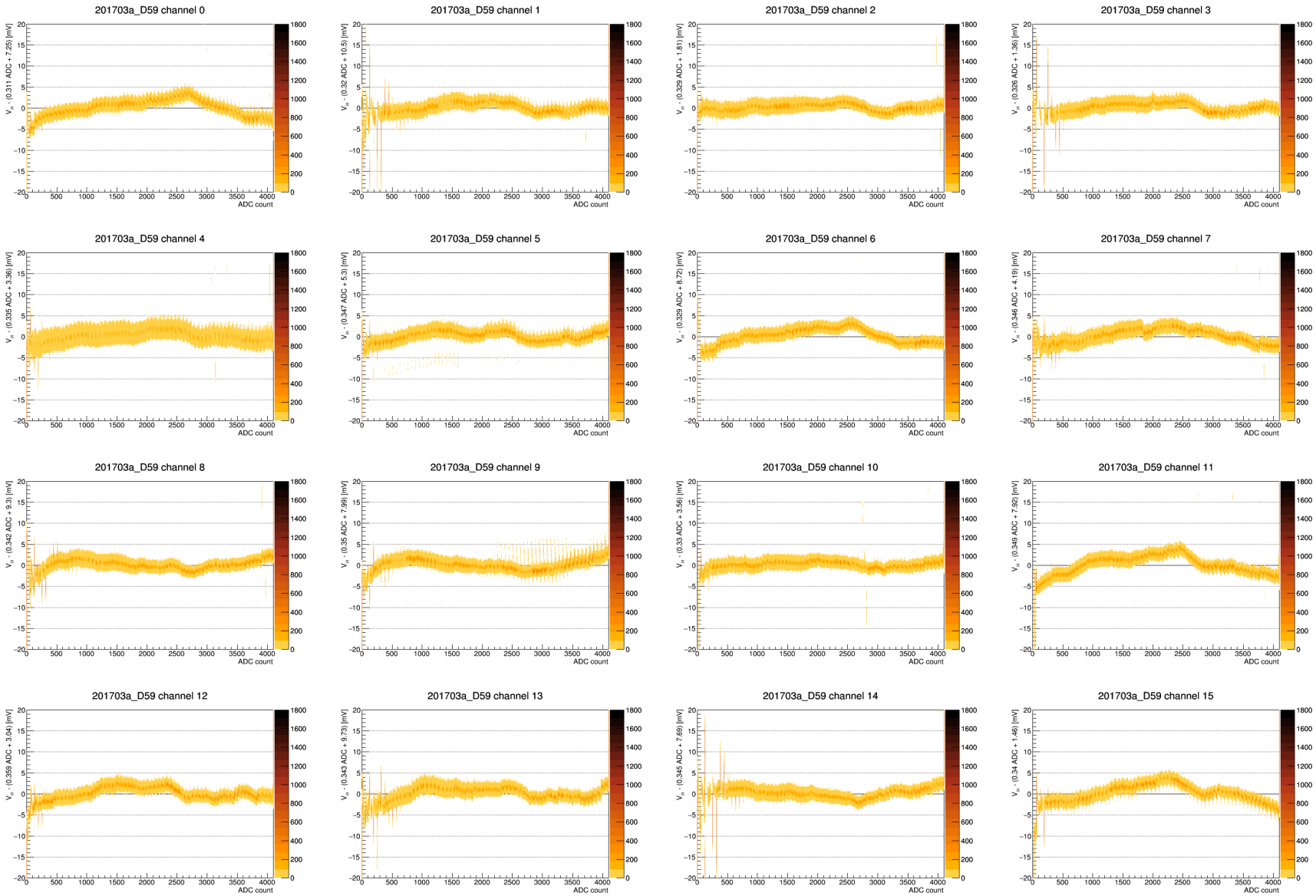
Chip D25 (rank=5, Q=0.979, a=0.998, m=0.989)



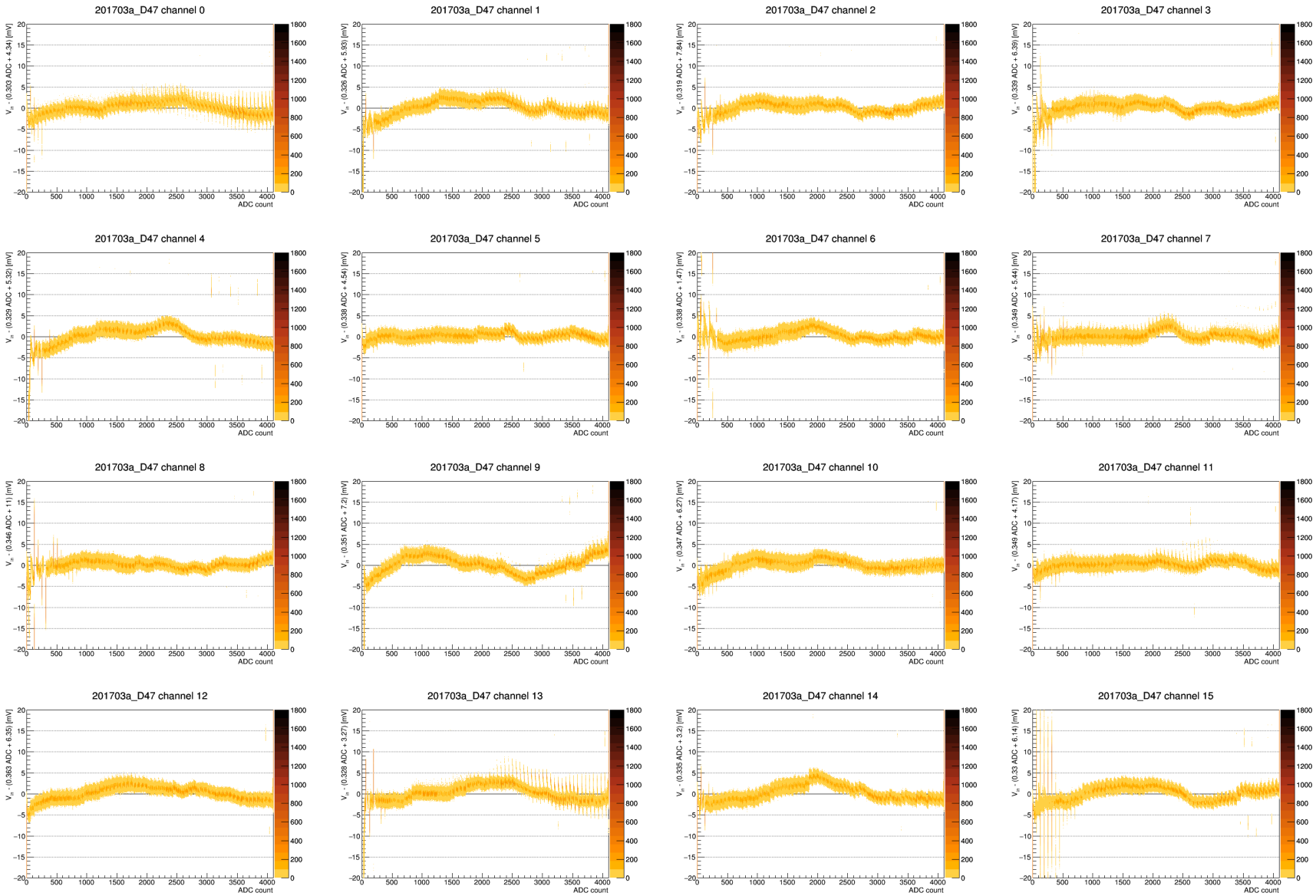
Chip D52 (rank=6, Q=0.975, a=0.998, m=0.990)



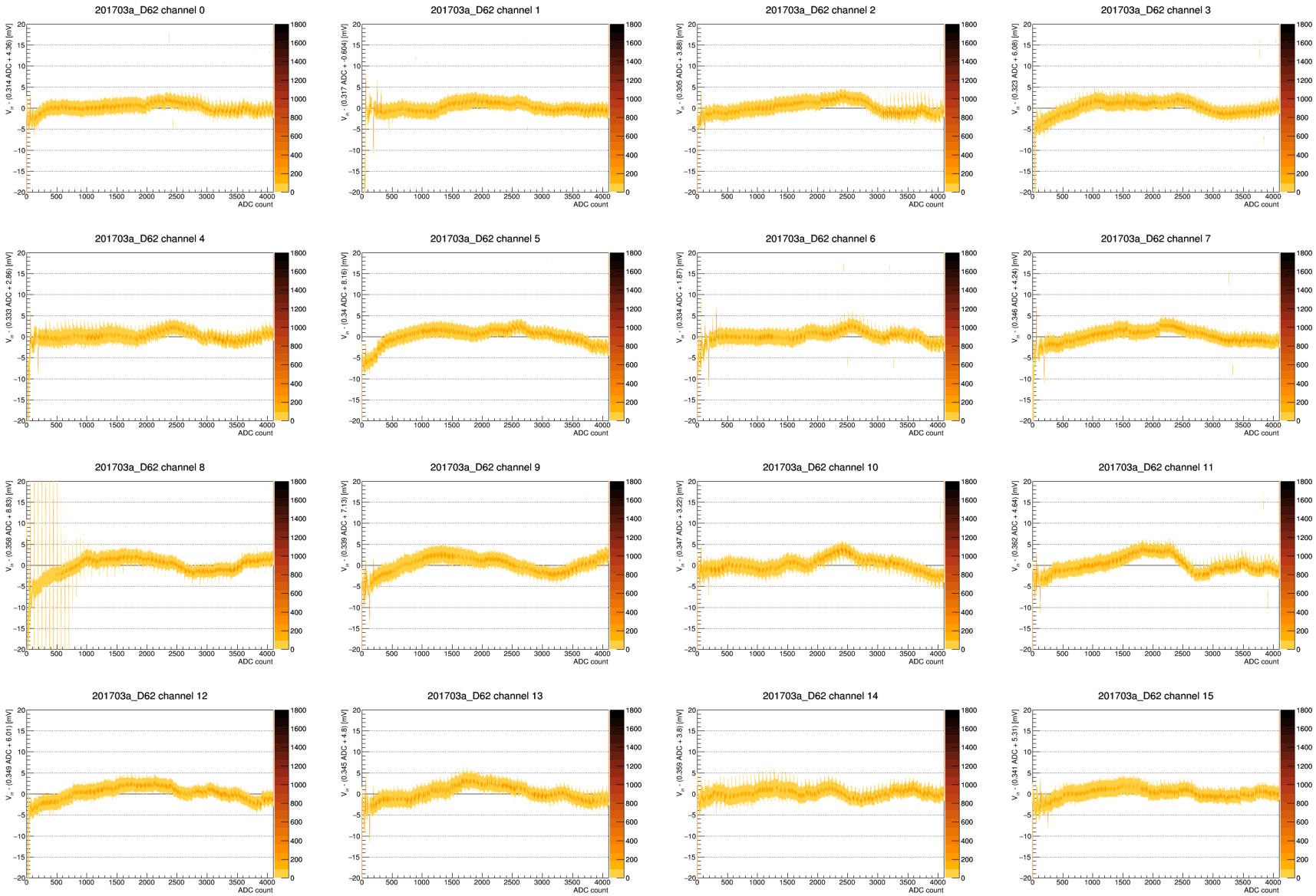
Chip D59 (rank=7, Q=0.974, a=0.998, m=0.989)



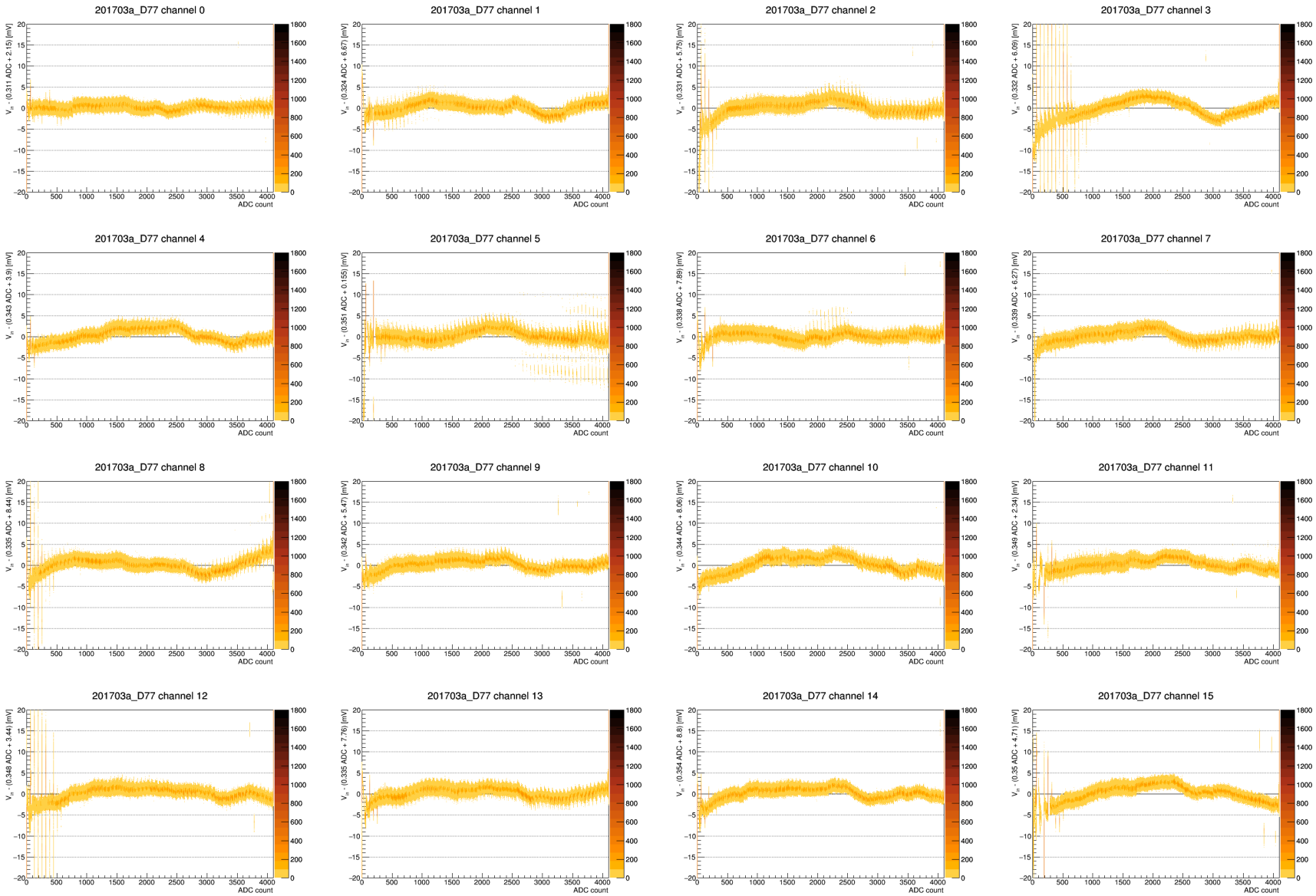
Chip D47 (rank=8, Q=0.973, a=0.998, m=0.990)



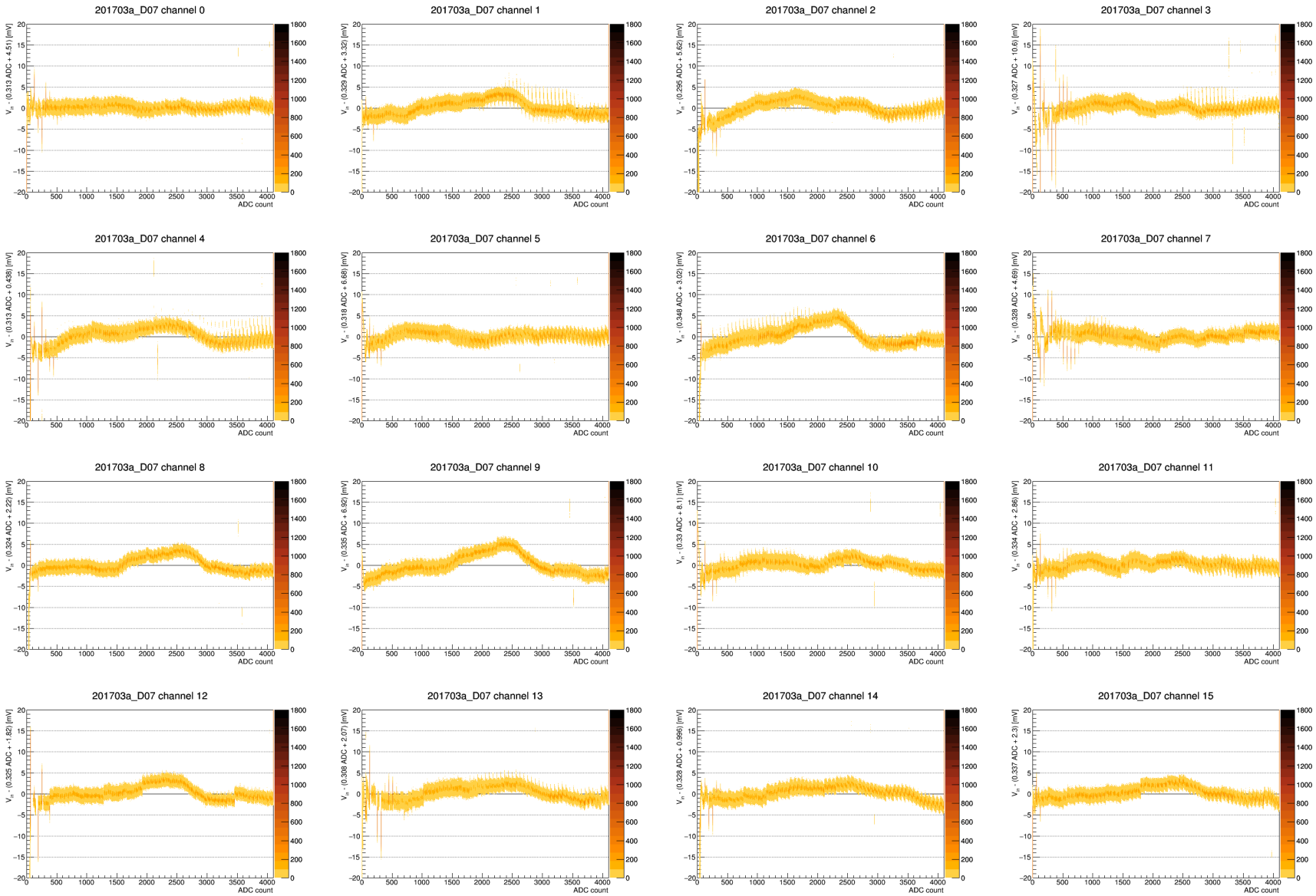
Chip D62 (rank=9, Q=0.970, a=0.998, m=0.985)



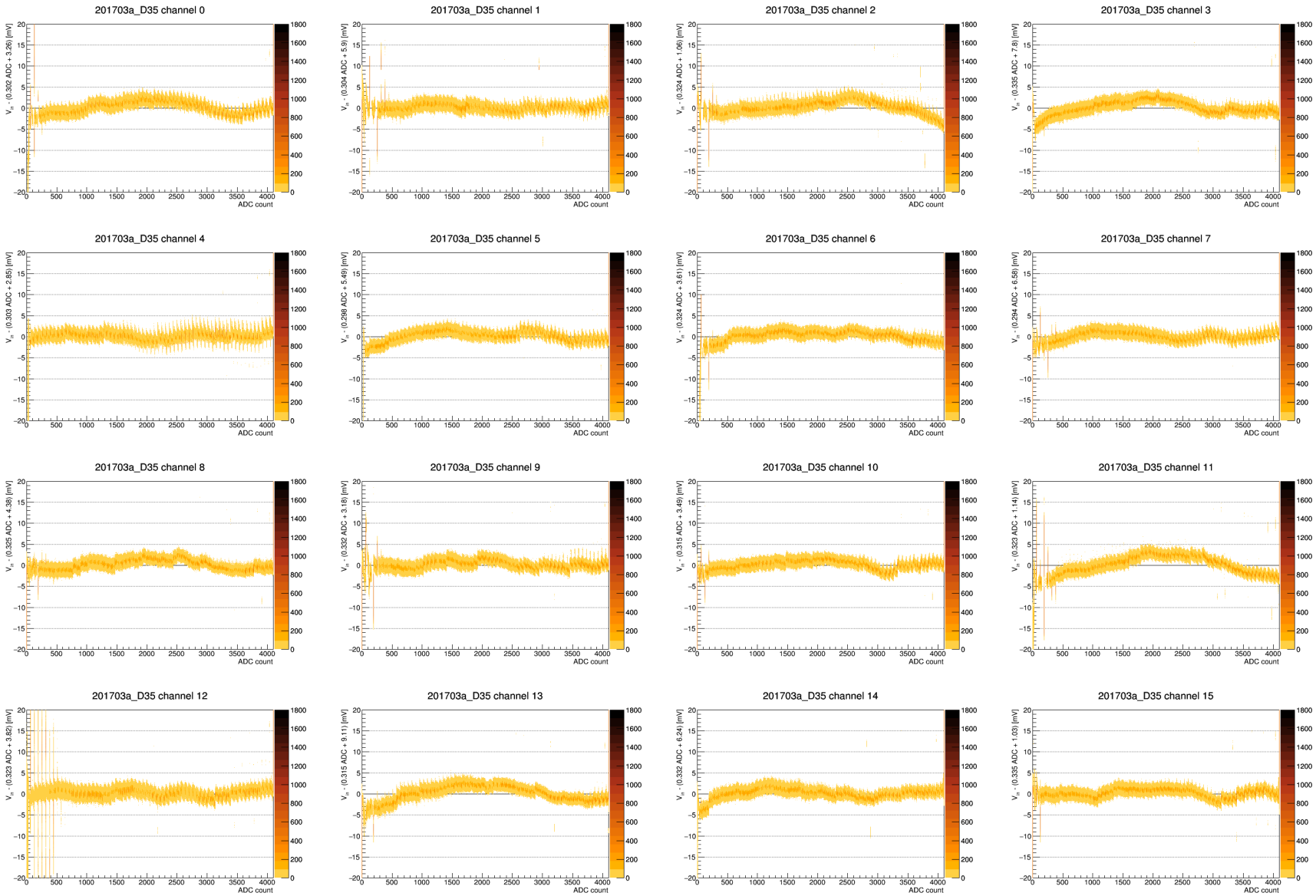
Chip D77 (rank=10, Q=0.969, a=0.998, m=0.981)



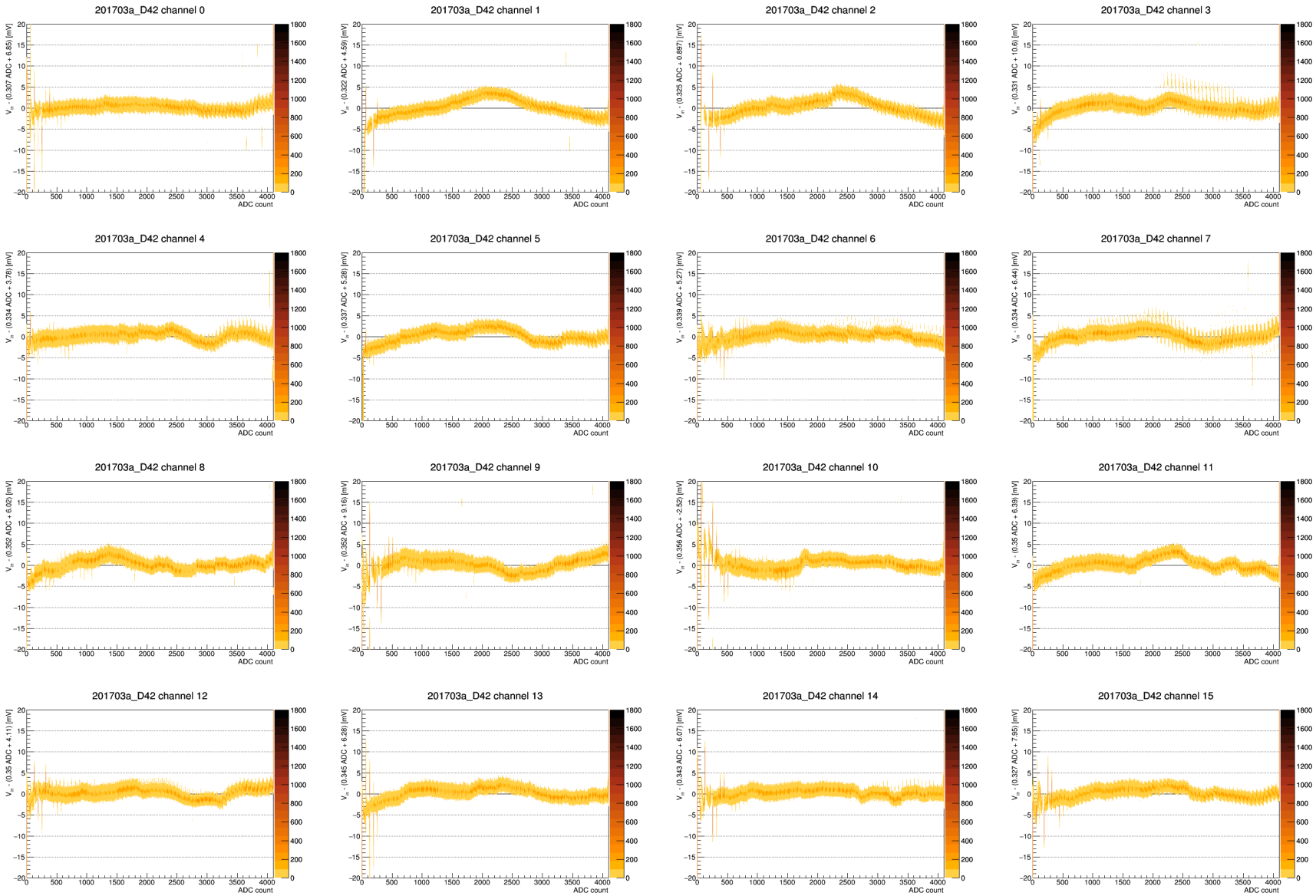
Chip D07 (rank=11, Q=0.959, a=0.997, m=0.988)



Chip D35 (rank=12, Q=0.959, a=0.997, m=0.964)

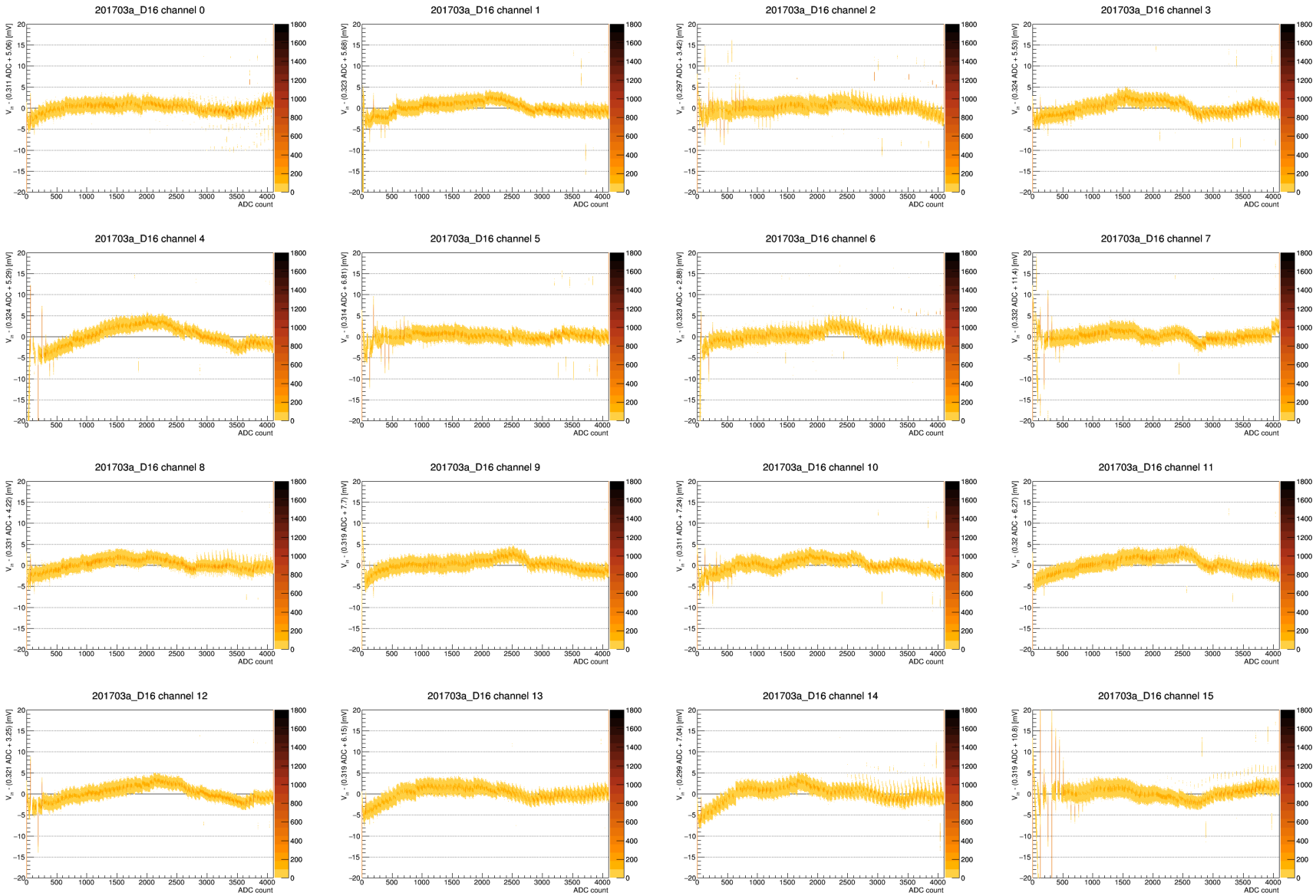


Chip D42 (rank=13, Q=0.957, a=0.997, m=0.989)

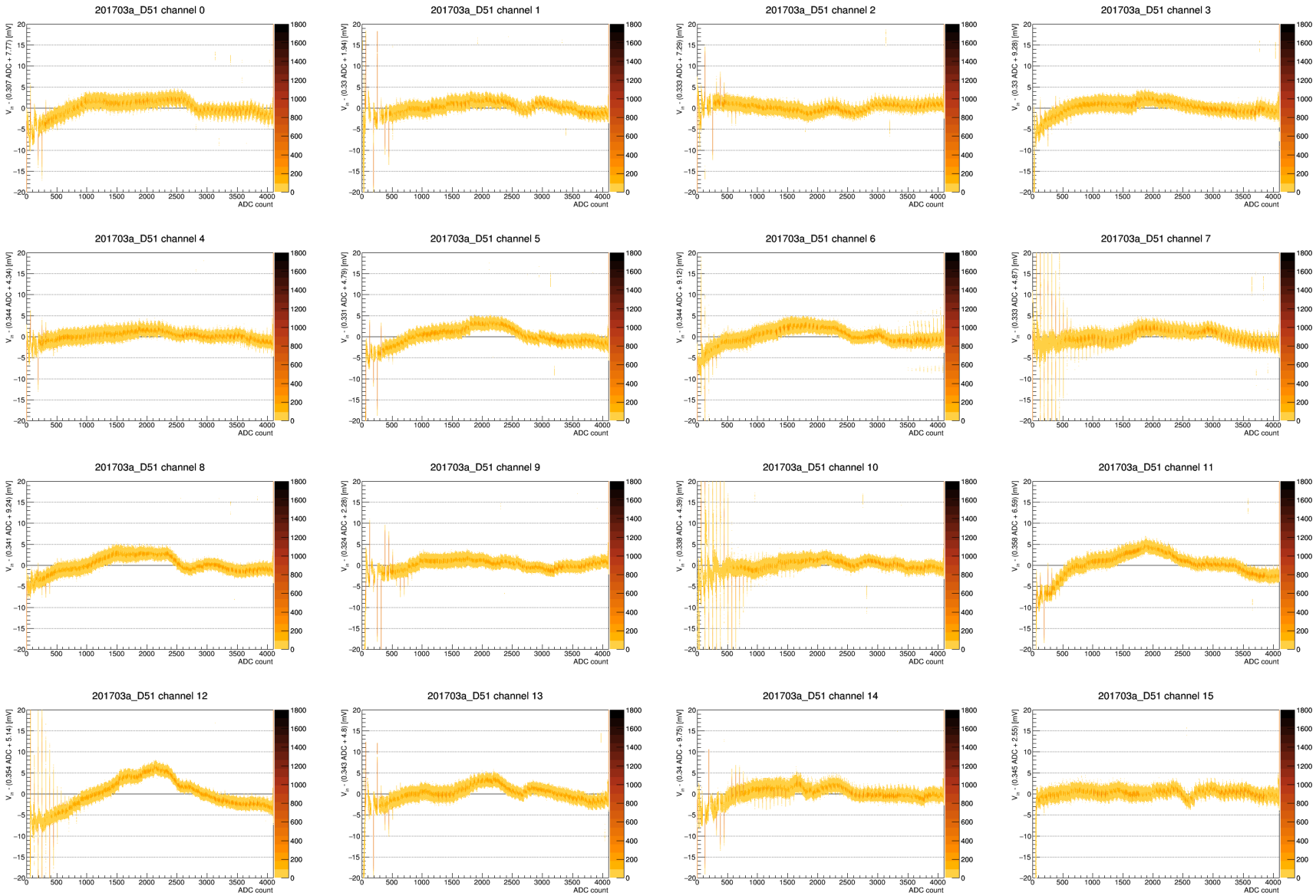


Fair chips

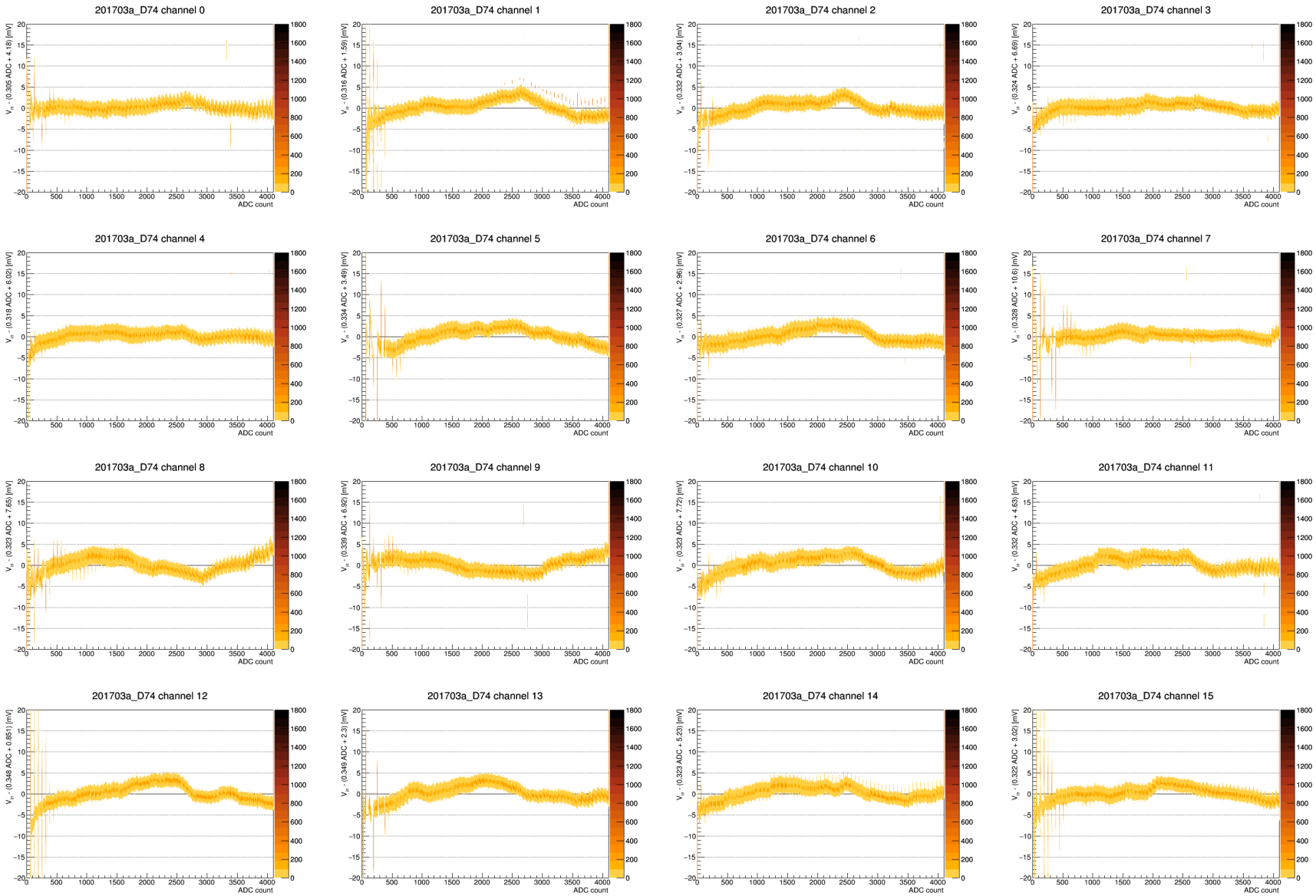
Chip D16 (rank=14, Q=0.949, a=0.996, m=0.982)



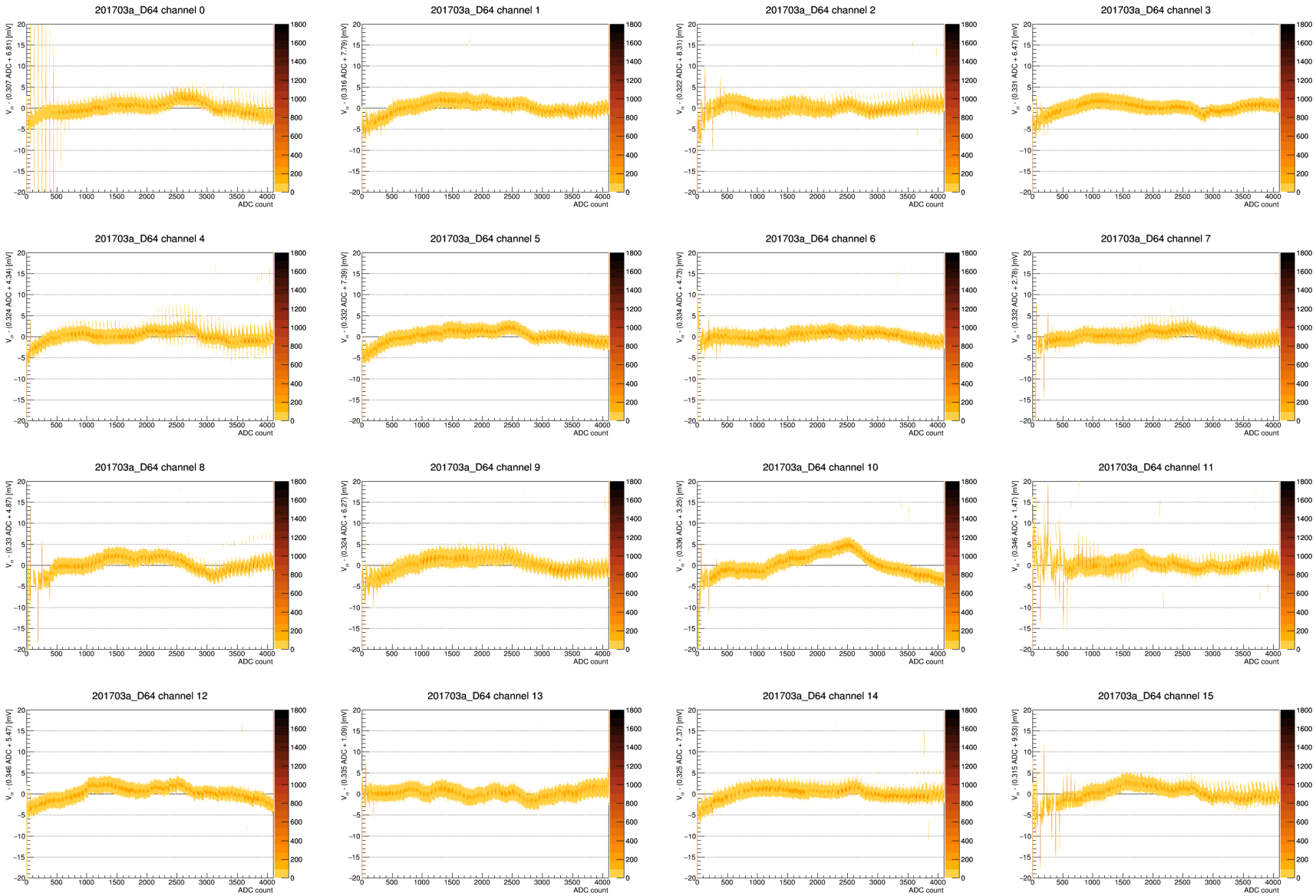
Chip D51 (rank=15, Q=0.948, a=0.996, m=0.981)



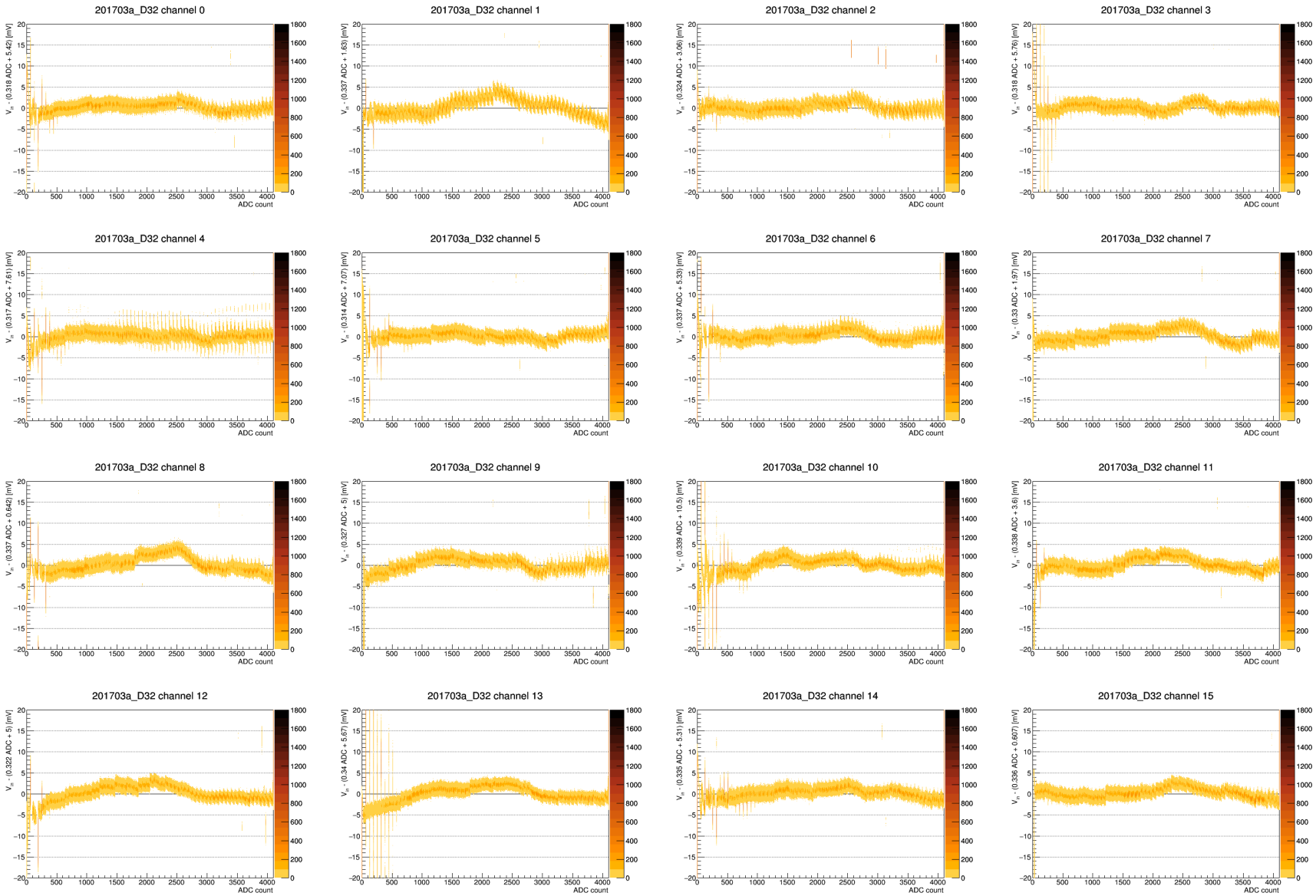
Chip D74 (rank=16, Q=0.948, a=0.996, m=0.964)



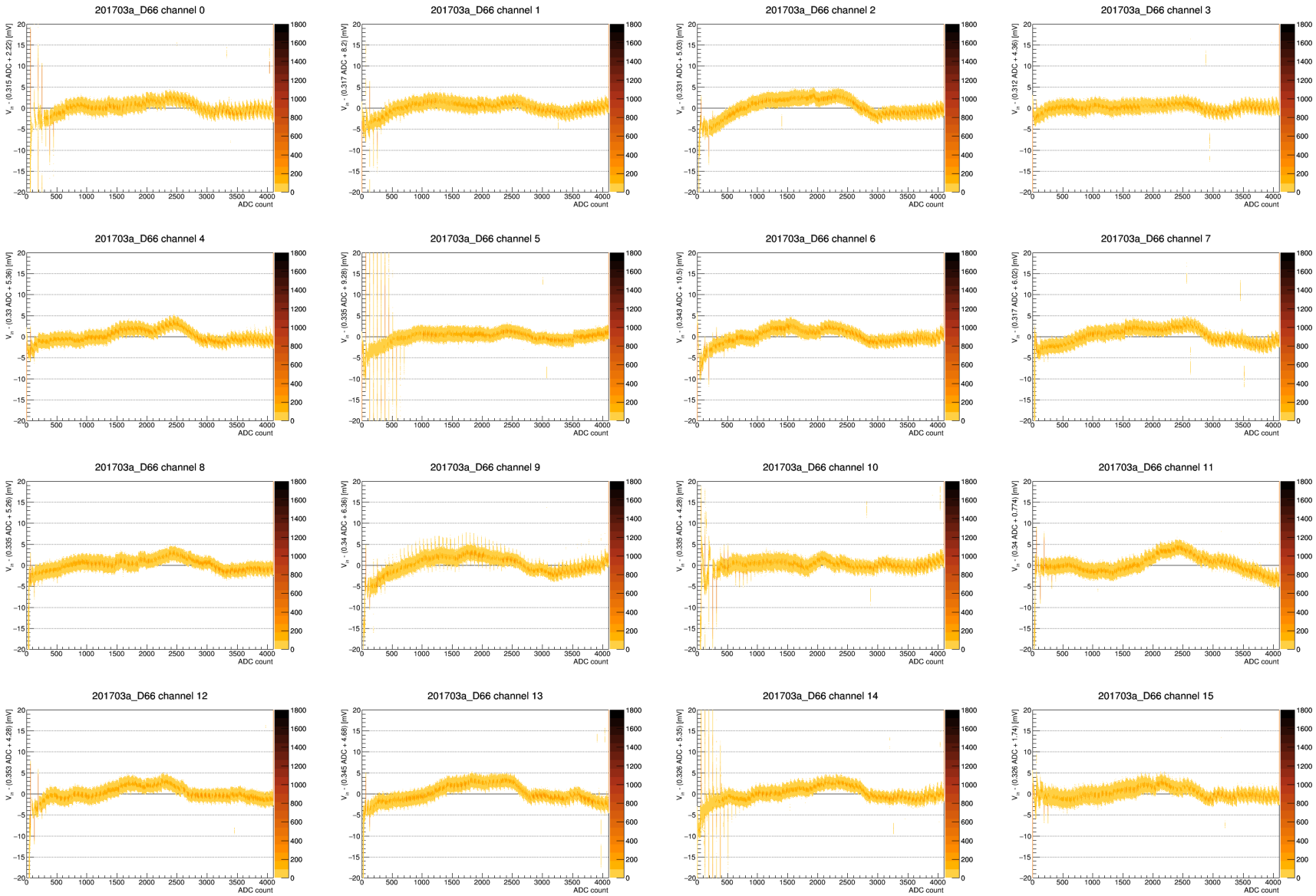
Chip D64 (rank=17, Q=0.947, a=0.996, m=0.972)



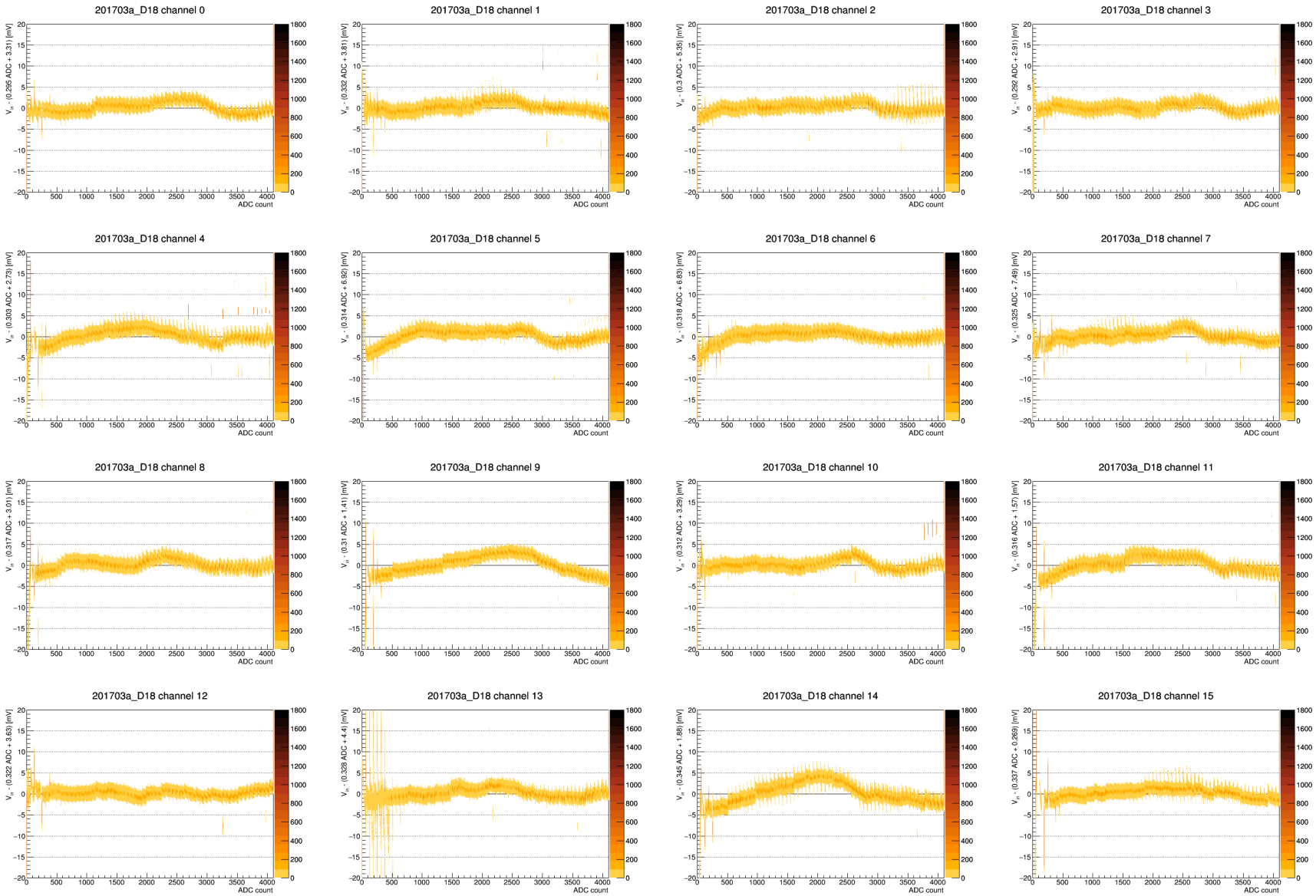
Chip D32 (rank=18, Q=0.946, a=0.996, m=0.982)



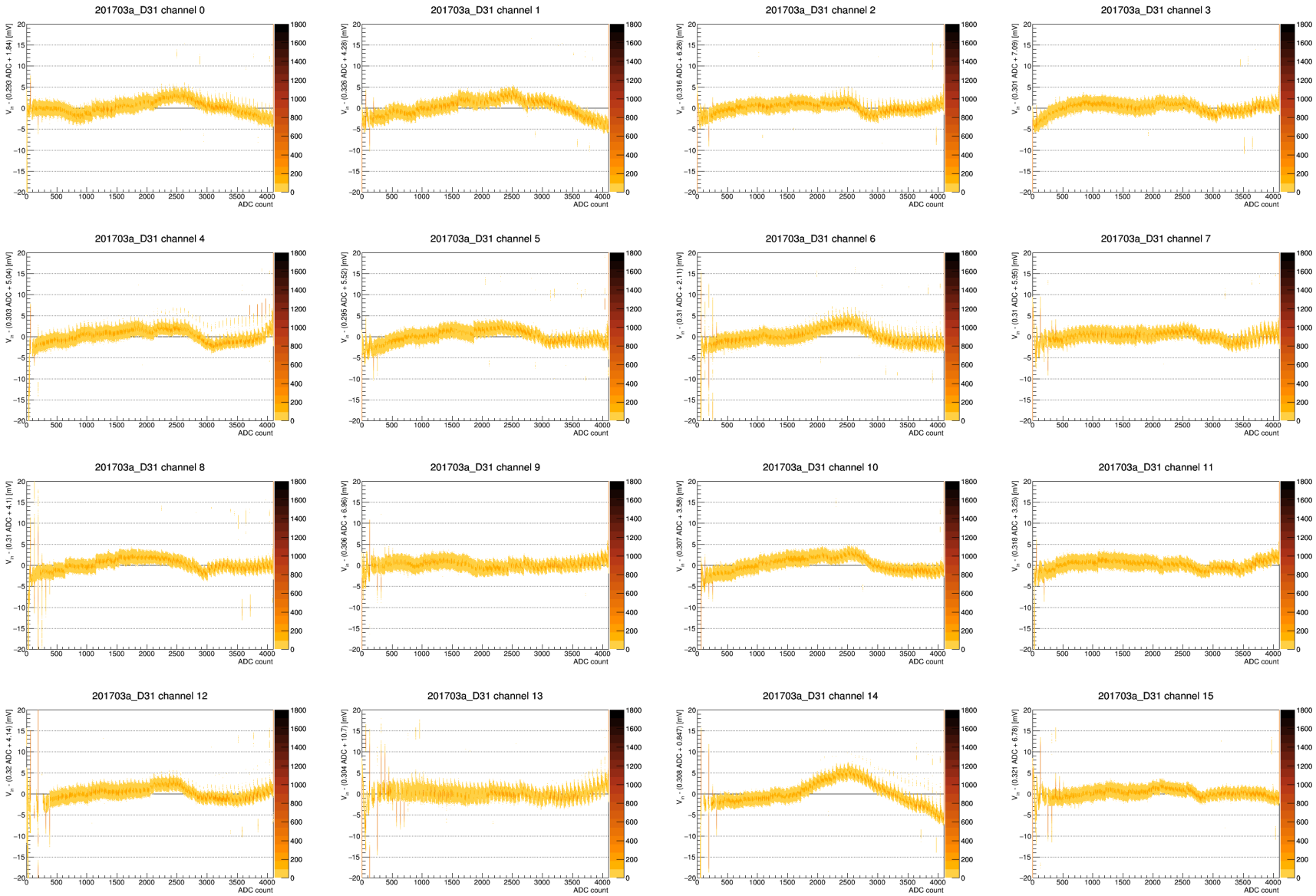
Chip D66 (rank=19, Q=0.945, a=0.996, m=0.966)



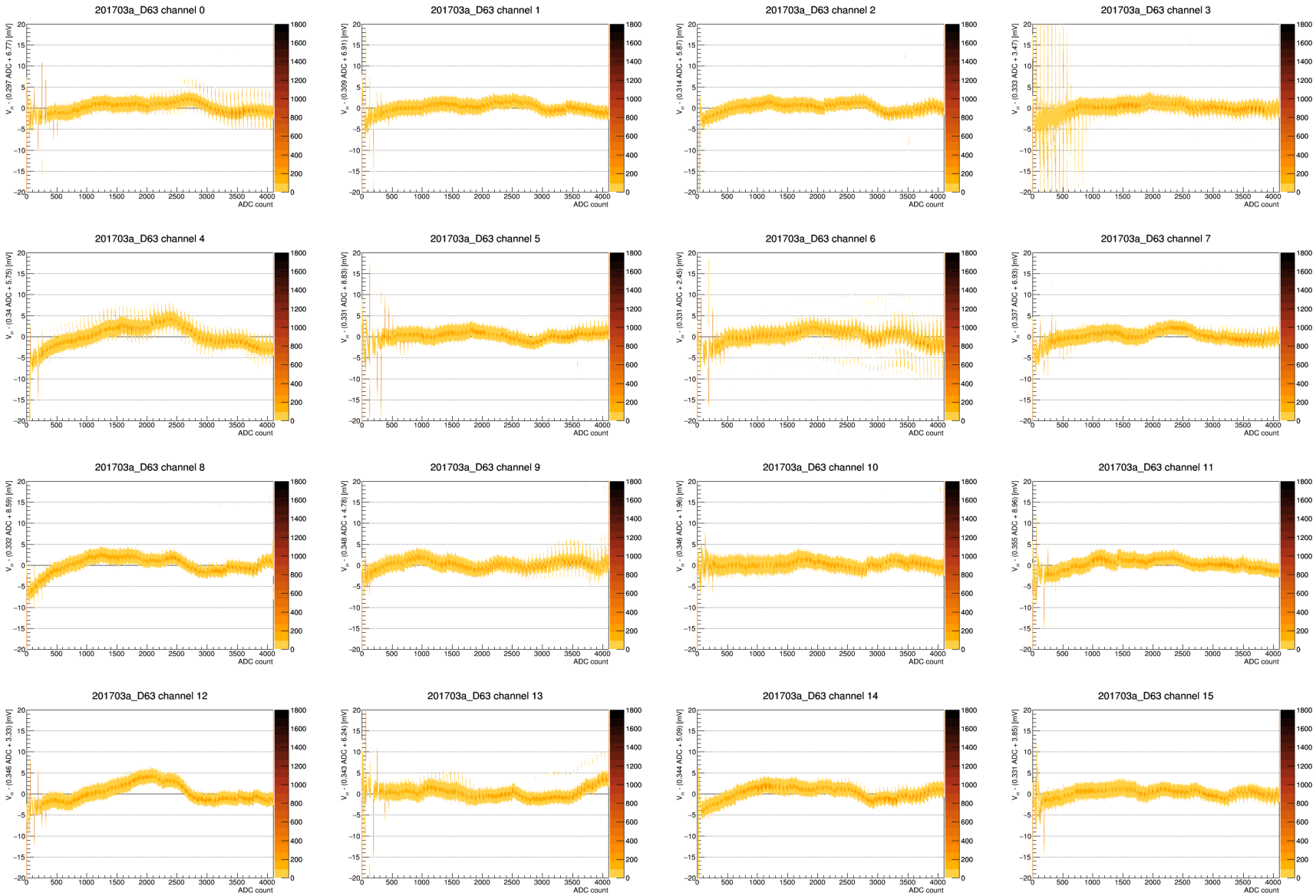
Chip D18 (rank=20, Q=0.943, a=0.996, m=0.980)



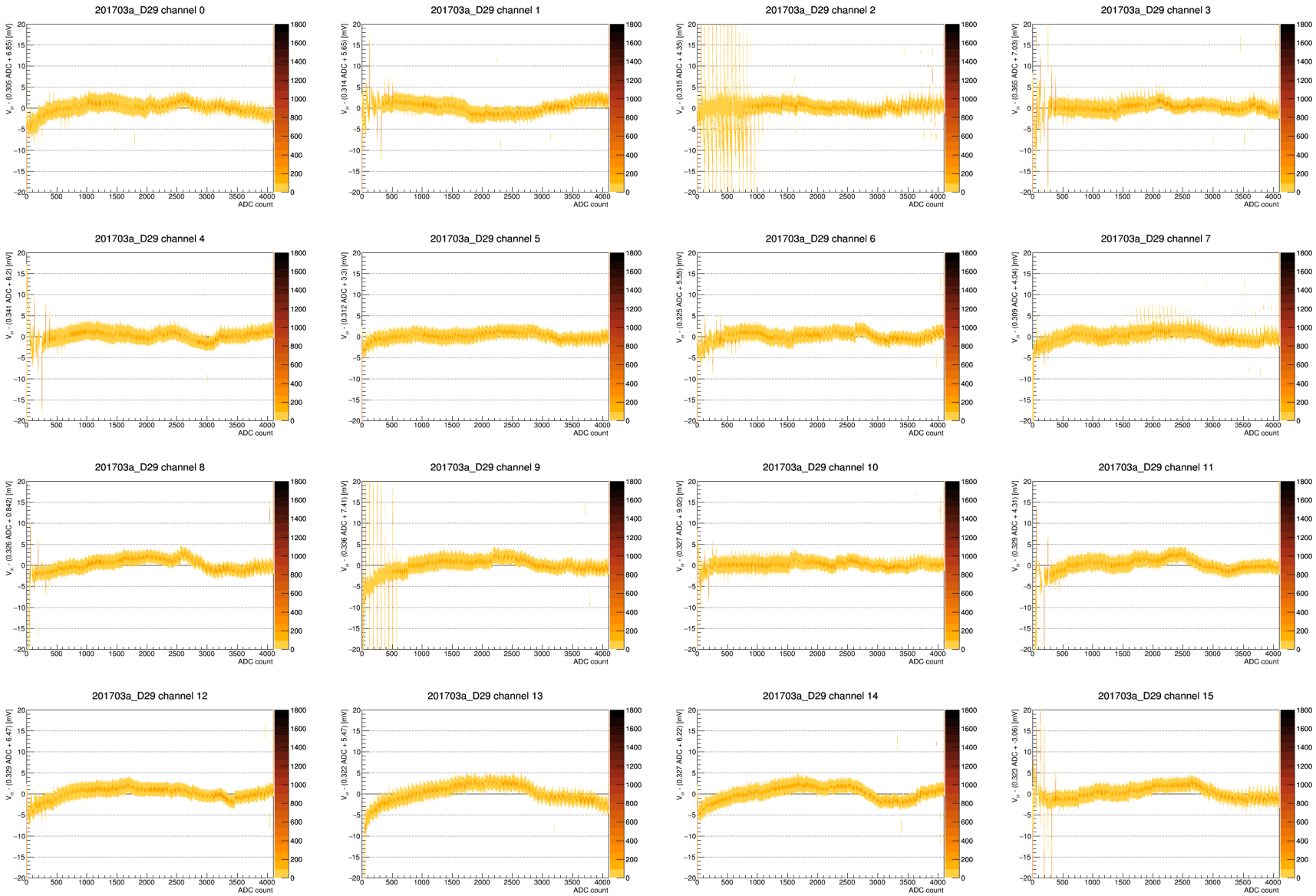
Chip D31 (rank=21, Q=0.942, a=0.996, m=0.975)



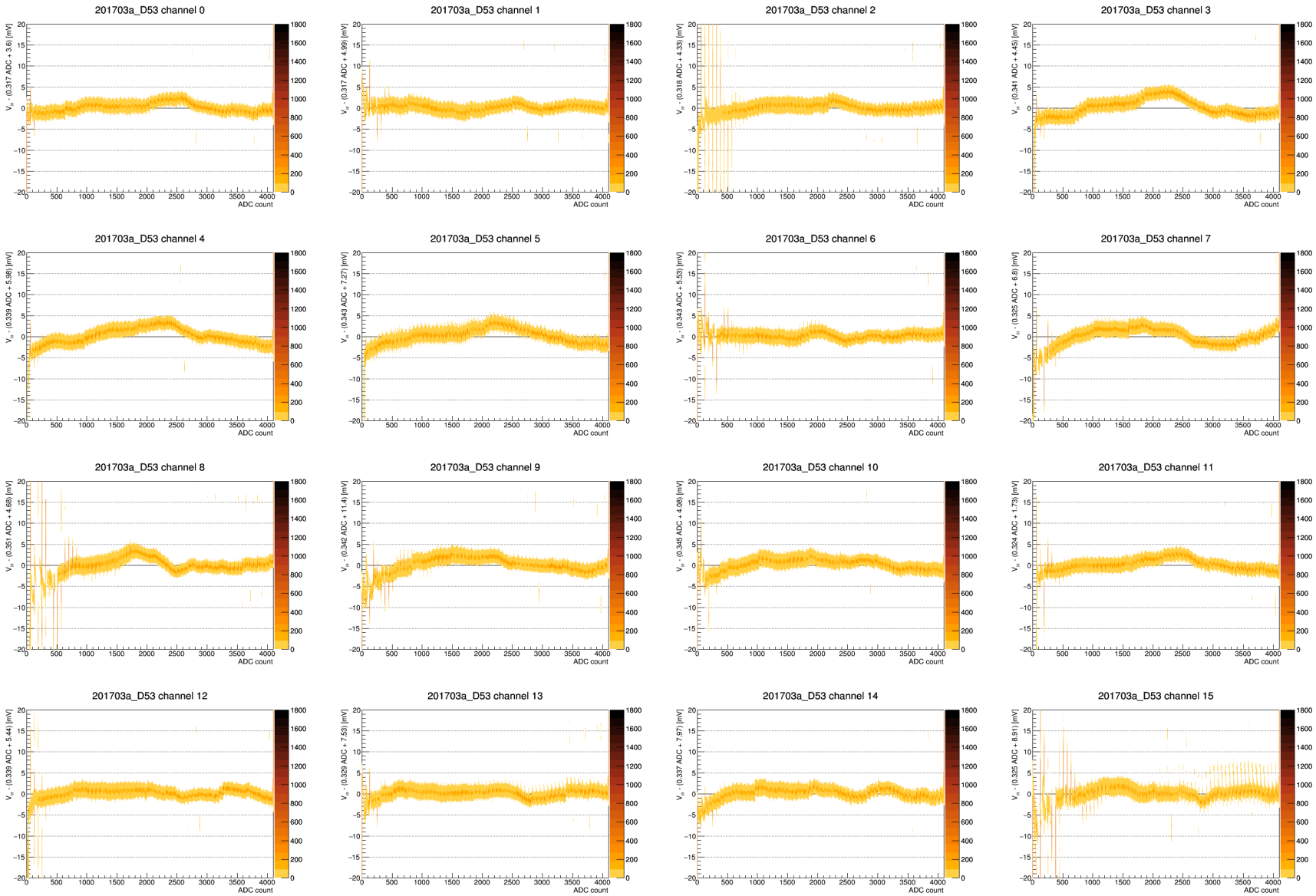
Chip D63 (rank=22, Q=0.941, a=0.996, m=0.978)



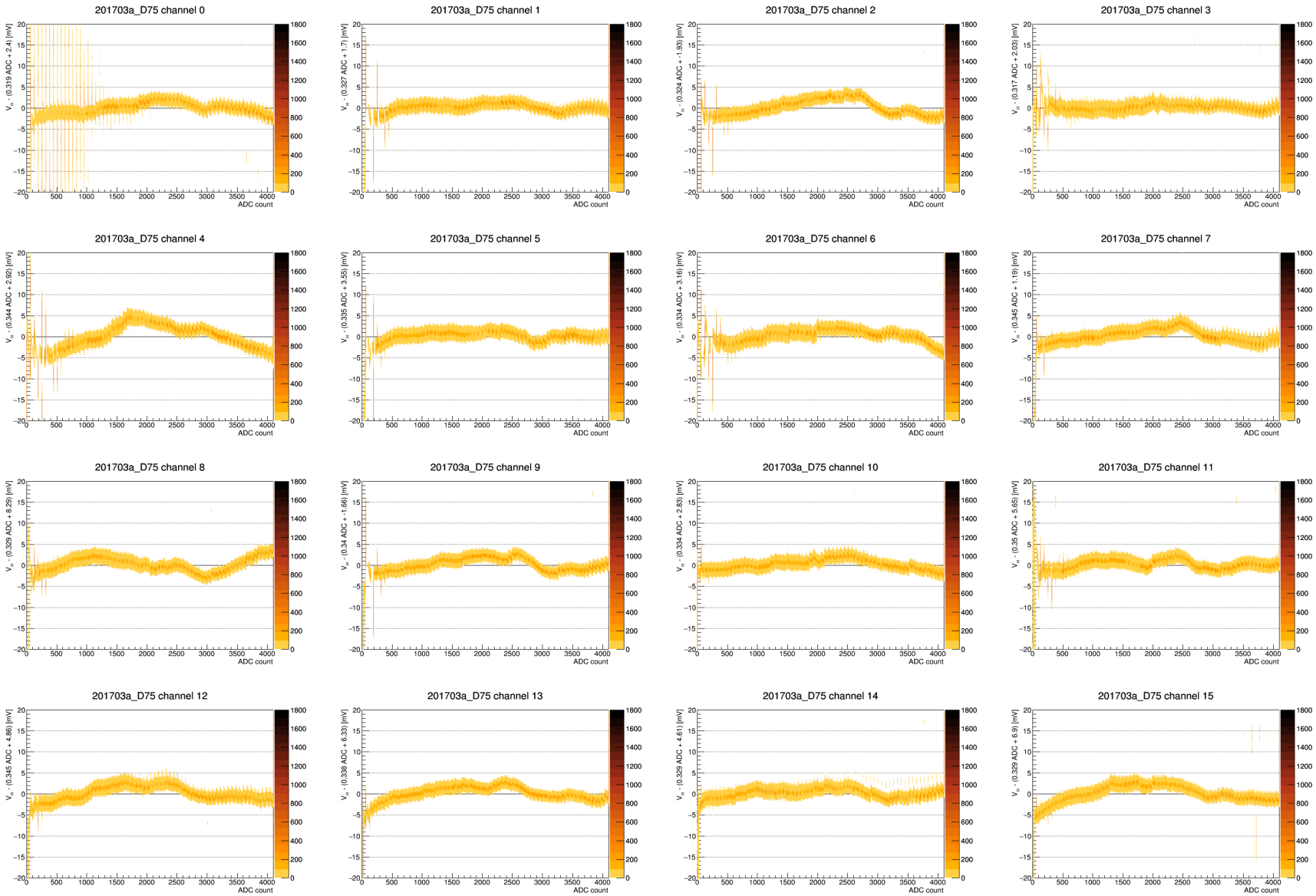
Chip D29 (rank=23, Q=0.940, a=0.996, m=0.951)



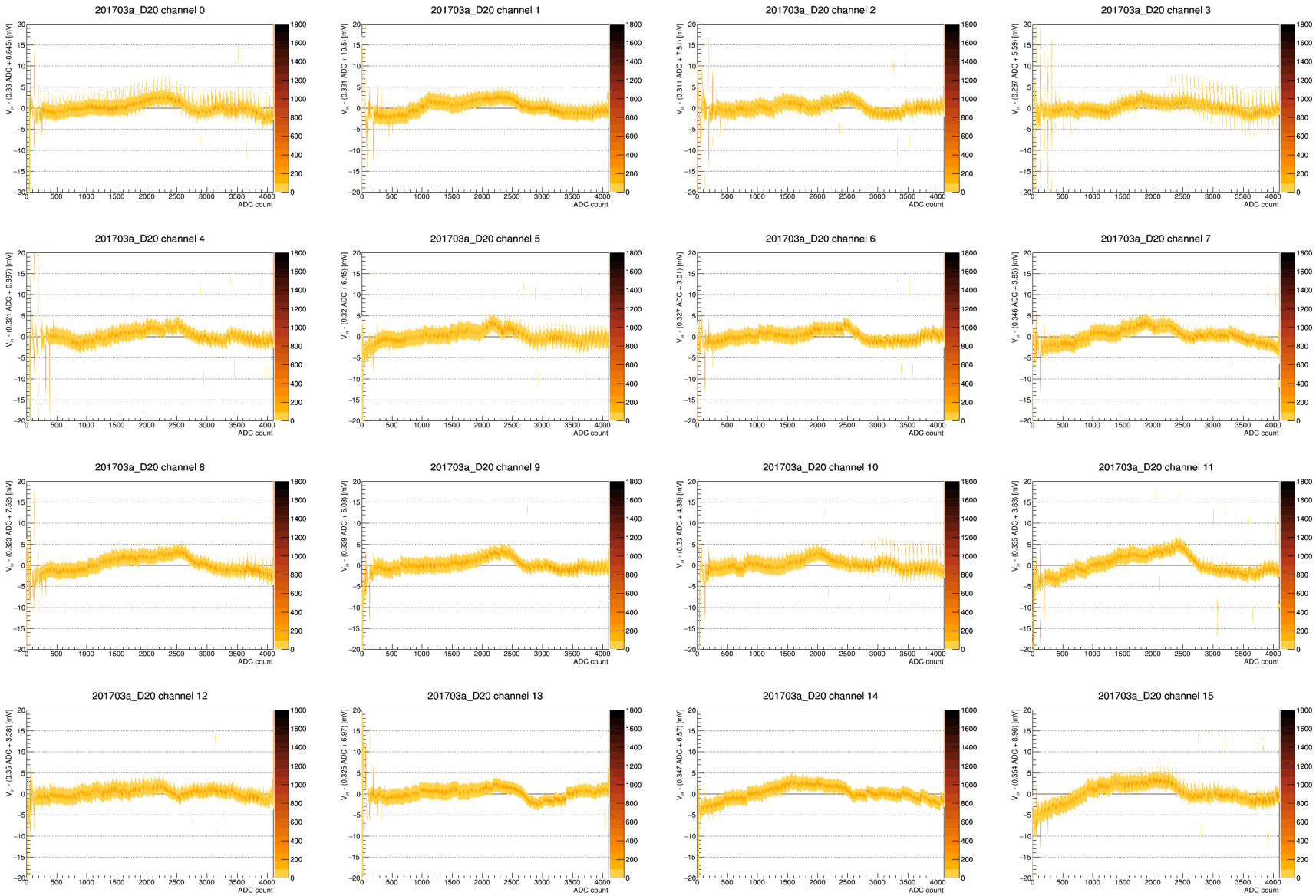
Chip D53 (rank=24, Q=0.926, a=0.995, m=0.963)



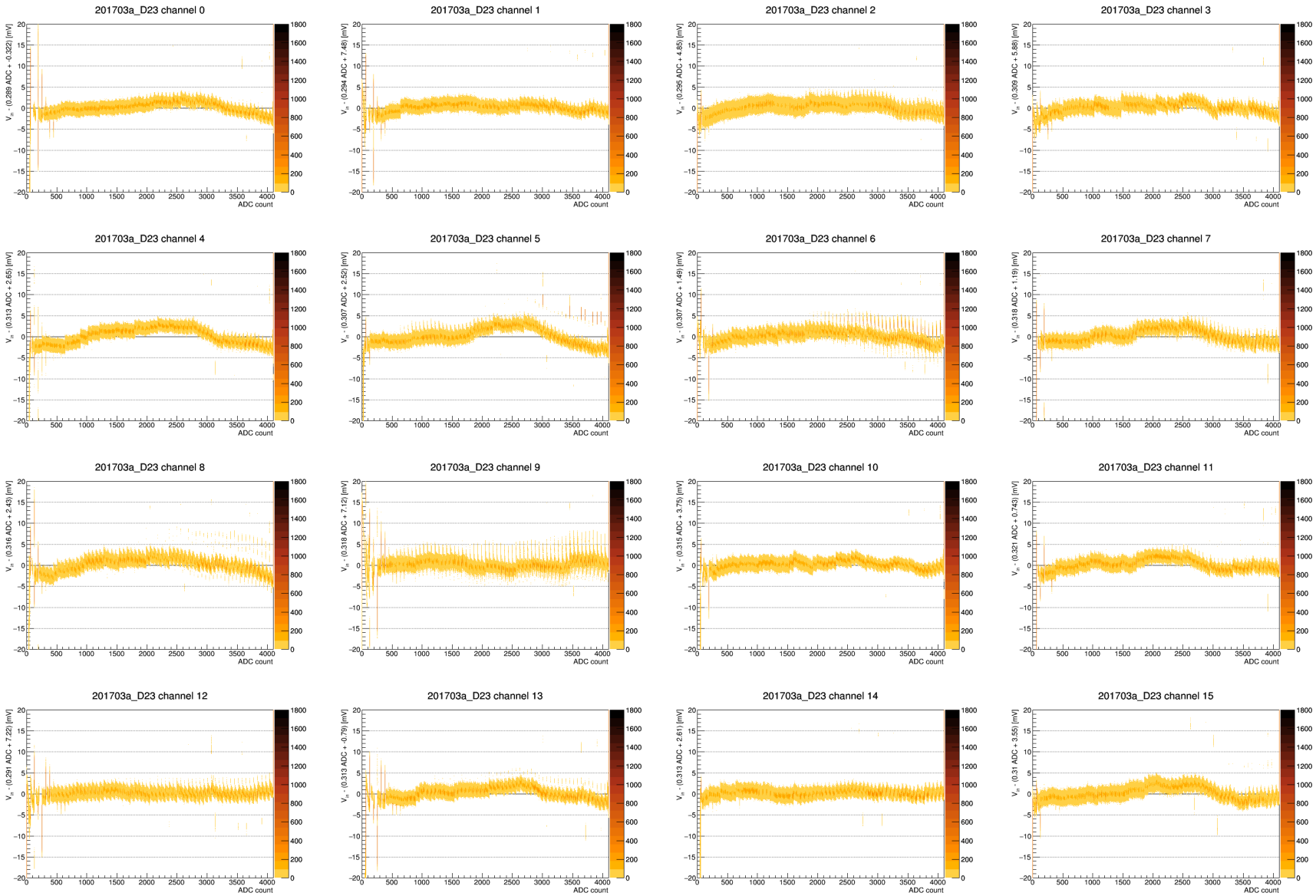
Chip D75 (rank=25, Q=0.924, a=0.995, m=0.936)



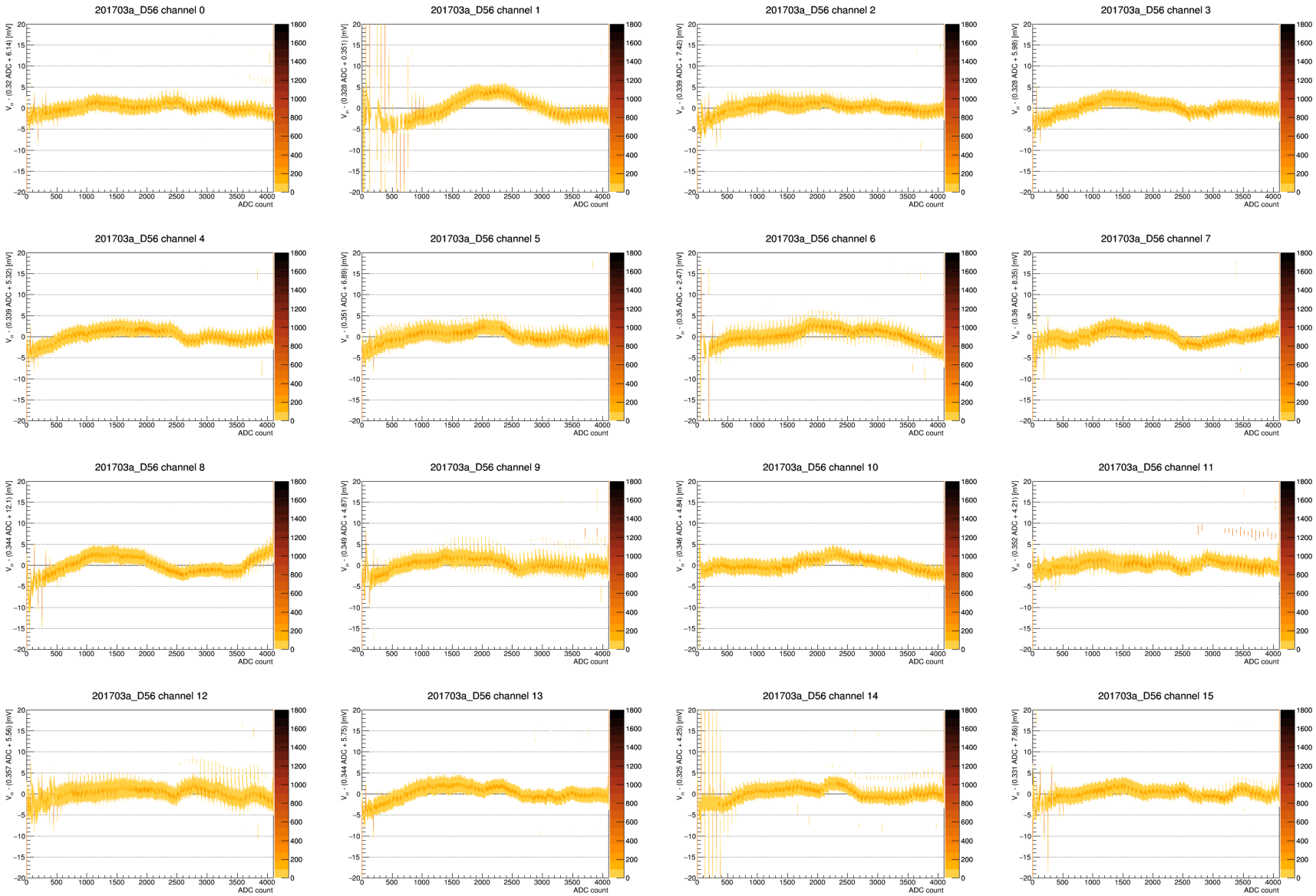
Chip D20 (rank=26, Q=0.919, a=0.994, m=0.974)



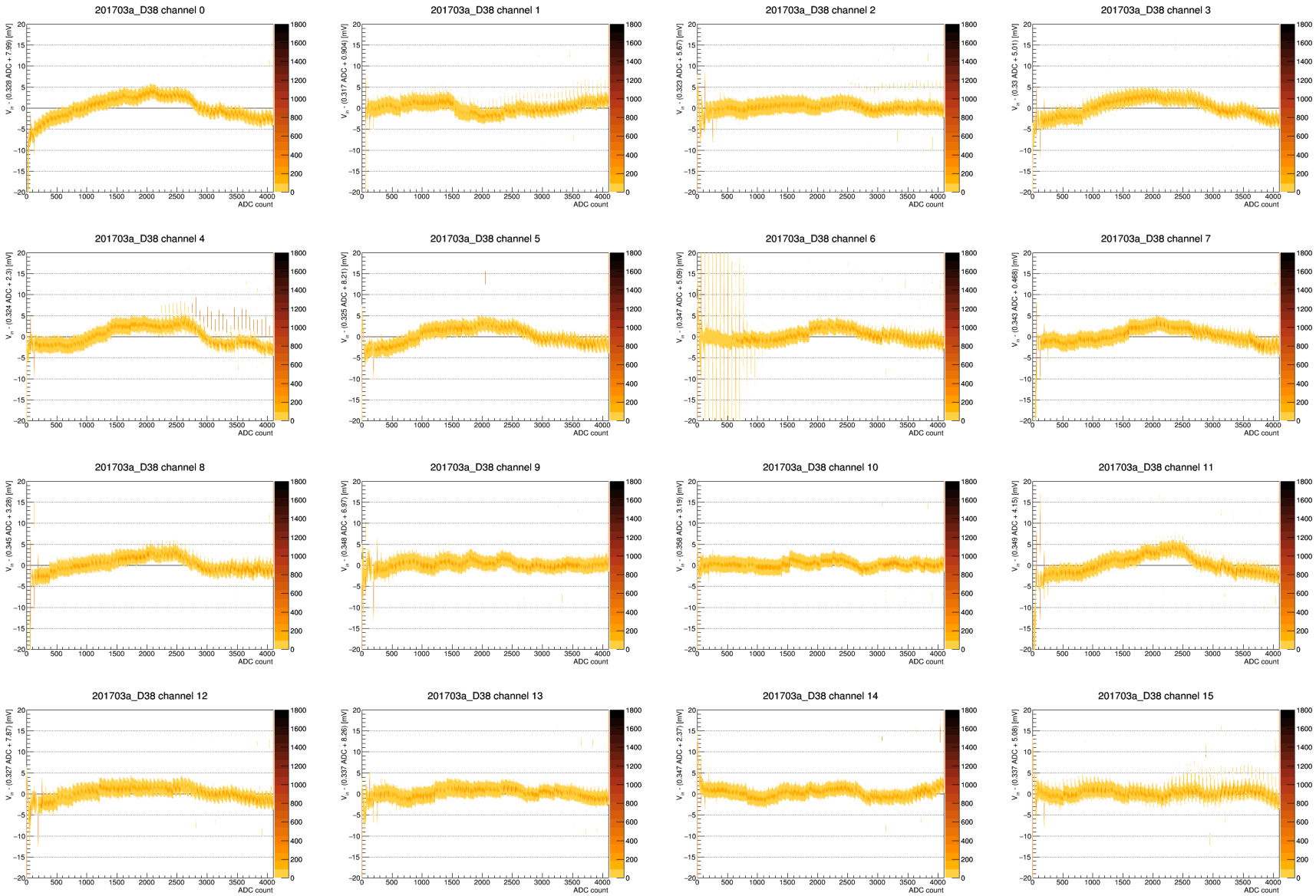
Chip D23 (rank=27, Q=0.905, a=0.993, m=0.961)



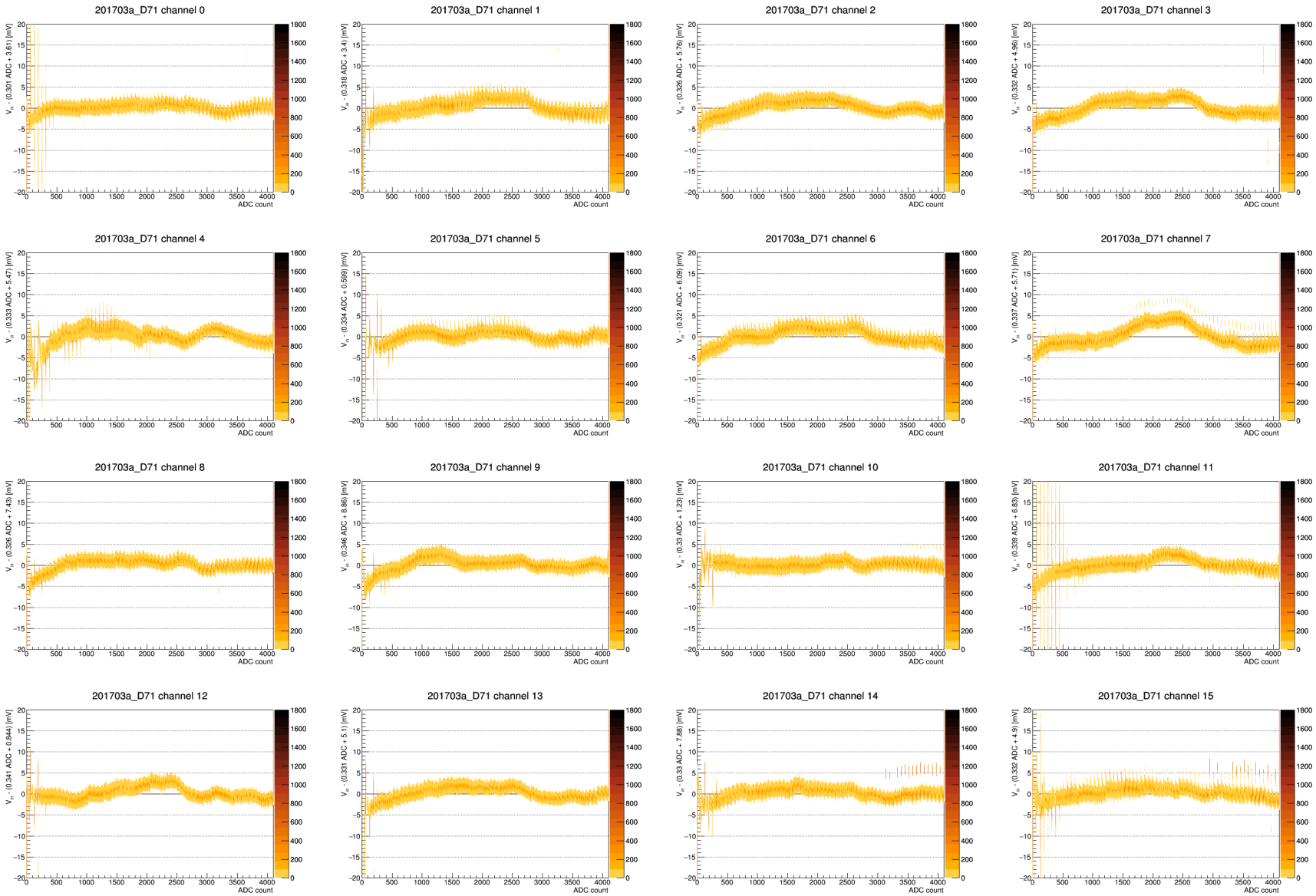
Chip D56 (rank=28, Q=0.904, a=0.993, m=0.960)



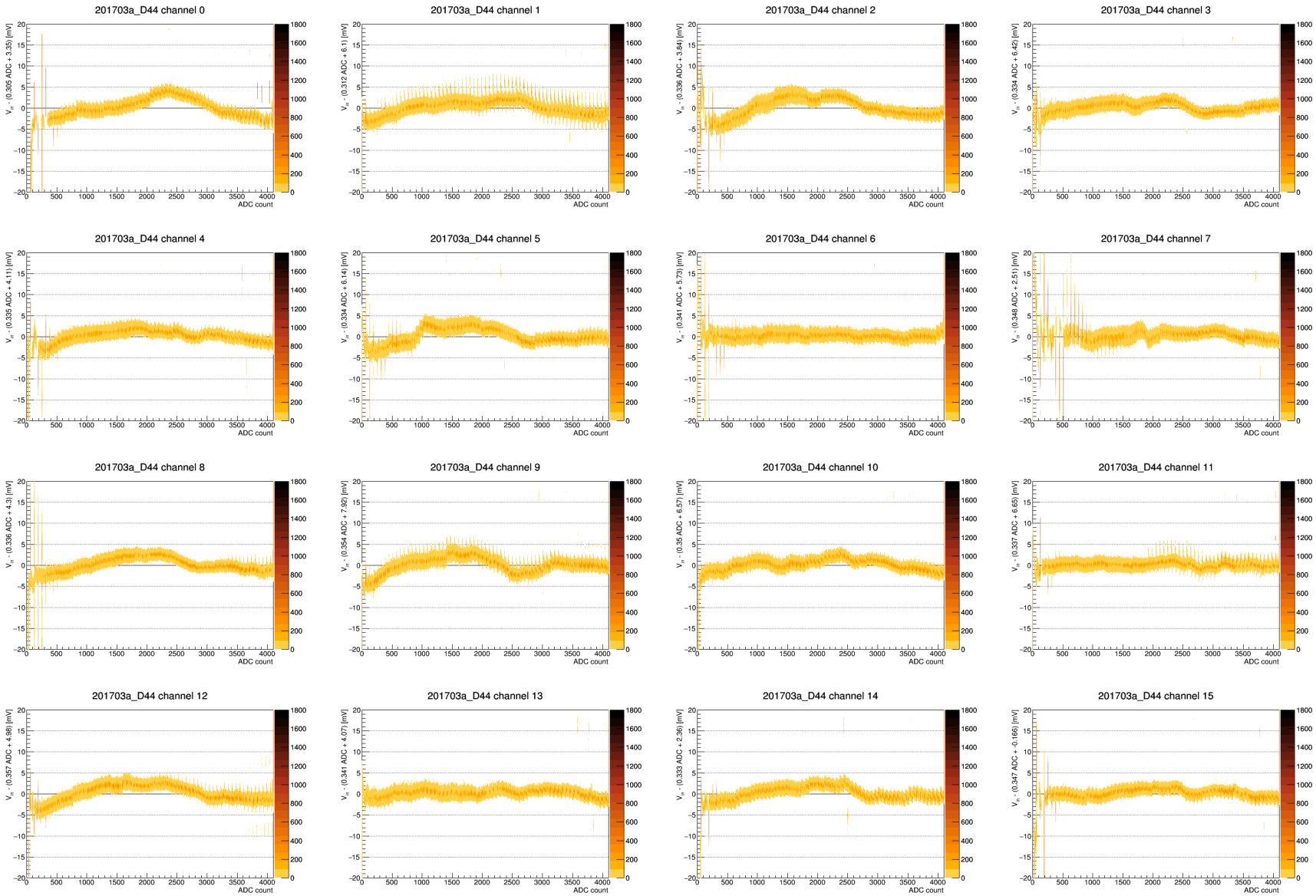
Chip D38 (rank=29, Q=0.895, a=0.993, m=0.930)



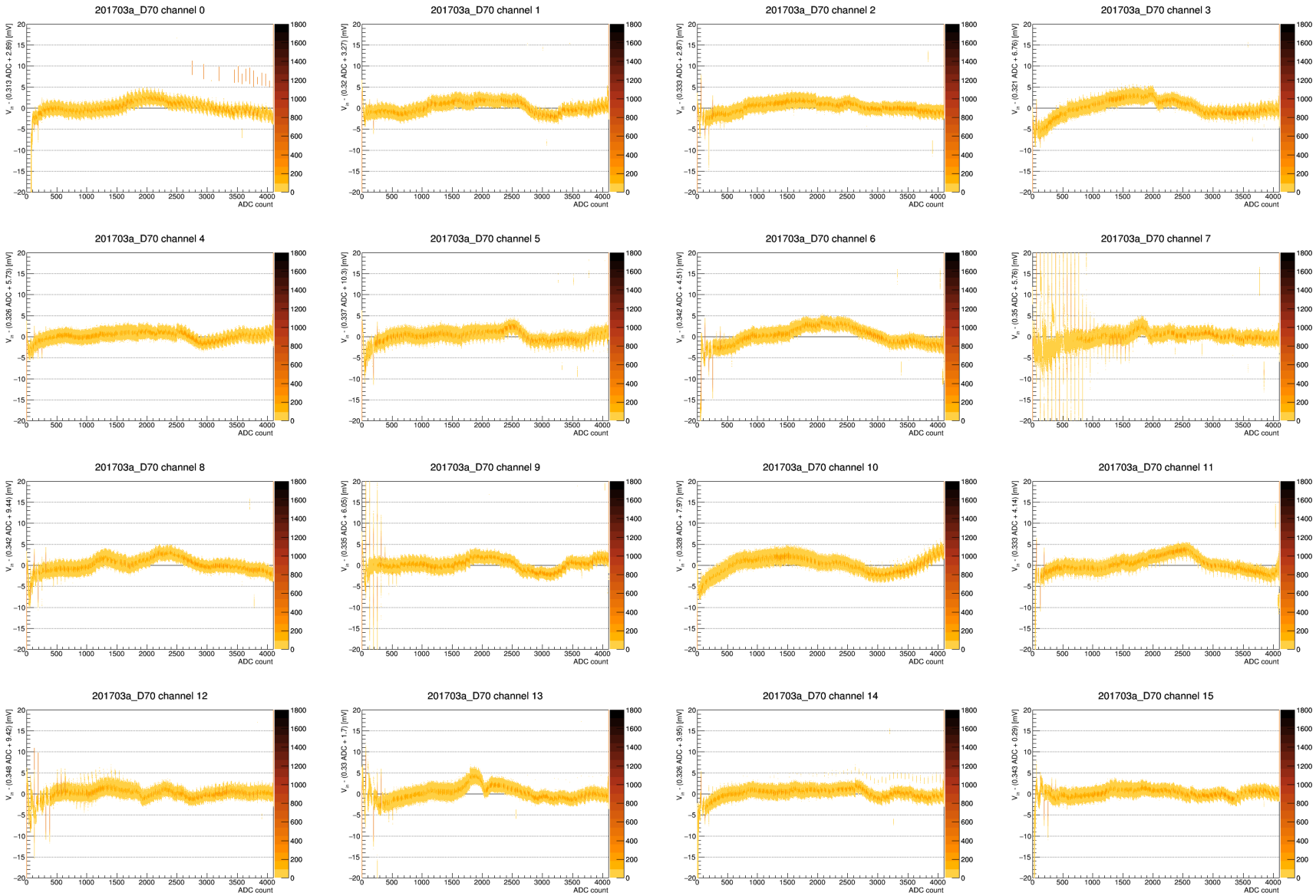
Chip D71 (rank=30, Q=0.893, a=0.993, m=0.956)



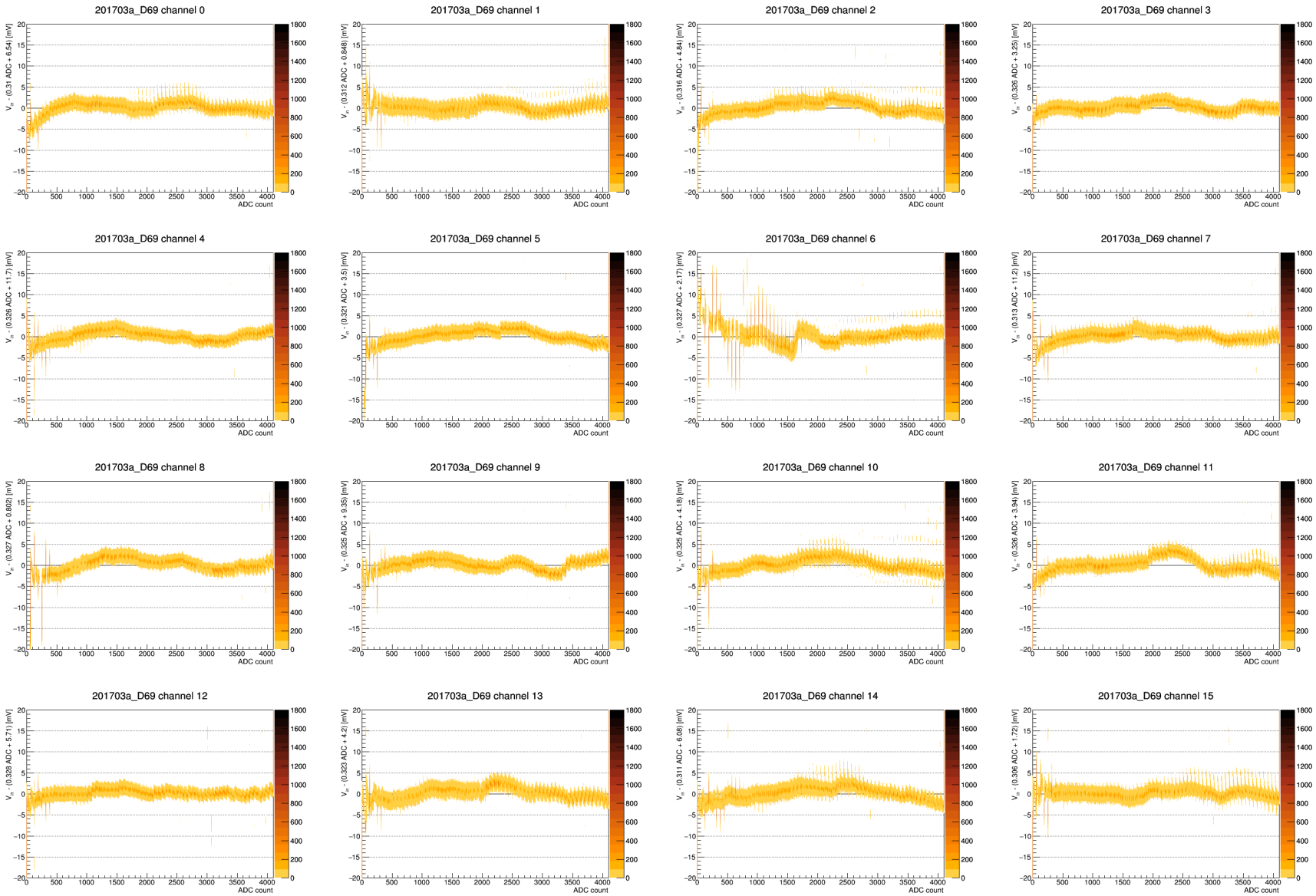
Chip D44 (rank=31, Q=0.877, a=0.991, m=0.960)



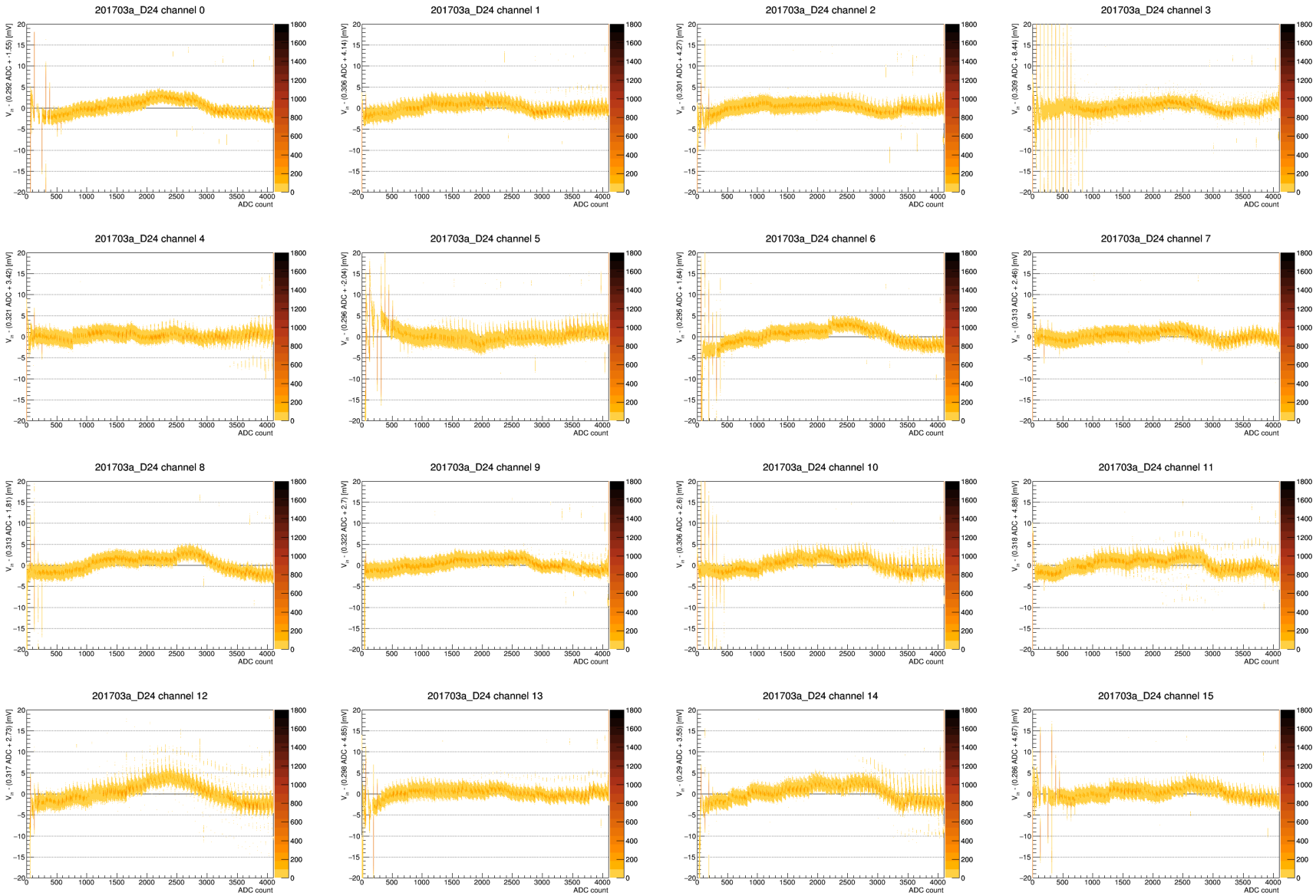
Chip D70 (rank=32, Q=0.875, a=0.991, m=0.924)



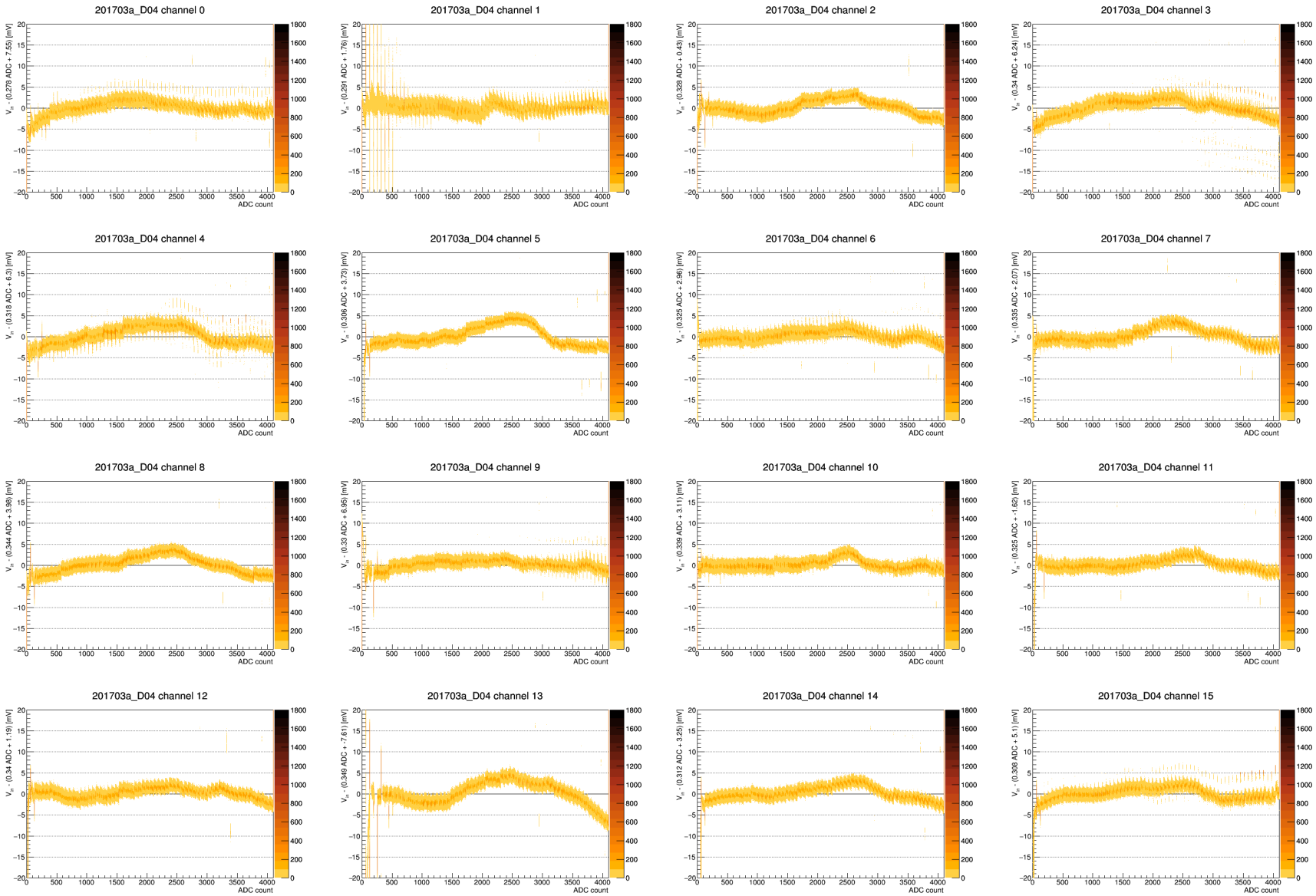
Chip D69 (rank=33, Q=0.875, a=0.992, m=0.895)



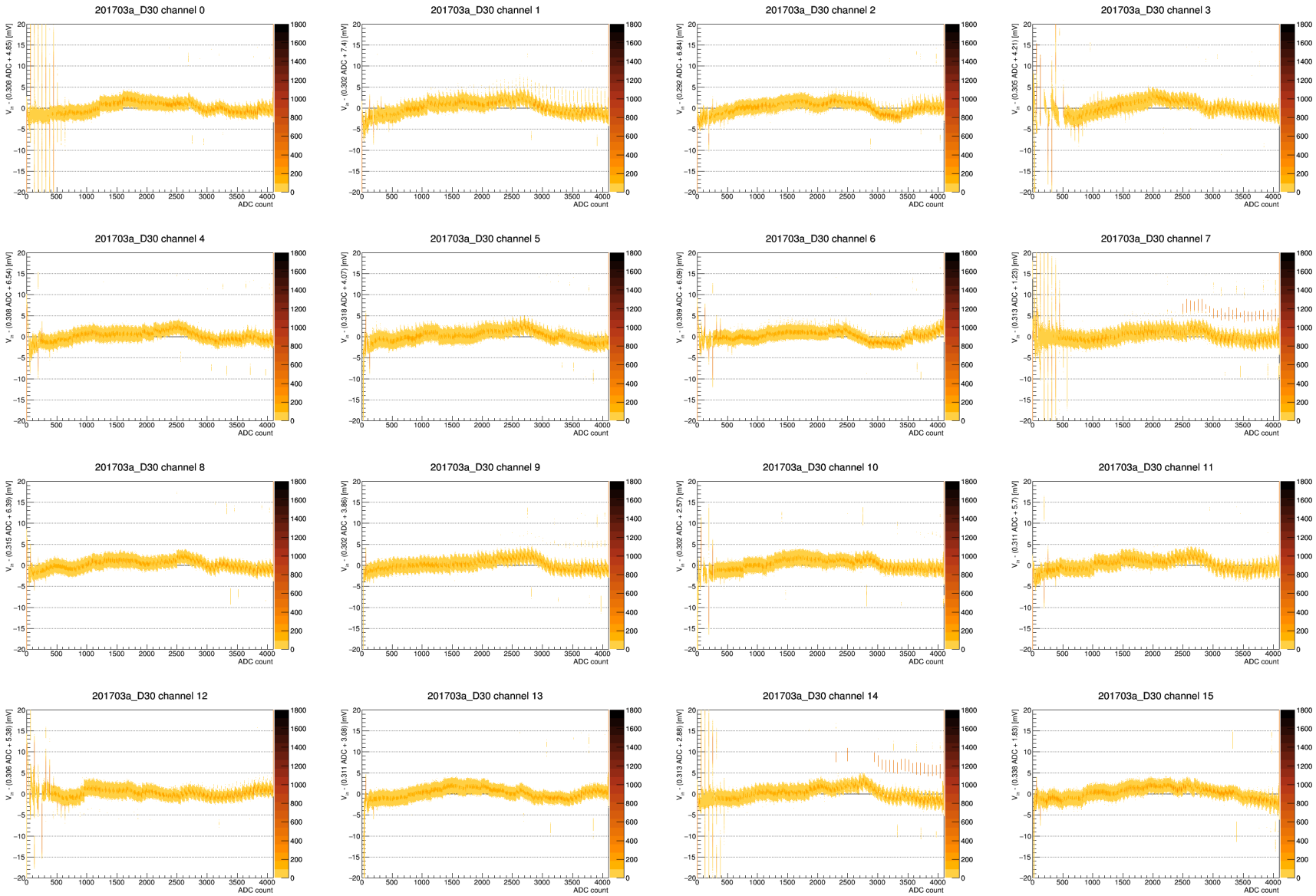
Chip D24 (rank=34, Q=0.873, a=0.991, m=0.968)



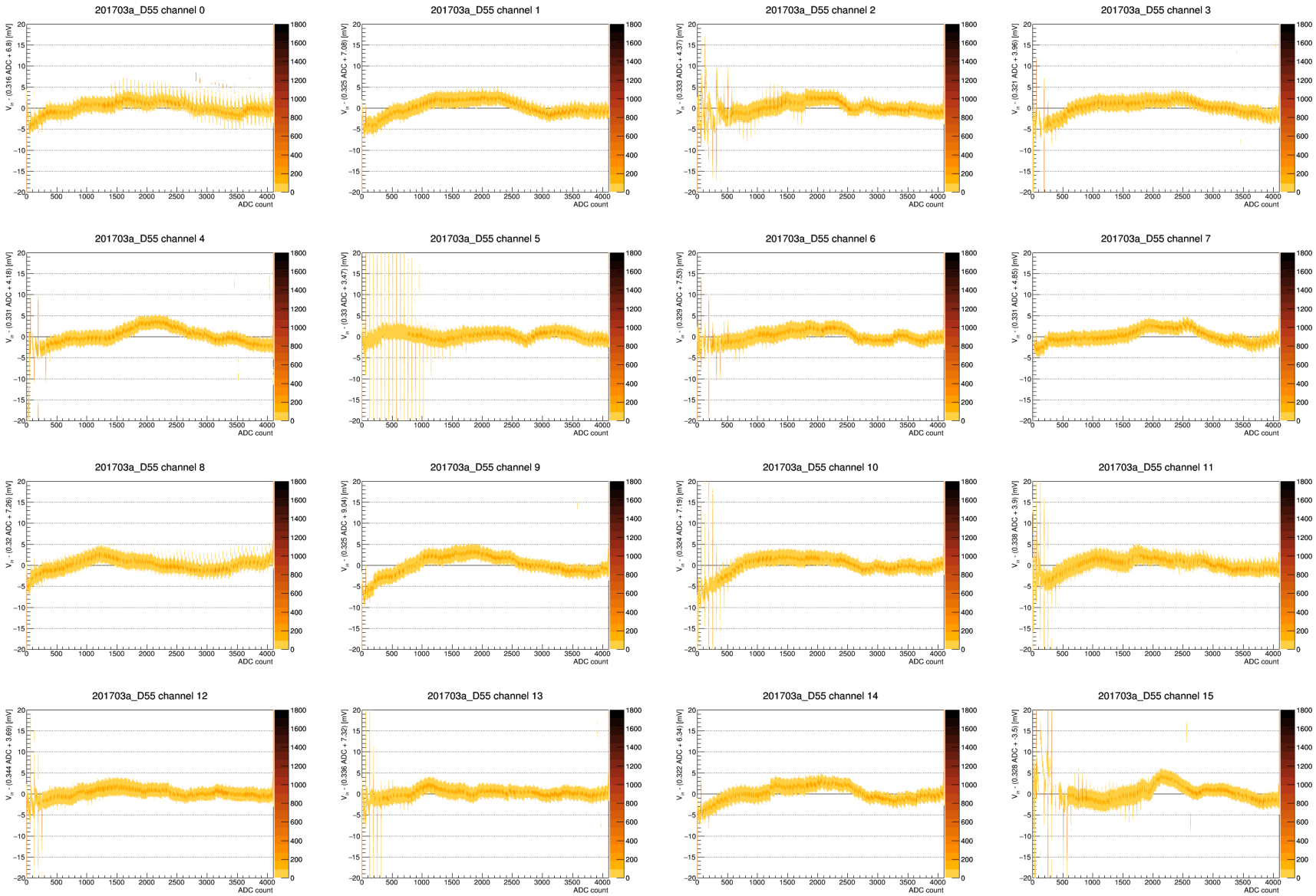
Chip D04 (rank=35, Q=0.867, a=0.991, m=0.935)



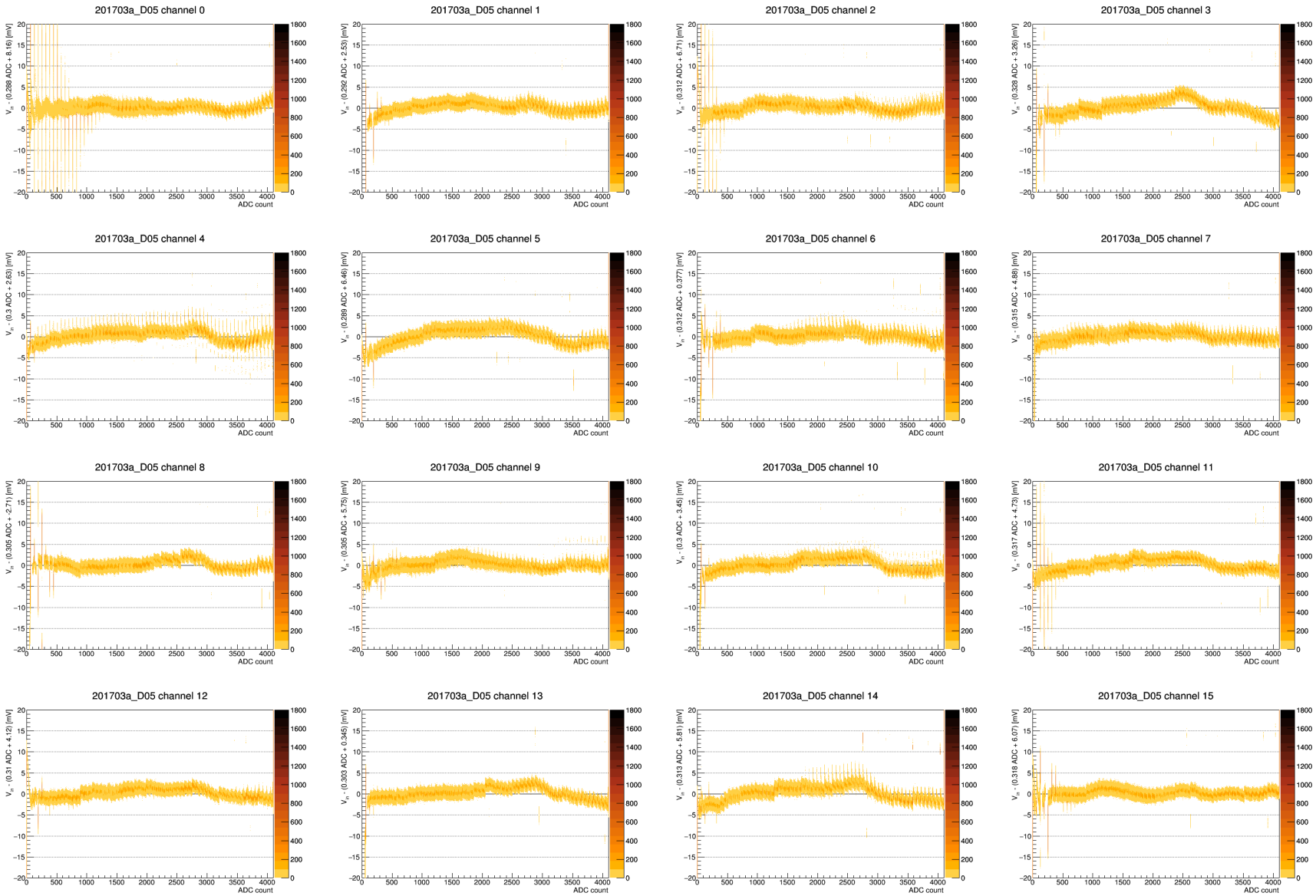
Chip D30 (rank=36, Q=0.864, a=0.991, m=0.933)



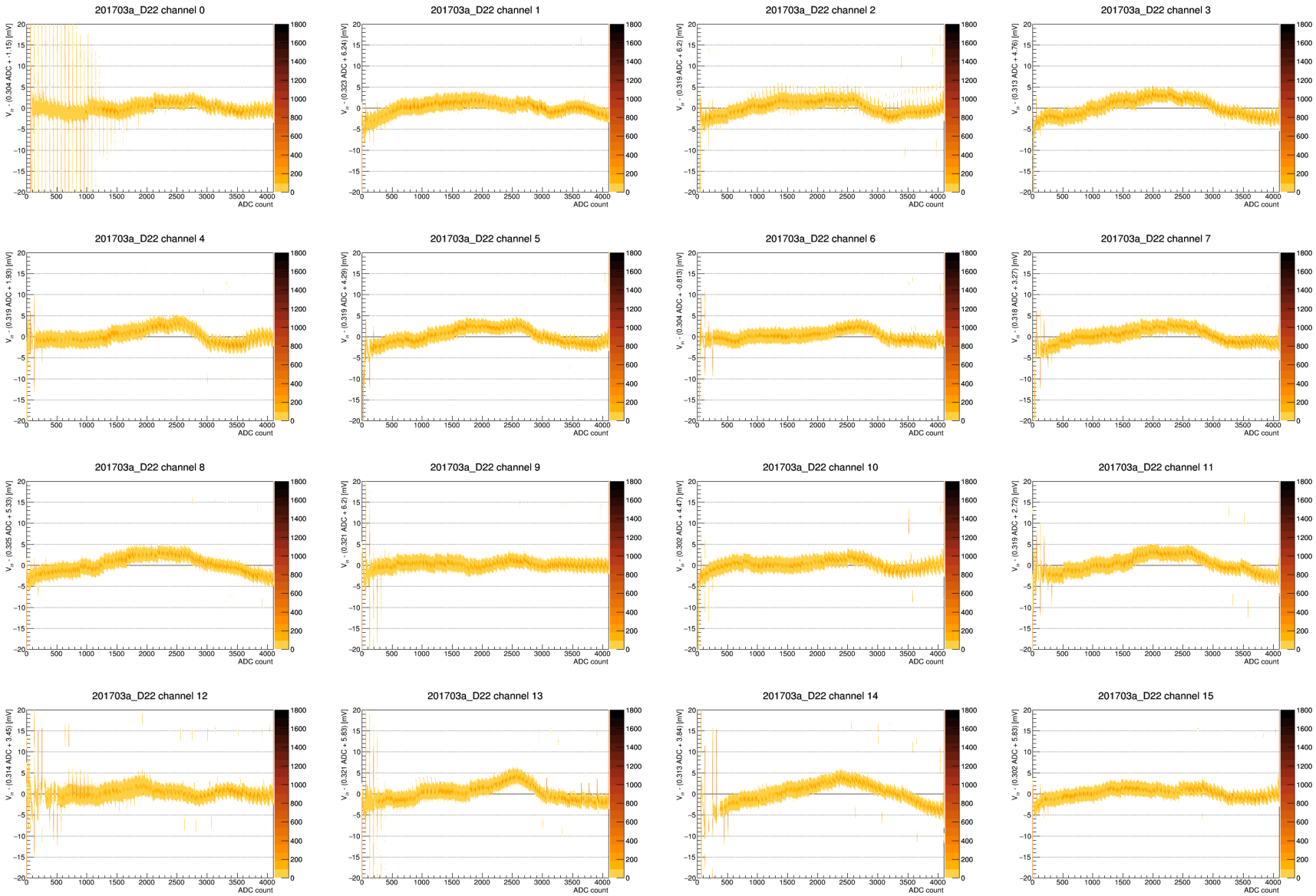
Chip D55 (rank=37, Q=0.863, a=0.991, m=0.942)



Chip D05 (rank=38, Q=0.857, a=0.990, m=0.934)

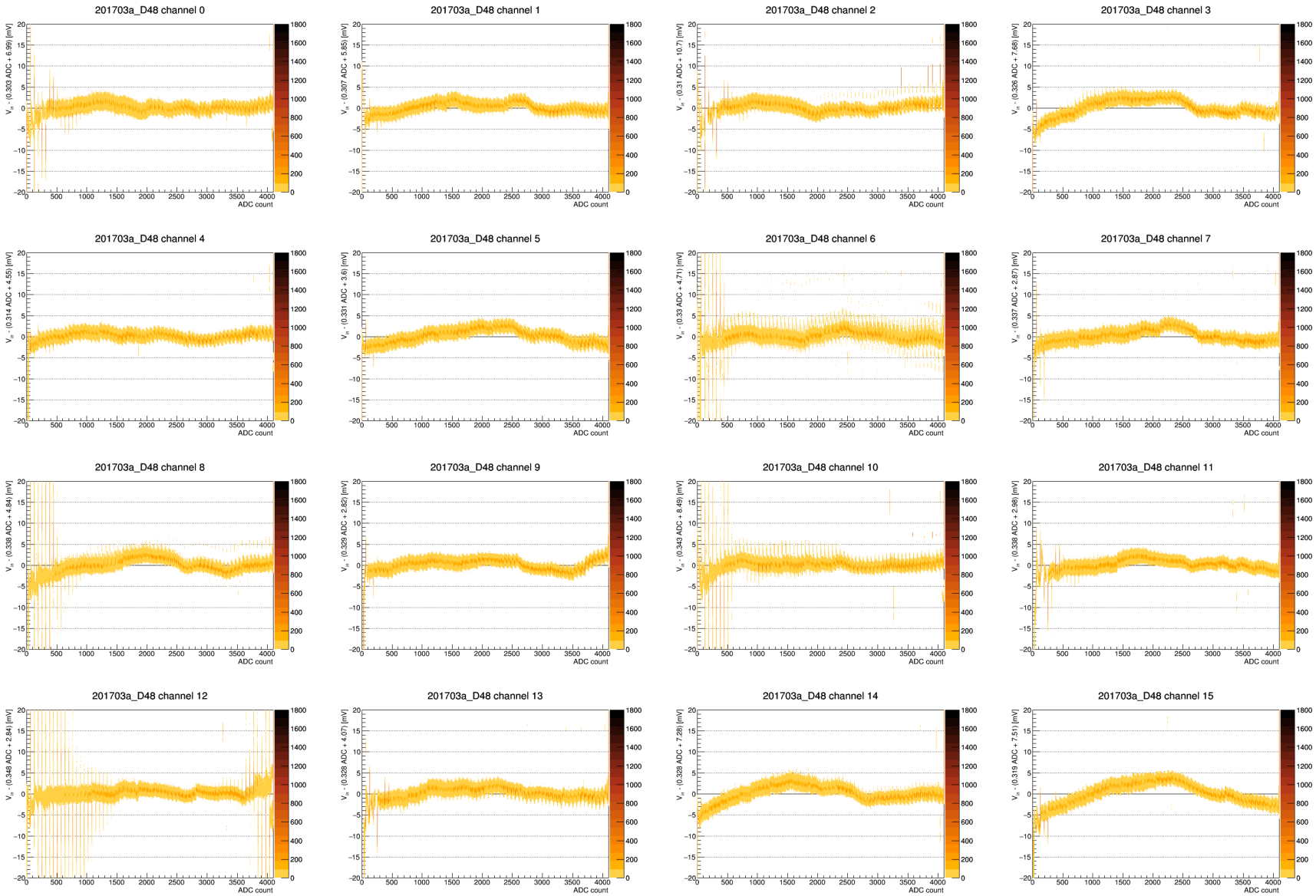


Chip D22 (rank=39, Q=0.850, a=0.990, m=0.912)

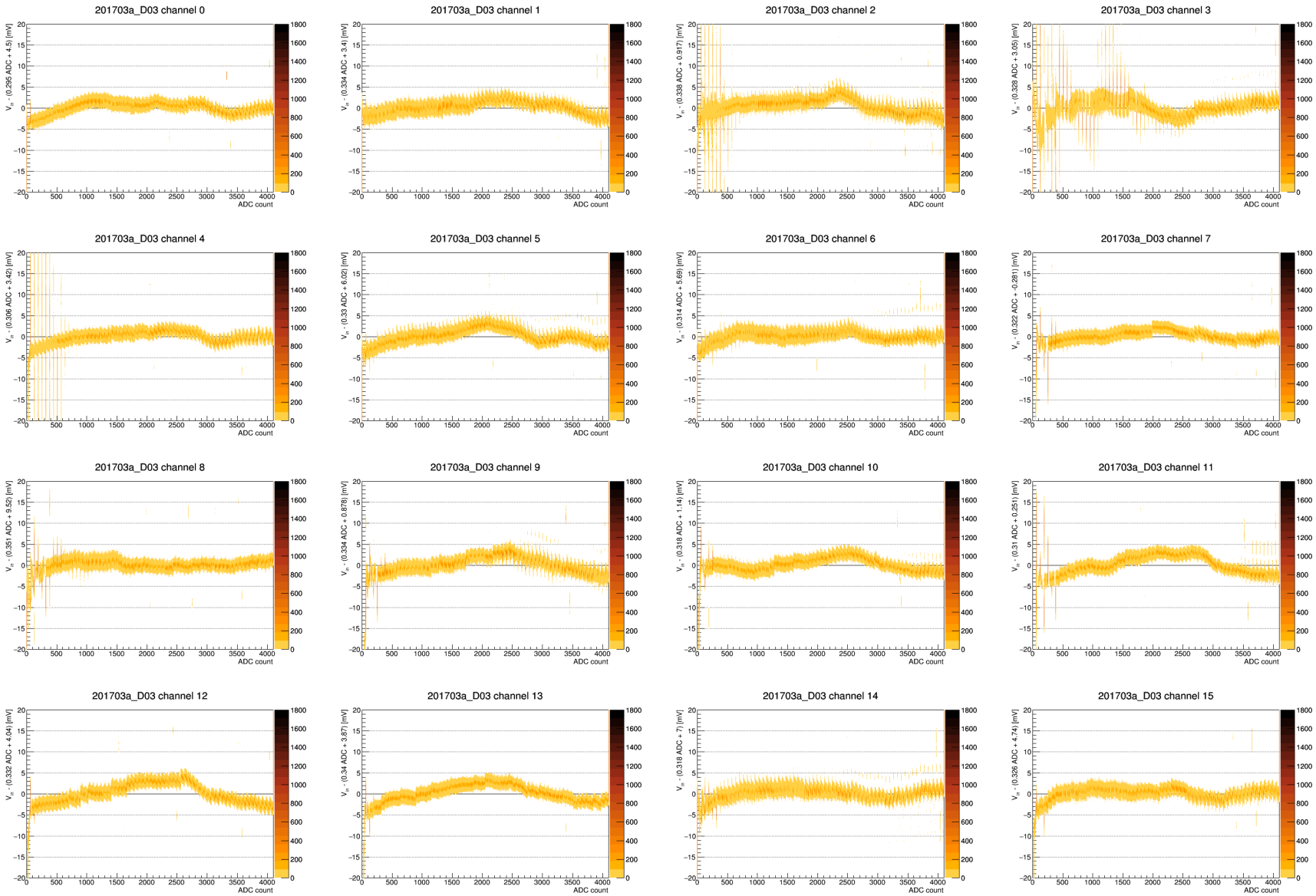


Poor chips

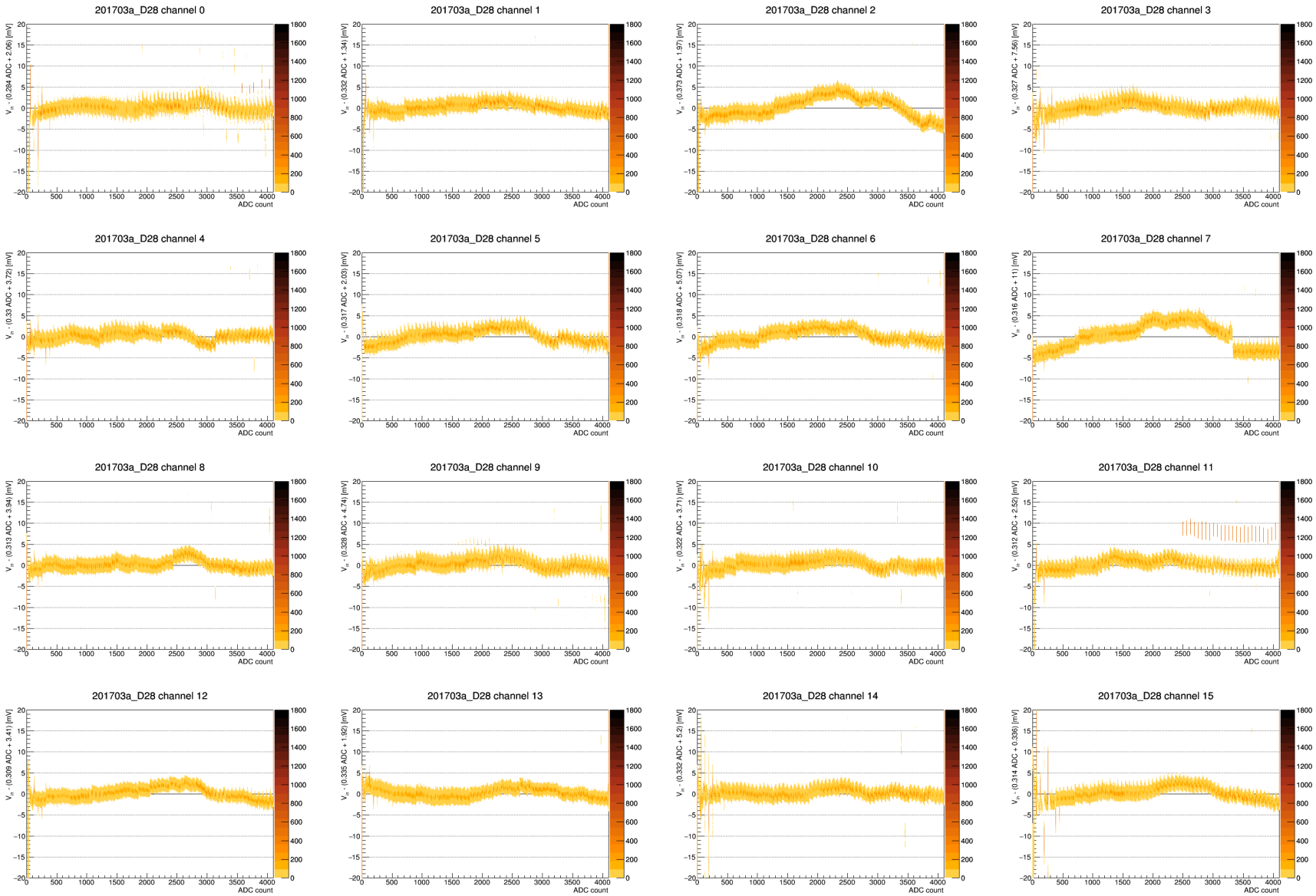
Chip D48 (rank=40, Q=0.845, a=0.989, m=0.922)



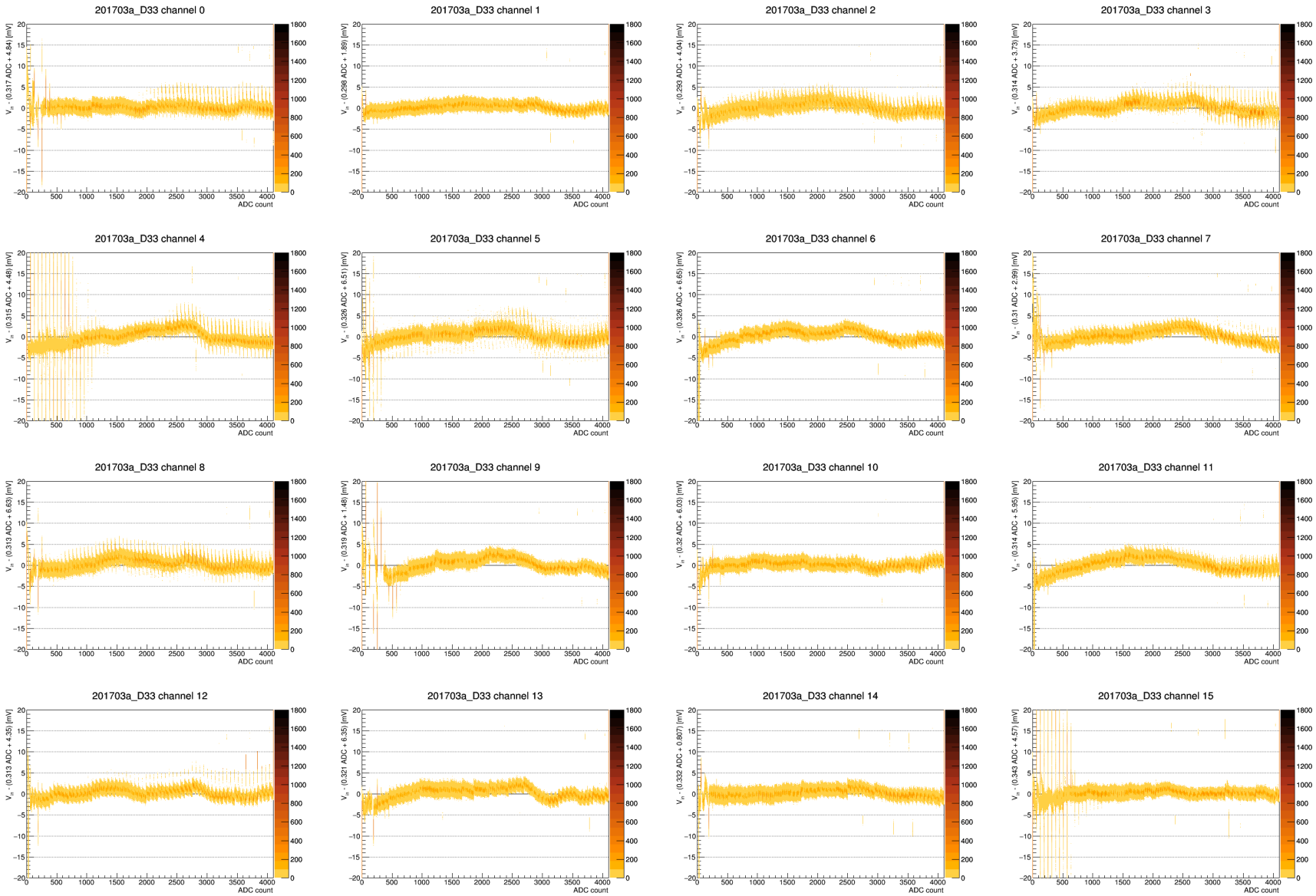
Chip D03 (rank=41, Q=0.841, a=0.989, m=0.881)



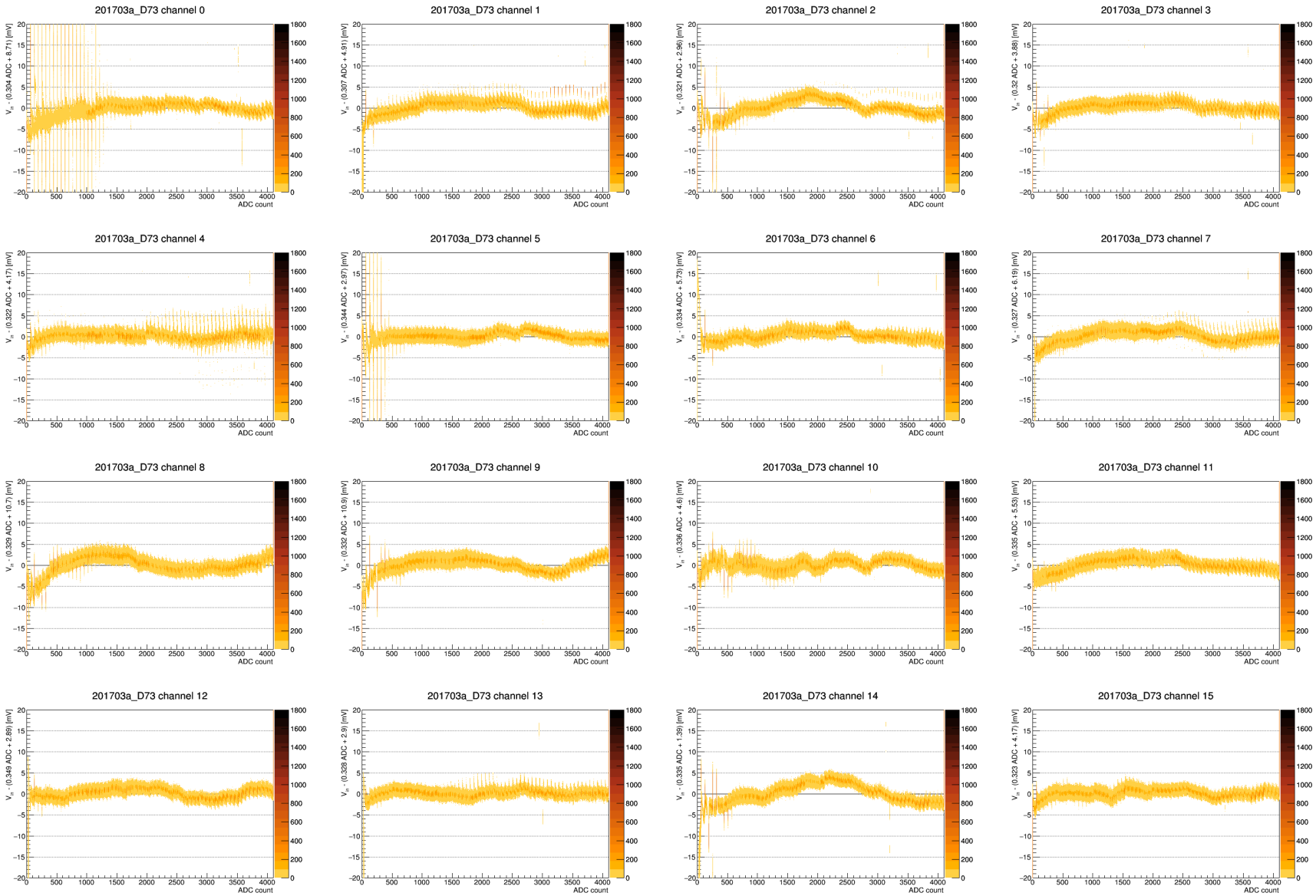
Chip D28 (rank=42, Q=0.841, a=0.989, m=0.903)



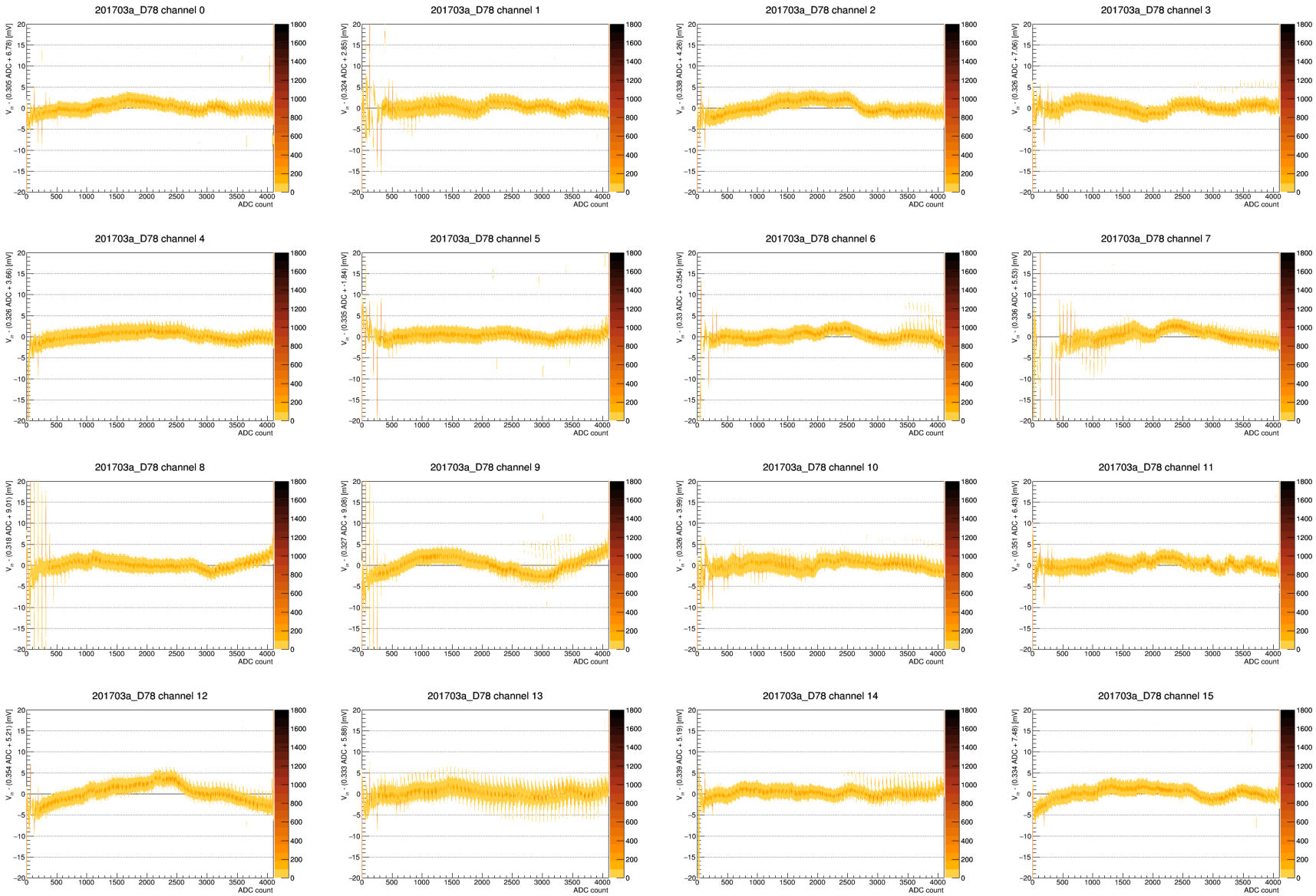
Chip D33 (rank=43, Q=0.833, a=0.988, m=0.942)



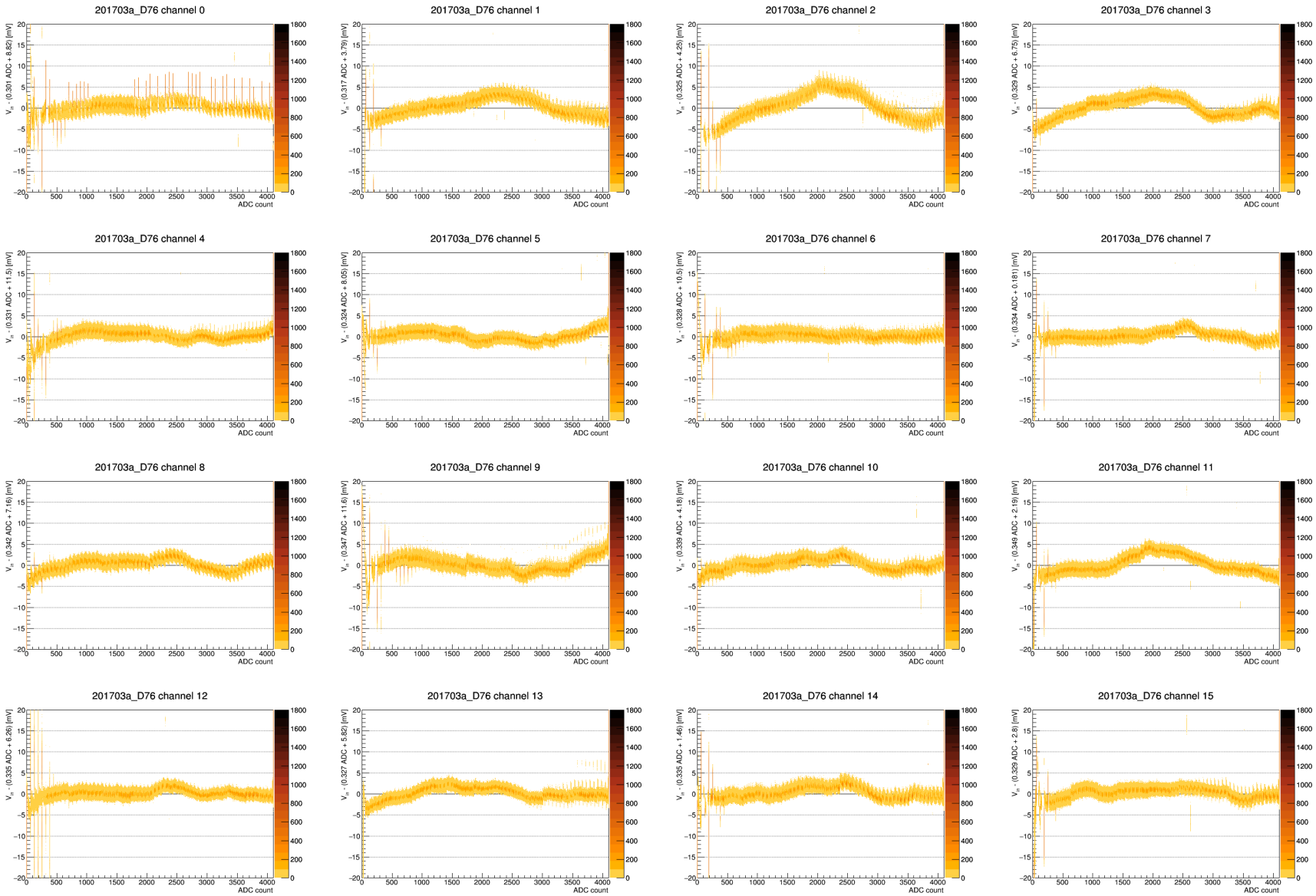
Chip D73 (rank=44, Q=0.818, a=0.987, m=0.902)



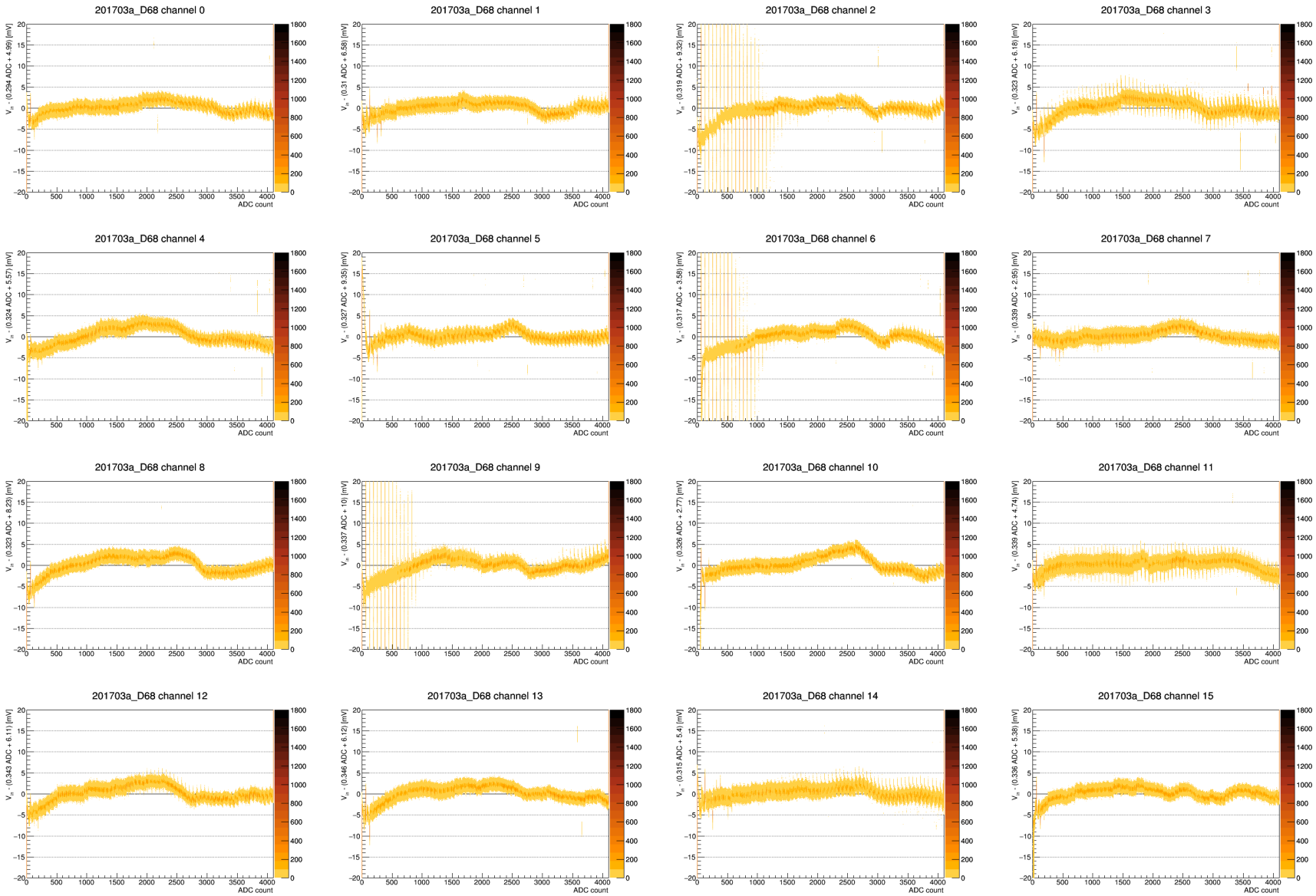
Chip D78 (rank=45, Q=0.799, a=0.986, m=0.862)



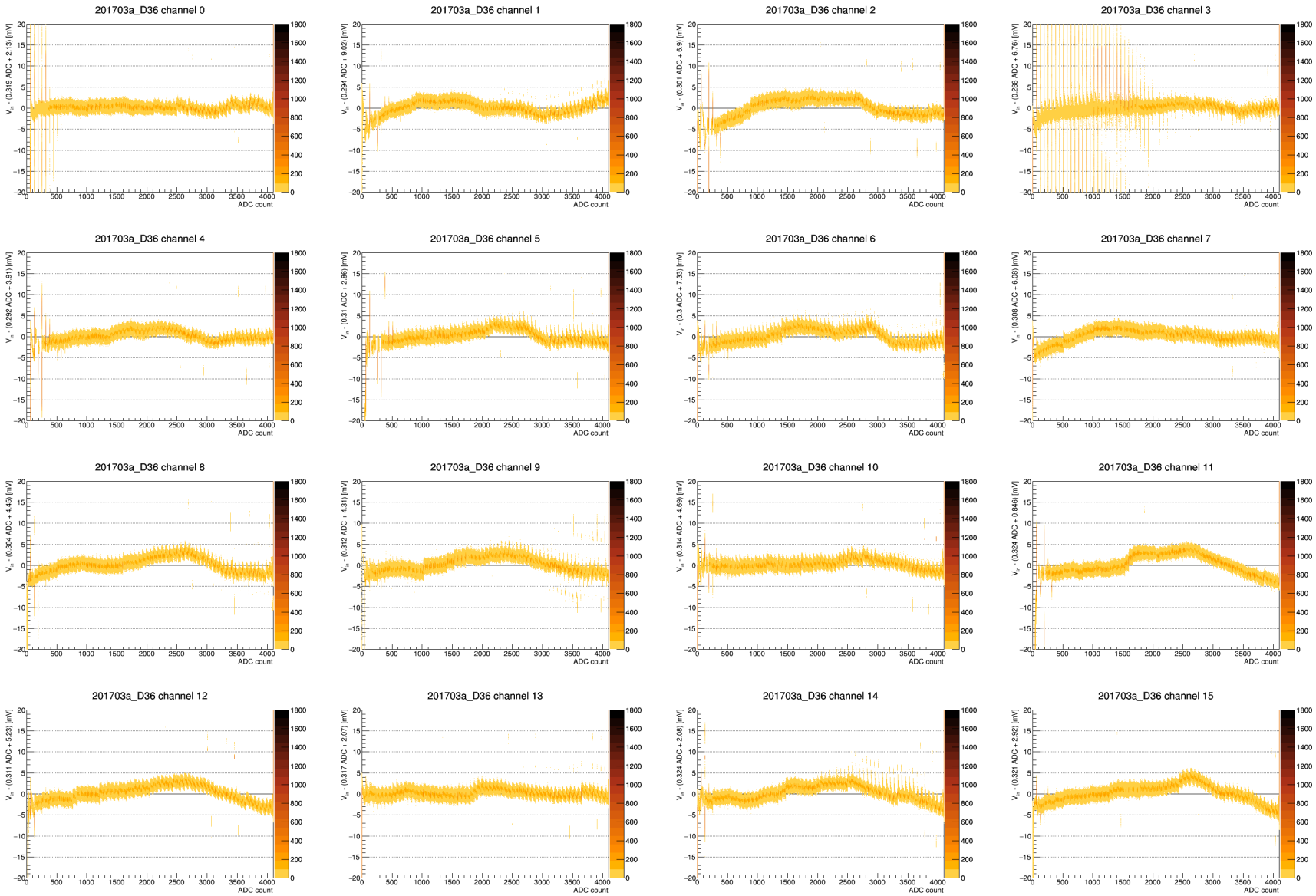
Chip D76 (rank=46, Q=0.780, a=0.985, m=0.808)



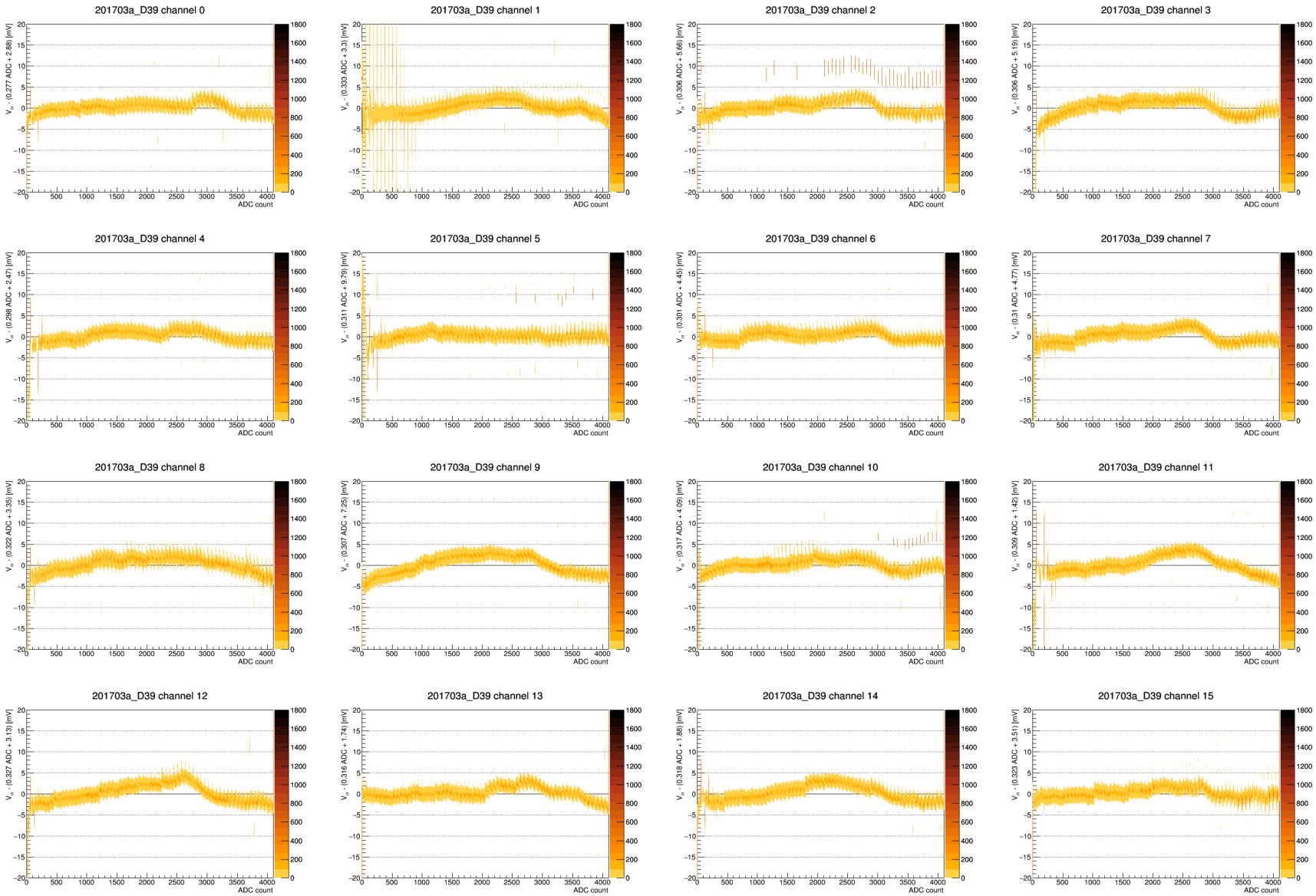
Chip D68 (rank=47, Q=0.770, a=0.984, m=0.897)



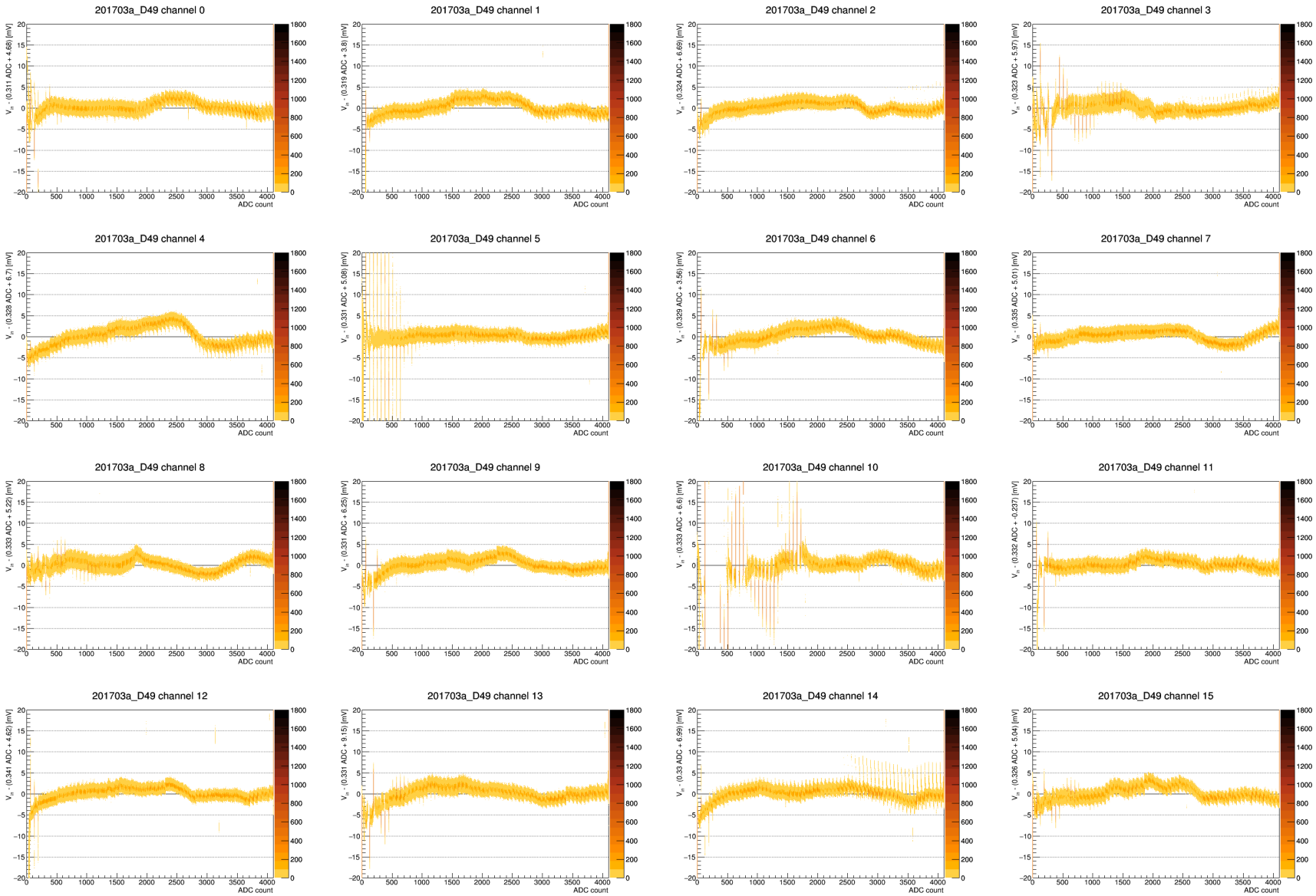
Chip D36 (rank=48, Q=0.757, a=0.984, m=0.782)



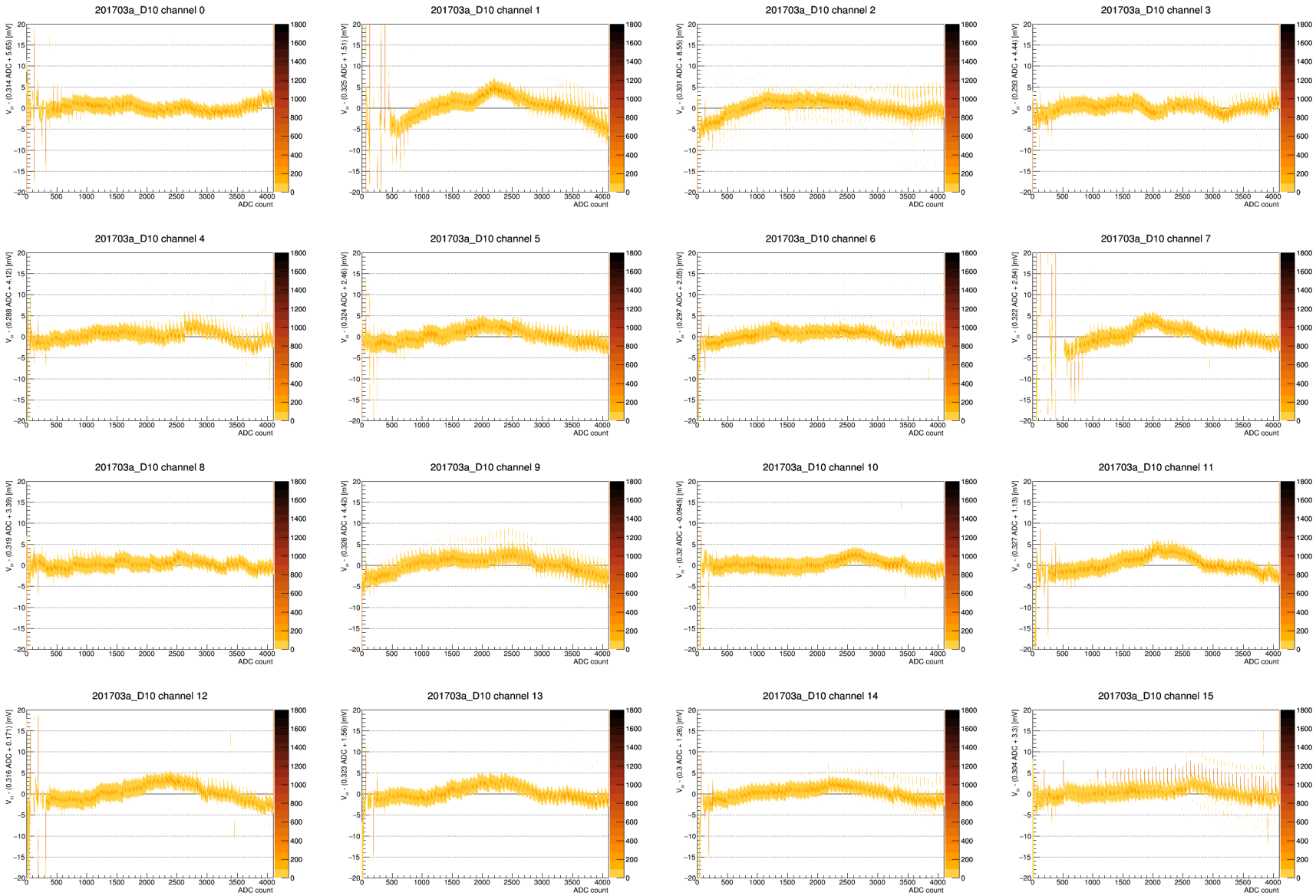
Chip D39 (rank=49, Q=0.754, a=0.983, m=0.872)



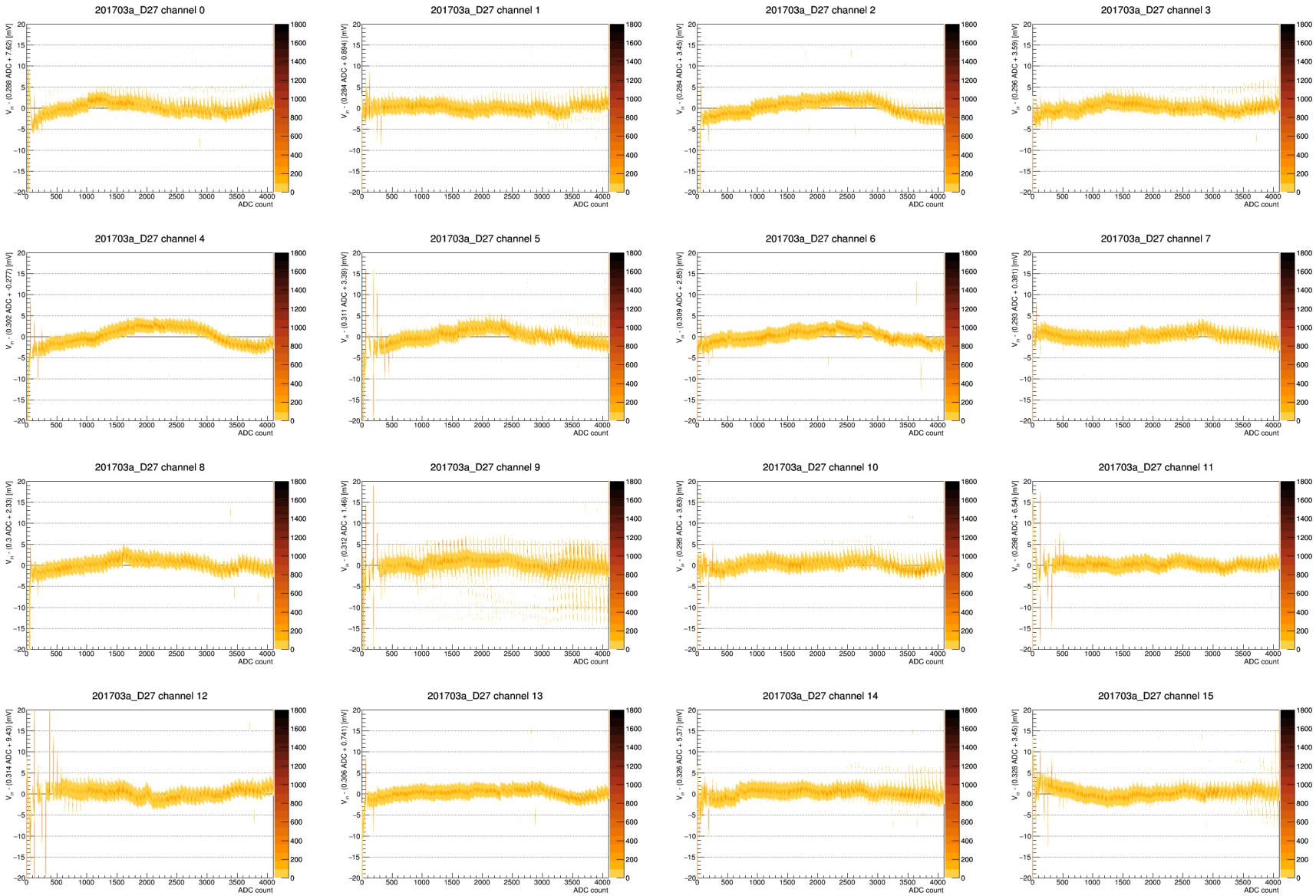
Chip D49 (rank=50, Q=0.736, a=0.982, m=0.816)



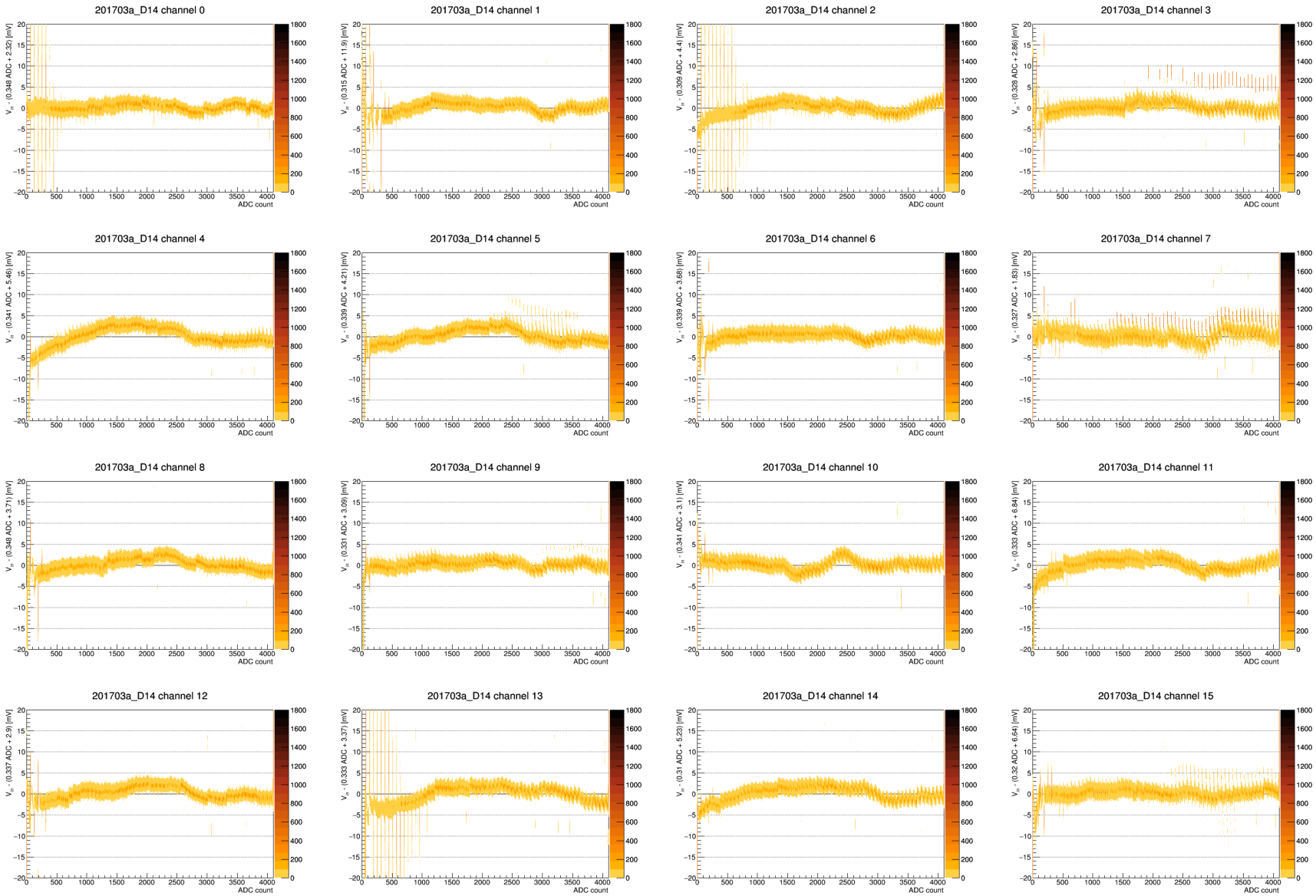
Chip D10 (rank=51, Q=0.735, a=0.982, m=0.818)



Chip D27 (rank=52, Q=0.726, a=0.981, m=0.812)

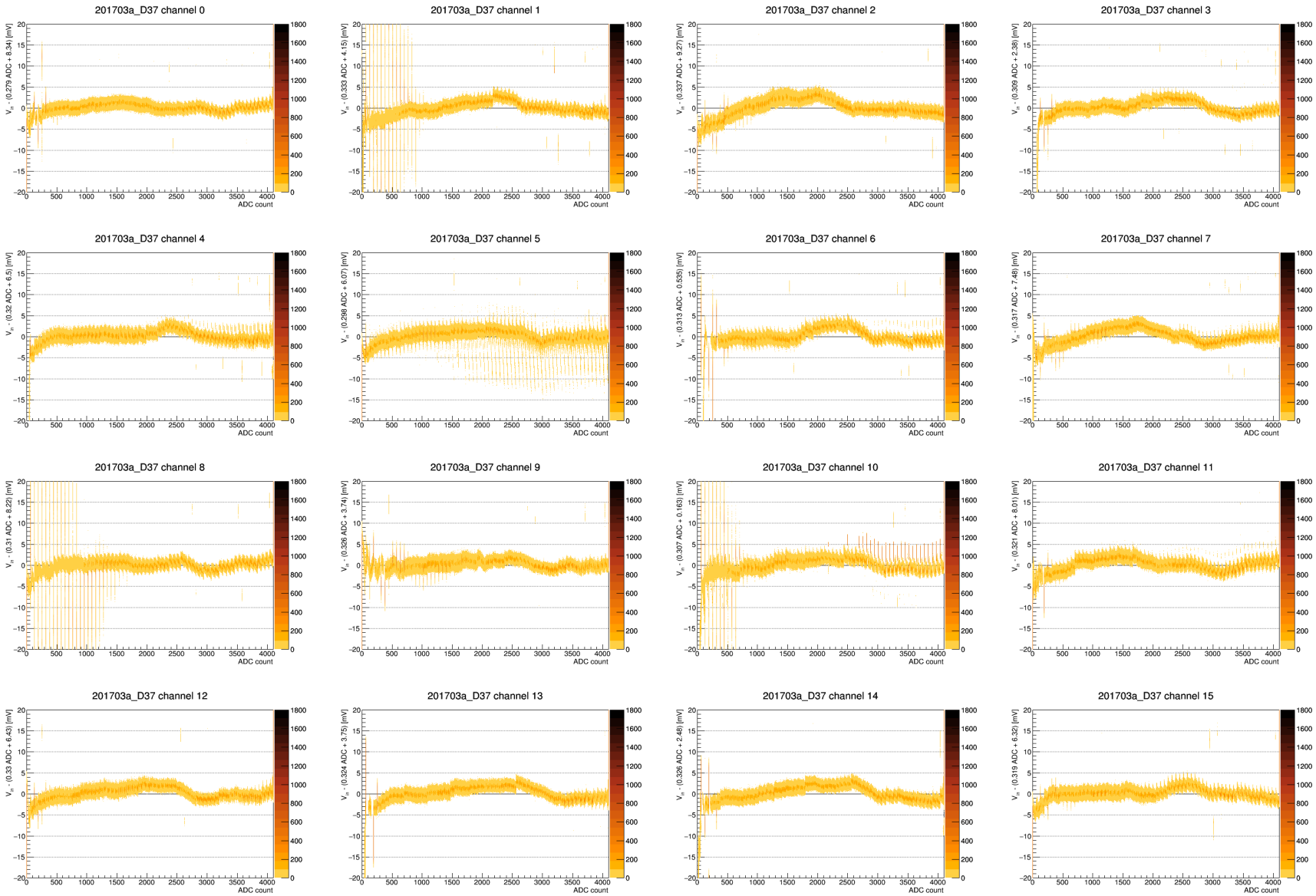


Chip D14 (rank=53, Q=0.715, a=0.980, m=0.846)

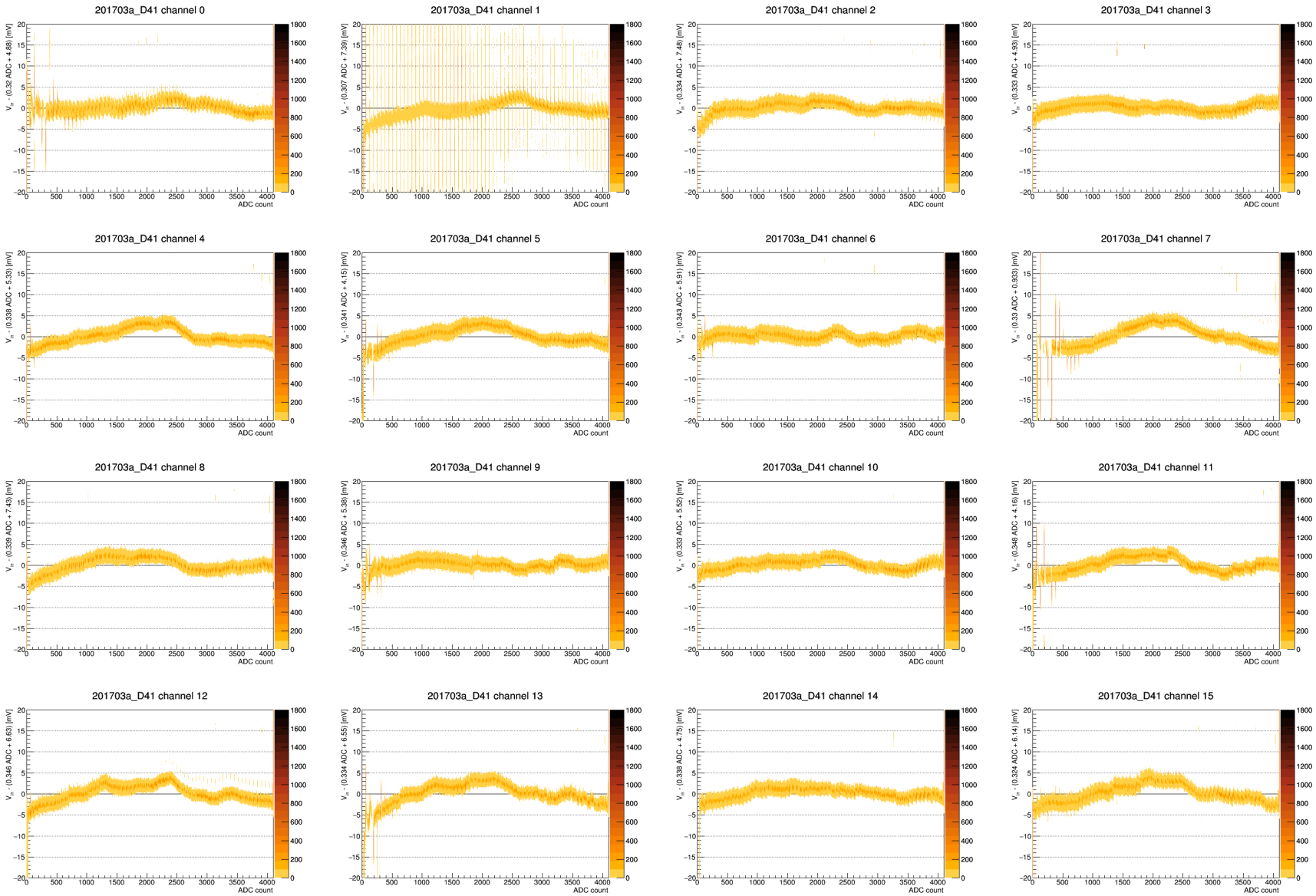


Bad chips

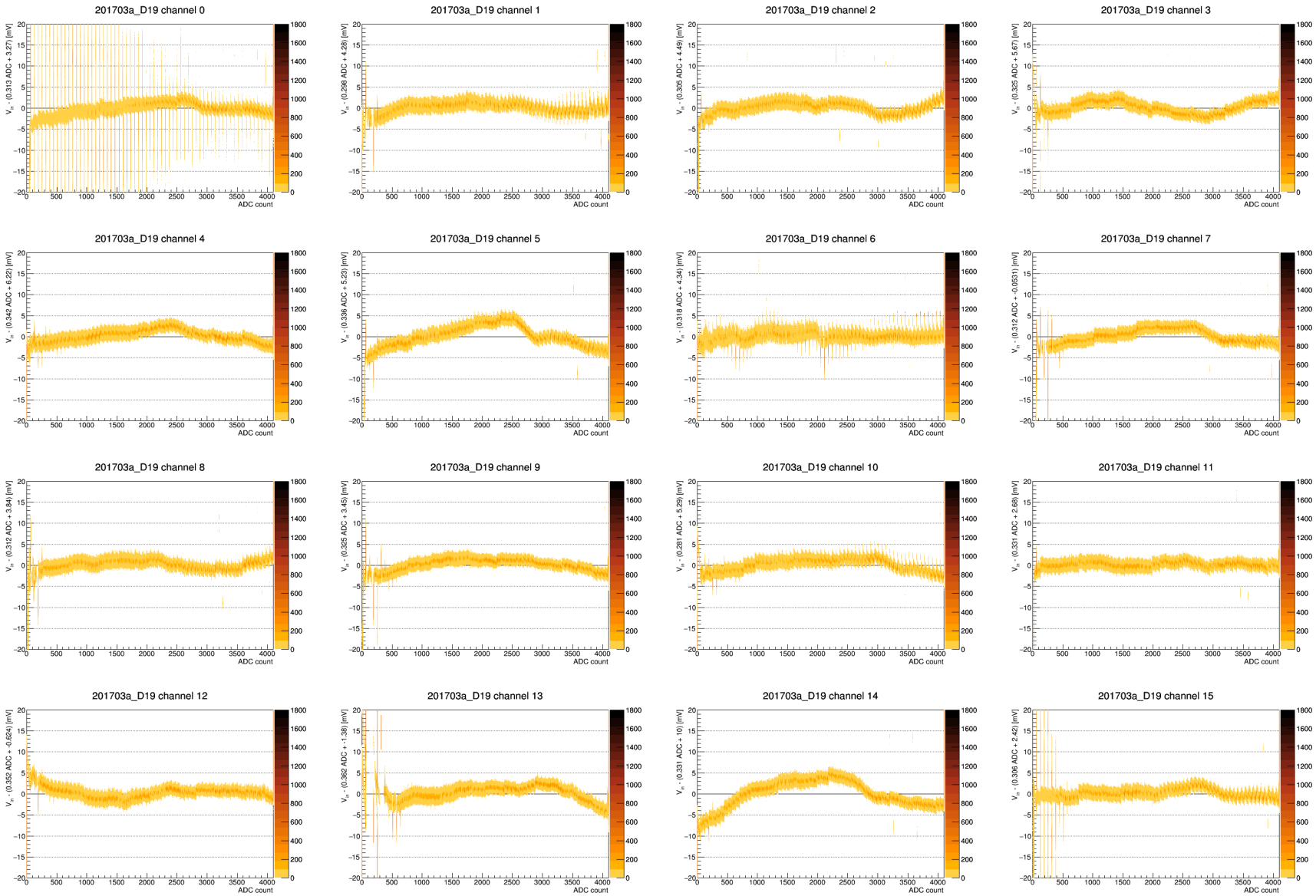
Chip D37 (rank=54, Q=0.652, a=0.974, m=0.890)



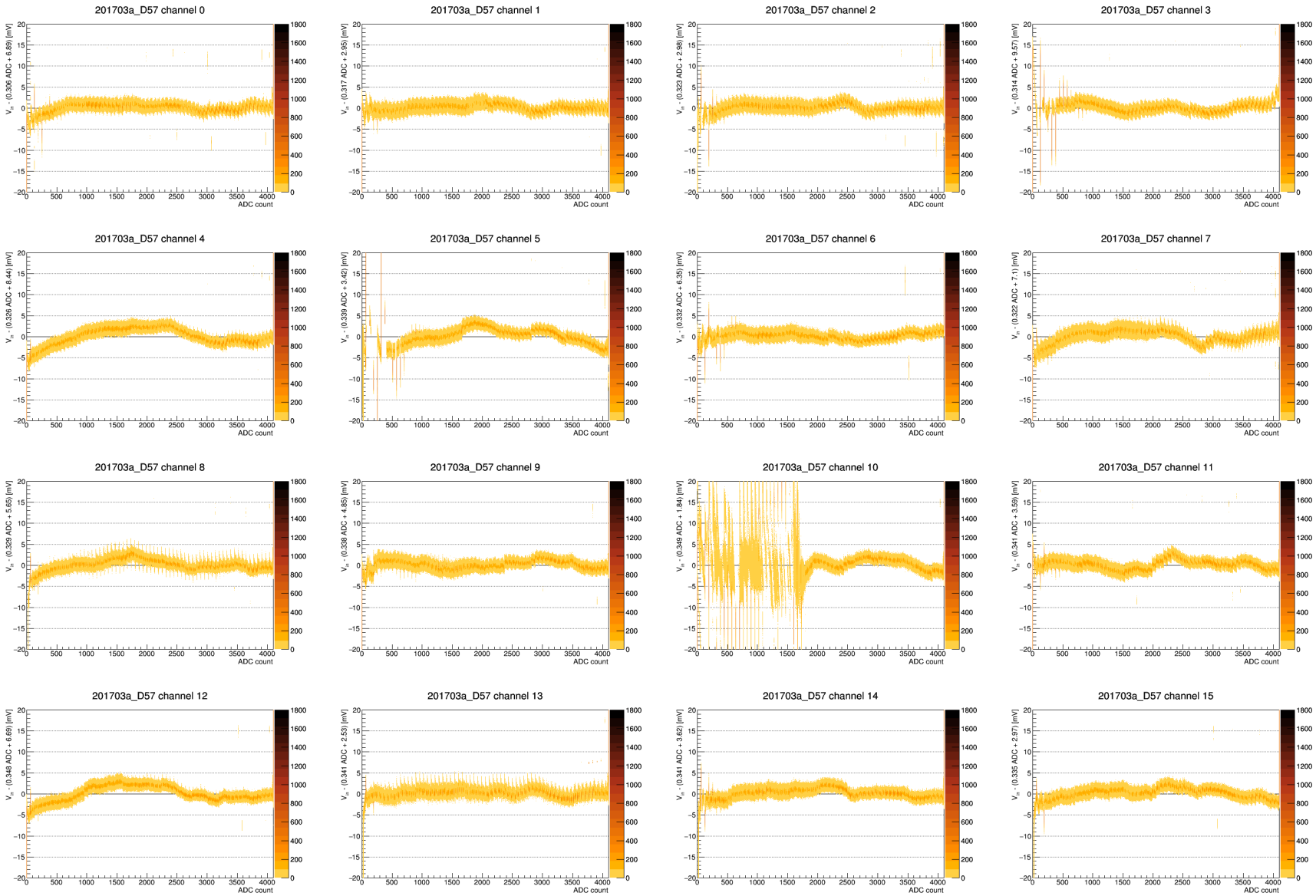
Chip D41 (rank=55, Q=0.621, a=0.975, m=0.640)



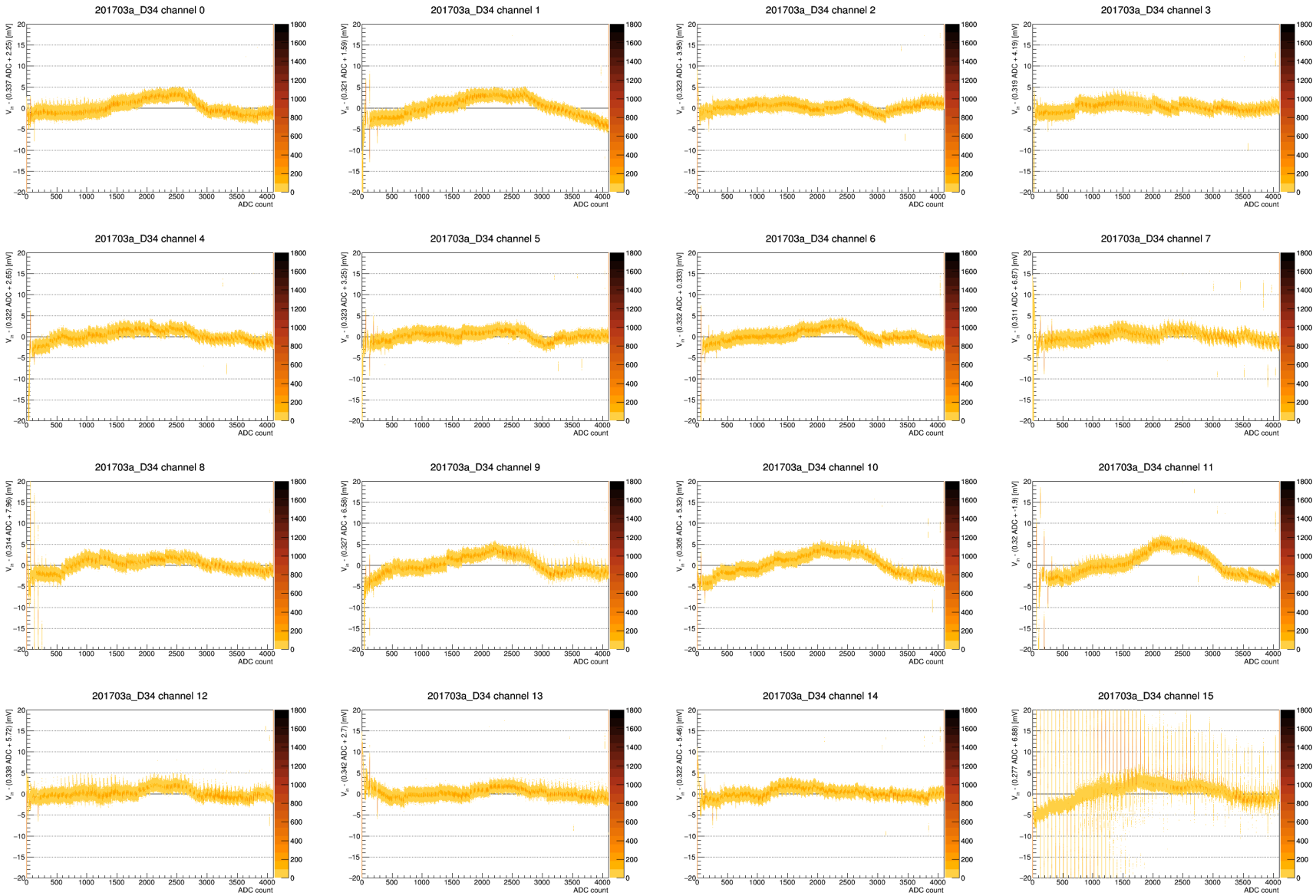
Chip D19 (rank=56, Q=0.621, a=0.973, m=0.703)



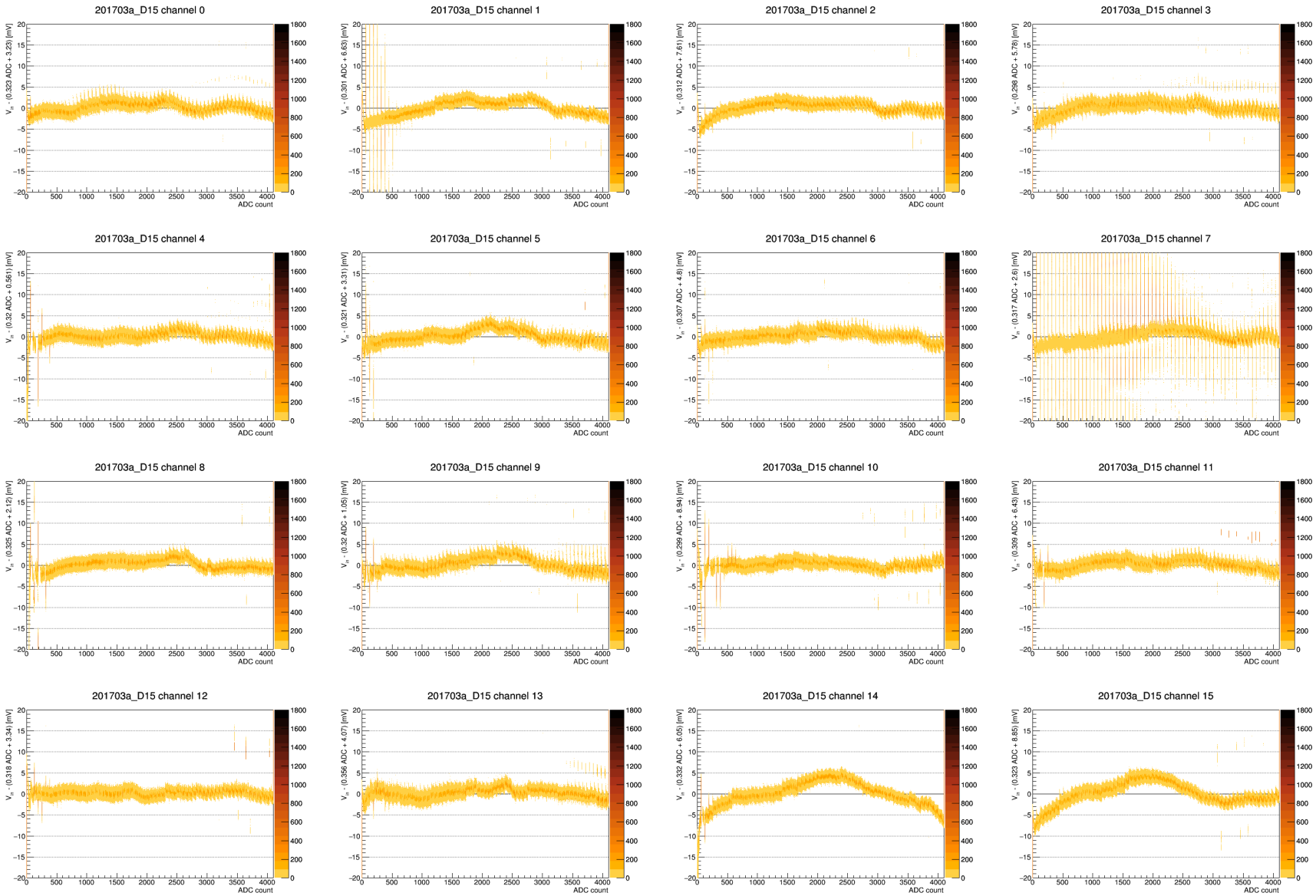
Chip D57 (rank=57, Q=0.575, a=0.973, m=0.584)



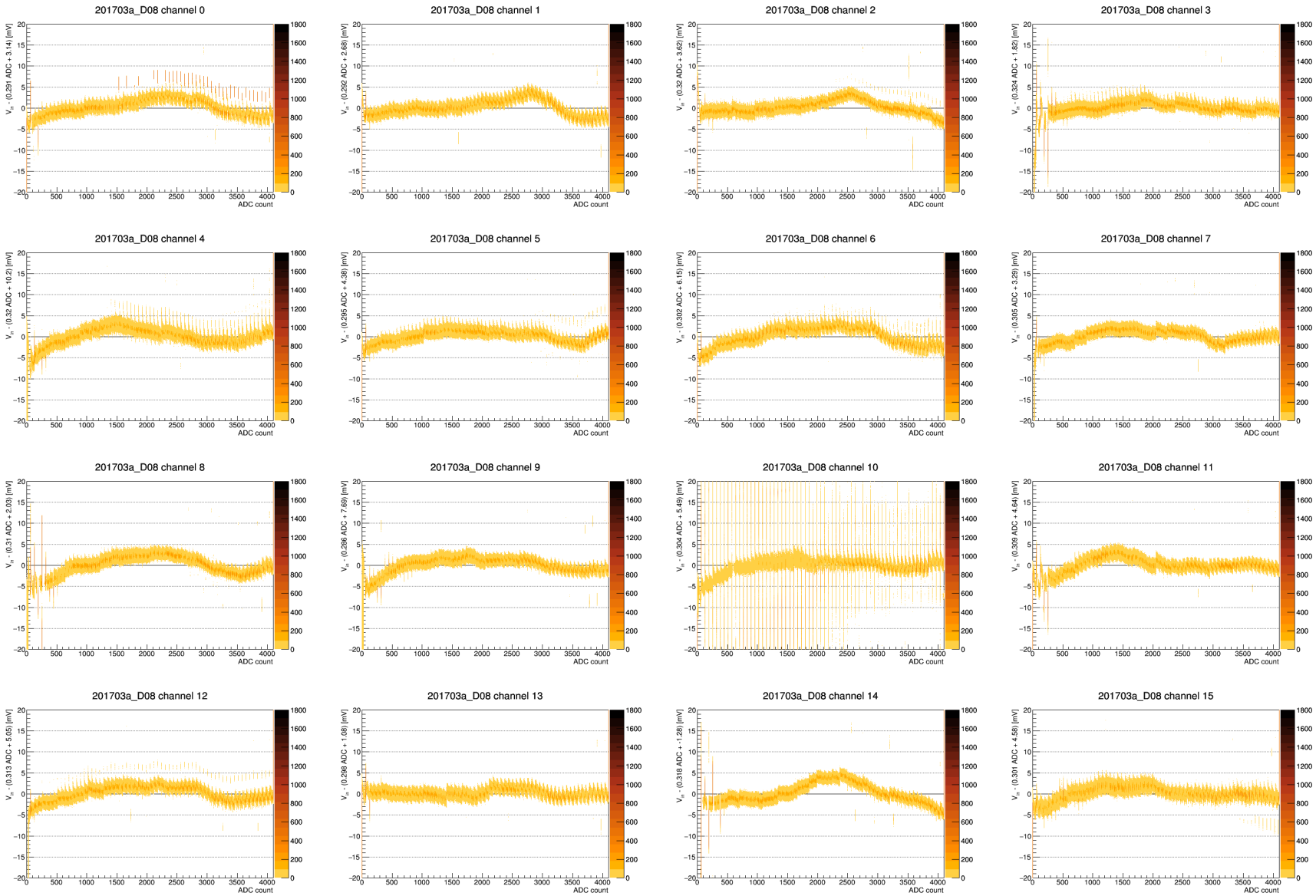
Chip D34 (rank=58, Q=0.557, a=0.971, m=0.568)



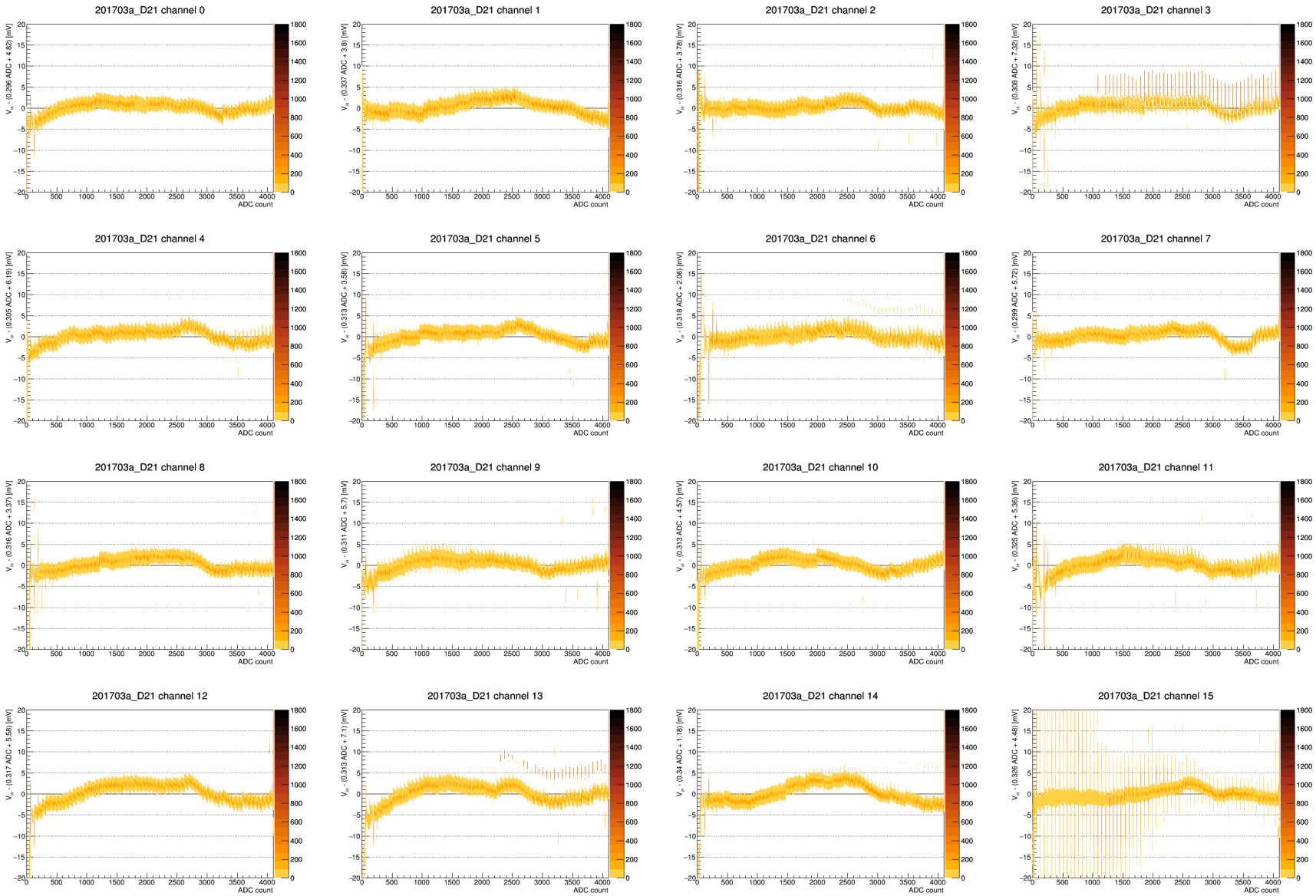
Chip D15 (rank=59, Q=0.533, a=0.969, m=0.560)



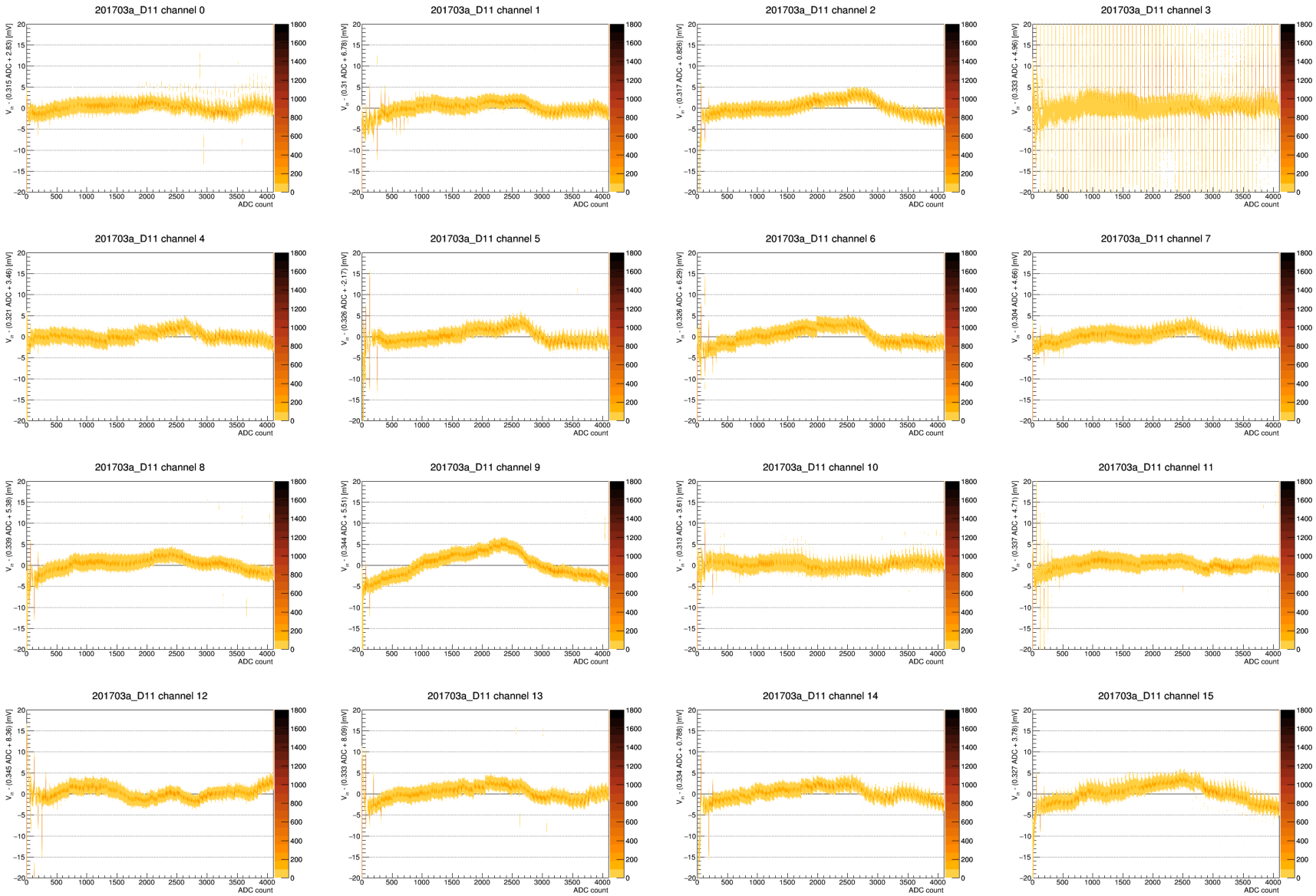
Chip D08 (rank=60, Q=0.486, a=0.962, m=0.589)



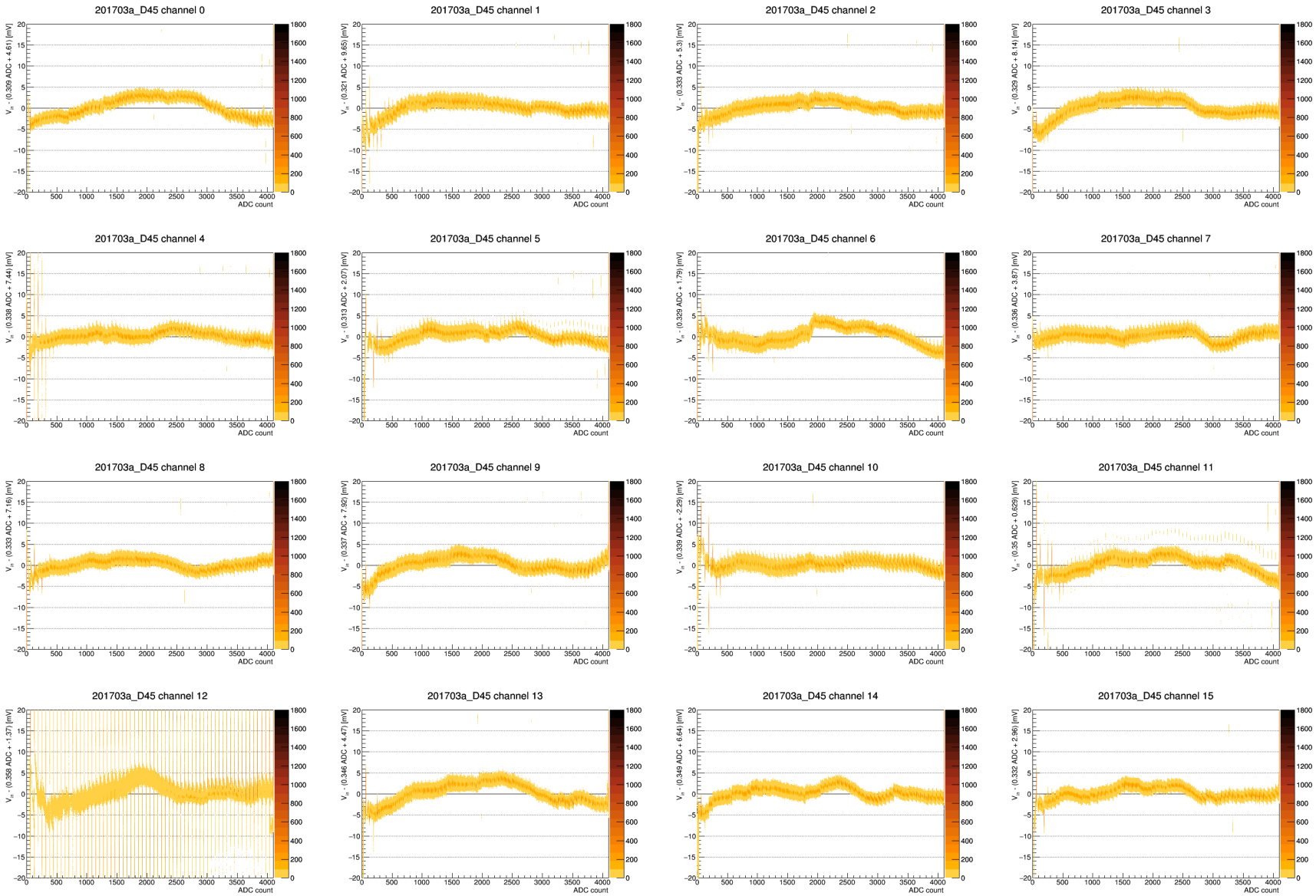
Chip D21 (rank=61, Q=0.472, a=0.959, m=0.711)



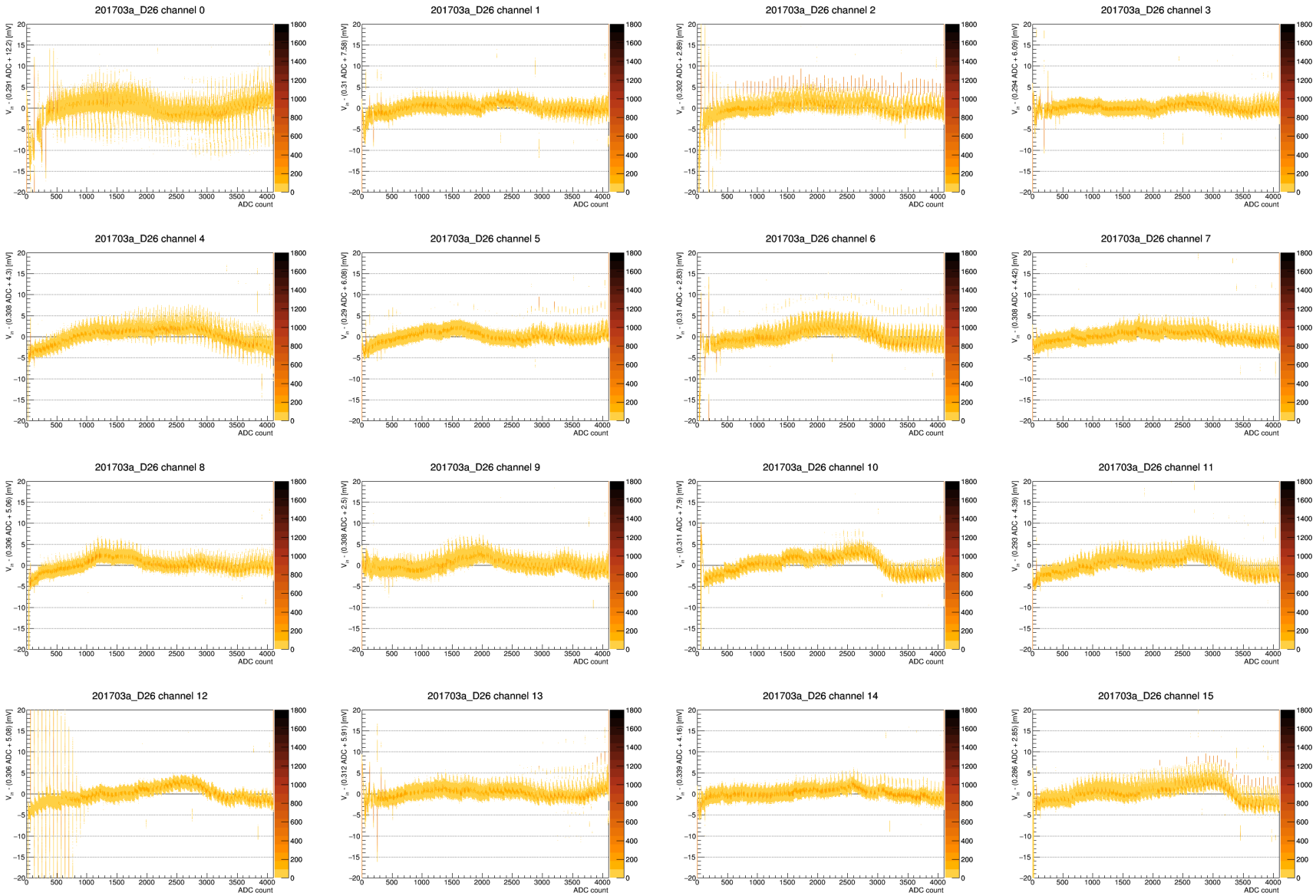
Chip D11 (rank=62, Q=0.340, a=0.958, m=0.345)



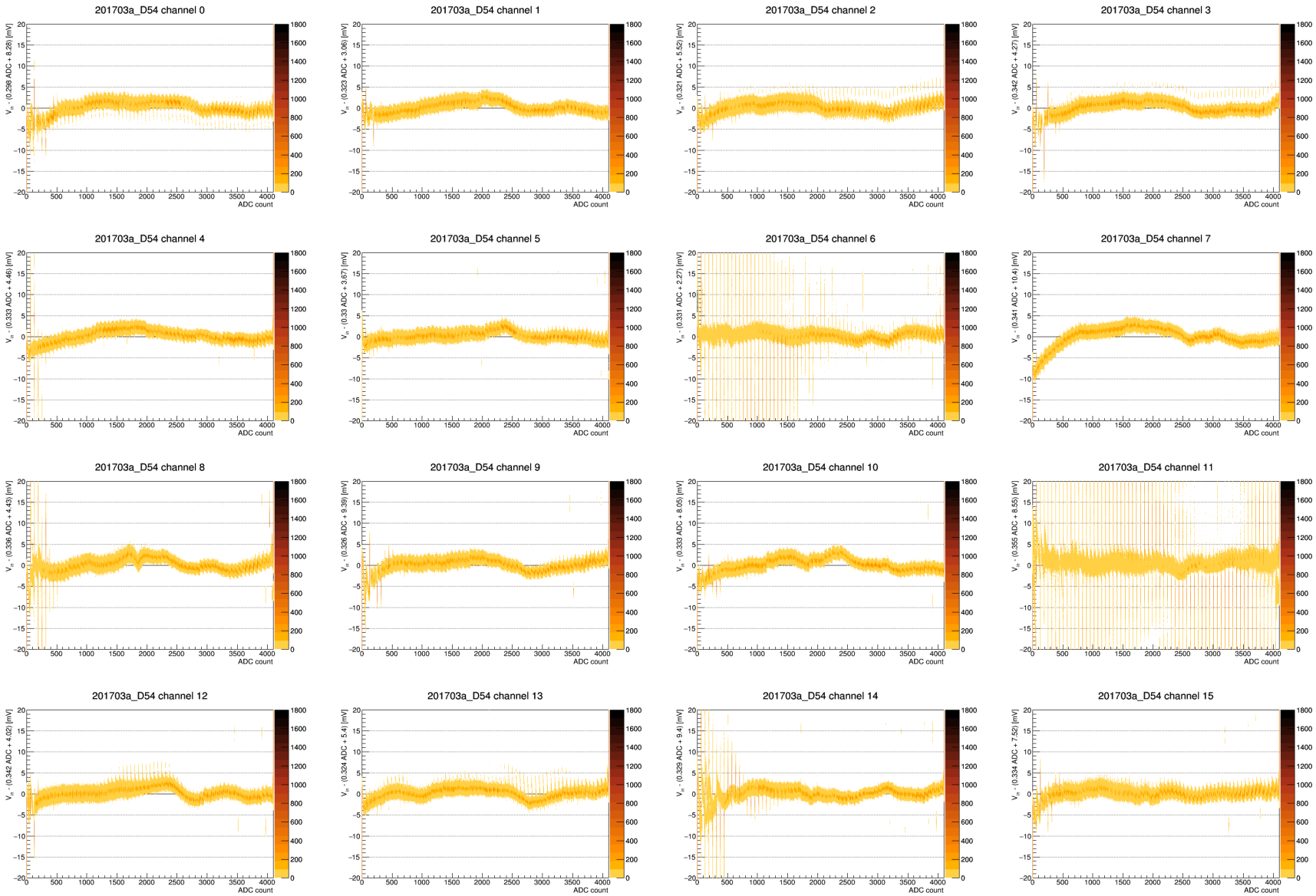
Chip D45 (rank=63, Q=0.286, a=0.954, m=0.290)



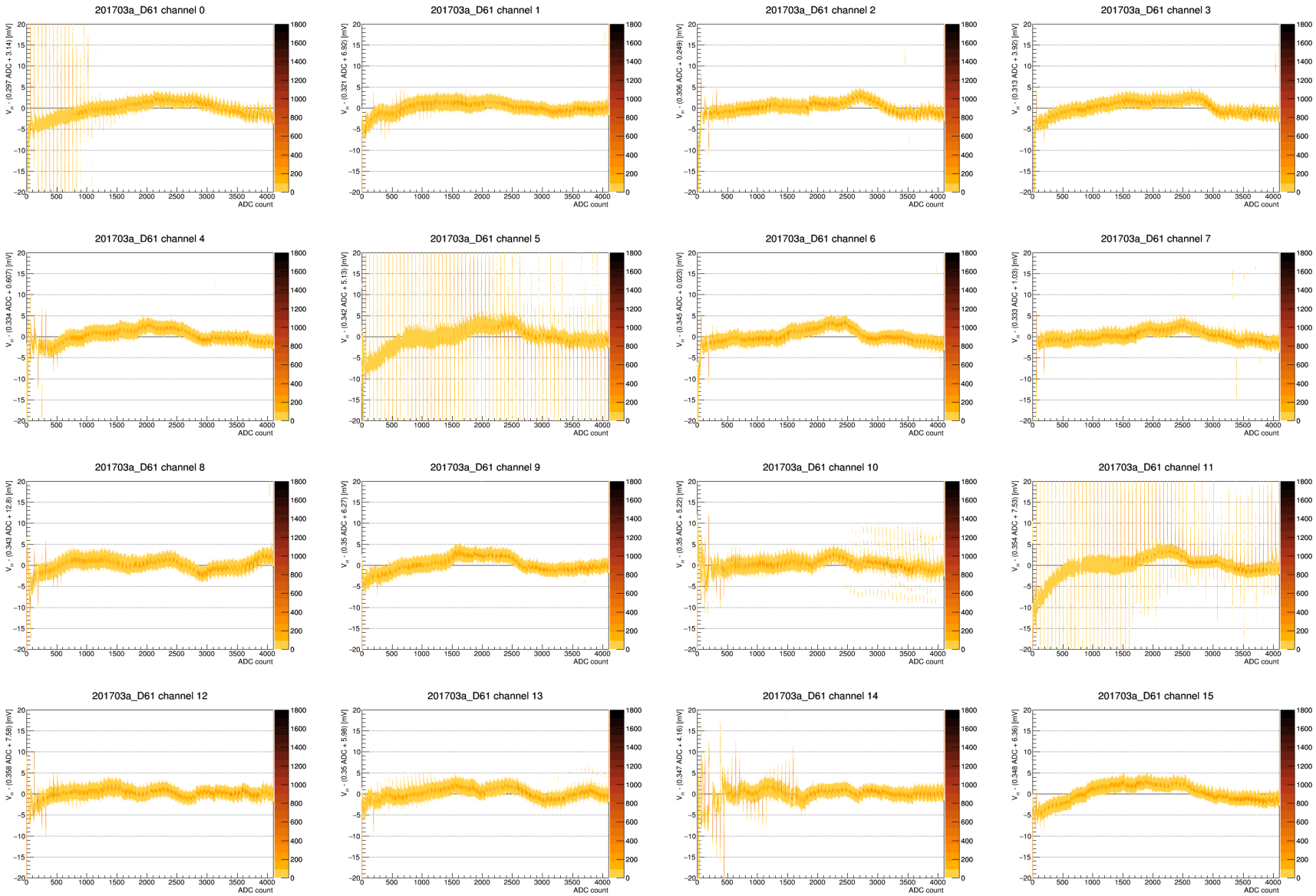
Chip D26 (rank=64, Q=0.249, a=0.922, m=0.663)



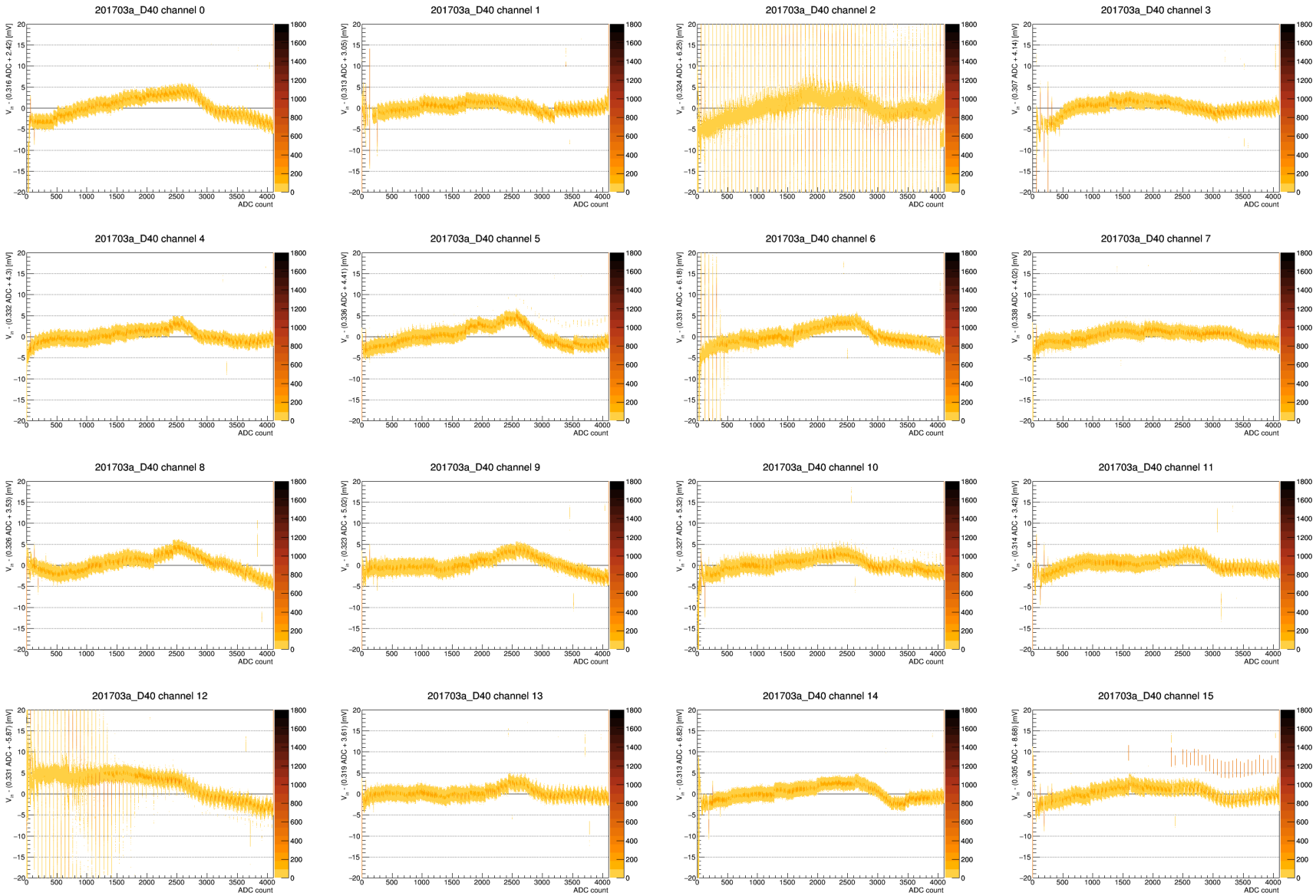
Chip D54 (rank=65, Q=0.217, a=0.938, m=0.297)



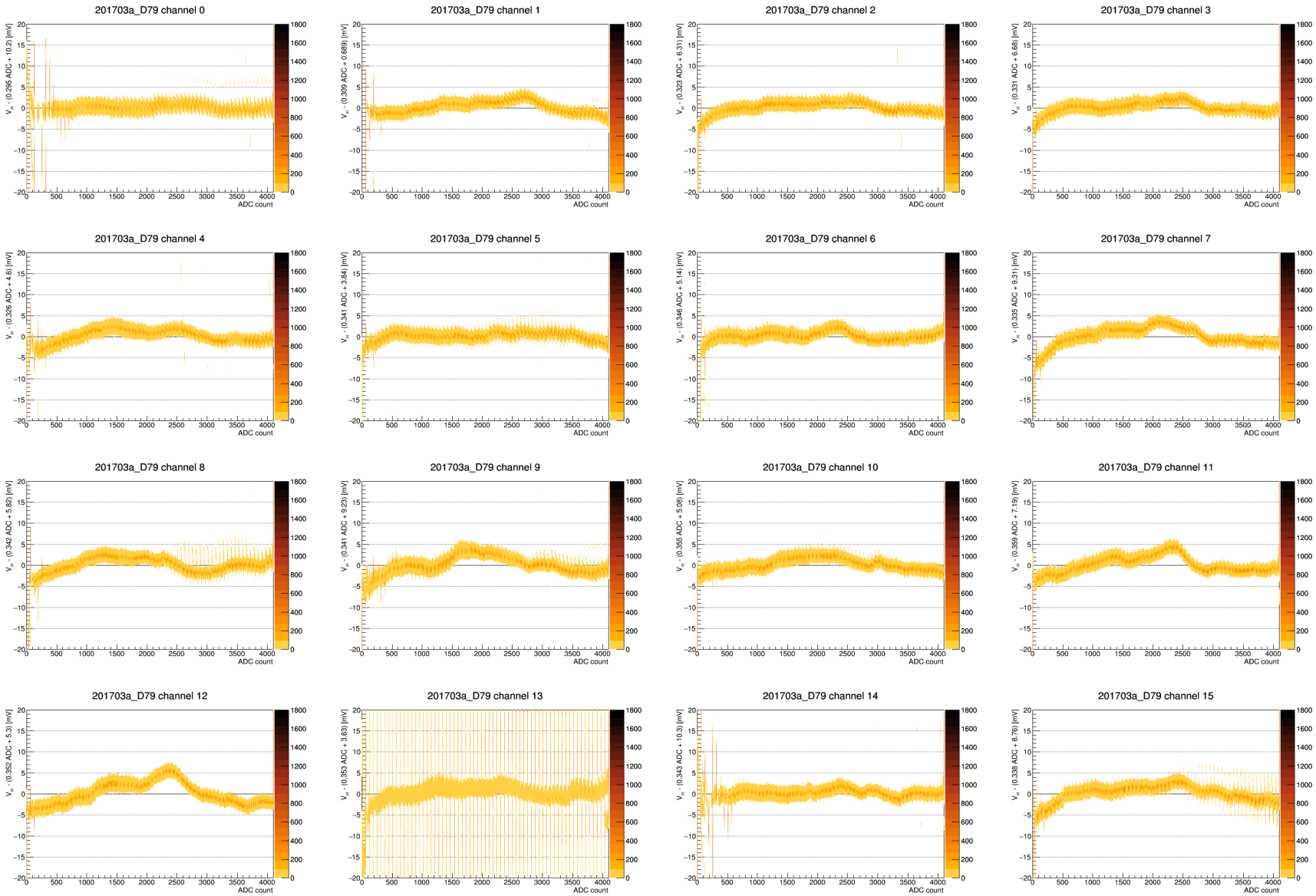
Chip D61 (rank=66, Q=0.202, a=0.926, m=0.461)



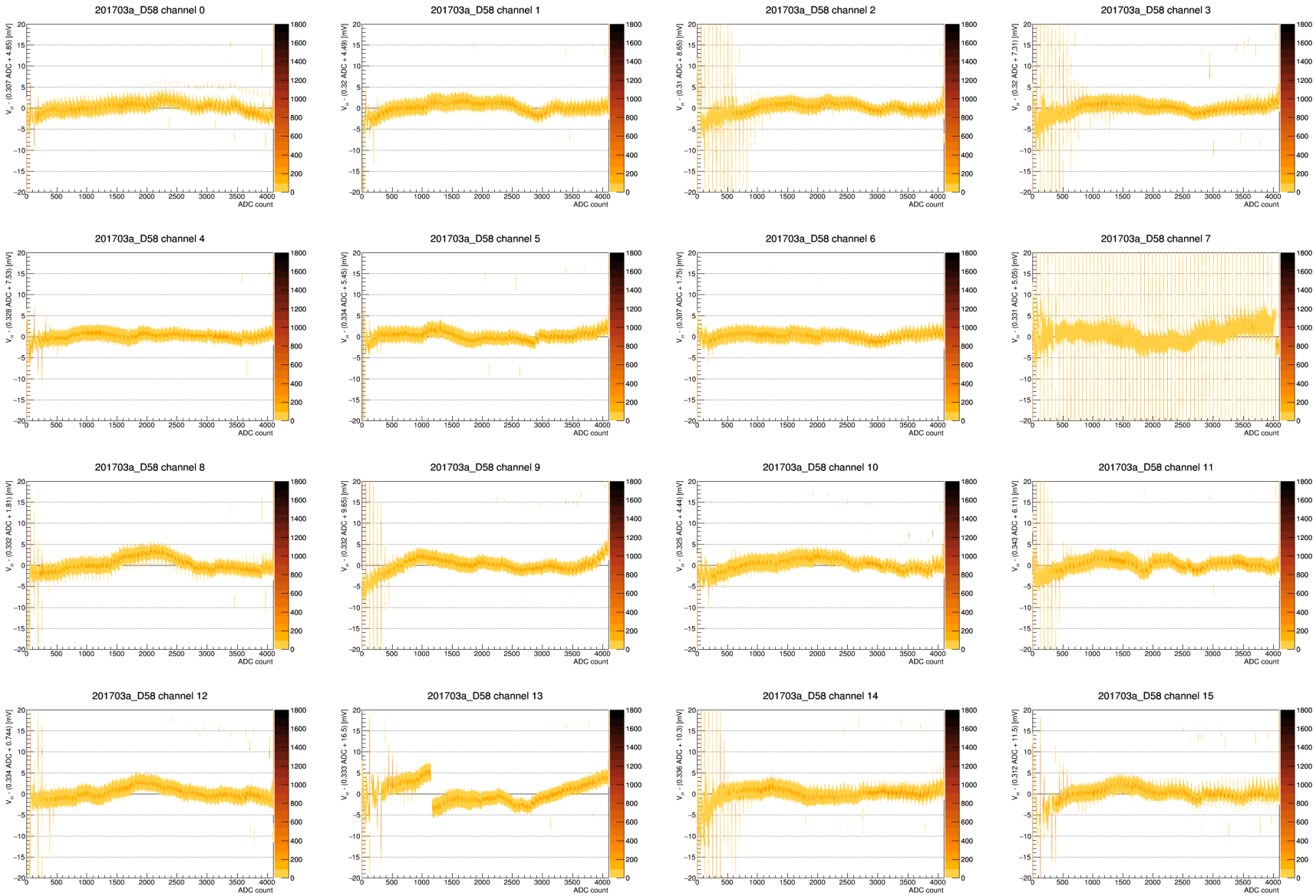
Chip D40 (rank=67, Q=0.199, a=0.935, m=0.277)



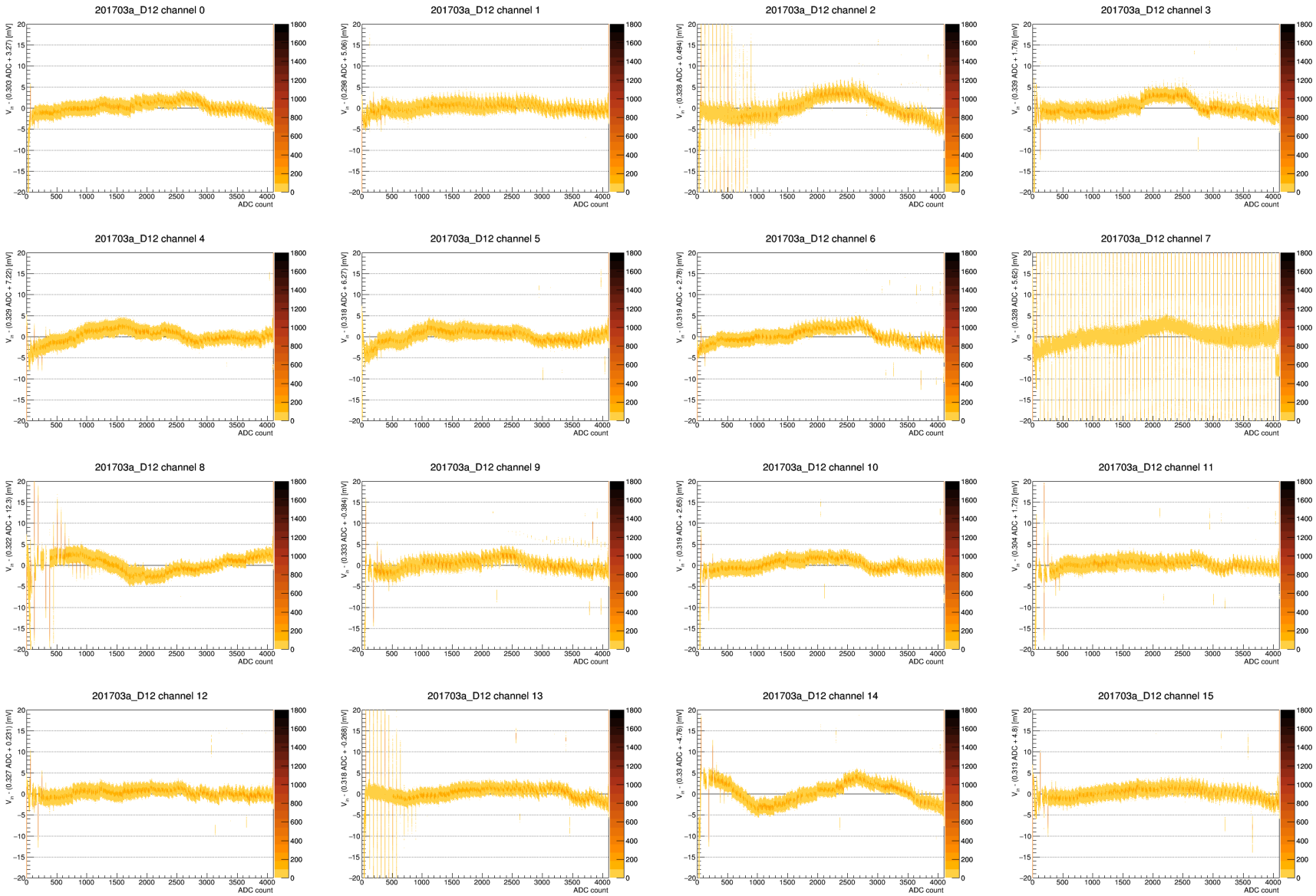
Chip D79 (rank=68, Q=0.196, a=0.947, m=0.205)



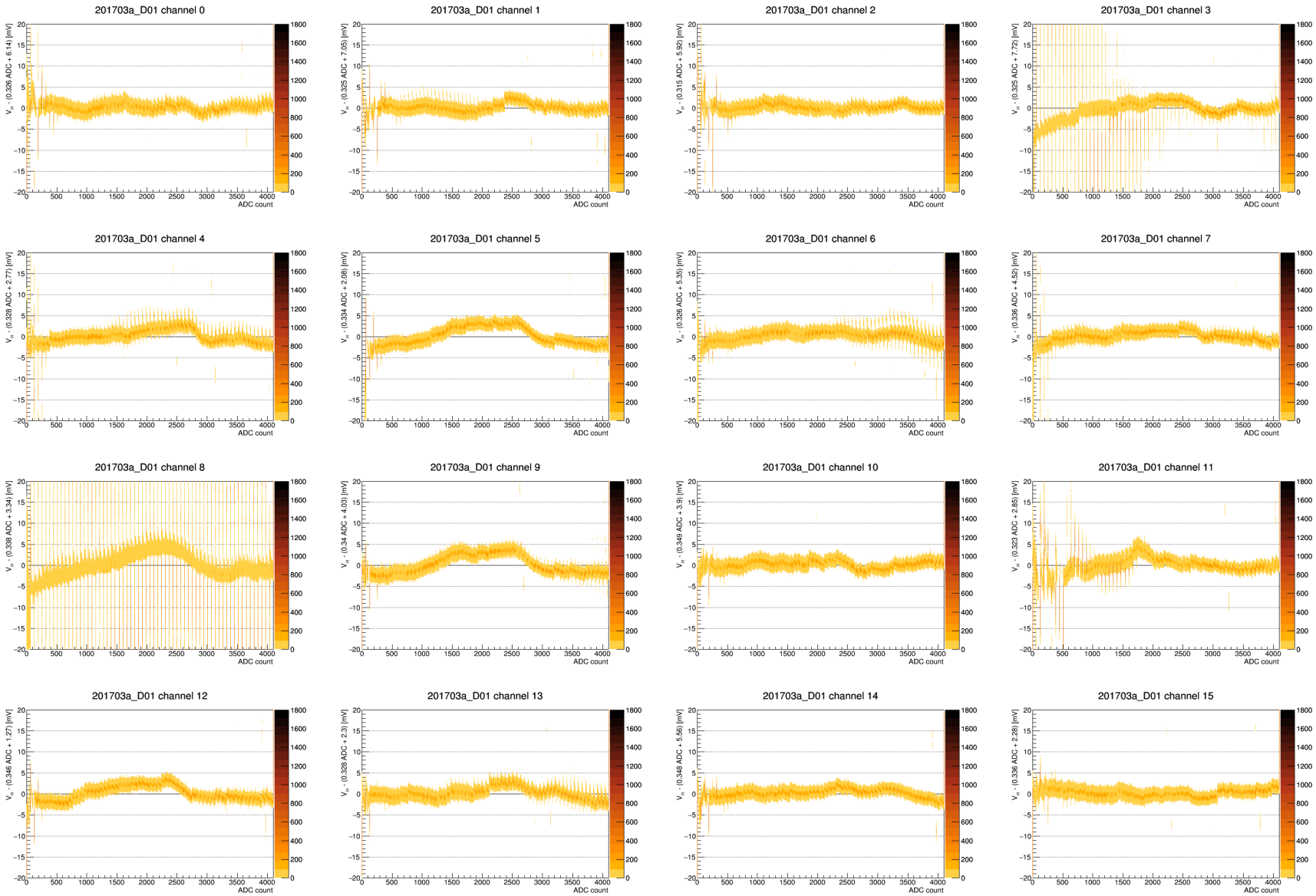
Chip D58 (rank=69, Q=0.184, a=0.943, m=0.204)



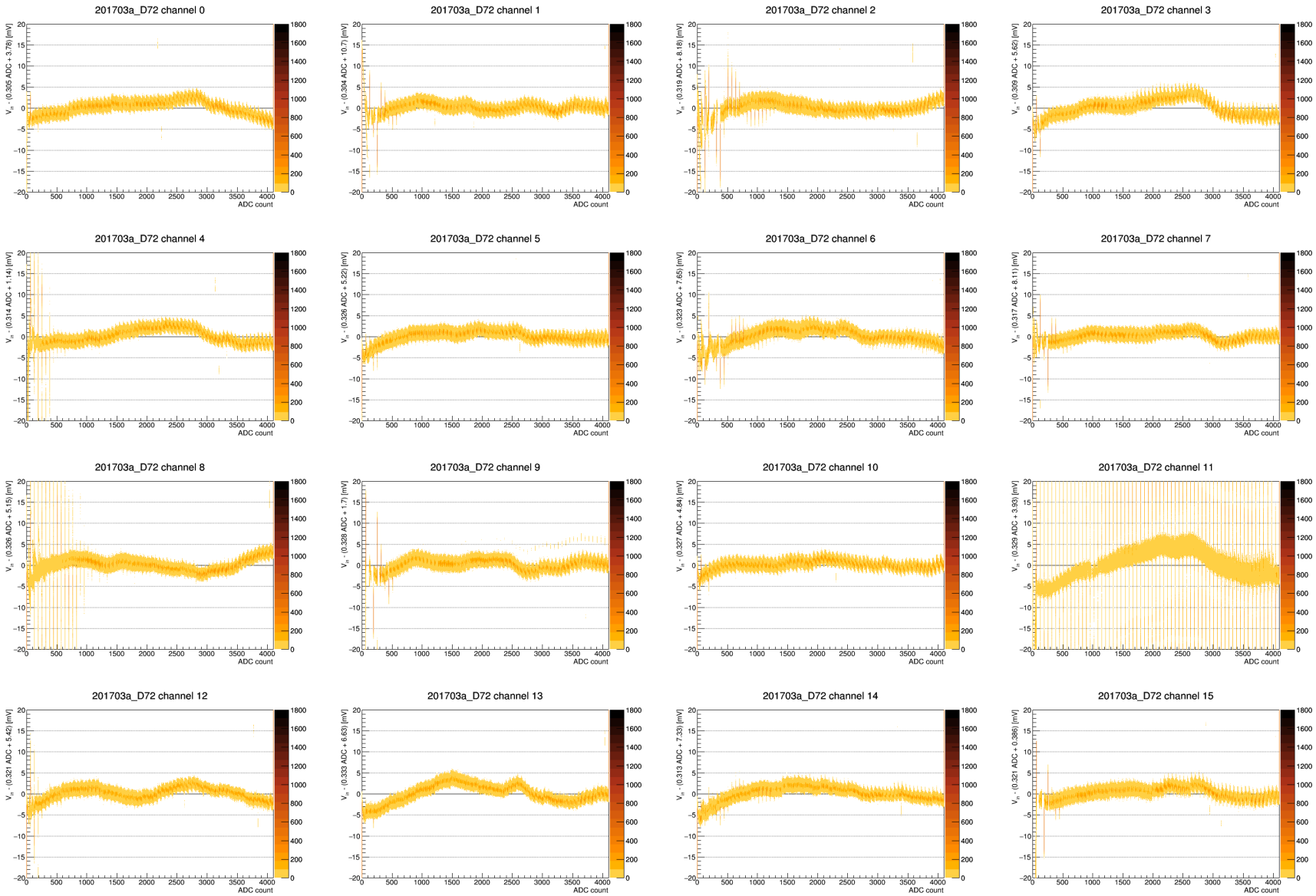
Chip D12 (rank=70, Q=0.162, a=0.942, m=0.177)



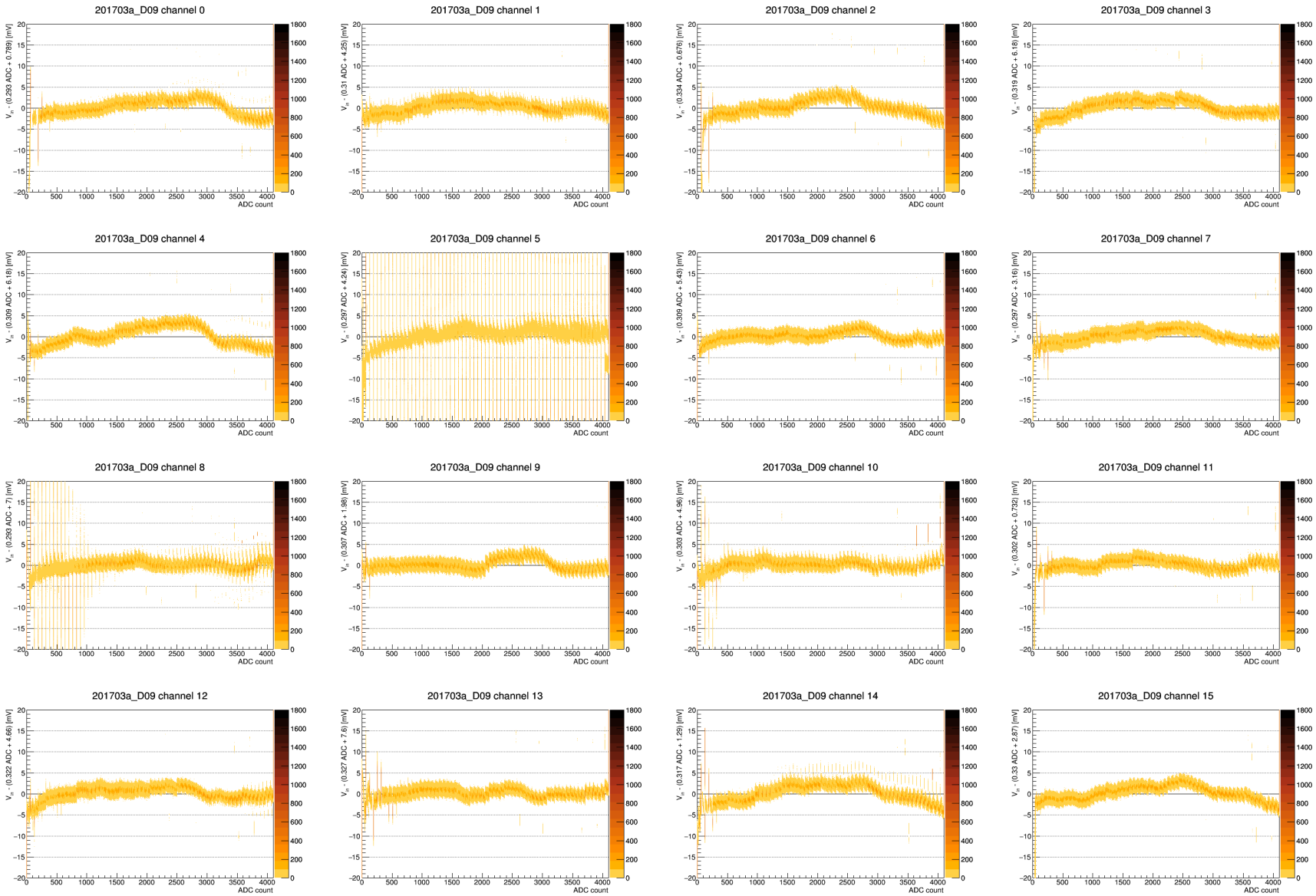
Chip D01 (rank=71, Q=0.125, a=0.927, m=0.186)



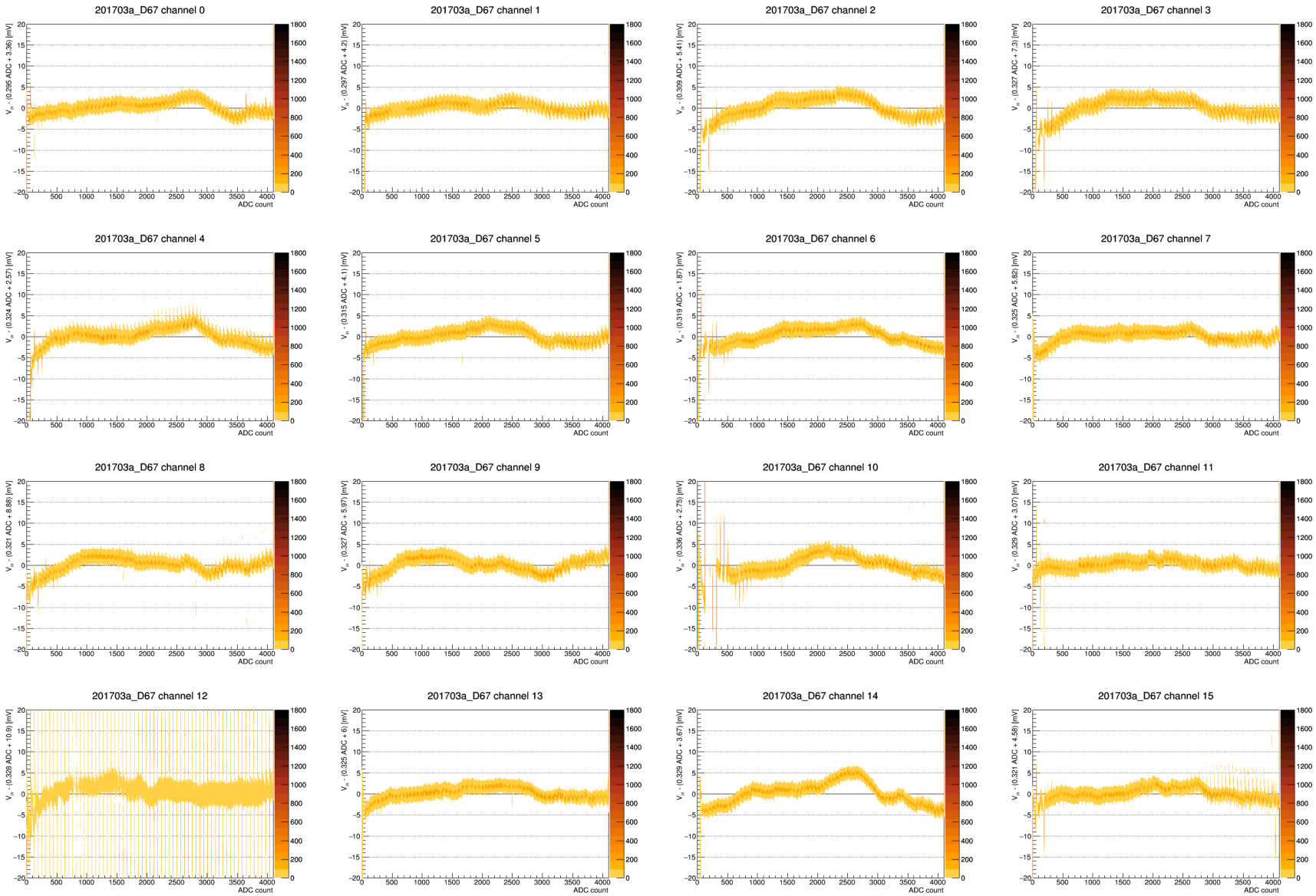
Chip D72 (rank=72, Q=0.114, a=0.941, m=0.122)



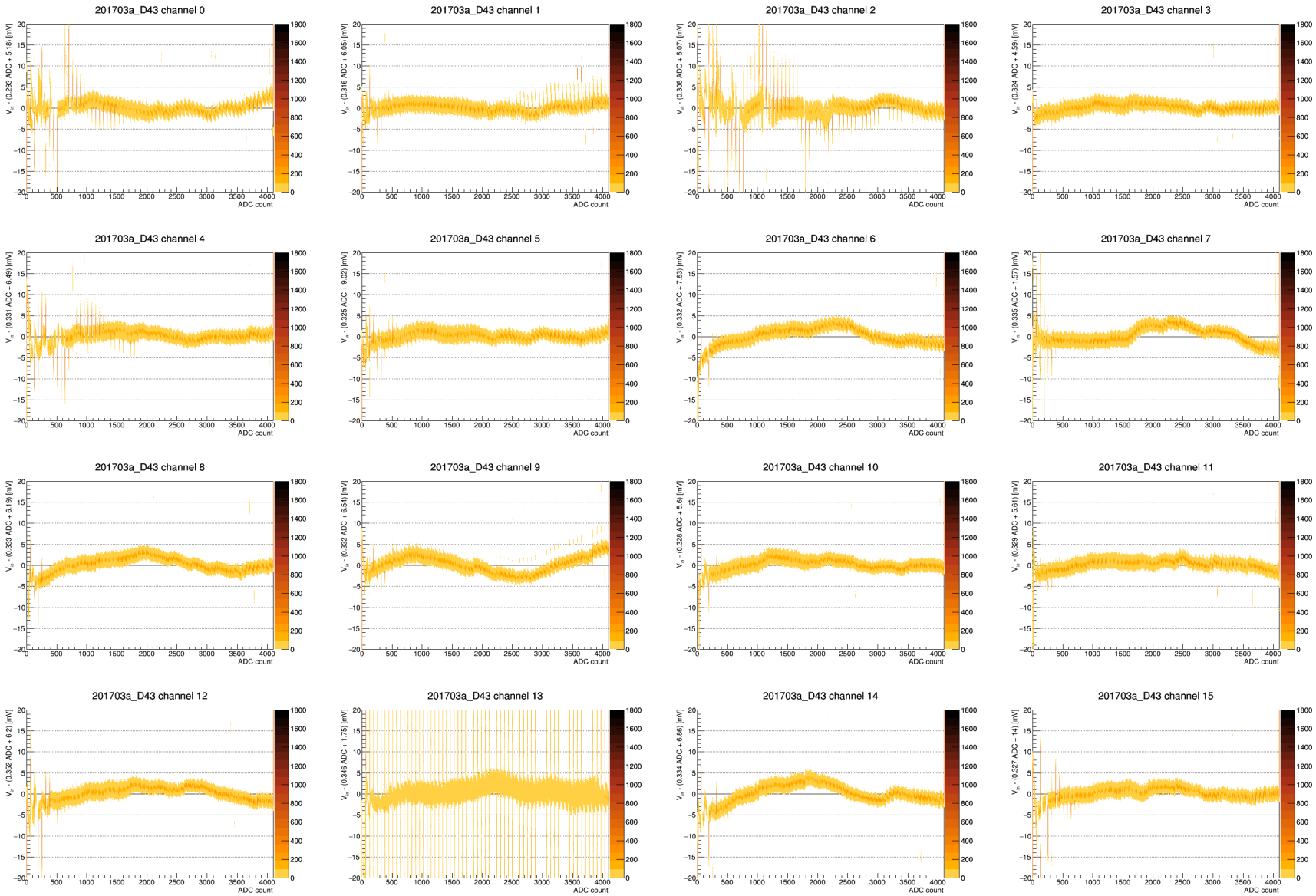
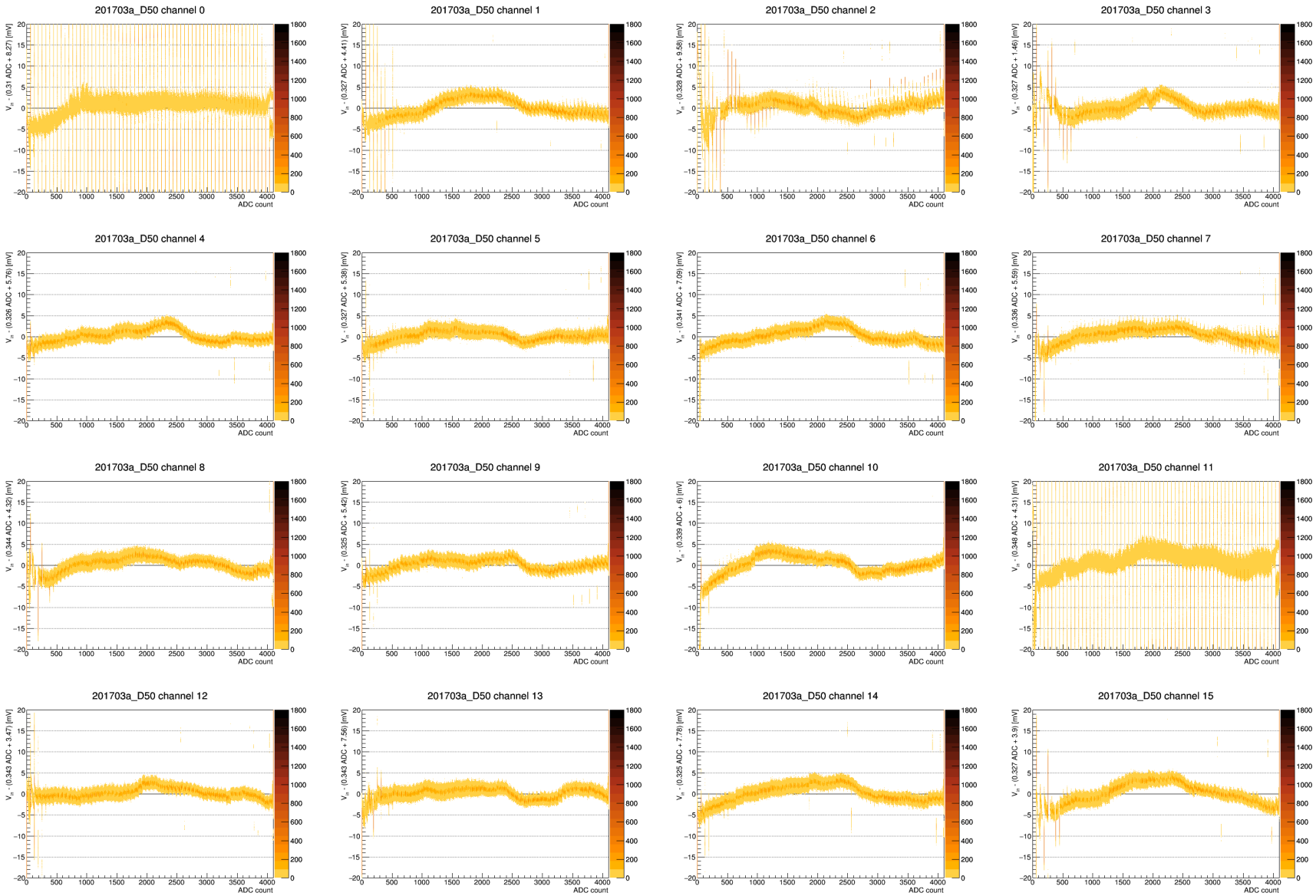
Chip D09 (rank=73, Q=0.102, a=0.939, m=0.110)



Chip D67 (rank=74, Q=0.069, a=0.939, m=0.072)



Chip D43 (rank=75, Q=0.043, a=0.916, m=0.066)



Chip D50 (rank=76, Q=0.017, a=0.887, m=0.105)