ADC performance: time dependence

BNL DUNE

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Introduction

I have been looking at ADC test data taken at BNL

- I report here on long-term data taken in March 2017
  - ADC samples are read out for input voltage steps with sawtooth envelope
  - 40M samples over 20s for each ADC channel
    - approximately 10k samples for each ADC bin
- Data is from new P1 chips for protoDUNE
- Data conditions
  - Cold (LN2)
    - There is warm data for one chip
  - 2 MHz sampling
  - All data taken with external clock
  - Single chip (D02) in board kept cold and powered
  - 18 samples taken over 10 days

Data taking

Data taken by the following team

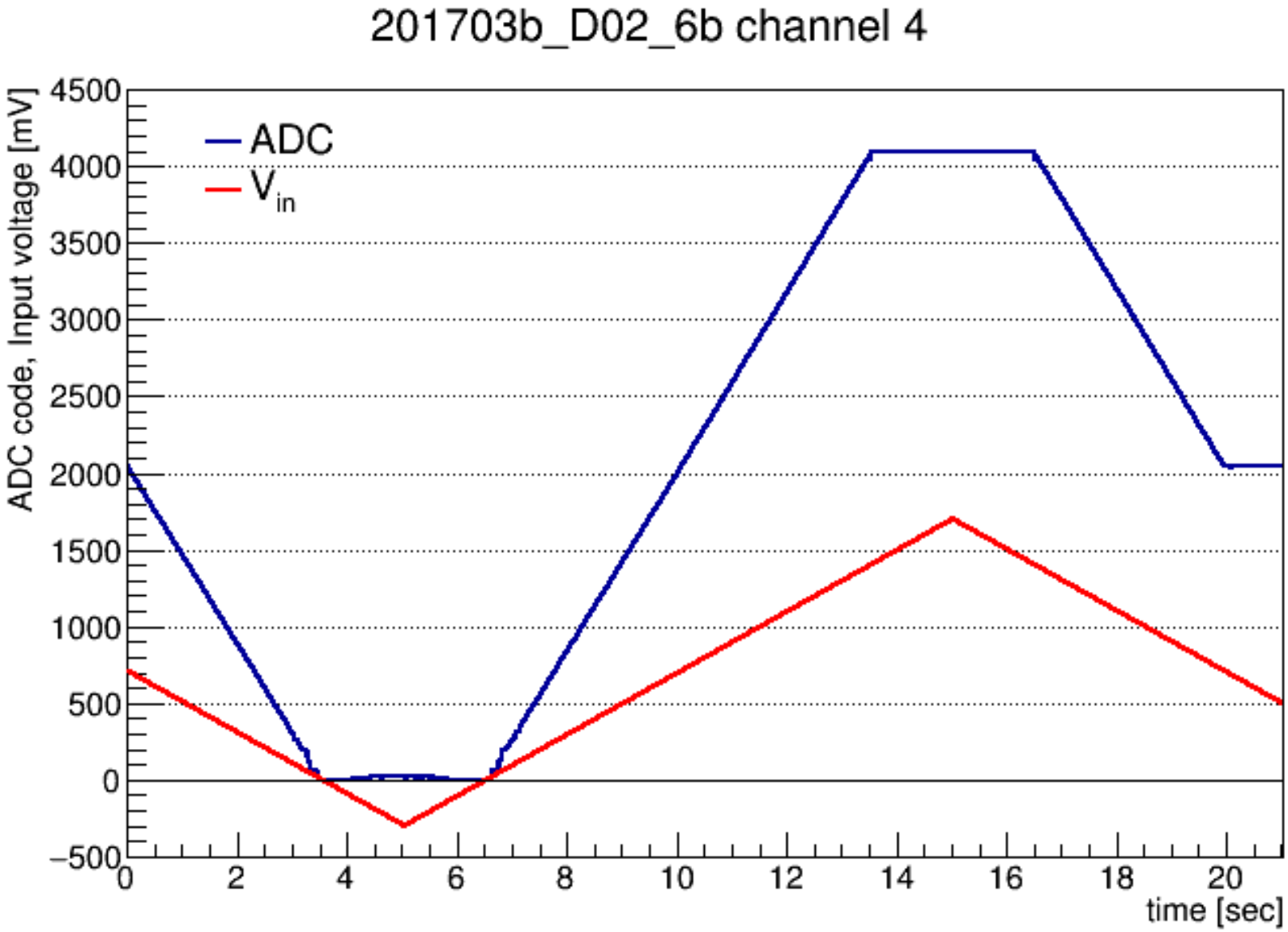
- Hucheng Chen, Shanshan Gao, Jack Fried, Feng Liu (BNL)
- Damian Goeldi (Univ. of Bern)

Thanks to them to making this data available to me

Data format

- ADC samples
- Input voltage ramp from –300 to 1700 mV at 200 mV/sec
- Data is approximately one period of sawtooth centered on the rise
  - See plot on following page
- I see ADC get stuck at a value near 2000 after 20 sec
  - See following example plot
  - I keep only the first 19.8 sec of data for each sample
  - Waveform plots show all samples then look OK

Example waveform



Data analysis

Data is analyzed as described in previous talks

- Also see appendix

First need input voltage

- This was provided by data takers for earlier samples
  - Those were in CSV format with one rise starting at a specified voltage
- Here data is ADC only (channel number packed in high bits)
  - Known waveform: sawtooth with 10 s rise/fall over (-300, 1700) mV
  - But time offset is not specified
- I determine the min and max points from ADC data in two ways
  - Data above or below a double threshold
  - Midpoints between peaks in the ADC bin distributions
  - Require these to agree with one another
- Assume the min and max found in this way correspond to the same for the input voltage ➔ timing offset and period
- Preceding plot shows V_{in} determined in this way

Results

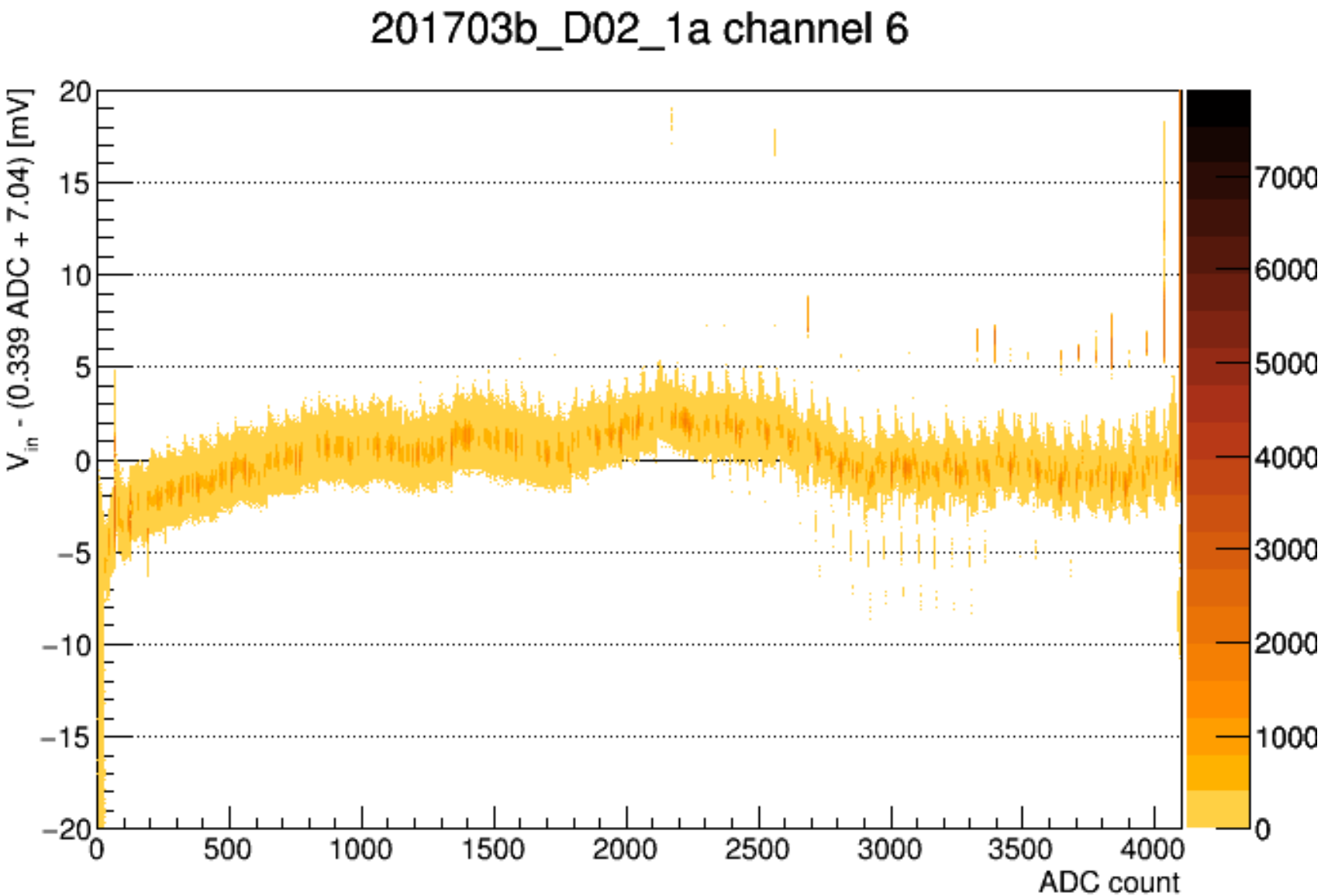
Performance plots are in appendix

- 18 samples for one chip
- Taken over 10 days

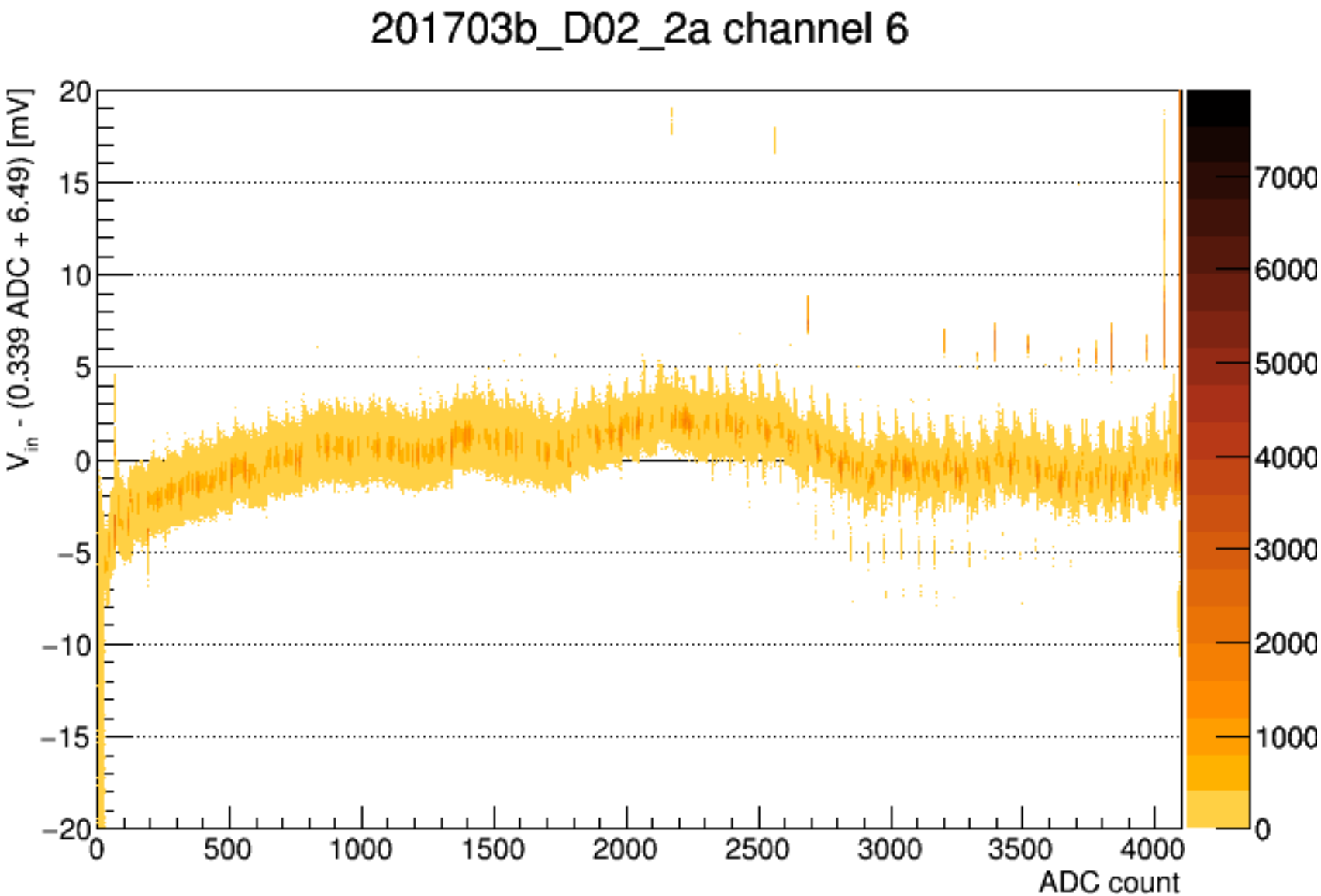
Comments

- Bulk response seems very consistent day-to-day
  - Overall gain RMS is 3.6% (primarily channel-to-channel variation)
  - Largest gain RMS for any one channel is 0.03%
  - No bulk changes evident in residual spectra
- There is some change in the bad channels and tails
  - Many the same day after day but some appear or disappear
  - Biggest changes in channel 6—plots on following pages
  - Many plots for all channels and times in appendix 2
- Work in progress to quantify these changes
  - E.g. what are bad and tail fractions if we combine all samples or take the worst of each?
  - Effect of using the “wrong” sample to identify problems

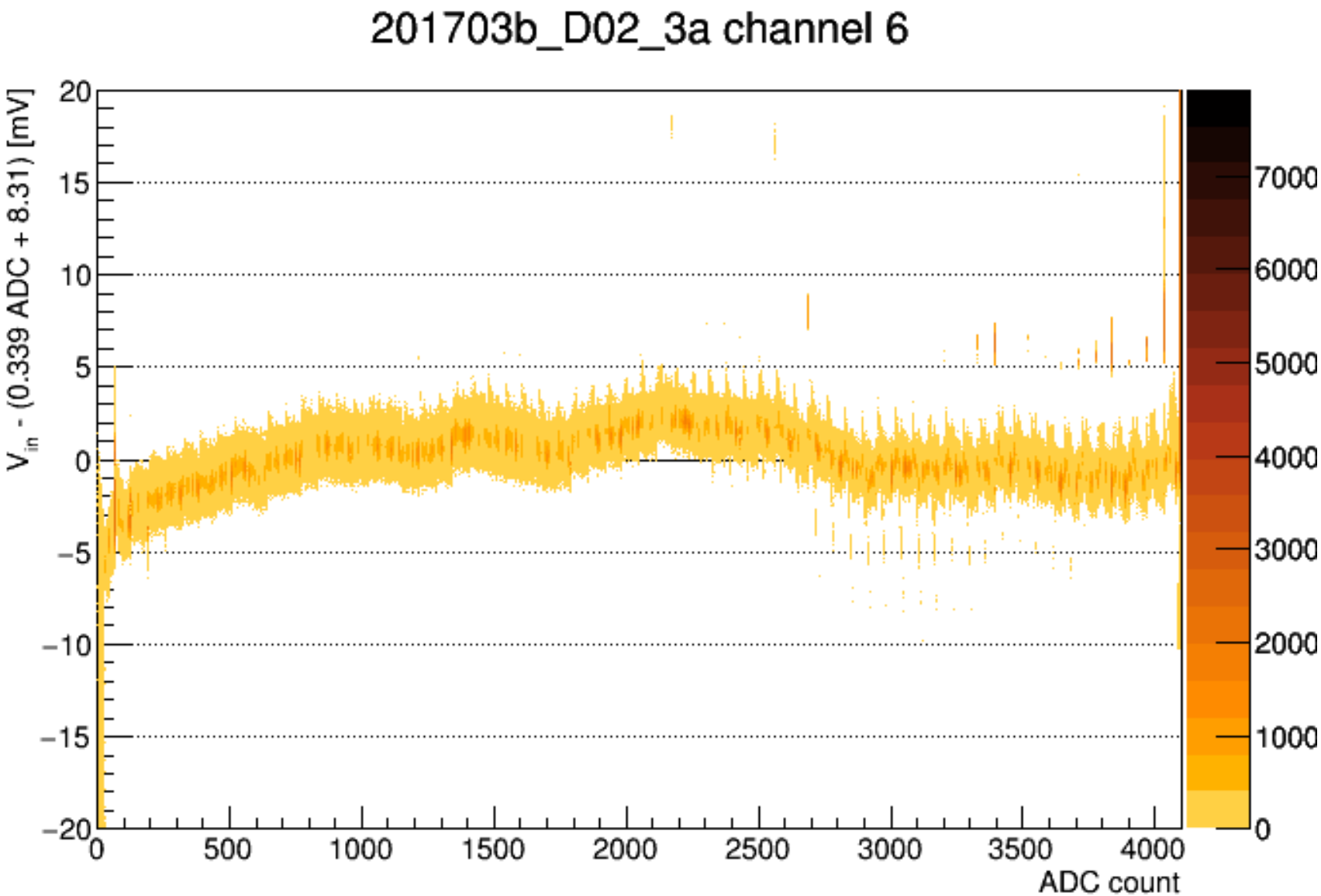
Chip D02, time 1a



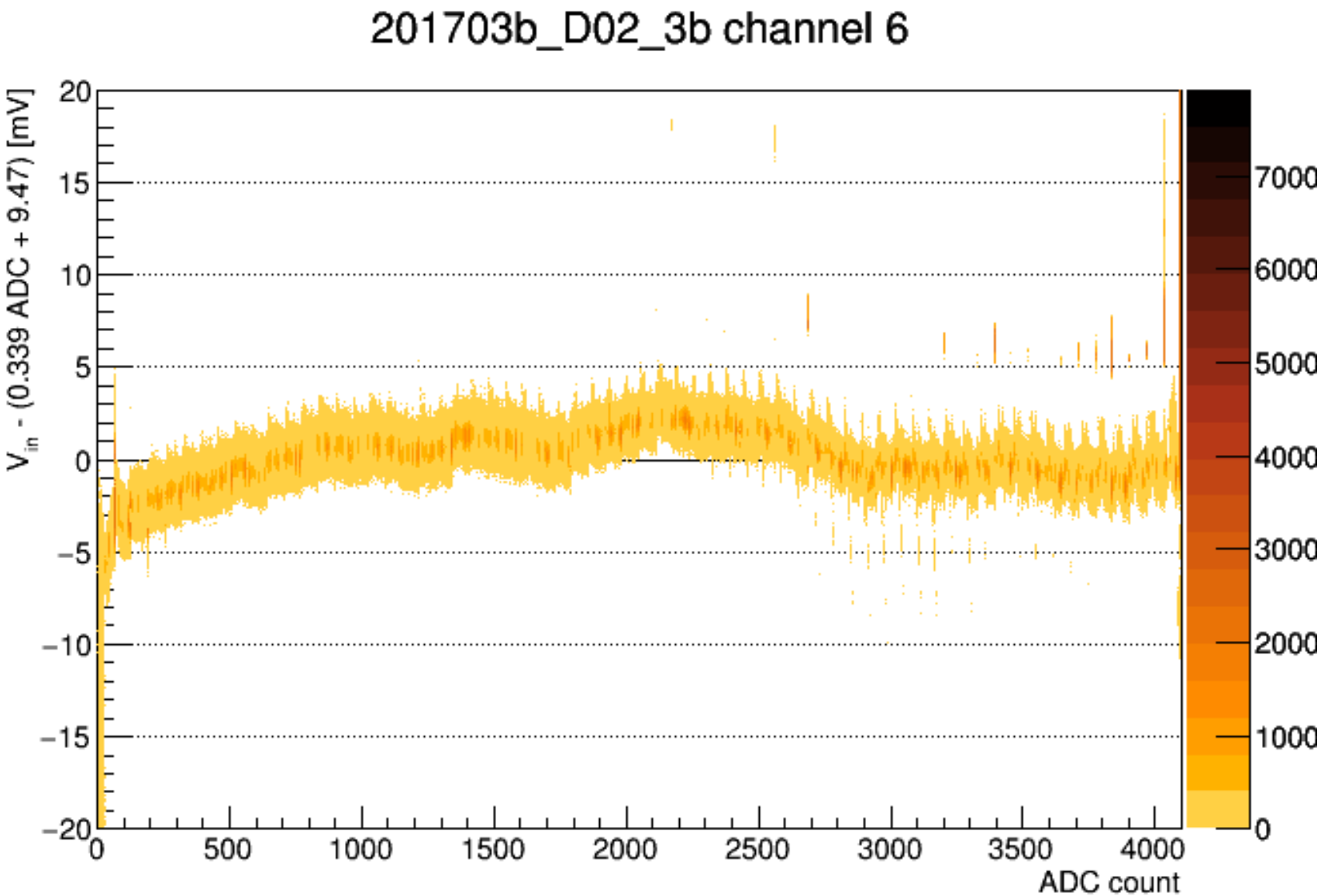
Chip D02, time 2a



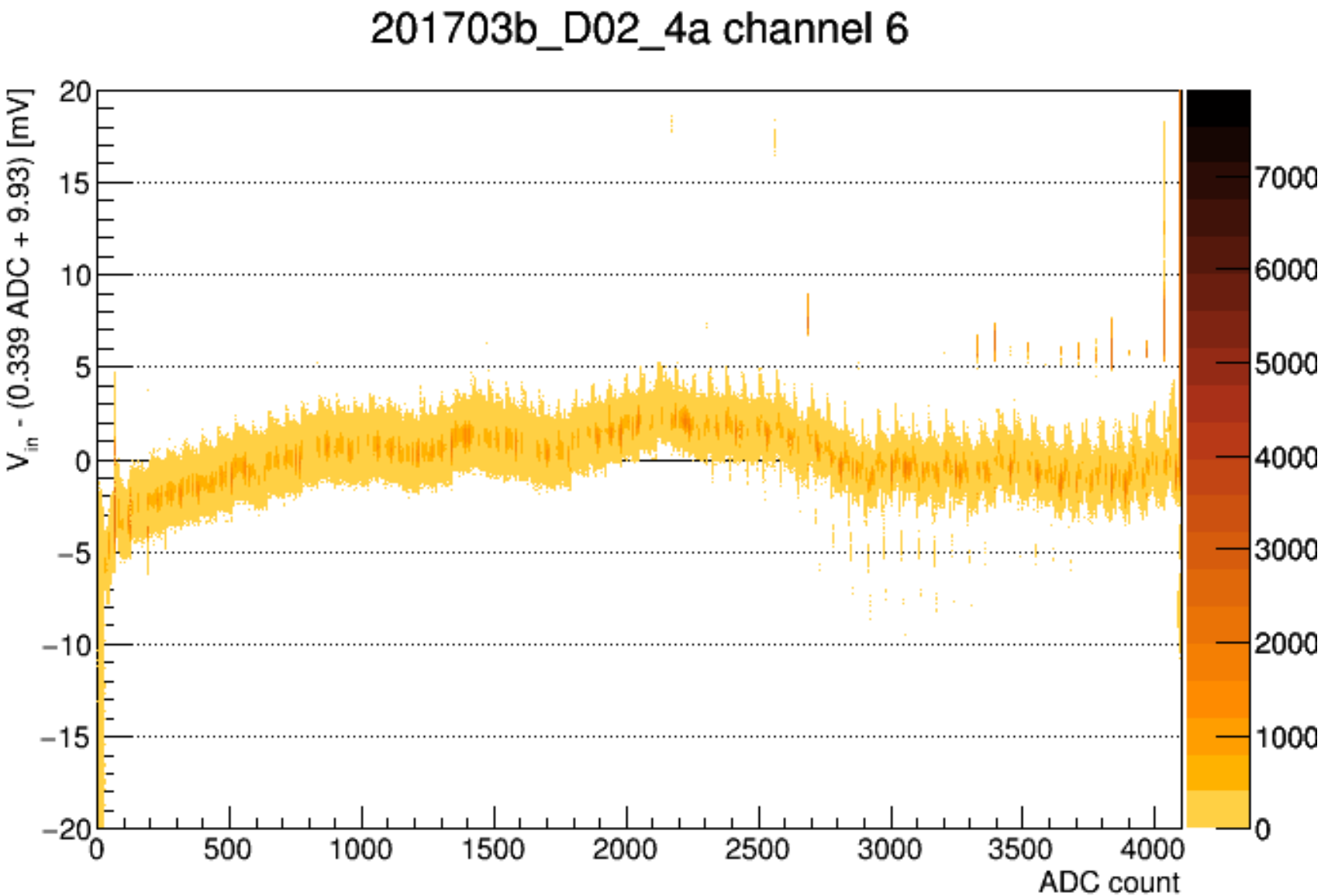
Chip D02, time 3a



Chip D02, time 3b



Chip D02, time 4a



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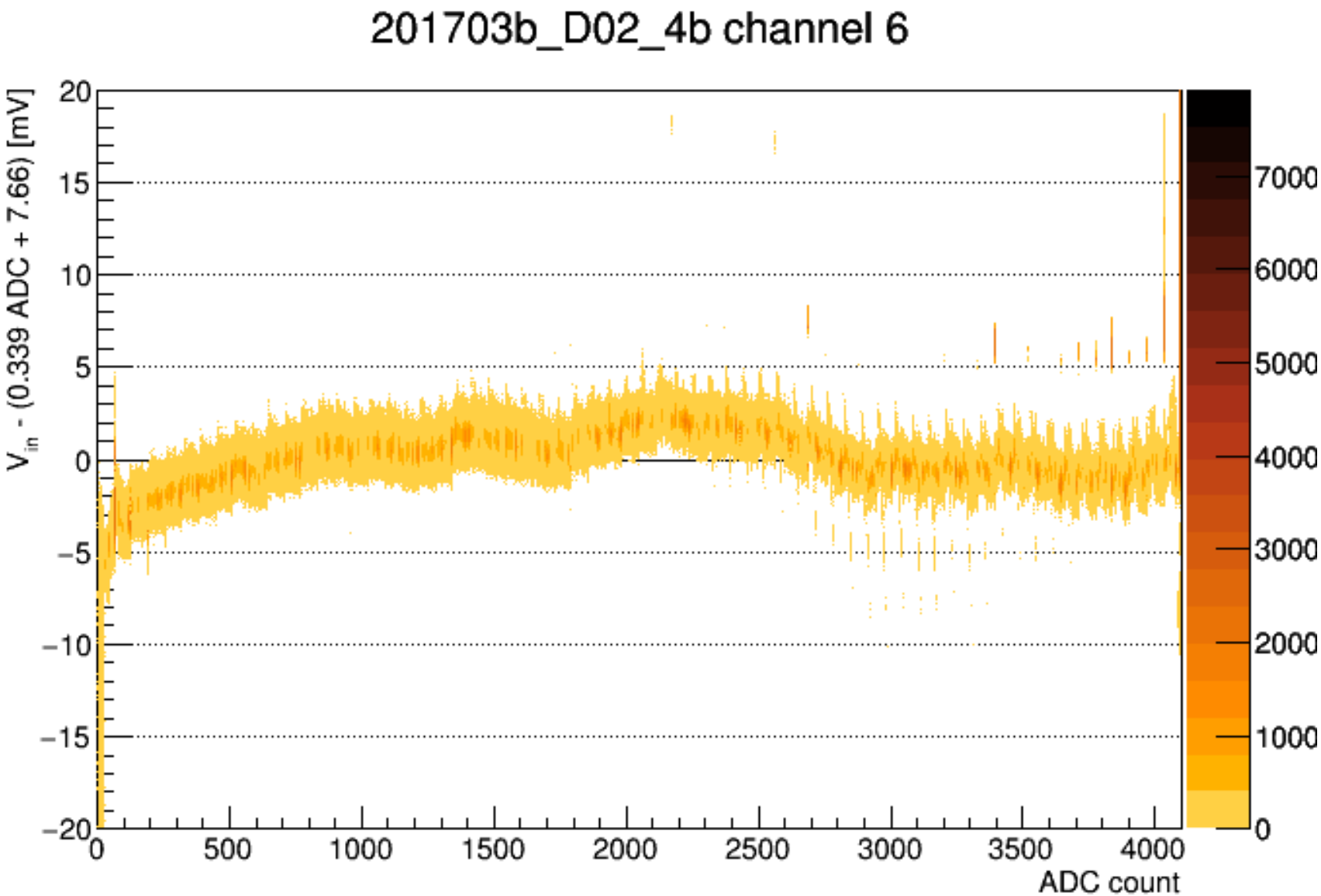
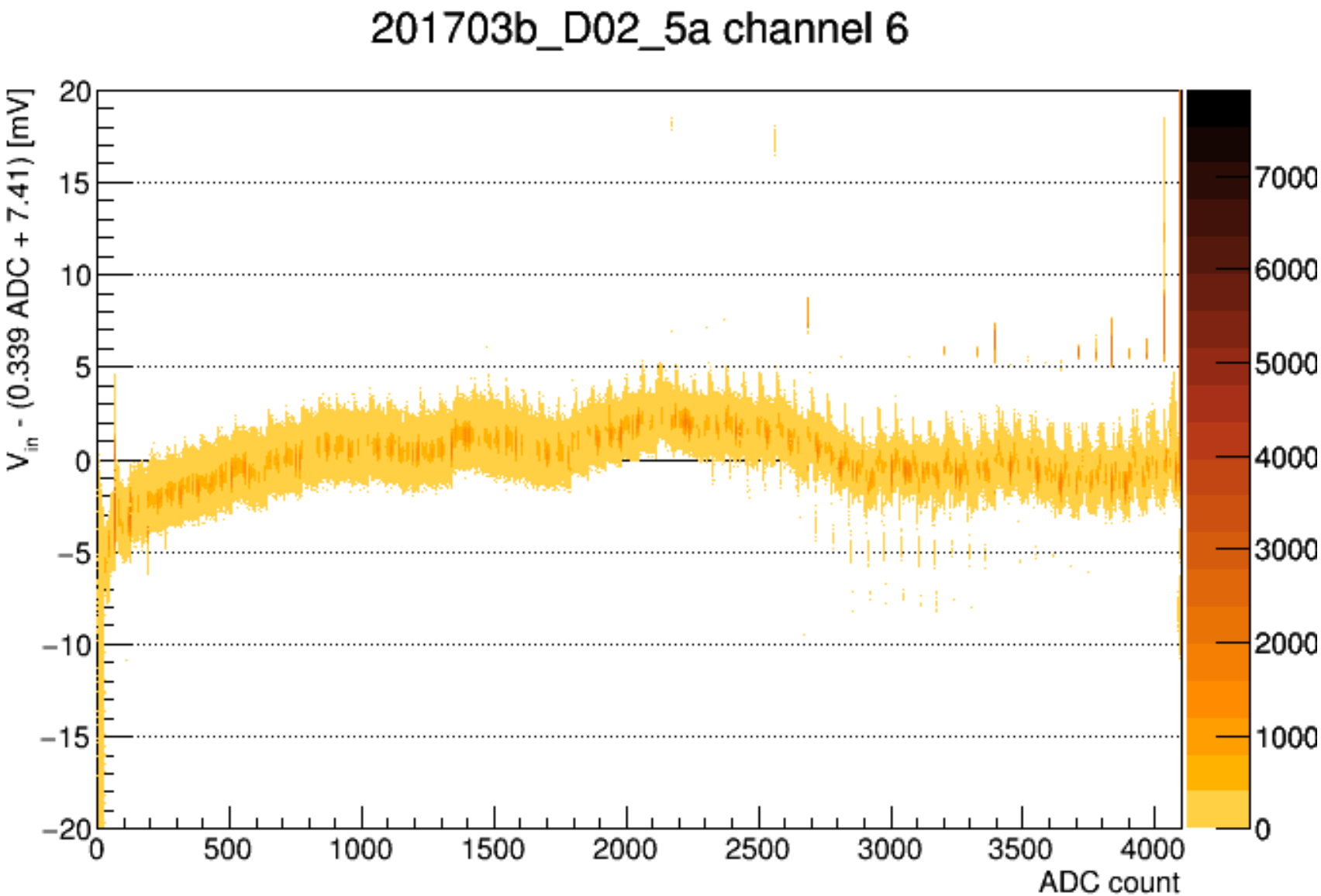
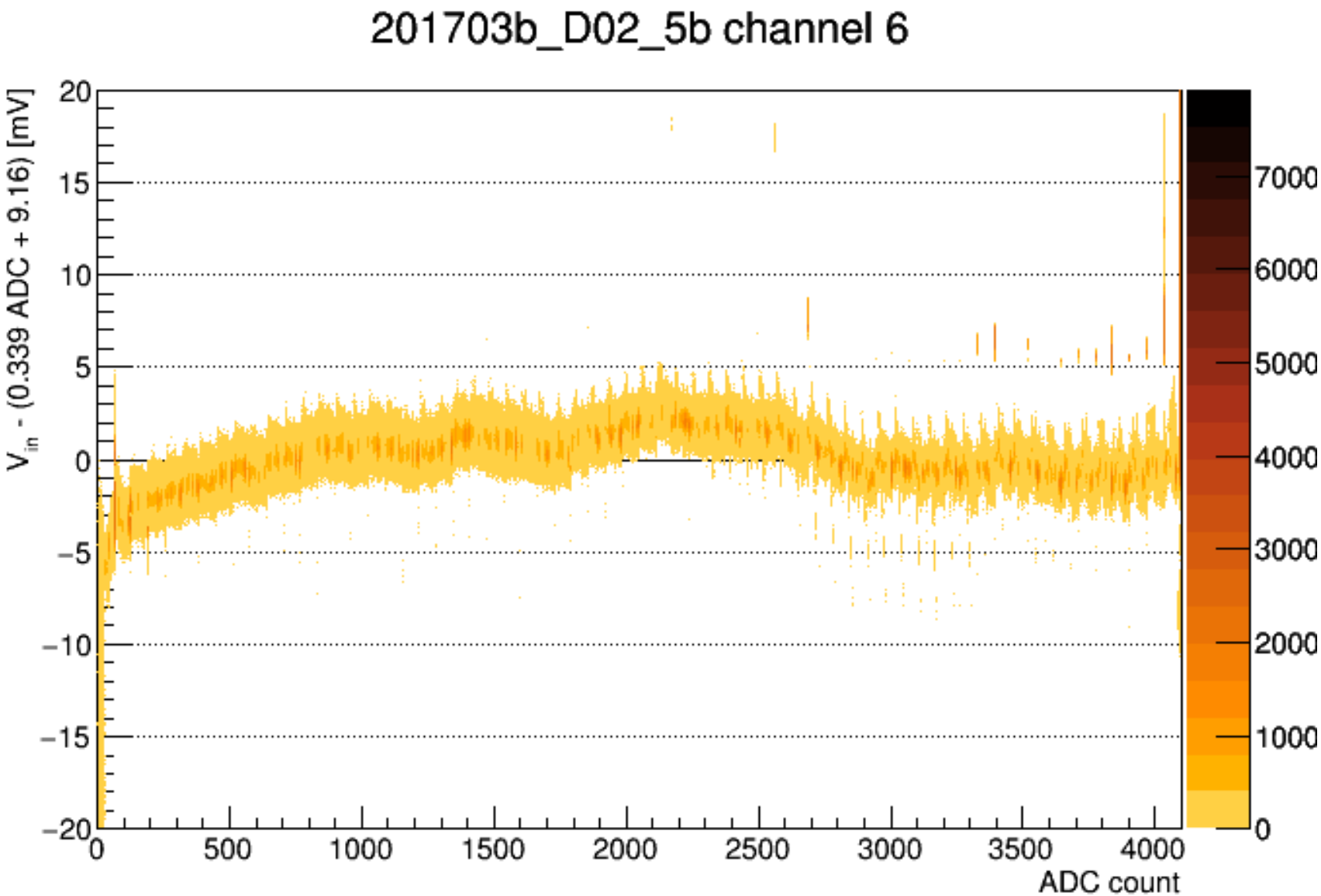


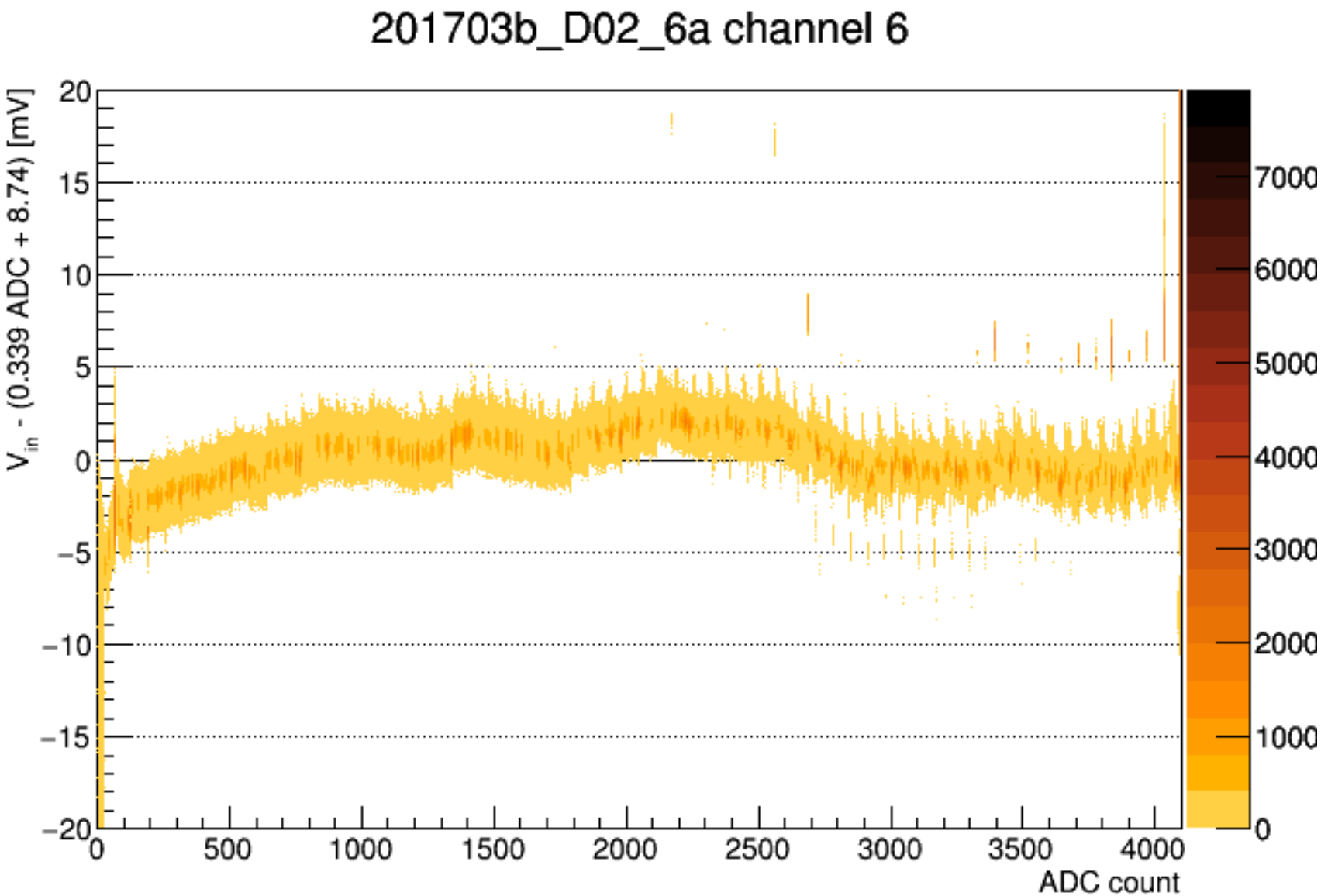
Chip D02, time 5a



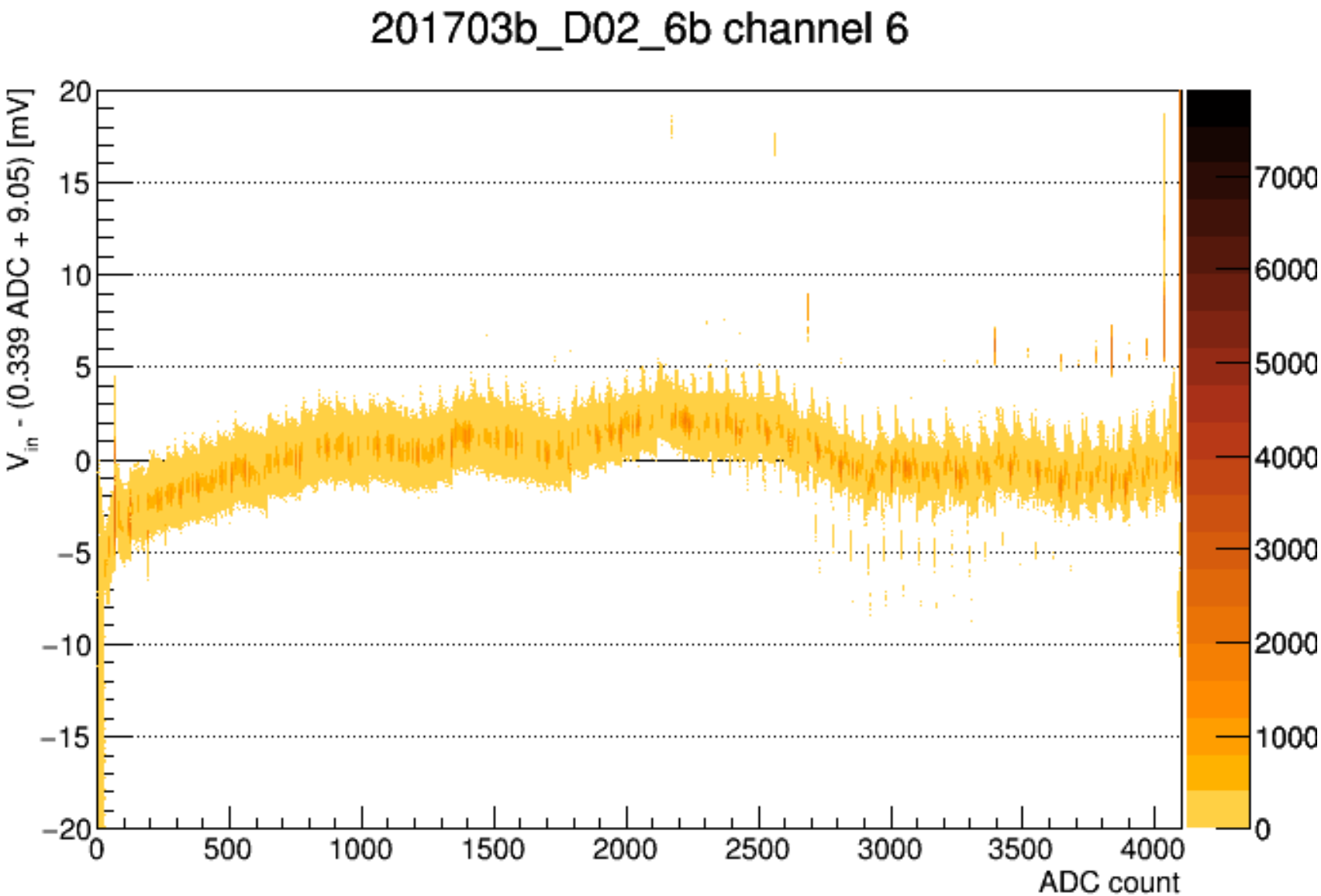
Chip D02, time 5b



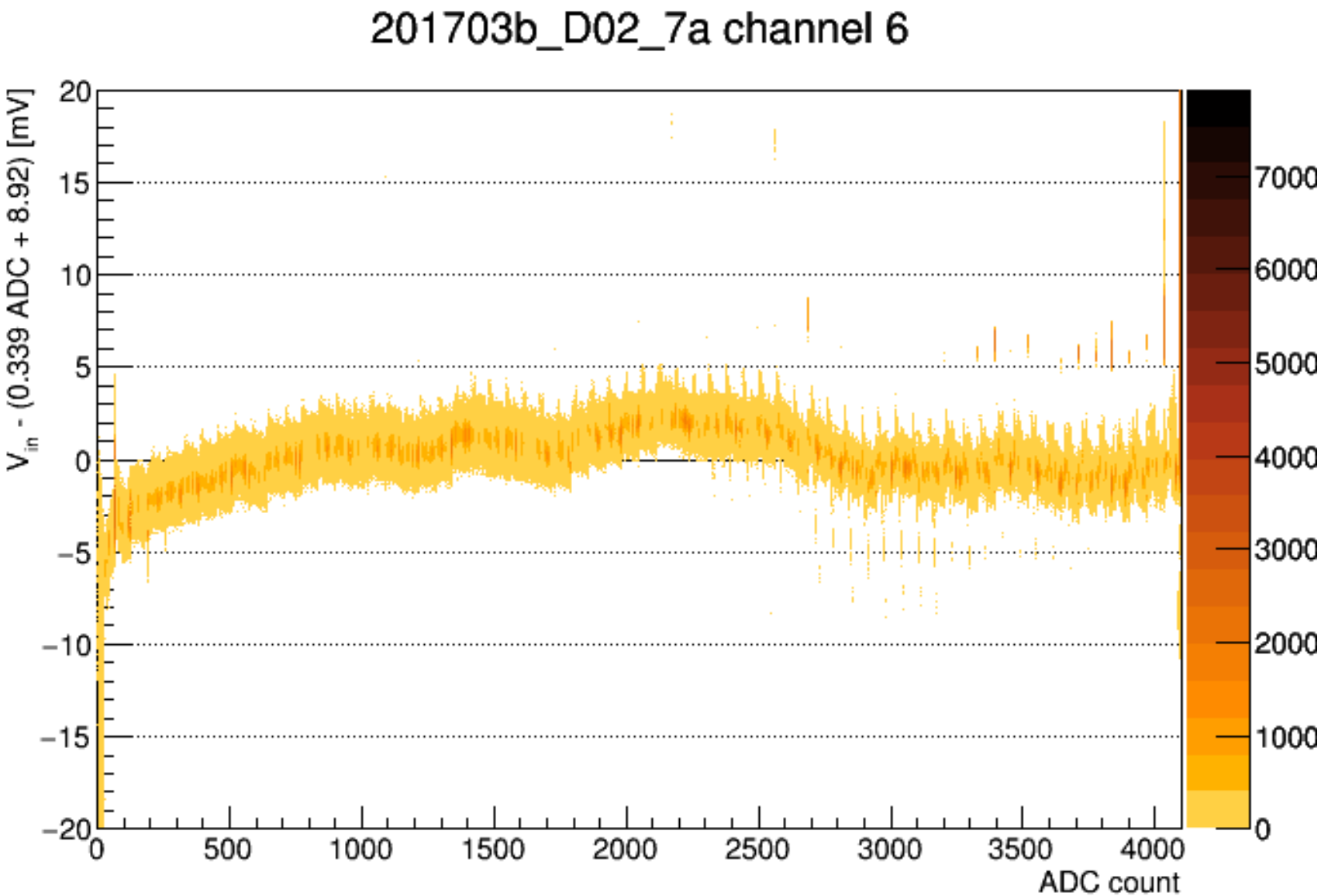
Chip D02, time 6a



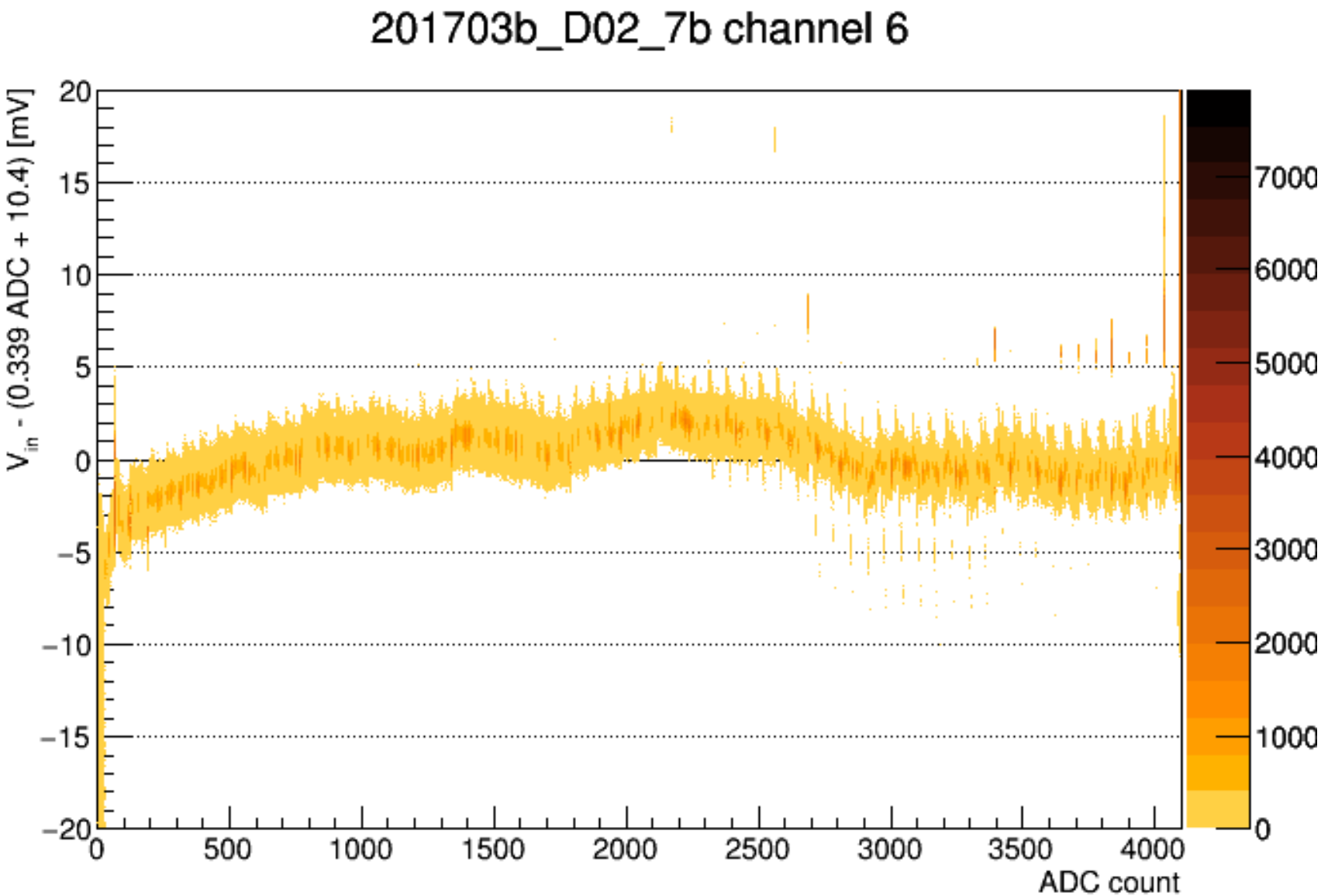
Chip D02, time 6b



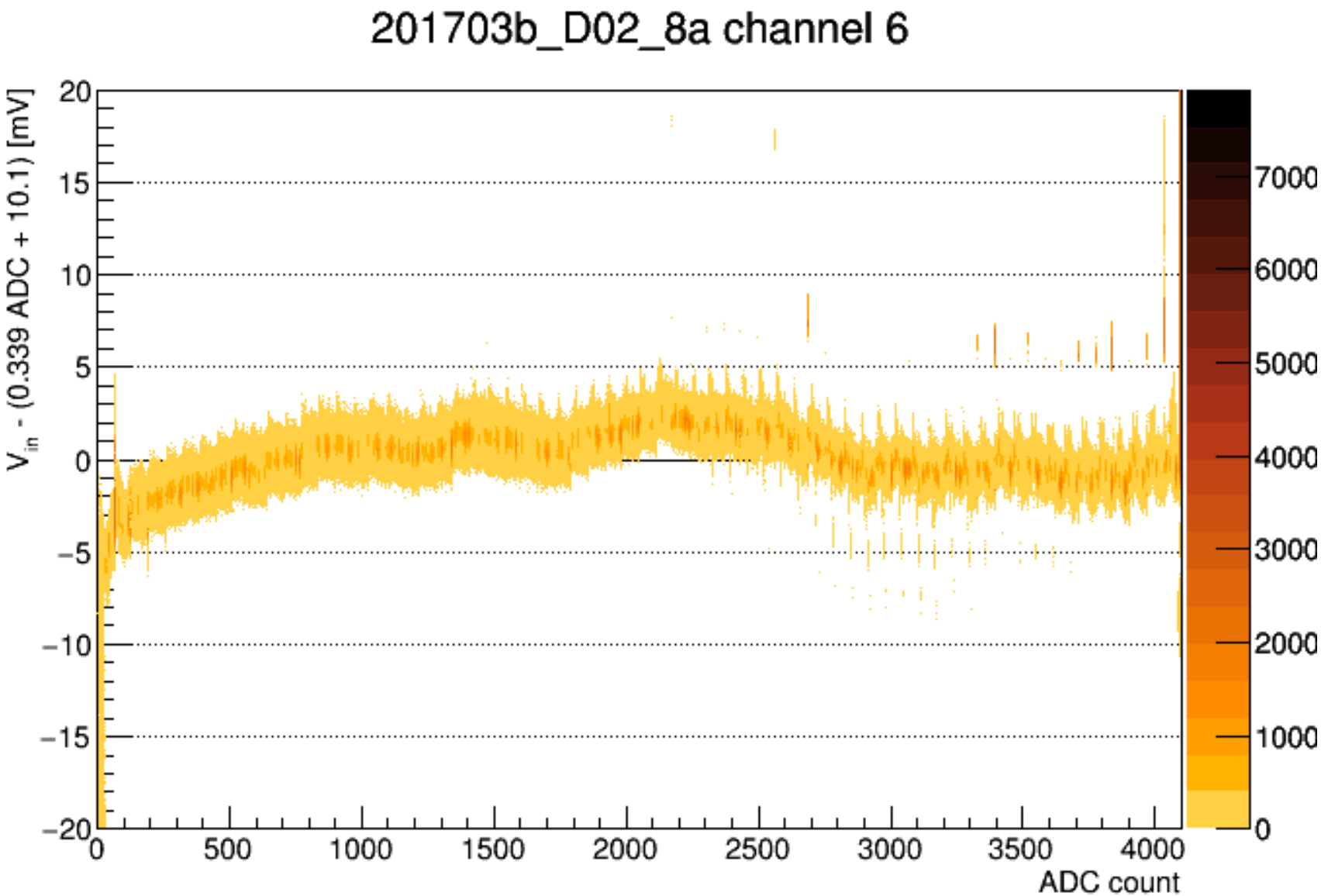
Chip D02, time 7a



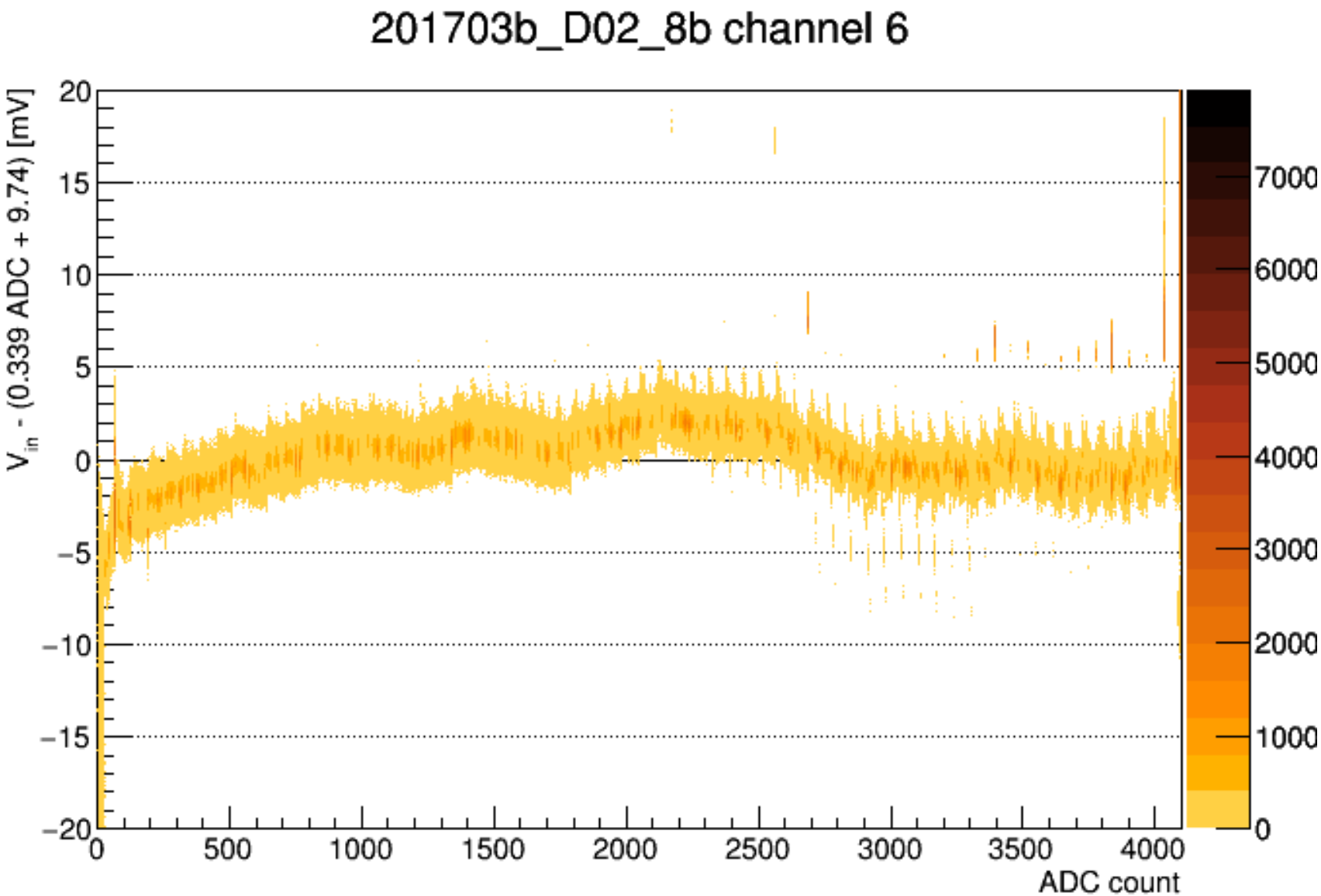
Chip D02, time 7b



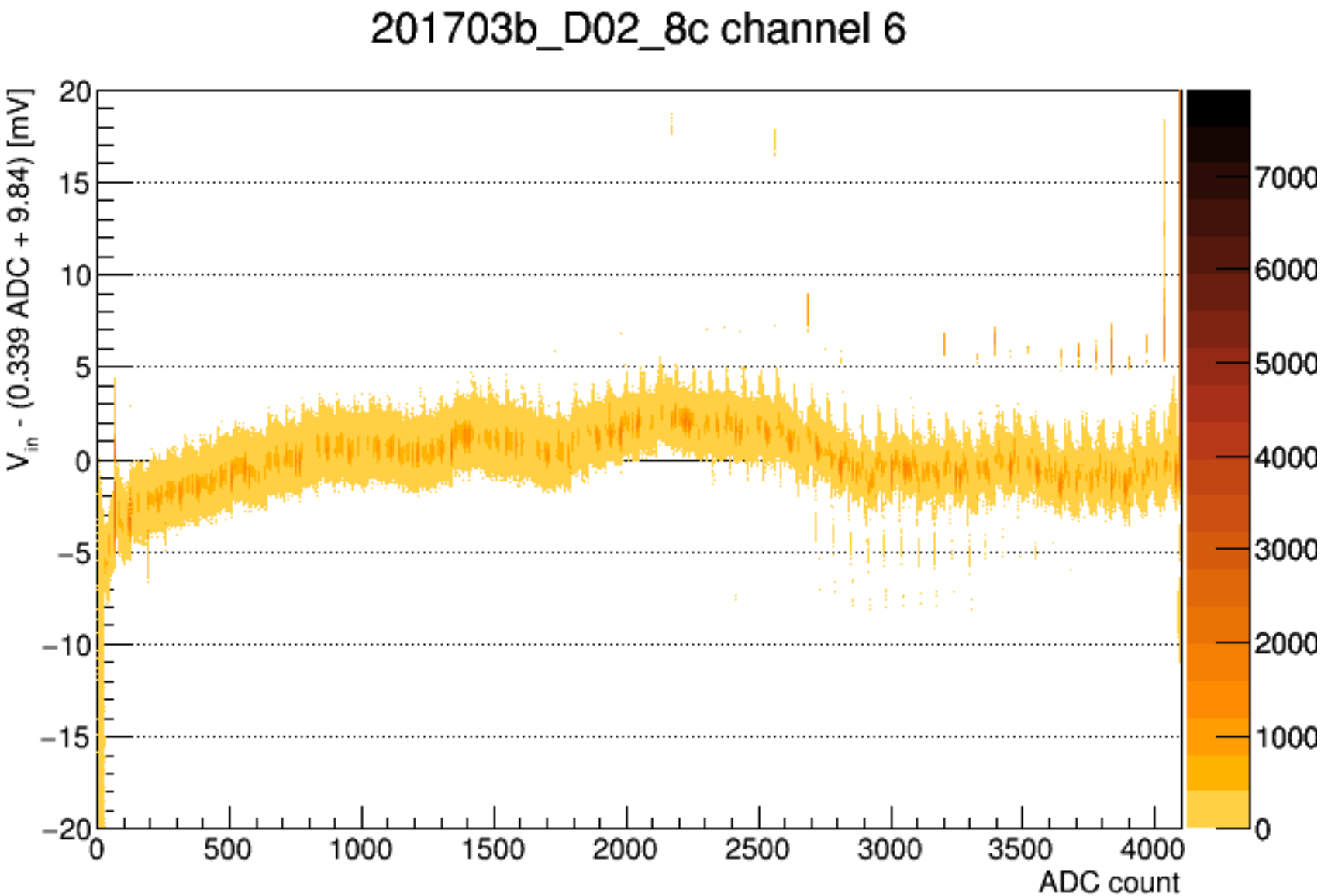
Chip D02, time 8a



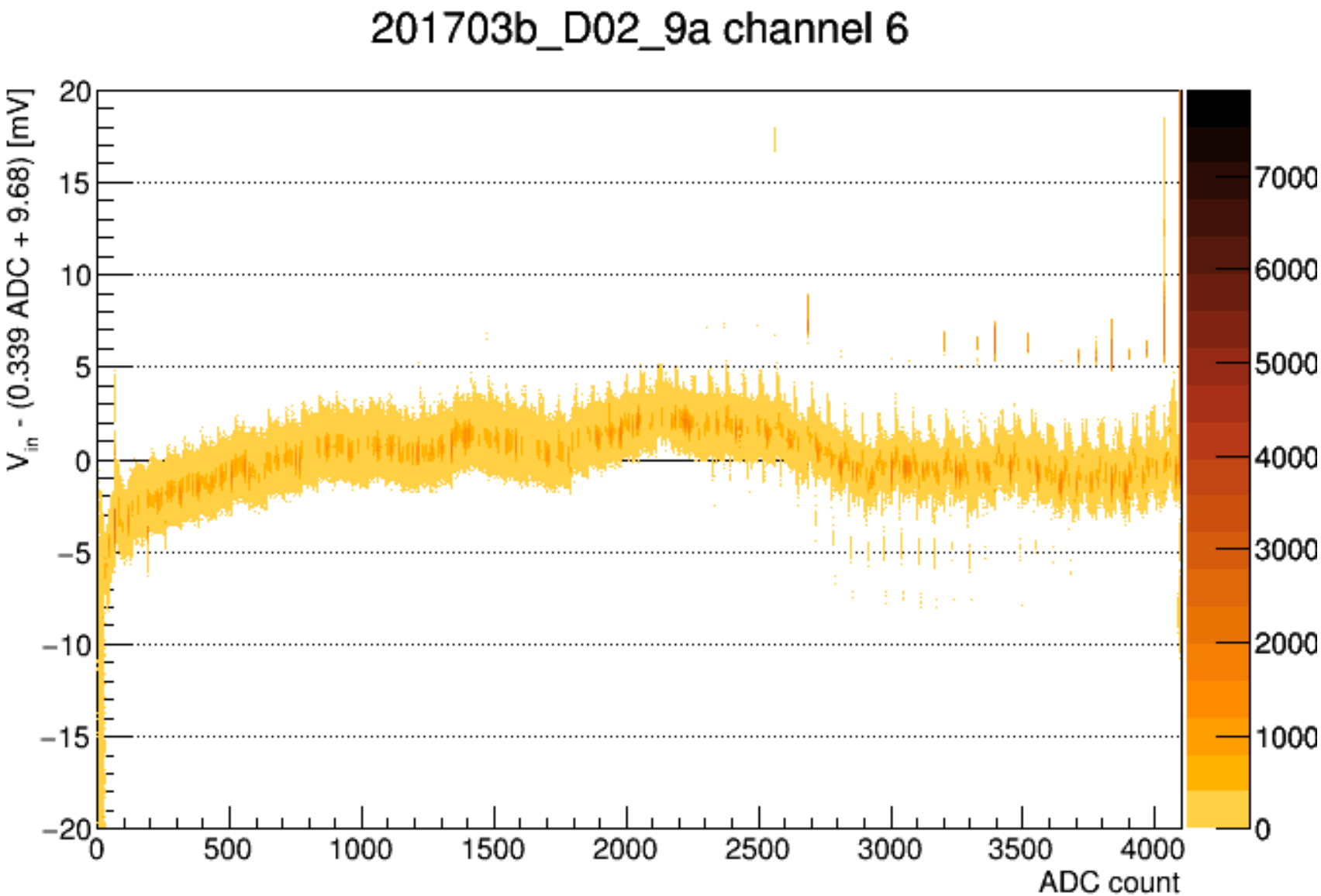
Chip D02, time 8b



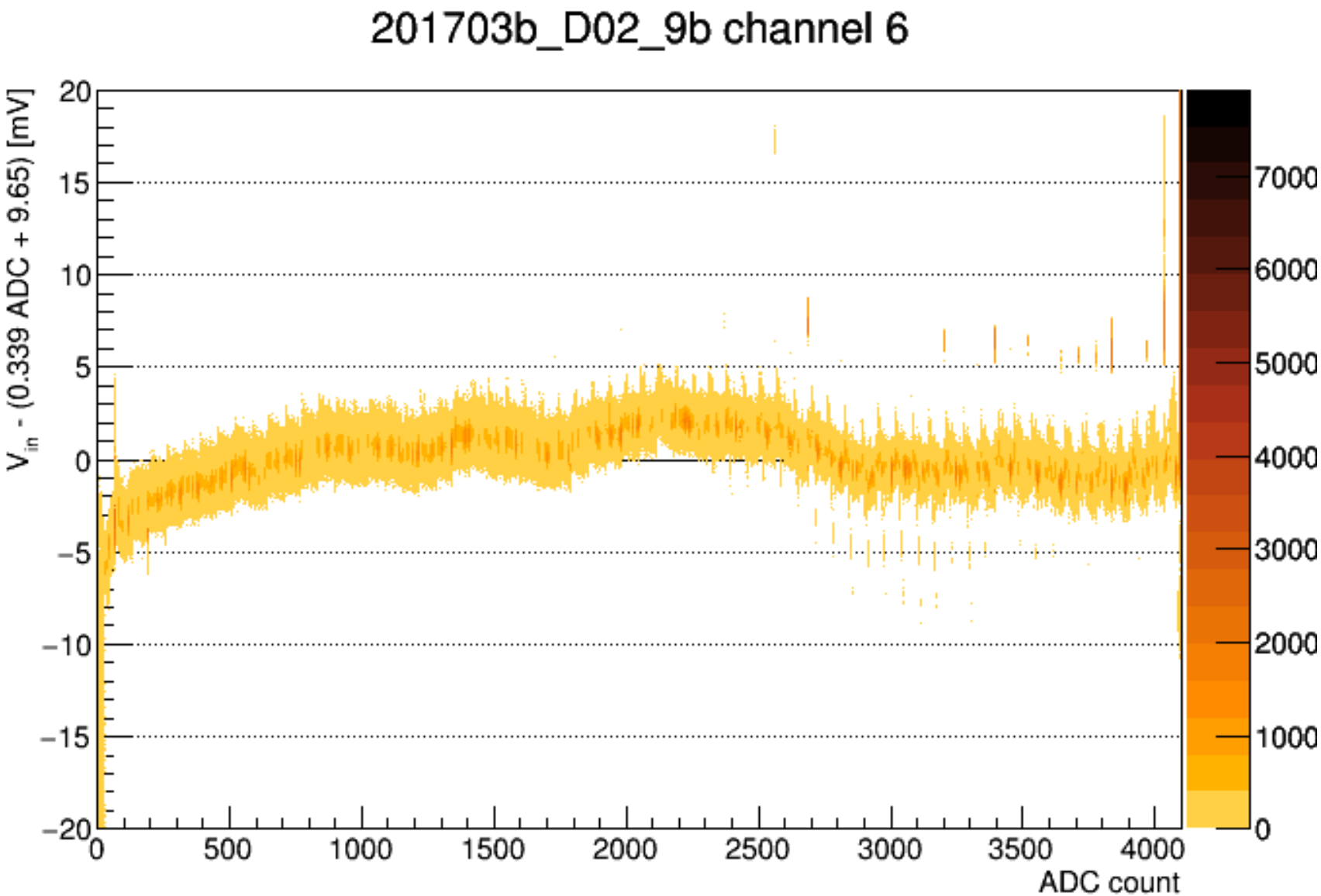
Chip D02, time 8c



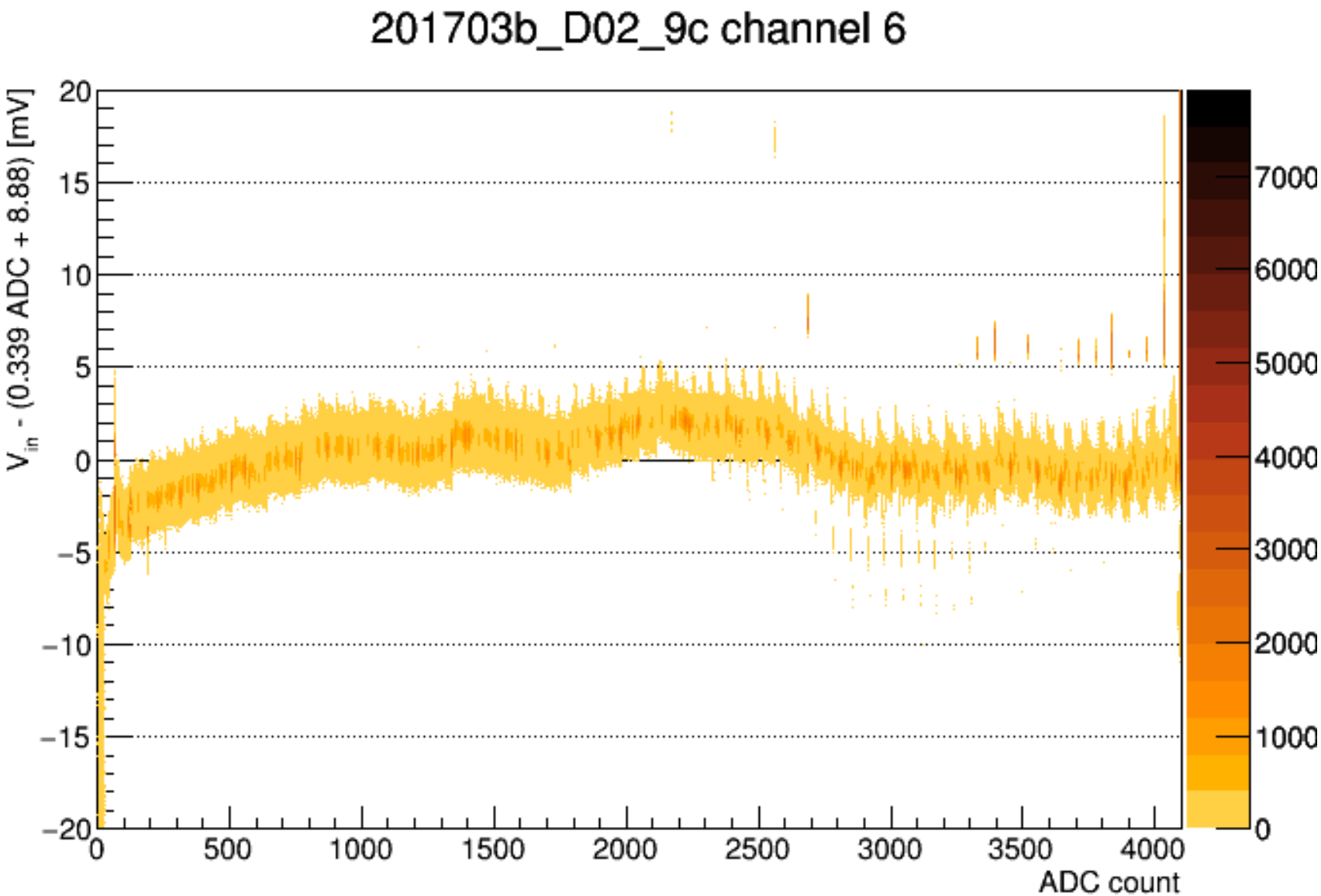
Chip D02, time 9a



Chip D02, time 9b



Chip D02, time 9c



How significant is time dependence?

I looked for channels which are sometimes bad

- I.e. RMS < 1.0 for some times and > 1.0 for others
- Table give % bins always good, always bad and varying for each channel

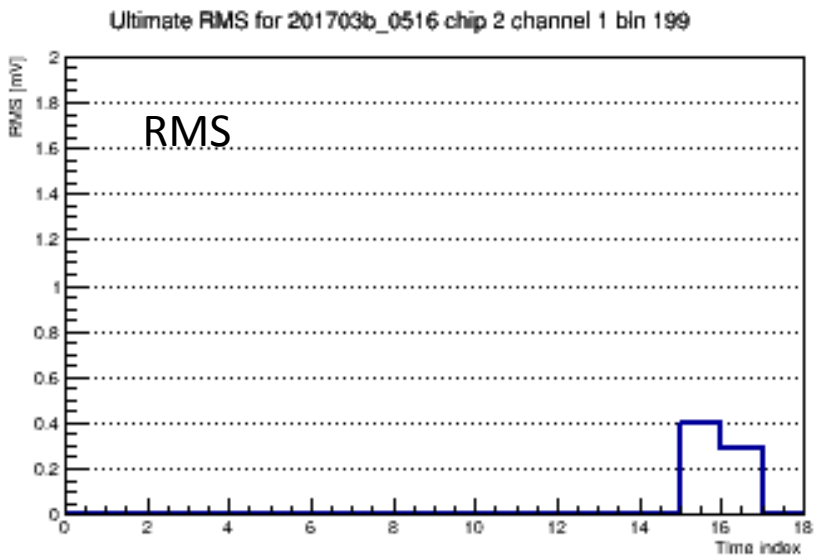
Chan	good	bad	vary	Chan	good	bad	vary
0	88.4	4.6	7.0	8	99.5	0.2	0.3
1	96.5	3.1	0.4	9	94.3	3.1	2.5
2	97.2	1.7	1.1	10	98.1	1.5	0.3
3	97.4	2.0	0.6	11	98.6	0.9	0.4
4	94.5	4.5	0.9	12	94.5	4.2	1.2
5	97.4	2.0	0.6	13	98.4	1.2	0.4
6	97.1	2.1	0.8	14	99.6	0.2	0.2
7	99.0	0.5	0.4	15	98.7	1.0	0.2

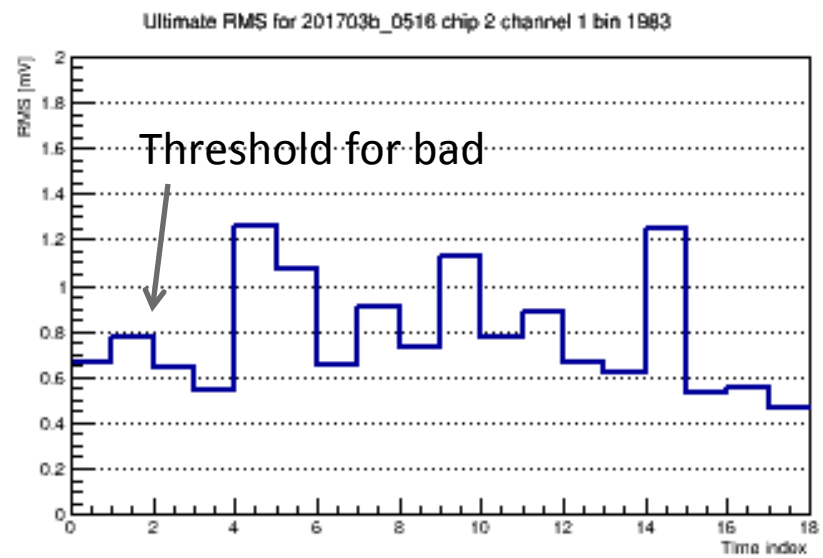
Significance of time variation (cont.)

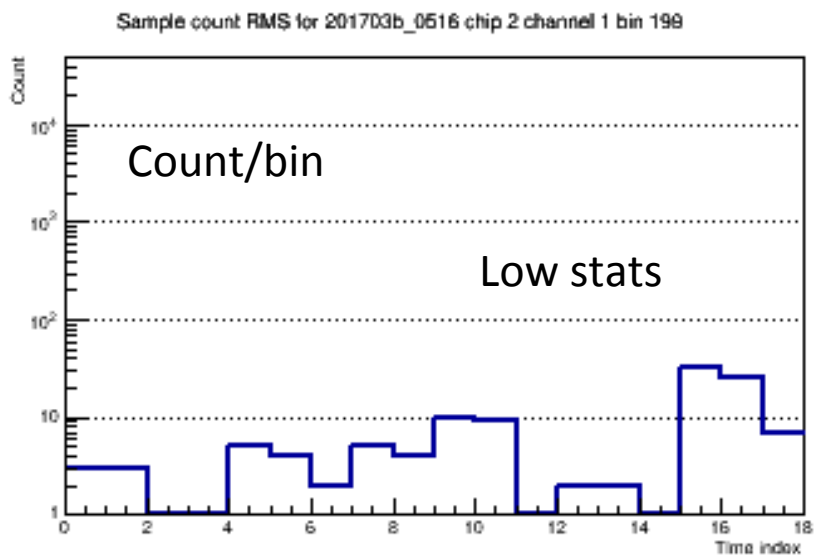
Significant fraction of bins show variation

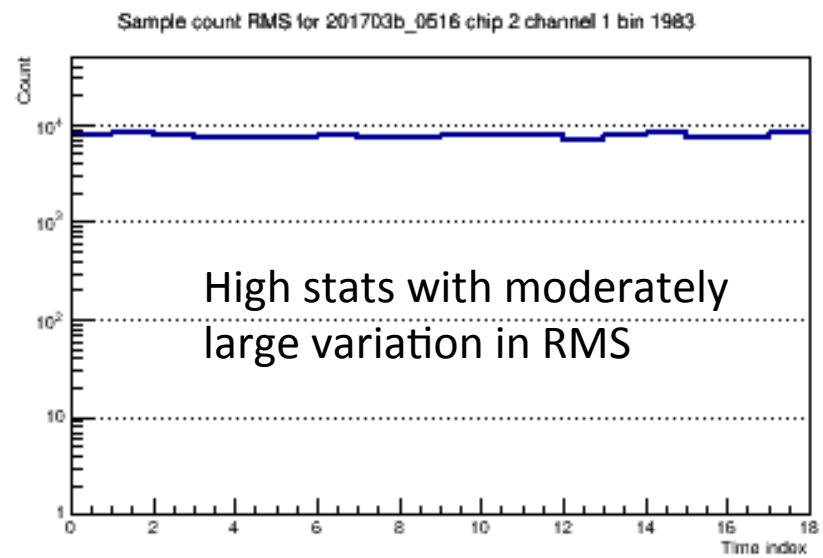
- But these may have low sample population
- Or may be right on the threshold
- See plots in appendix 3
  - One example on following page
- More work needed to quantify behavior

Time varying bins 6









Comments/Conclusions

ADC does show some time dependence

- For chip in board, kept cold and powered
- Gain is very stable
- Residual from linear calibration is also pretty stable
- But there are changes in bad channels (RMS) and tails day-to-day
  - Probably want to look at multiple ramps to identify all bad/tail channels

Next

- Quantify changes in bad channels and tails

Appendix 1

Analysis procedure is described on the following slides

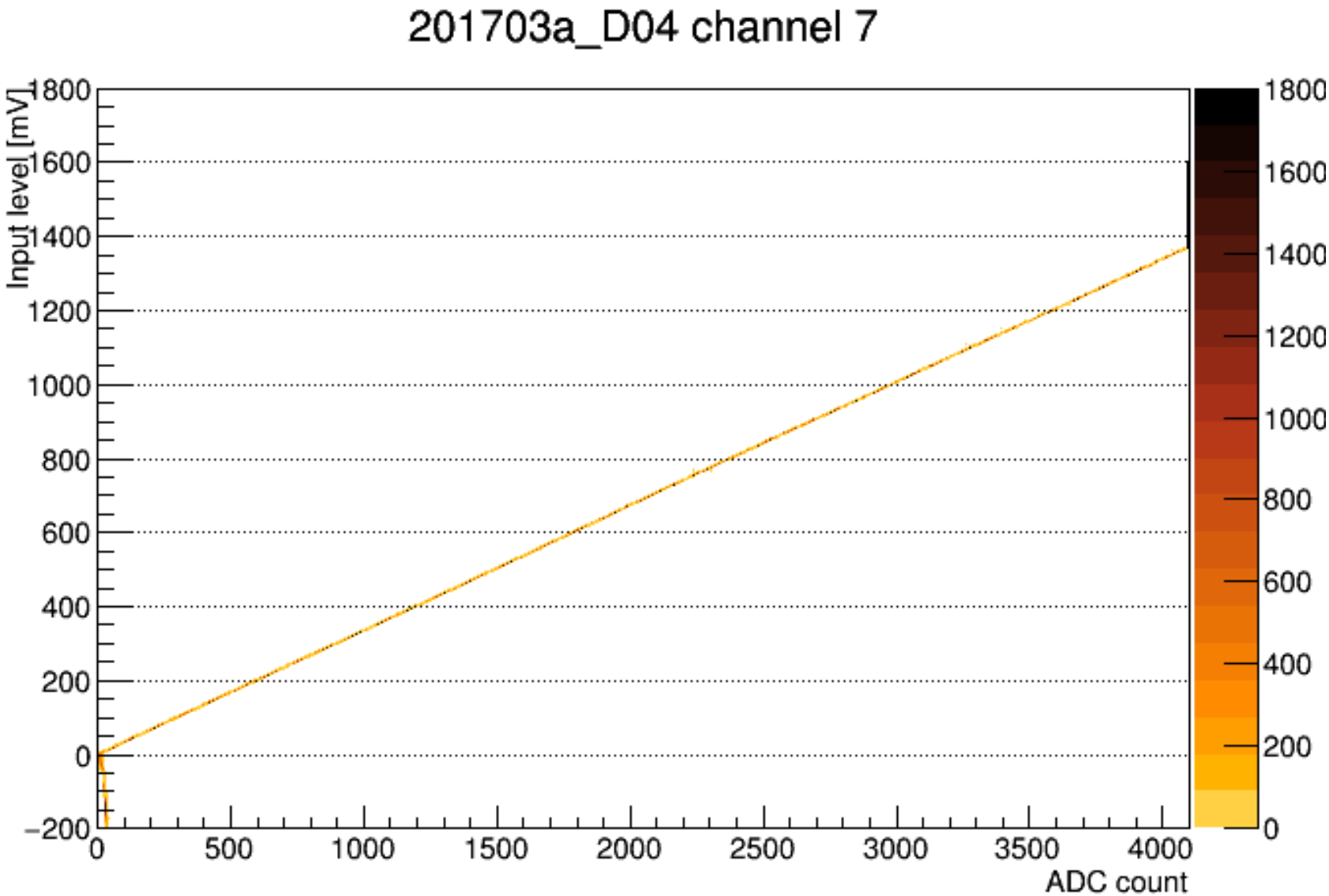
Data analysis 1: linear fit and residual

I process each channel separately

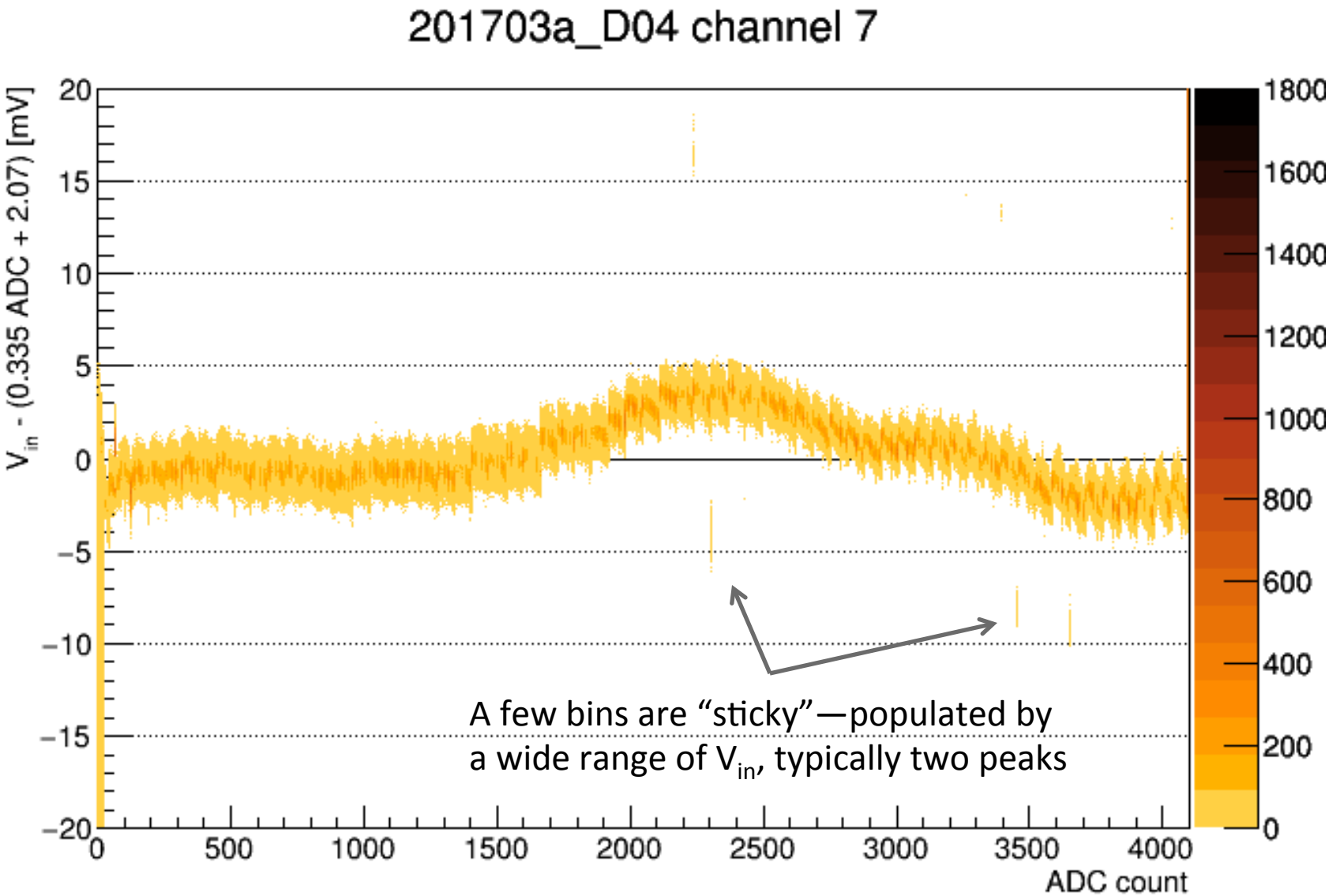
Initial data analysis

- Read samples from the provided file for the chip and channel
- Create 2D histograms of inverse response: V_{in} vs. bin
  - bin = ADC code and covers the range [0, 4095]
- I make a linear fit of the inverse response for each channel
  - V_{in} = gain×(ADC code) + offset
  - Require 64 < ADC < 4095
  - And 0 < V_{in} < 1600 mV
- I then plot the linear-fit residual
  - I.e. the difference between the measured V_{in} and the linear-fit value for each sample
- Examples for one channel follow
  - March data for chip D04 channel 7
  - This is a “good” channel

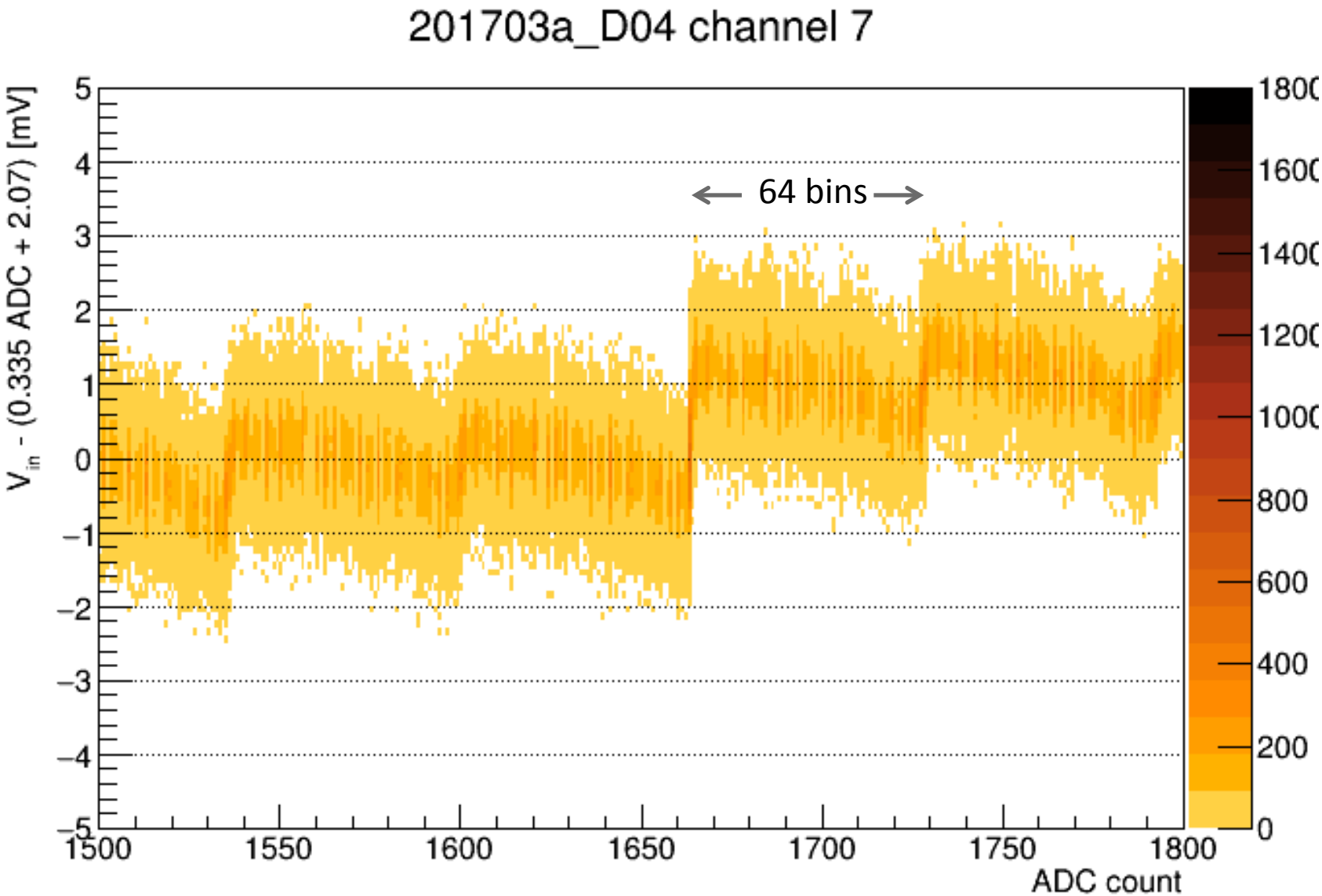
Inverse response



Linear fit residual



Linear fit residual zoomed



Data analysis 2: calibration and resolution

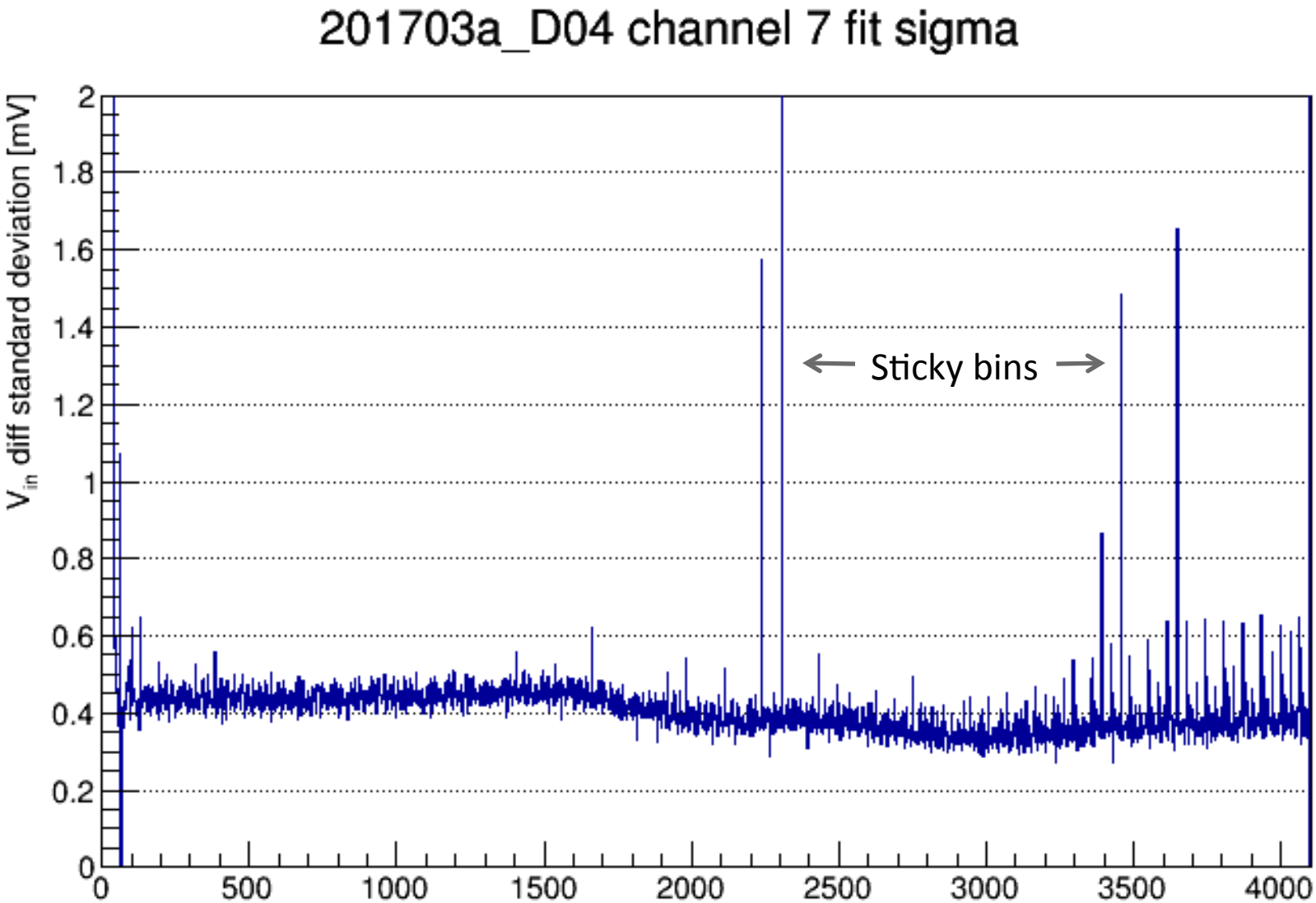
From fit and residual, define ultimate calibration for each bin

- Mean of the residual plus the linear fit is the calibrated value
- I.e. a lookup table for each channel with approximately 4000 entries
- May not be final calibration strategy but this is the best we can do

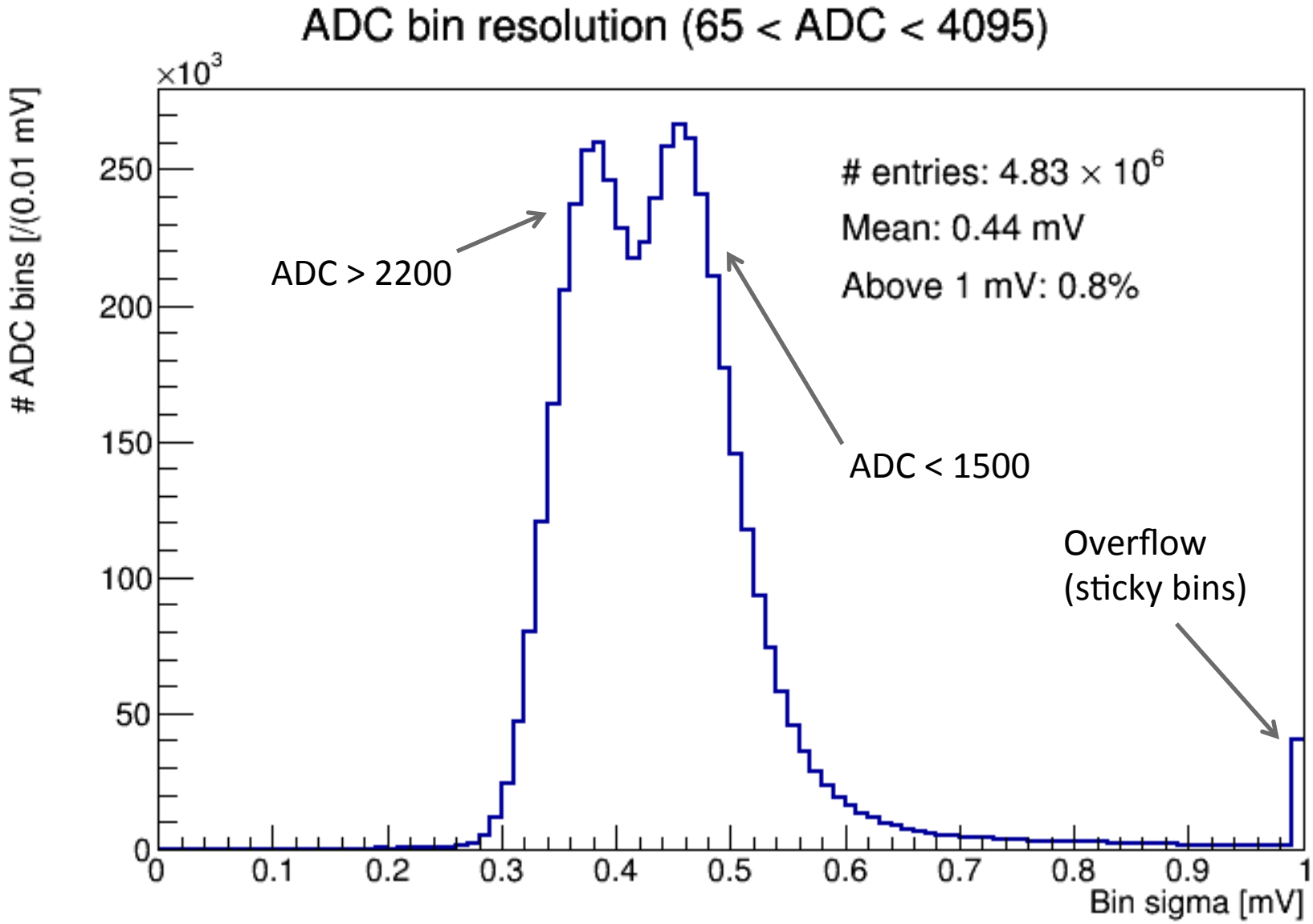
Ultimate resolution

- The spread in V_{in} provides a measure of the uncertainty in the voltage measurement for each bin
- Characterize this with the standard deviation, the RMS from the mean
- Typical example follows (again a "good" channel)
- Typically this is around 0.5 mV
  - Naïve expectation for perfect 12-bit ADC is 0.1 mV
- Following page shows the distribution for all chips

Ultimate resolution for one channel



Ultimate resolution for all chips



Data analysis 3: sticky bins

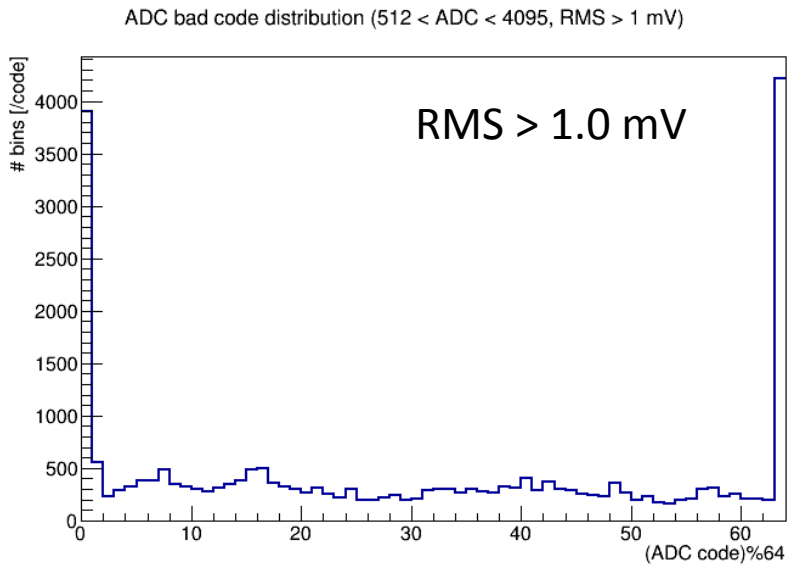
Sticky bins

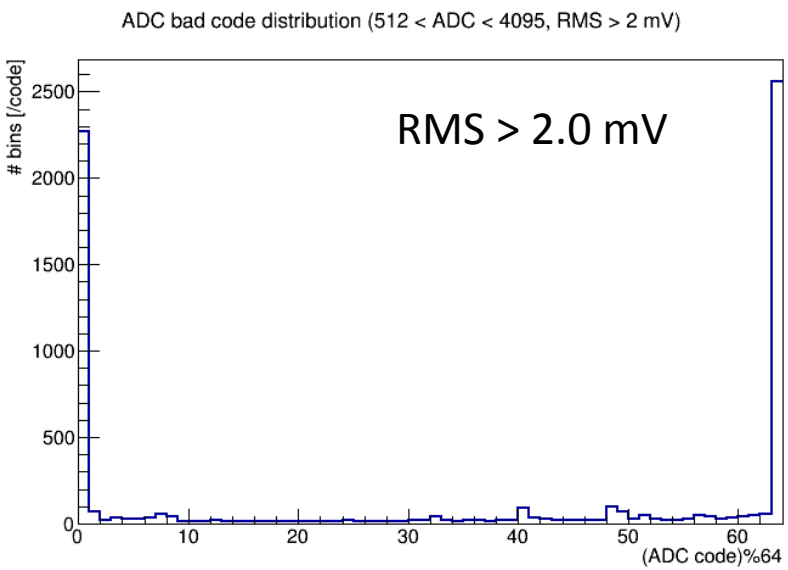
- There are always a few (sometimes many) bins populated by a wide range of input voltage
  - Can be identified by poor resolution i.e. large RMS
  - Often bins where LSB6 (lower six bits) are all 0 or all 1
  - Often a double peak where one peak is in the expected place
- Distribution for March 2017 data shown on following slide
  - 25 chips ➔ 400 channels ➔ 1.6M bins
- When resolution for a bin is too large, we can get better precision by discarding that measurement and interpolating between neighboring bins
- Plan to maintain a list of sticky bins for each channel so we know which bins to discard
  - Use the resolution (RMS from mean) to identify sticky bins
  - Here define sticky as RMS > 1.0 mV
    - This is equivalent to an input noise of 450 e for preamp gain 14 mV/fC

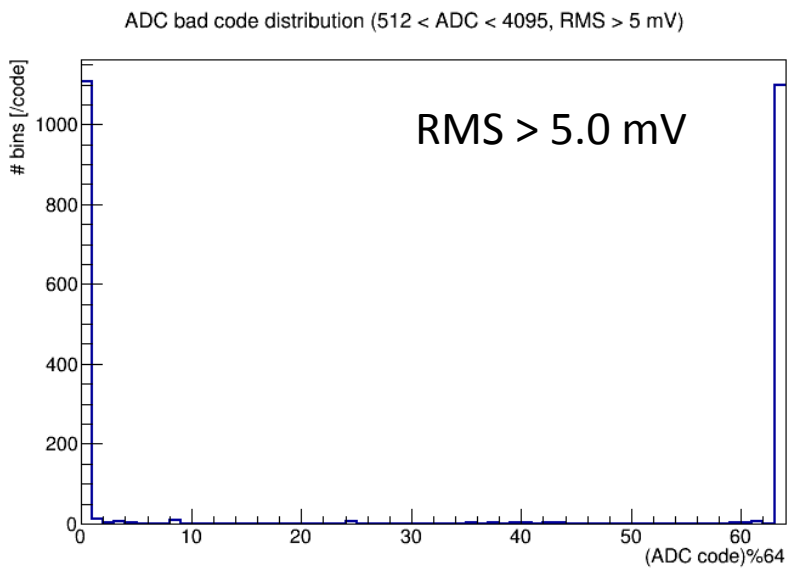
Sticky bins: LSB6 distributions

Plots show LSB6 for bad bins

- LSB6 = six least significant bits
  - I.e. bin%64
- For different RMS thresholds
- Classic values of 0 and 63 are enhanced for all thresholds
  - Dominate for high threshold







Data analysis 4: ADC quality

Voltage response

- We evaluate ADC quality as a function of voltage
  - No ADC channel covers the full range of interest (0, 1600) mV
- Evaluate three metrics: efficiency, resolution and tails
- All evaluated as functions of V_{in} in bins of 20 mV
- Results presented in "performance summary plots" (PSPs)
  - Example plot for an ADC bin follows
  - Not the bin used in earlier example plots—instead one with issues

ADC efficiency

- Define efficiency to be fraction of samples that land in good ADC bins
  - For each range of input voltage
  - Good means RMS(V_{in} residual) < 1.0 mV
- Performance summary plots show efficiency vs. V_{in} (blue histogram)
  - Following example is the same "good" channel as in earlier plots
  - Plots for all 76 chips in appendix

Data analysis 4: ADC quality (2)

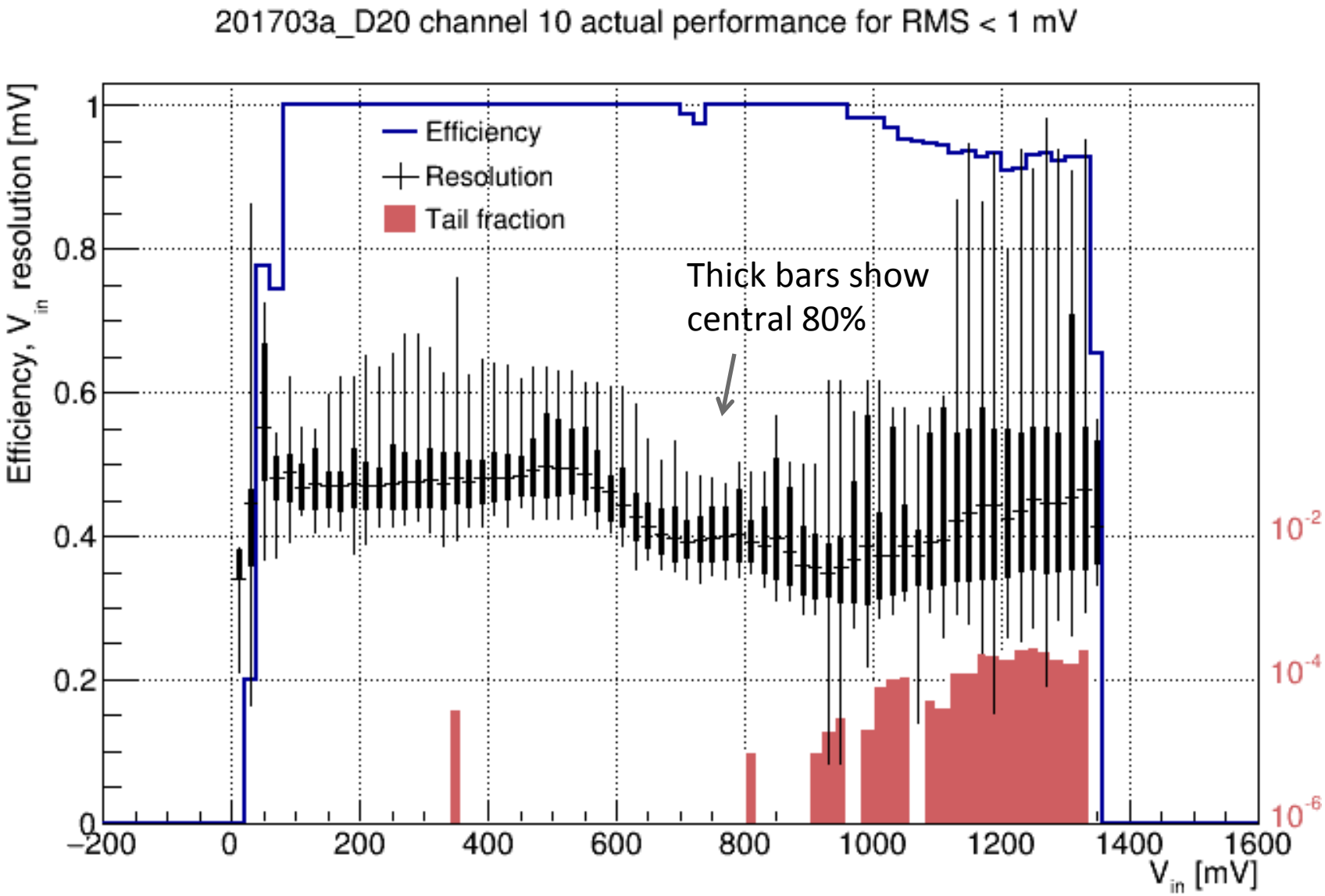
Resolution

- Resolution vs. V_{in} is shown on the same plot (black markers)
  - Evaluated as the RMS difference between the measured and true V_{in} for each sample in the voltage bin
    - Measured V_{in} is obtained by applying the calibration to the ADC count
  - Horizontal bars indicate the mean of this RMS for each bin
  - Error bars show the extent of the distribution of assigned uncertainties
    - Using all ADC bins populated by the samples in the voltage bin
    - Full range (earlier plots only showed central 80%)
    - Assigned uncertainty for and ADC bin is RMS(V_{in} residual)

Tail fraction

- The tail fraction is also shown (filled red histogram)
  - Fraction of samples in the voltage bin less than 5 mV from the true V_{in}
    - Previously used 5σ to define tail but this seems too tight
    - Because uncertainty at input to ADC is 1.3 mV
      - » 600 e with a gain of 14 mV/fC

Example performance summary plot



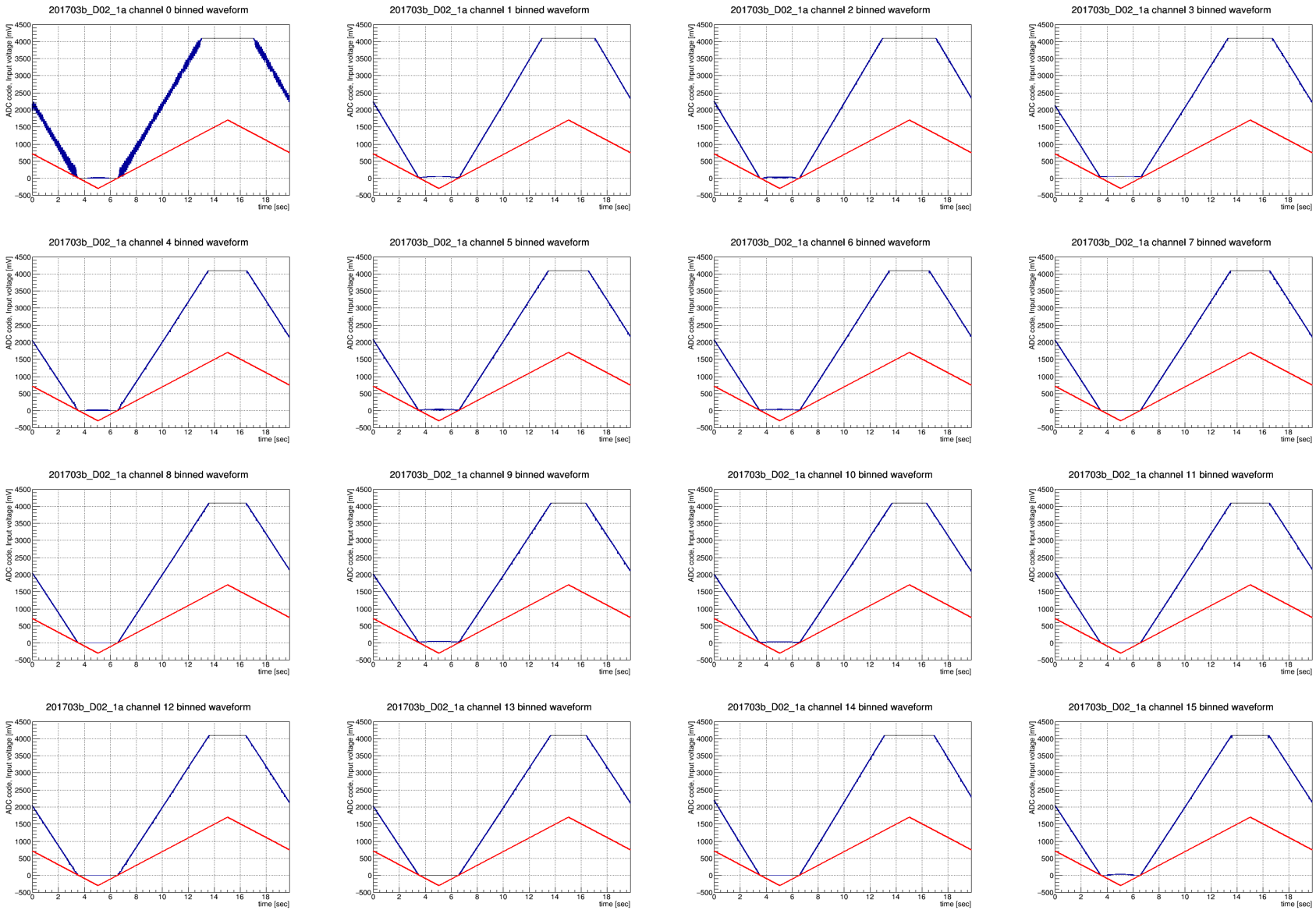
Appendix 2

Plots for all samples

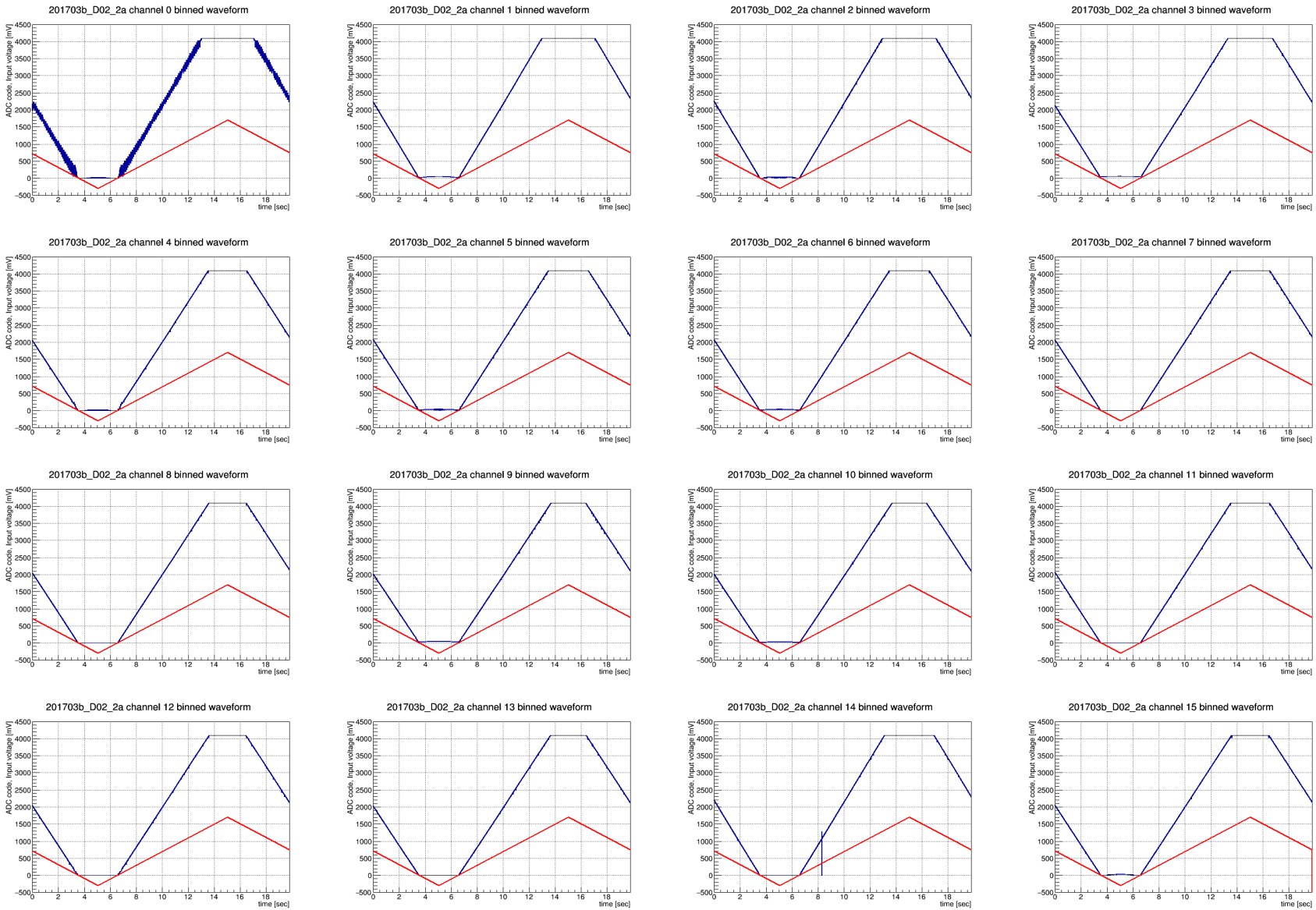
- Each page shows all channels for sample taken near the same time
- All 18 time samples for many variables:
  - Raw waveform and derived input voltage
  - Residual from linear fit
  - RMS from optimal calibration for each bin
    - Note we cut at 1 mV to identify bad channels
  - Tail fraction (RMS > 5 mV)
  - Performance plots
    - Efficiency (fraction of samples not bad)
    - Resolution (RMS distribution of good samples)
    - Tail fraction
    - All in bins of input voltage

Waveforms

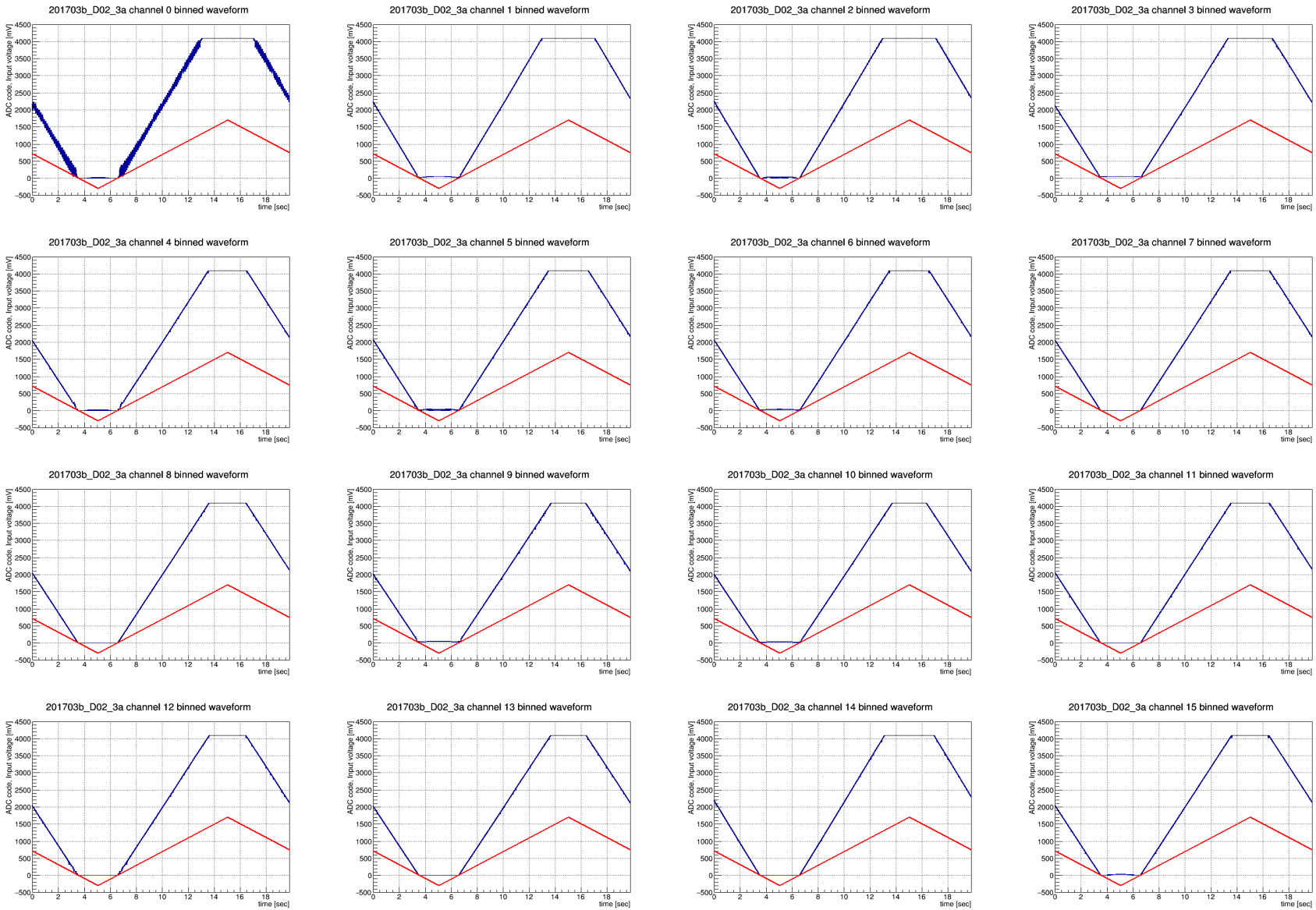
Waveforms: chip D02, time 1a



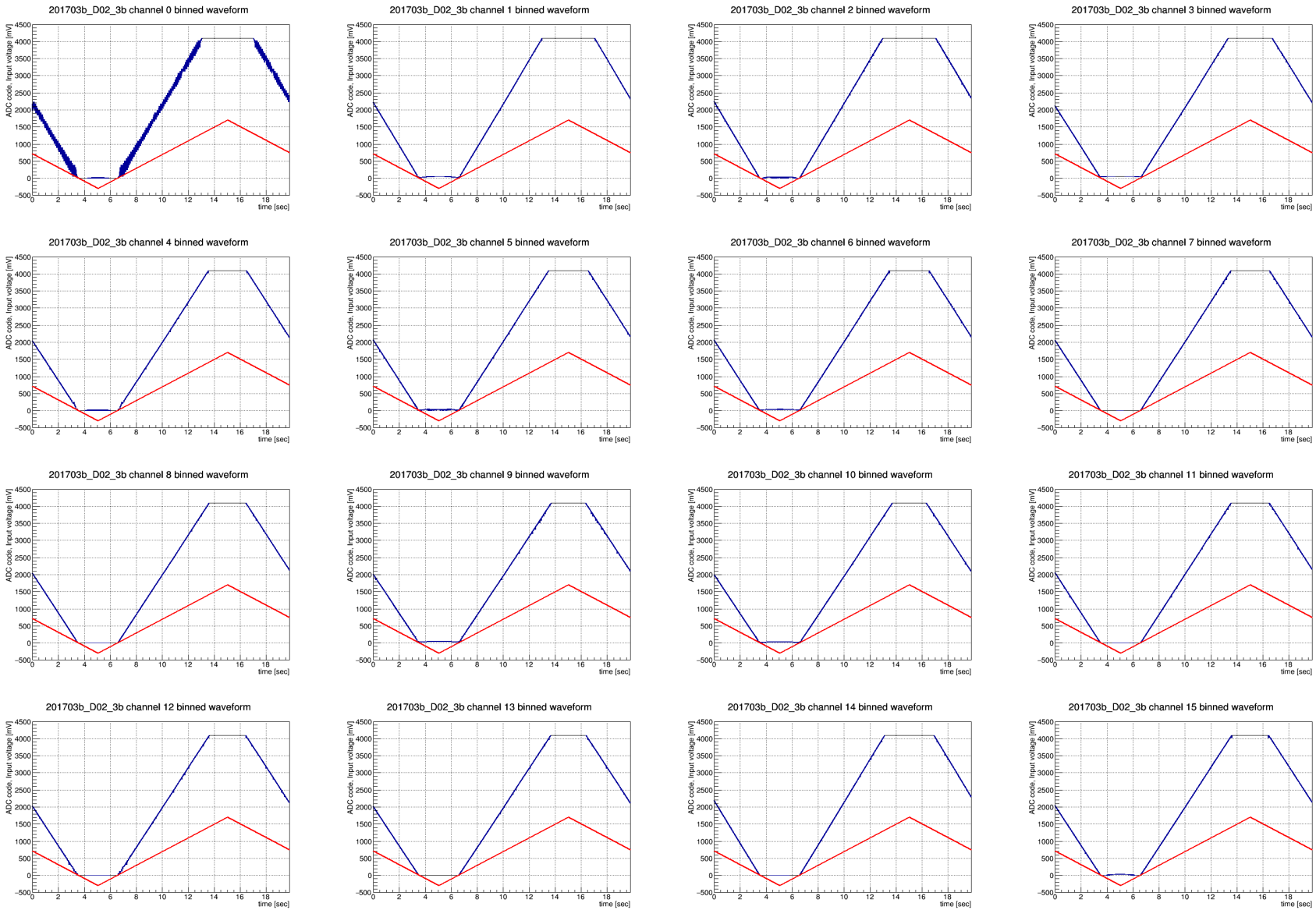
Waveforms: chip D02, time 2a



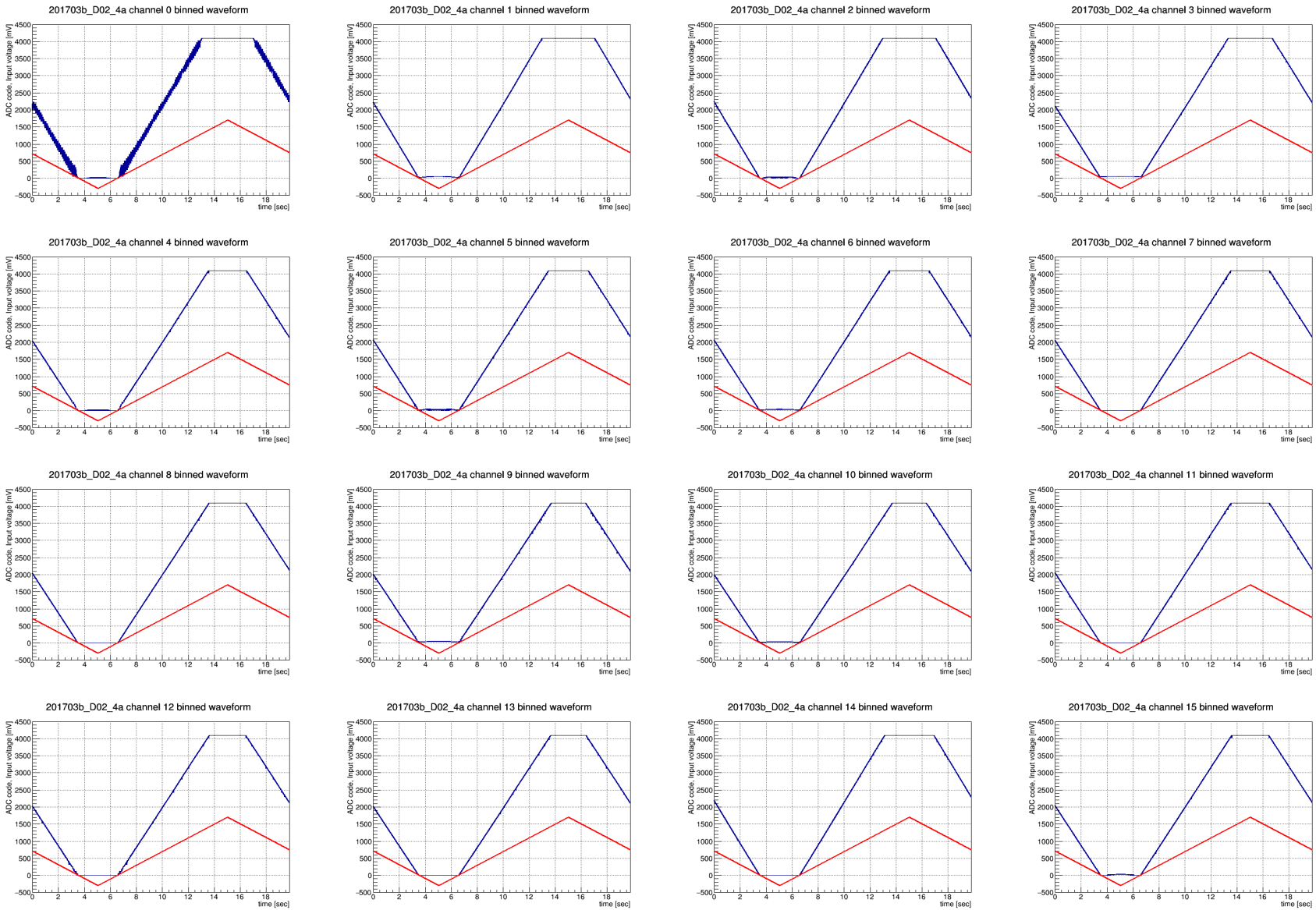
Waveforms: chip D02, time 3a



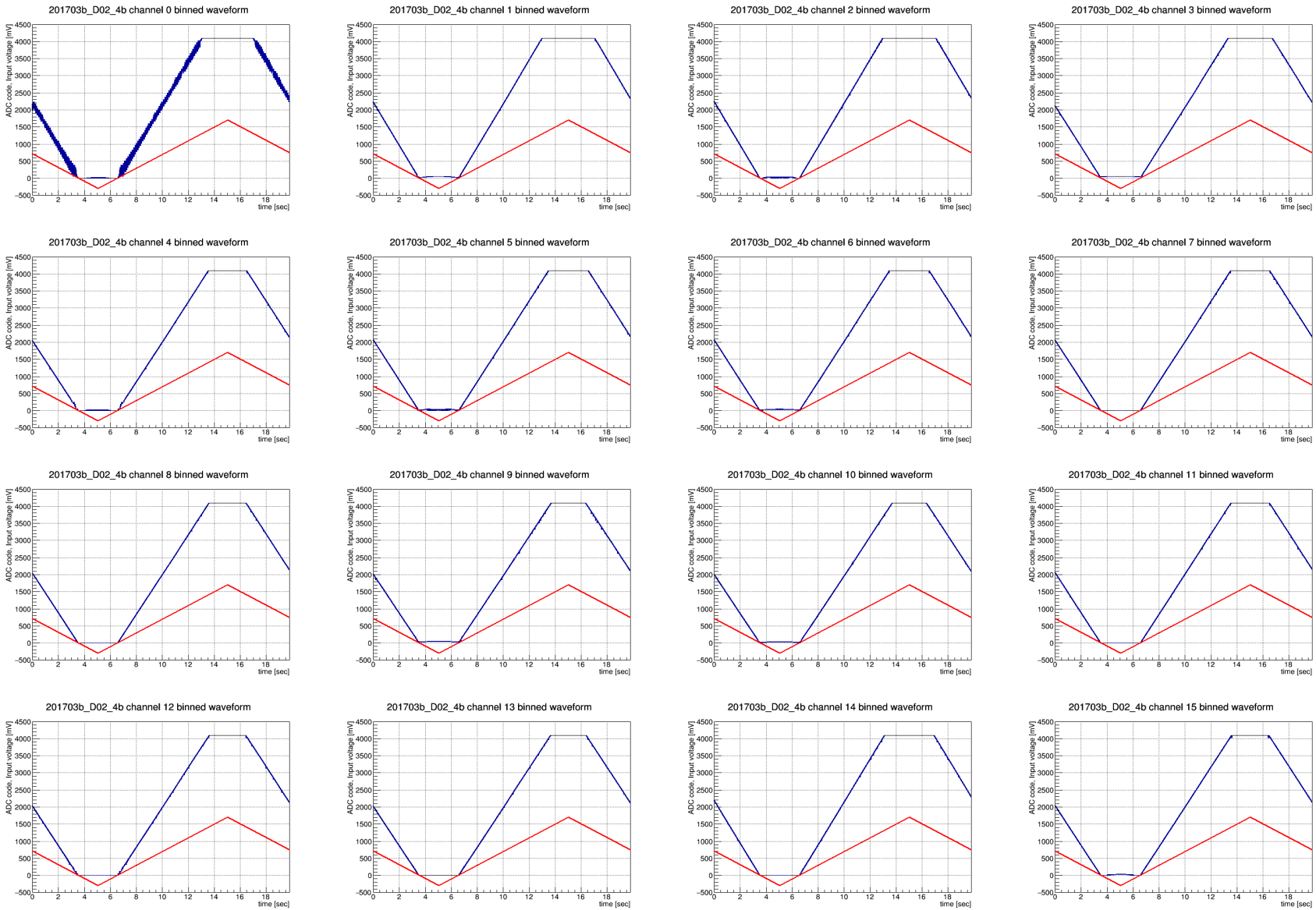
Waveforms: chip D02, time 3b



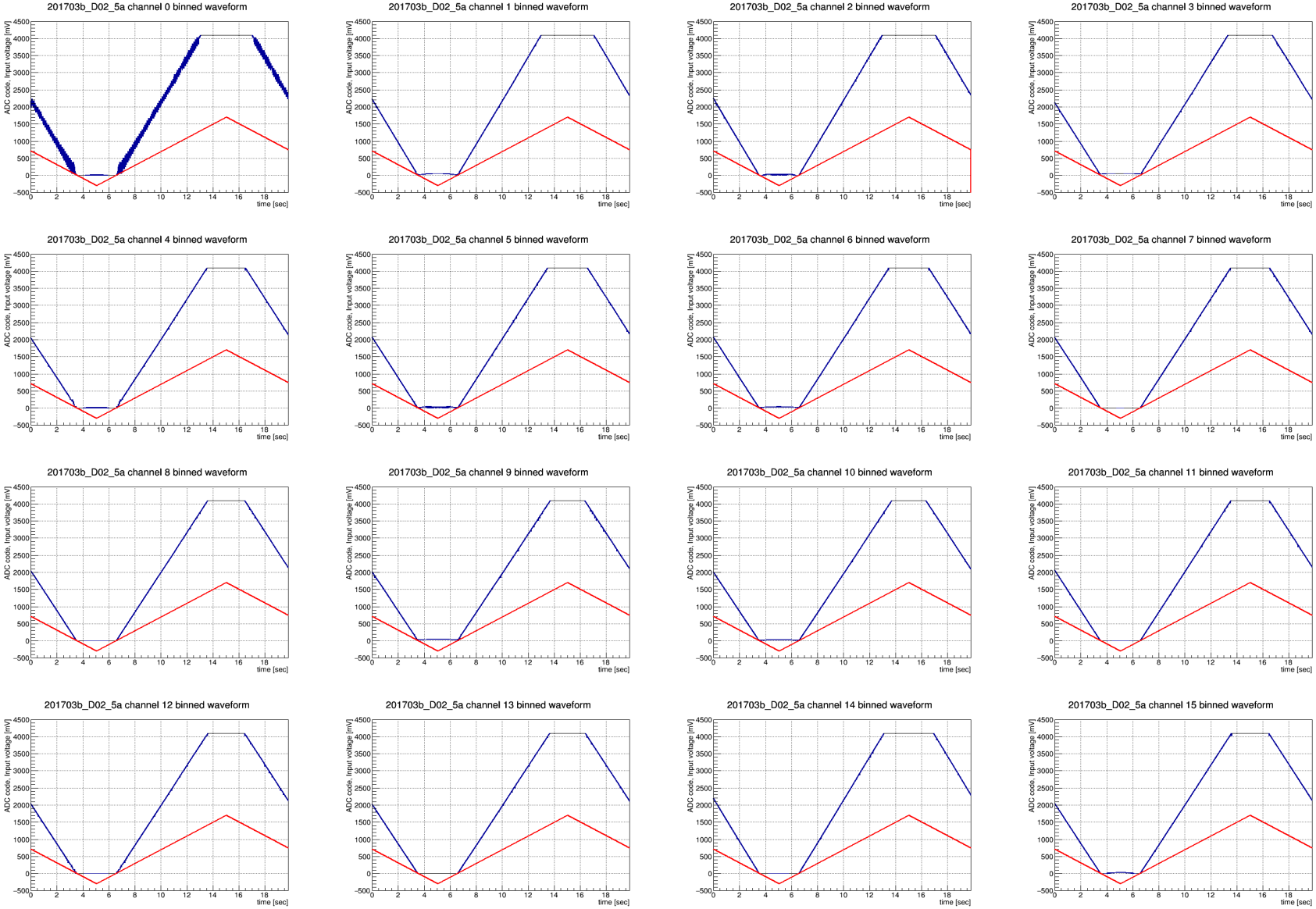
Waveforms: chip D02, time 4a



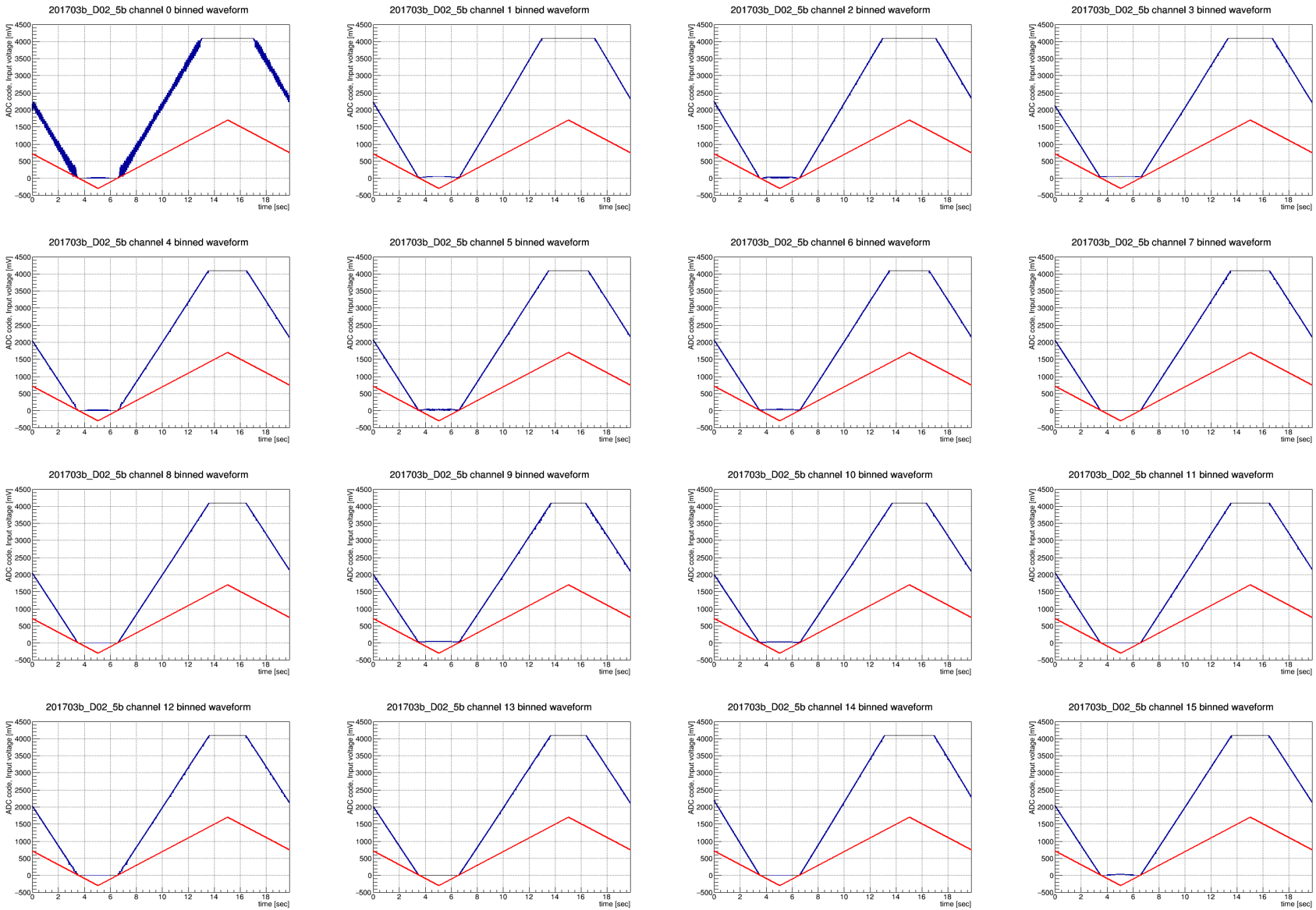
Waveforms: chip D02, time 4b



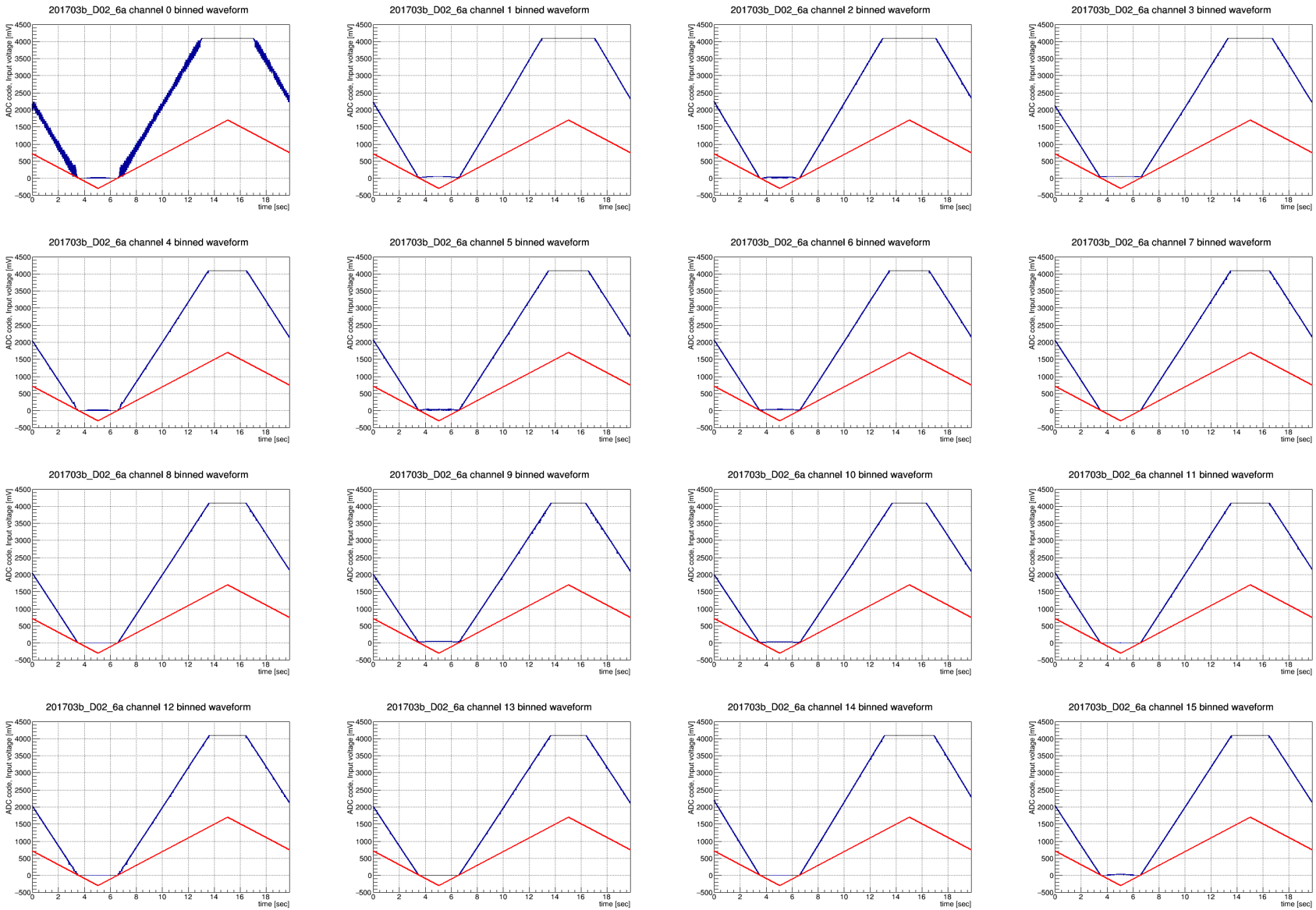
Waveforms: chip D02, time 5a



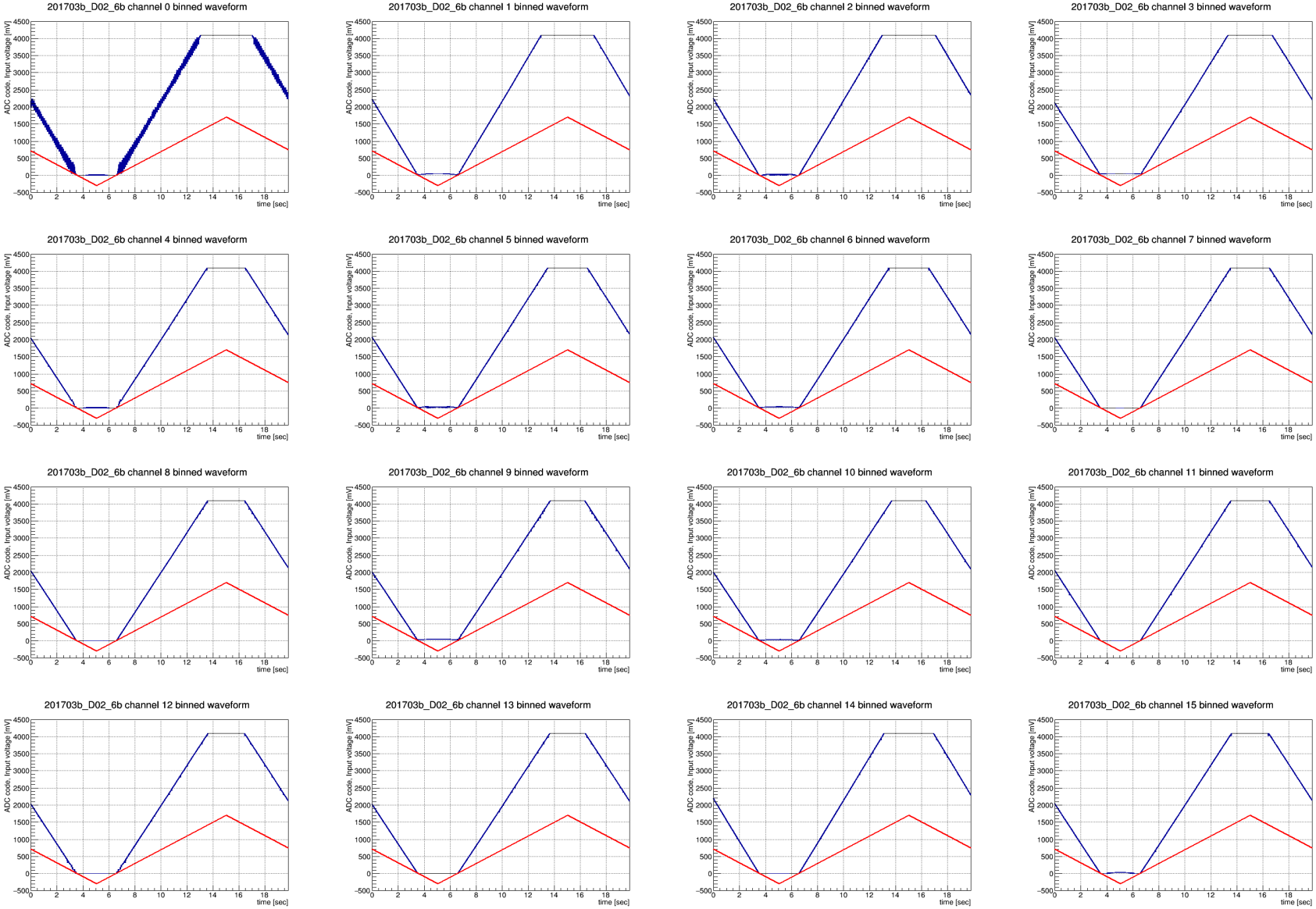
Waveforms: chip D02, time 5b



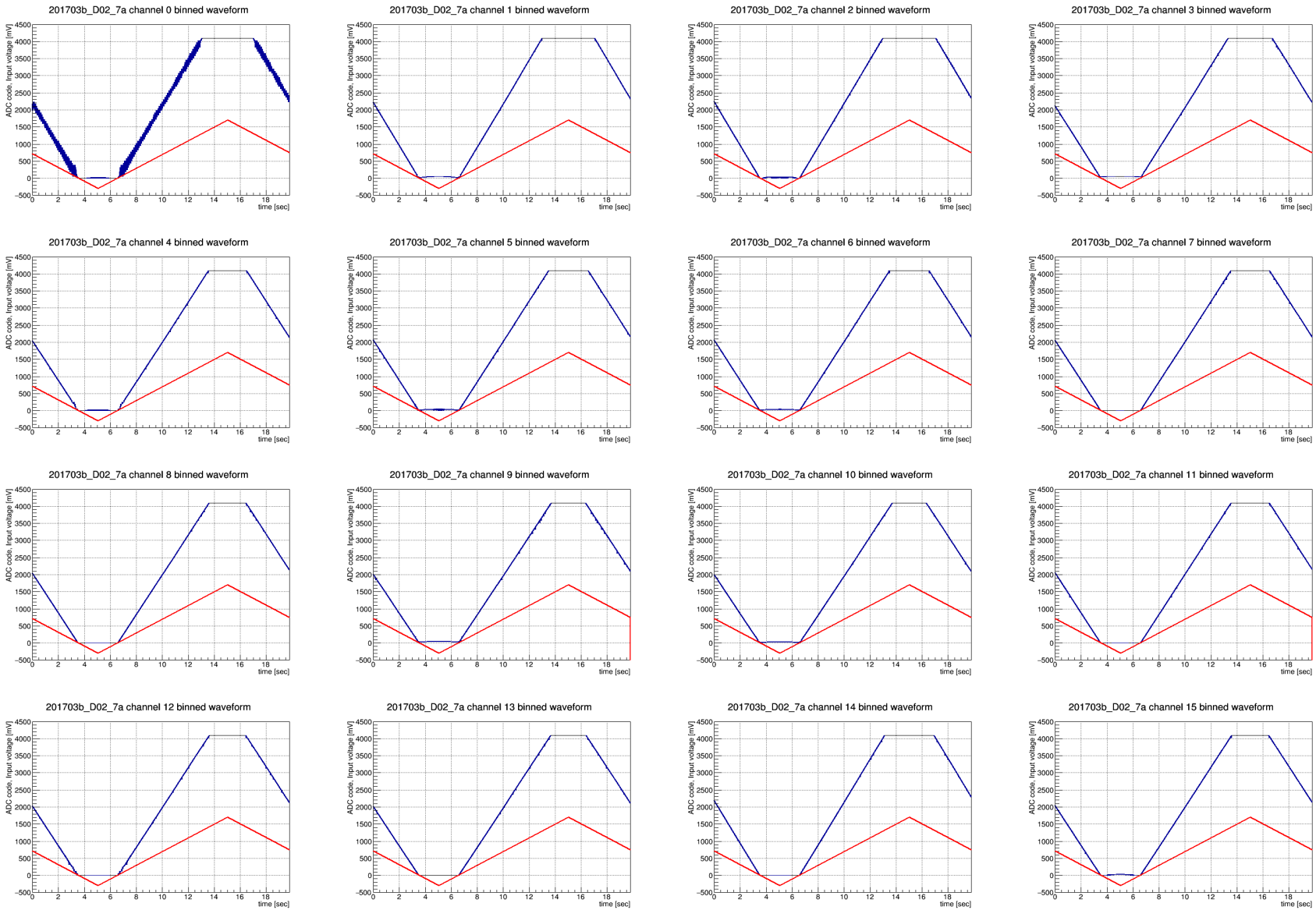
Waveforms: chip D02, time 6a



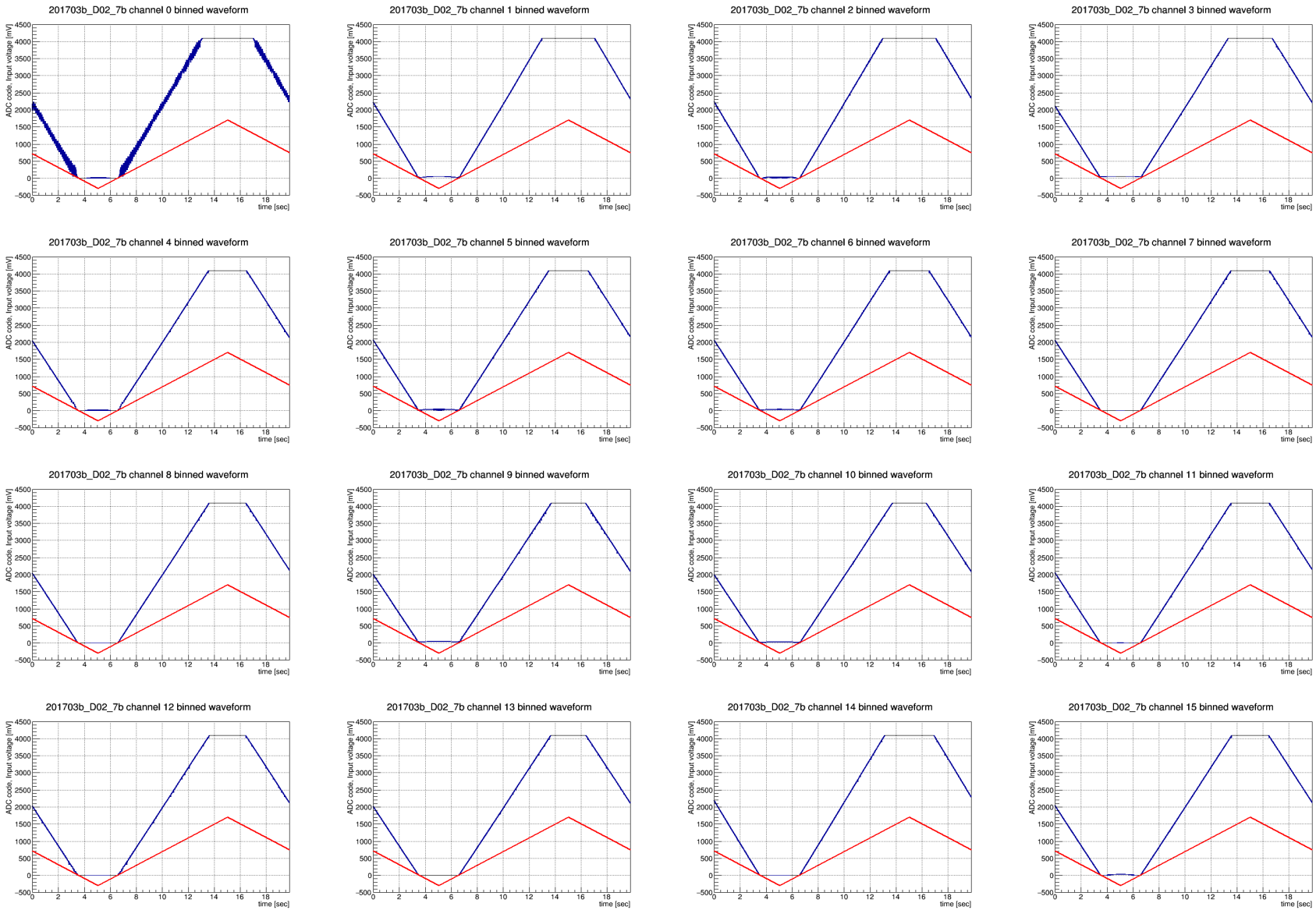
Waveforms: chip D02, time 6b



Waveforms: chip D02, time 7a



Waveforms: chip D02, time 7b



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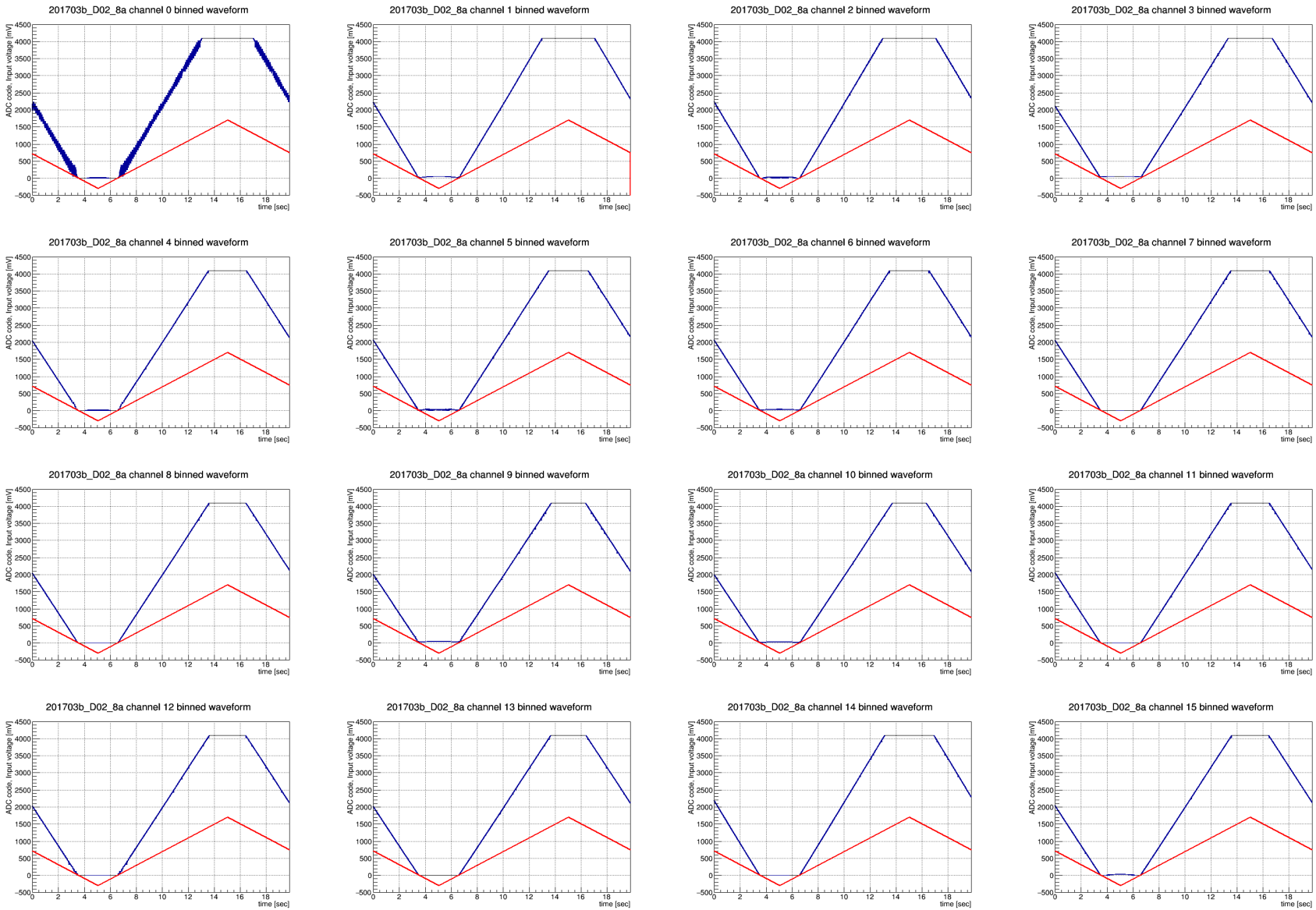

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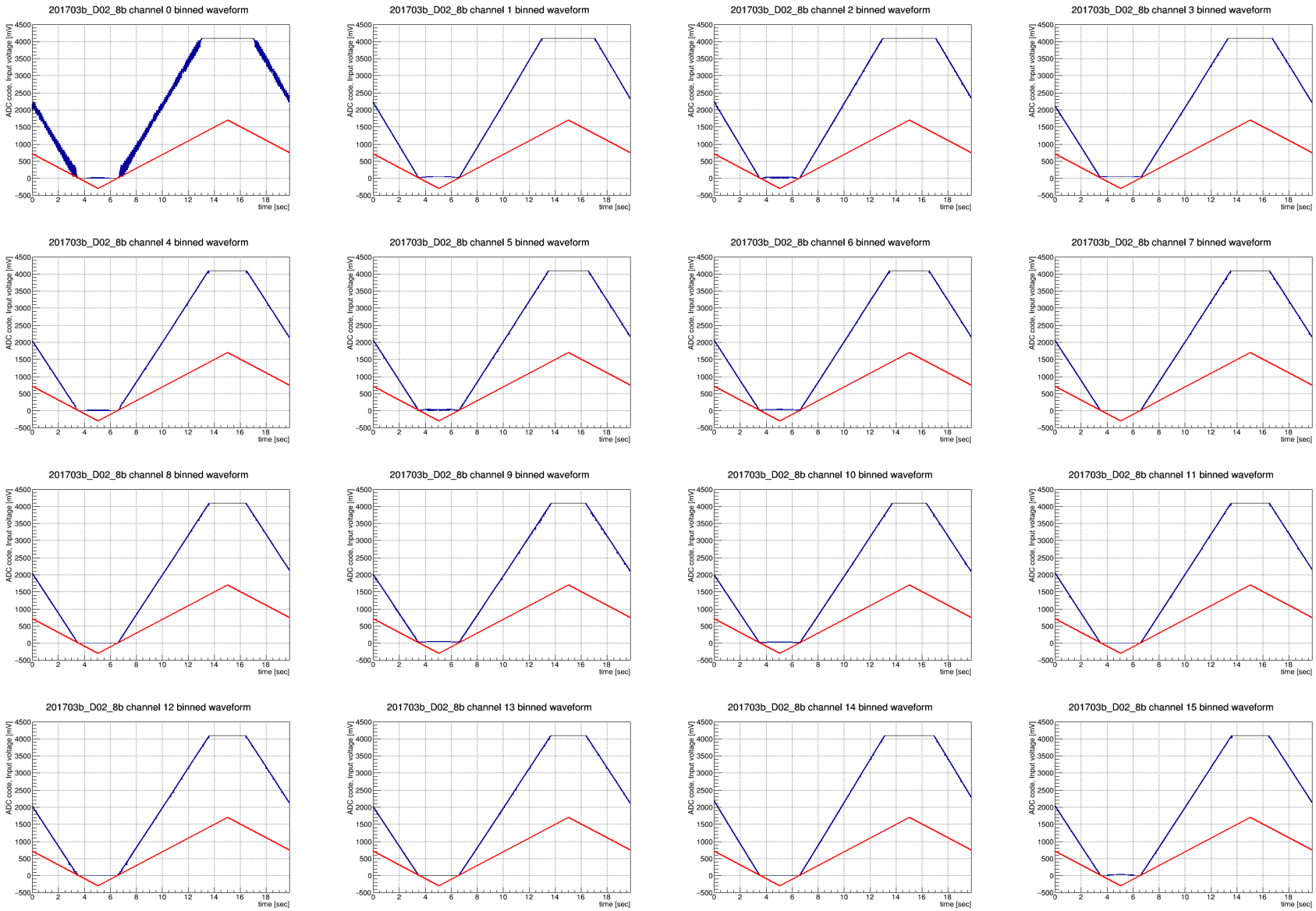

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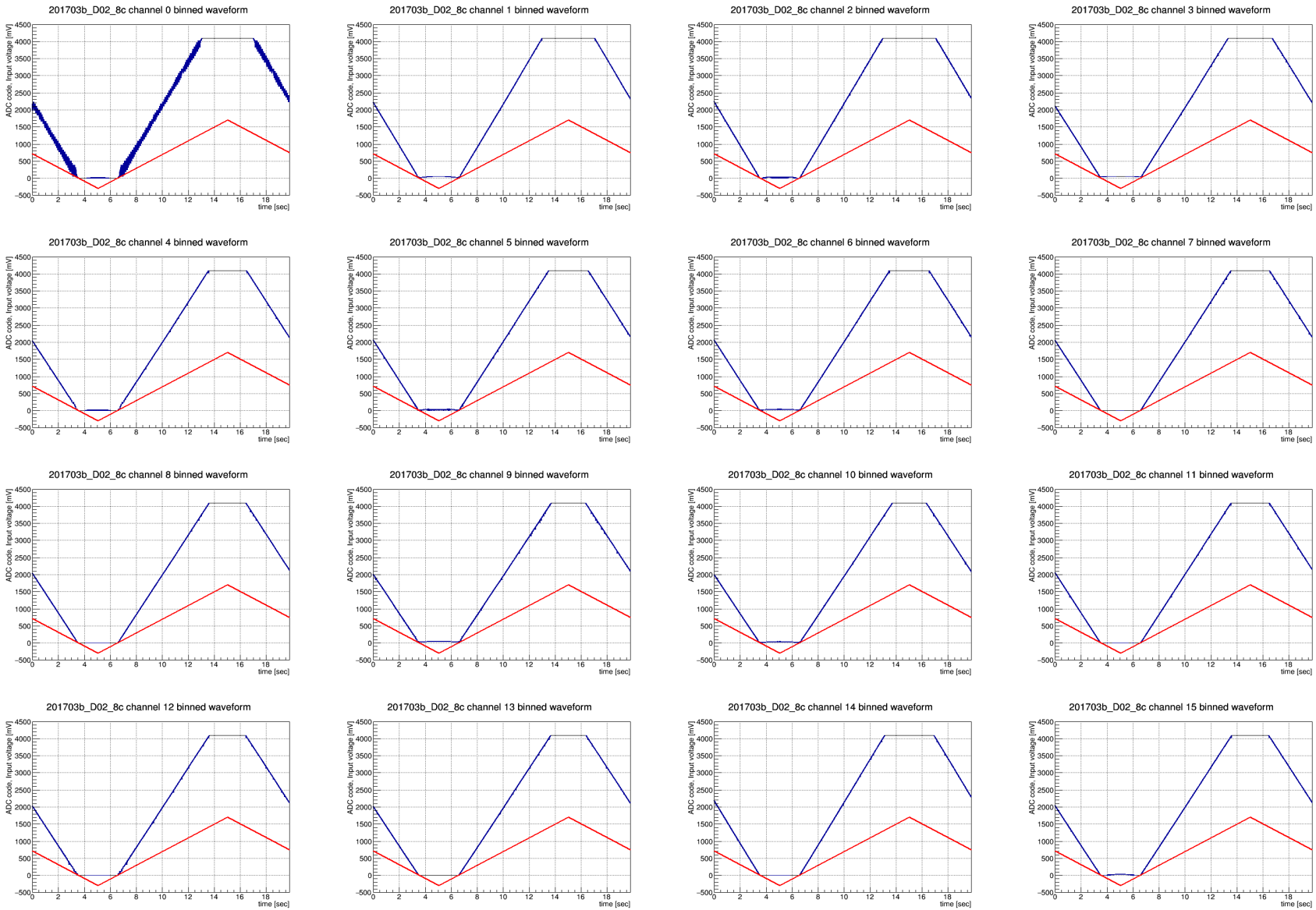

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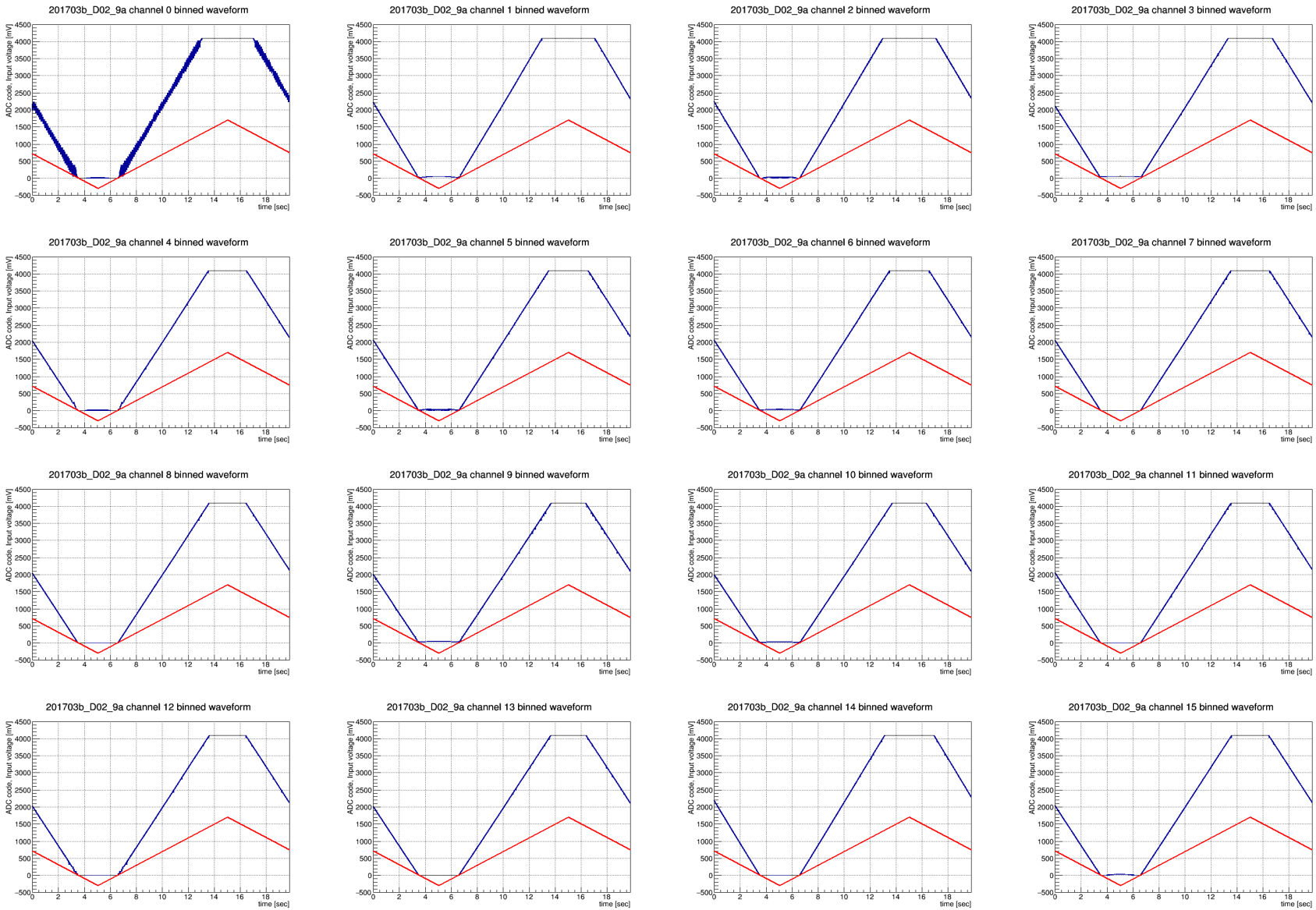

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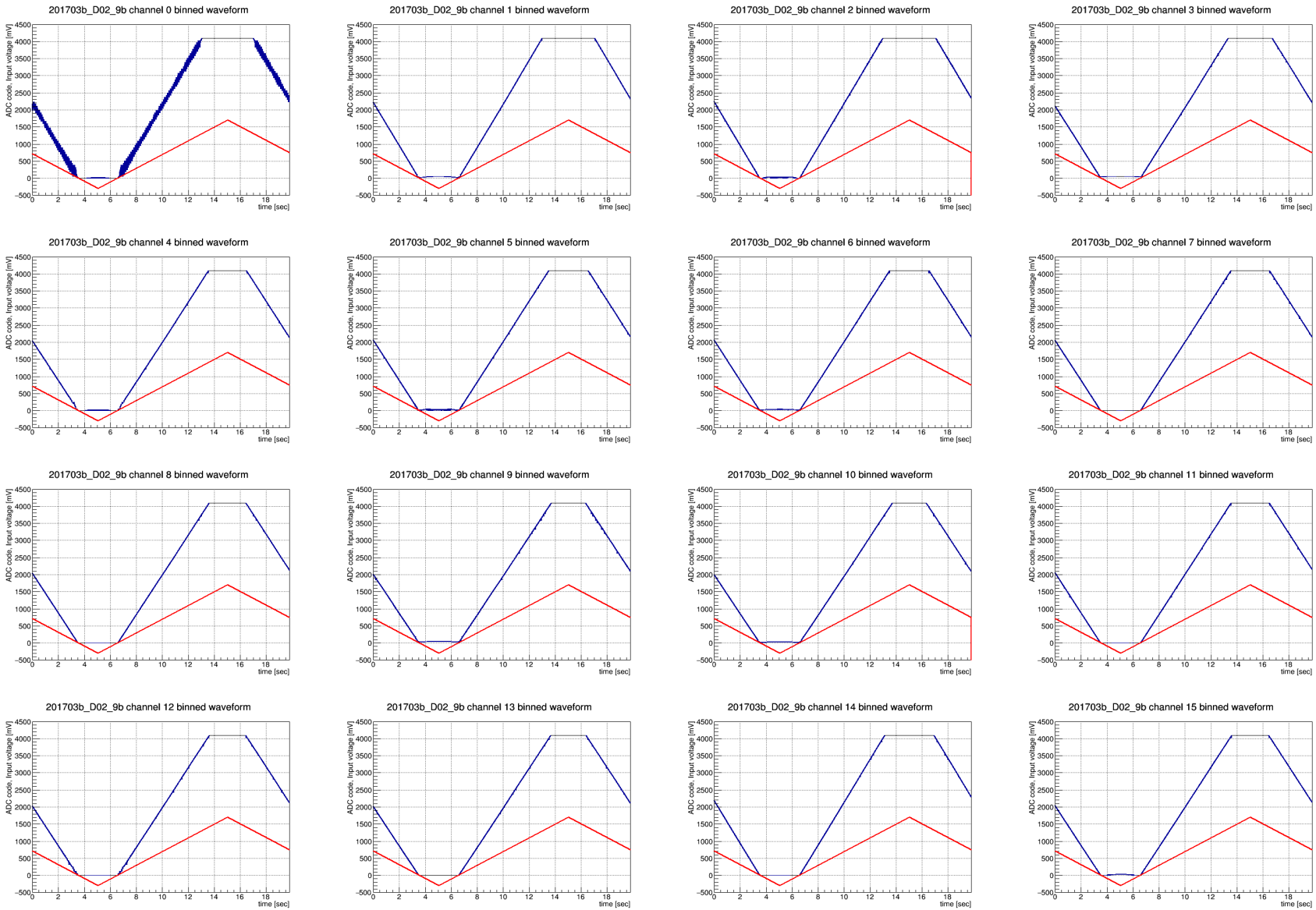

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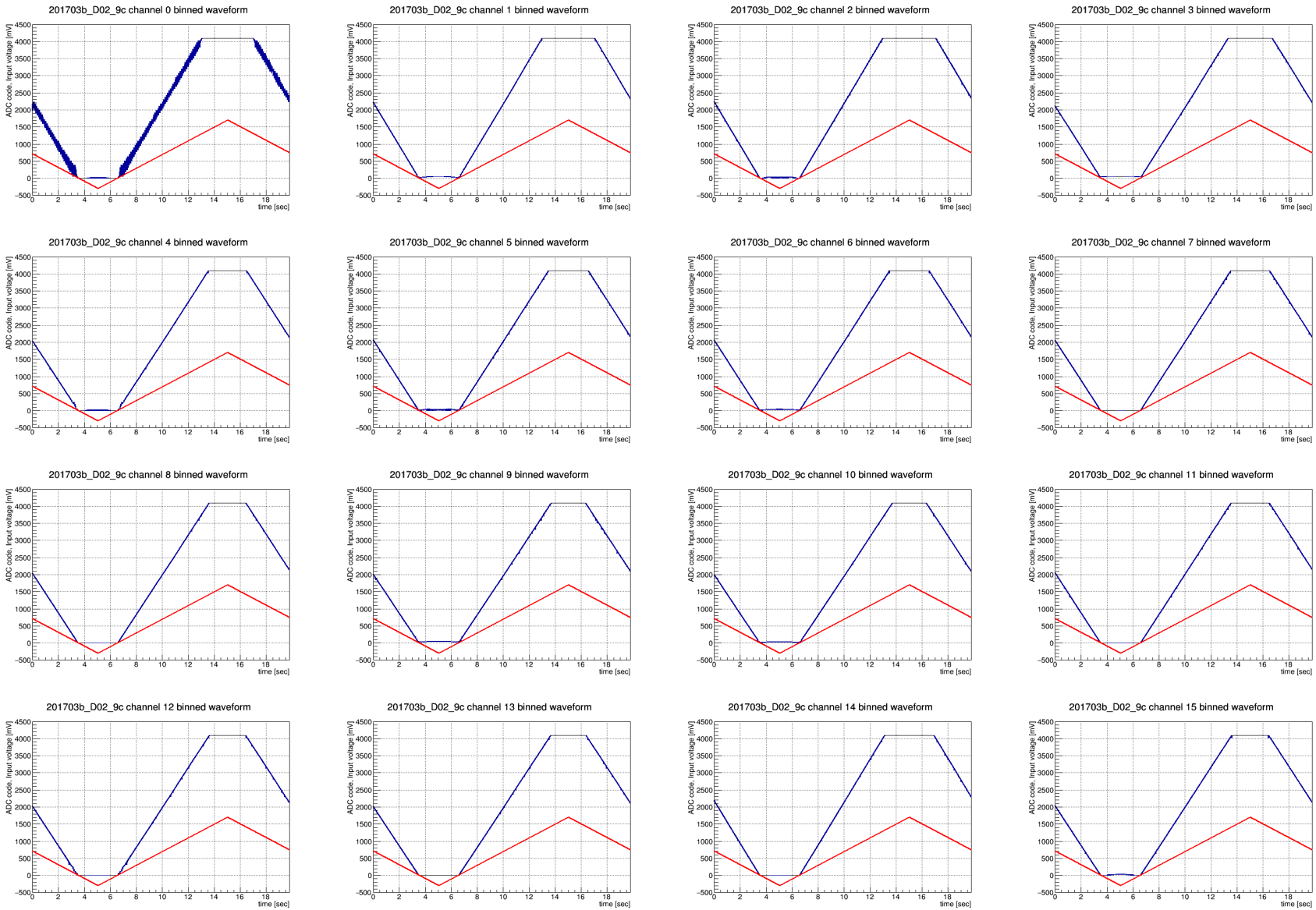
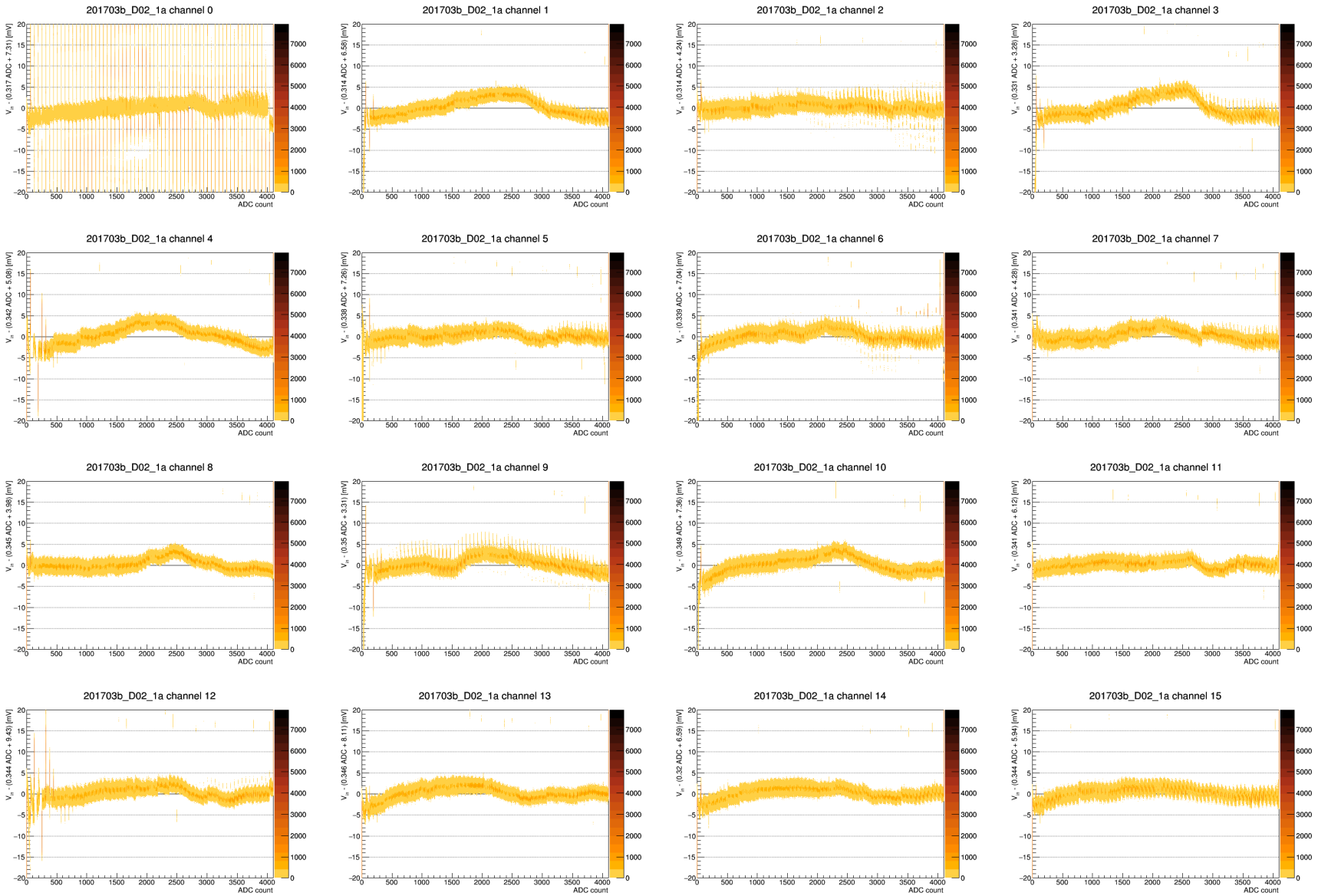
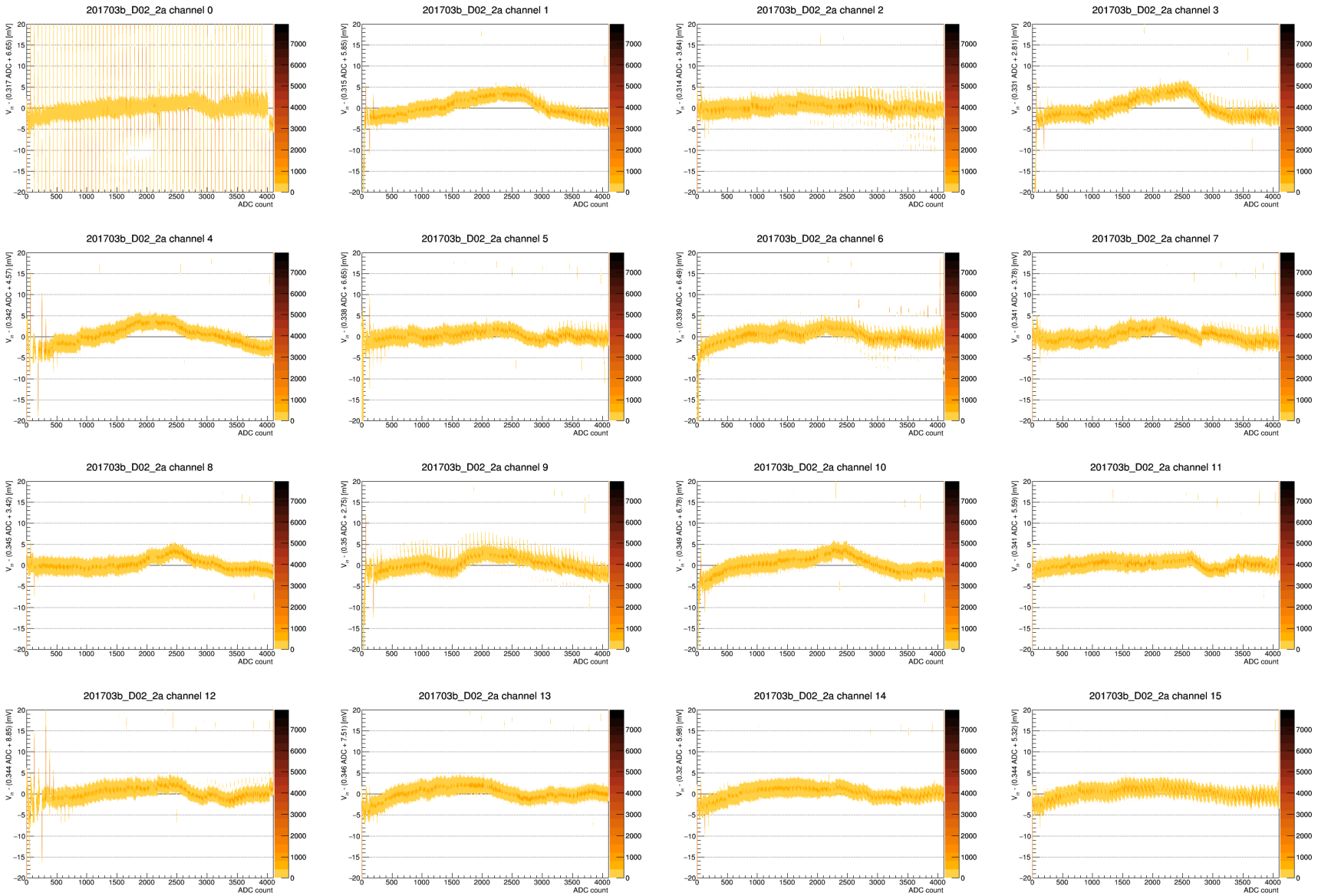


Residuals

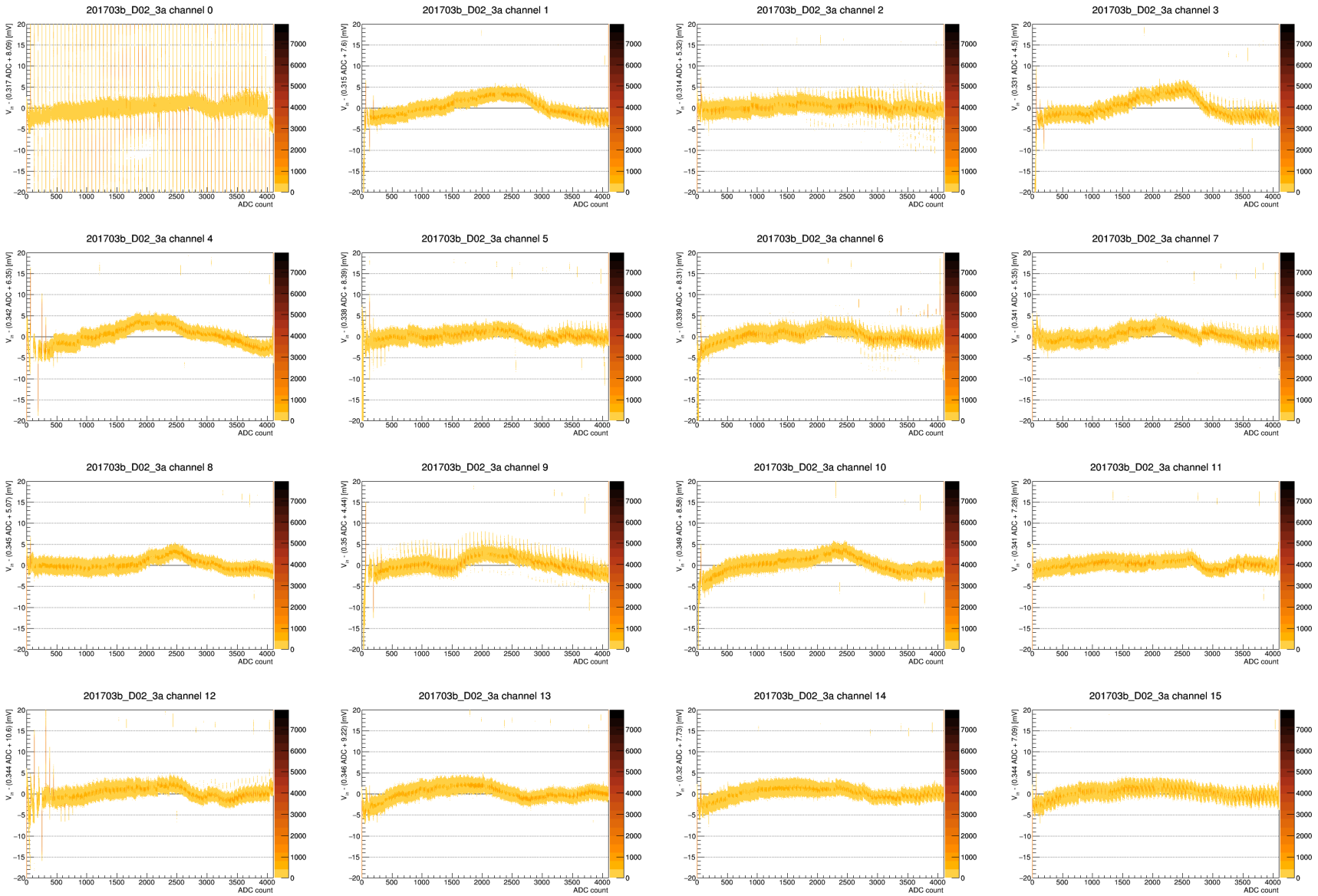
Residuals: chip D02, time 1a



Residuals: chip D02, time 2a



Residuals: chip D02, time 3a



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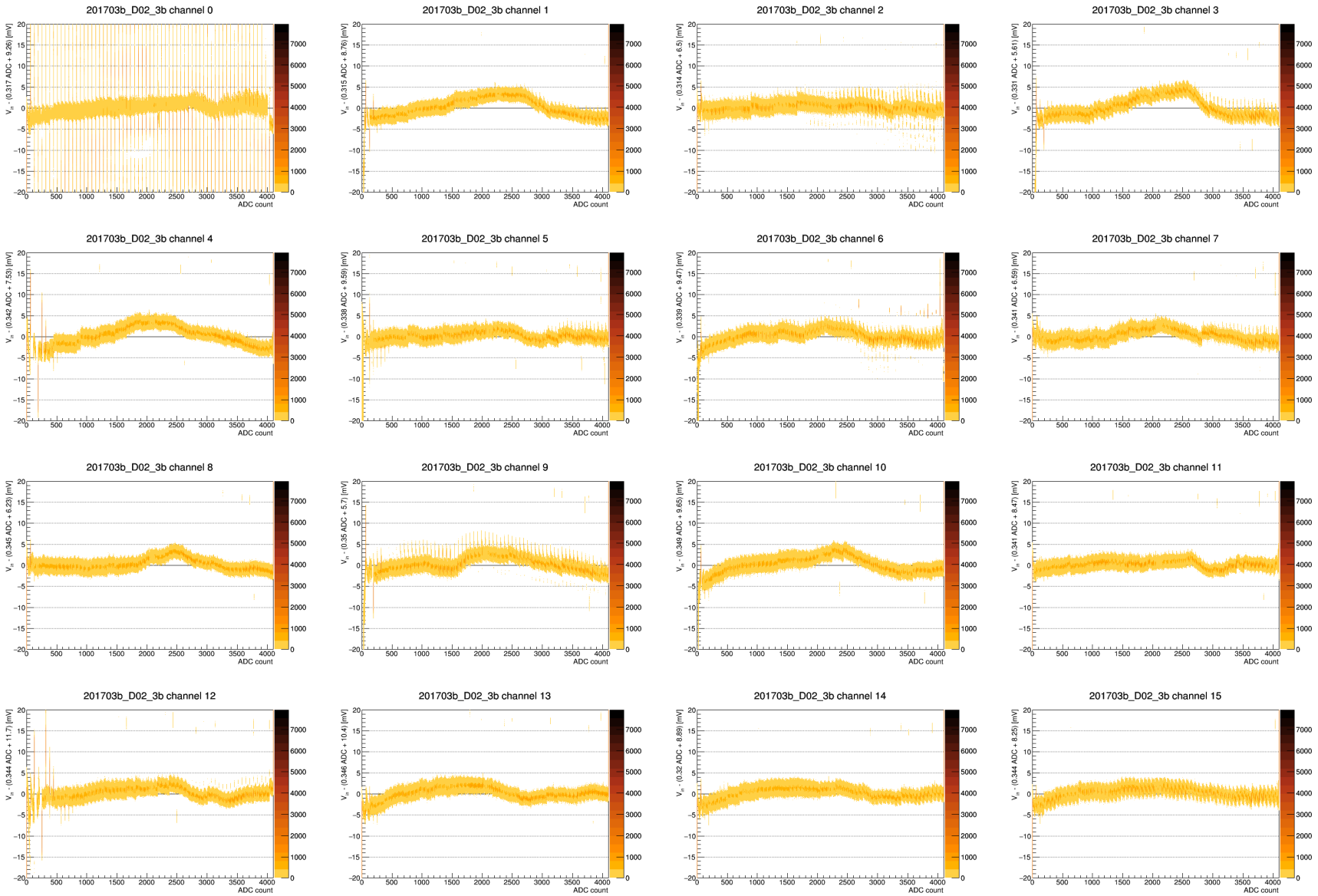
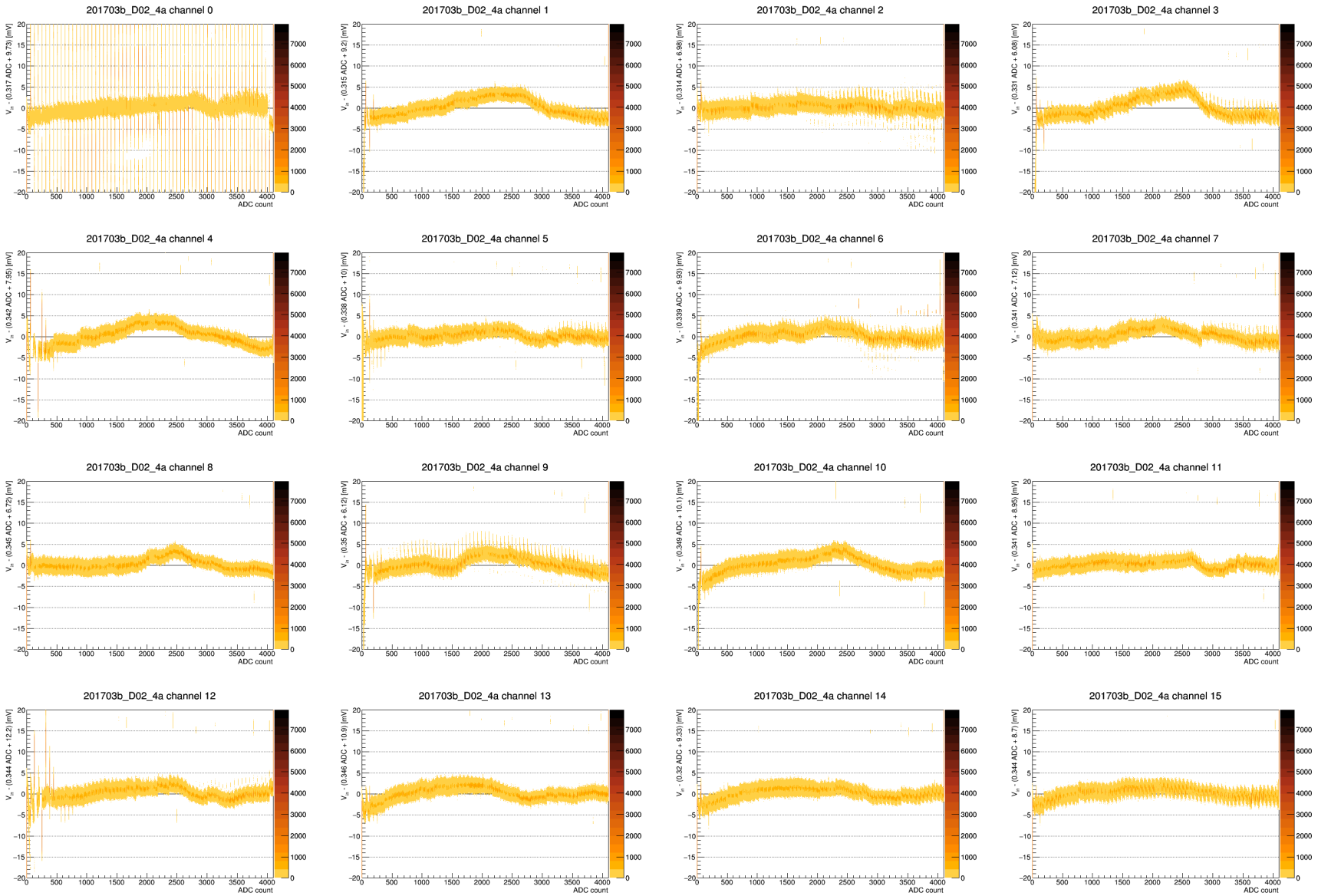
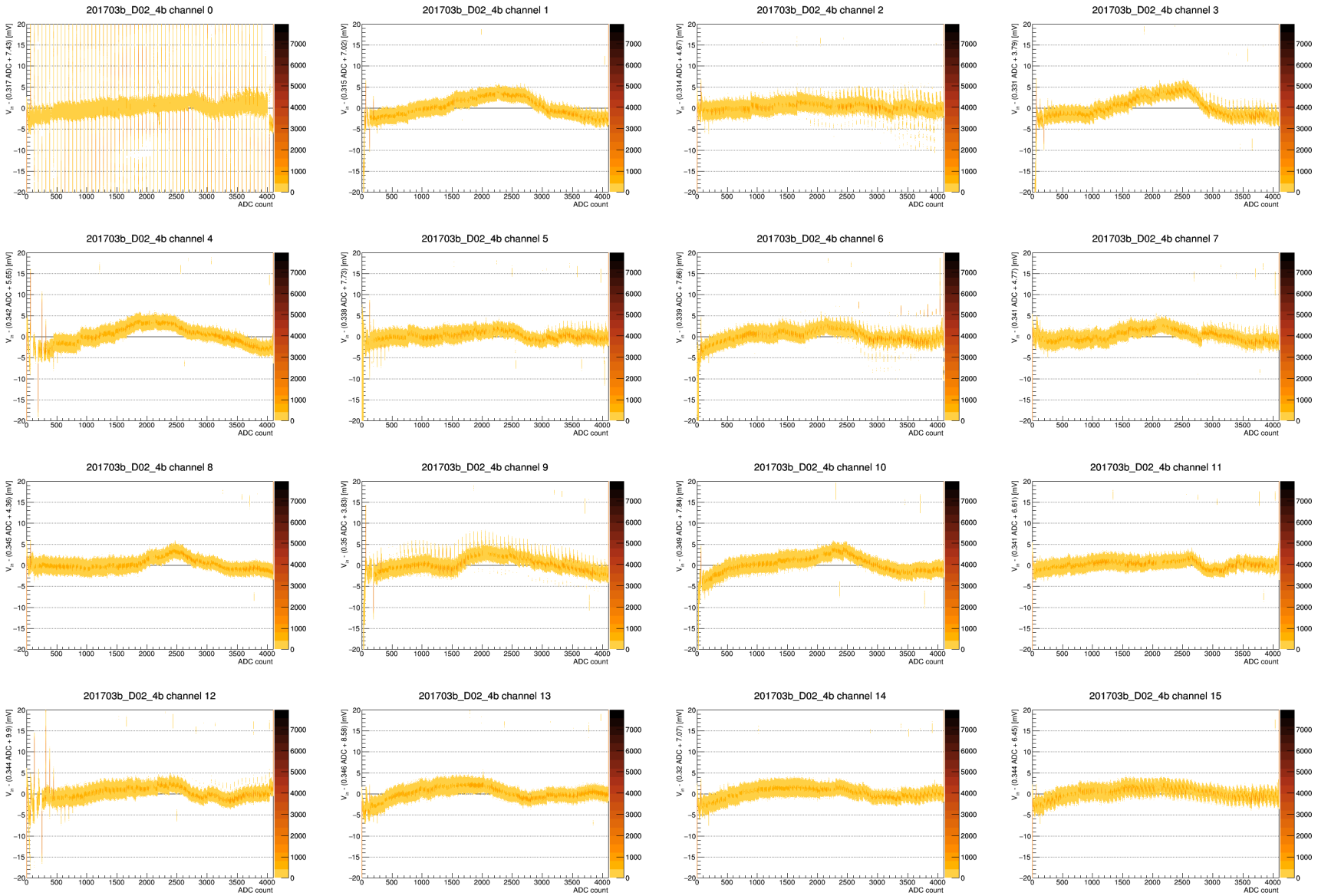


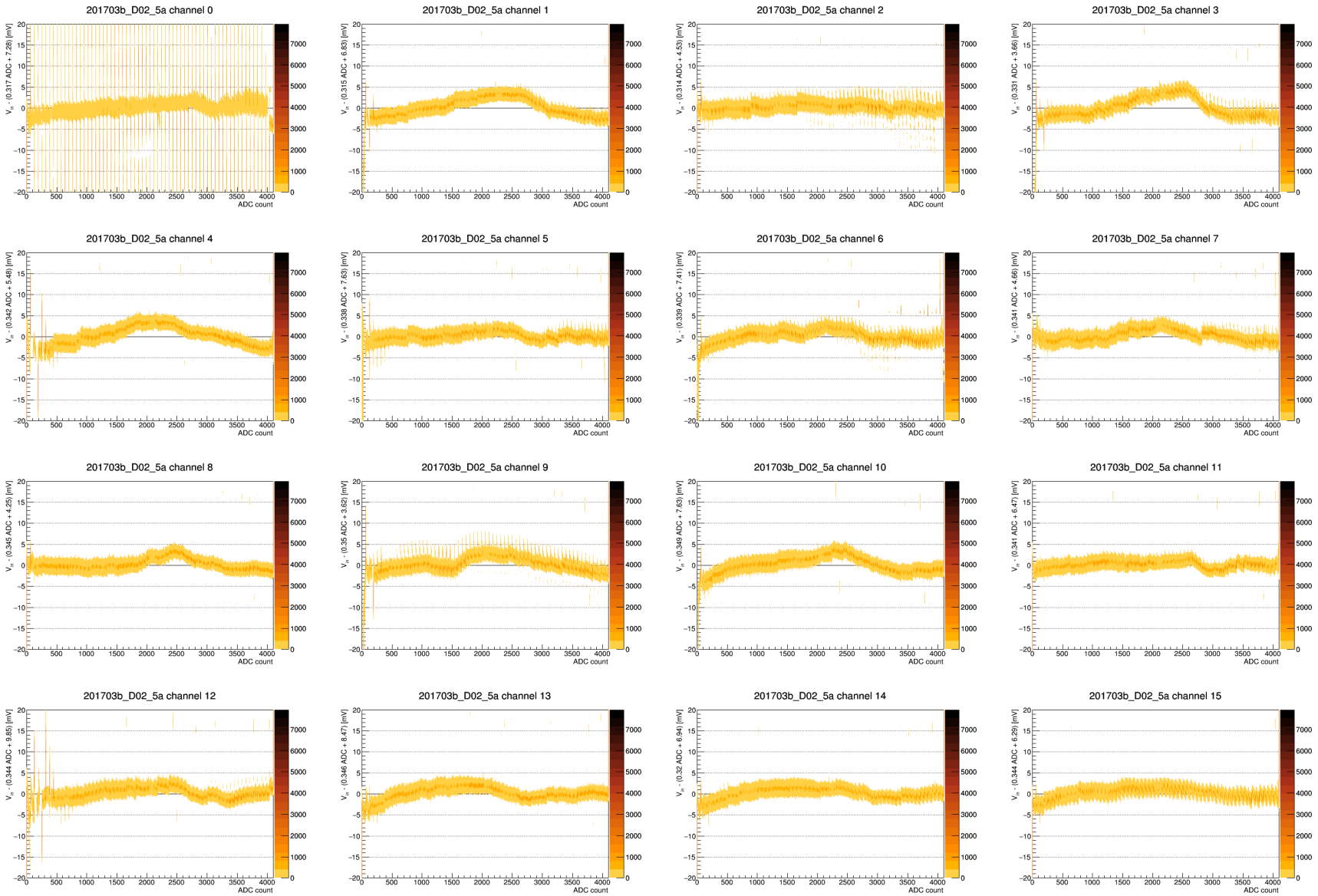
Residuals: chip D02, time 4a



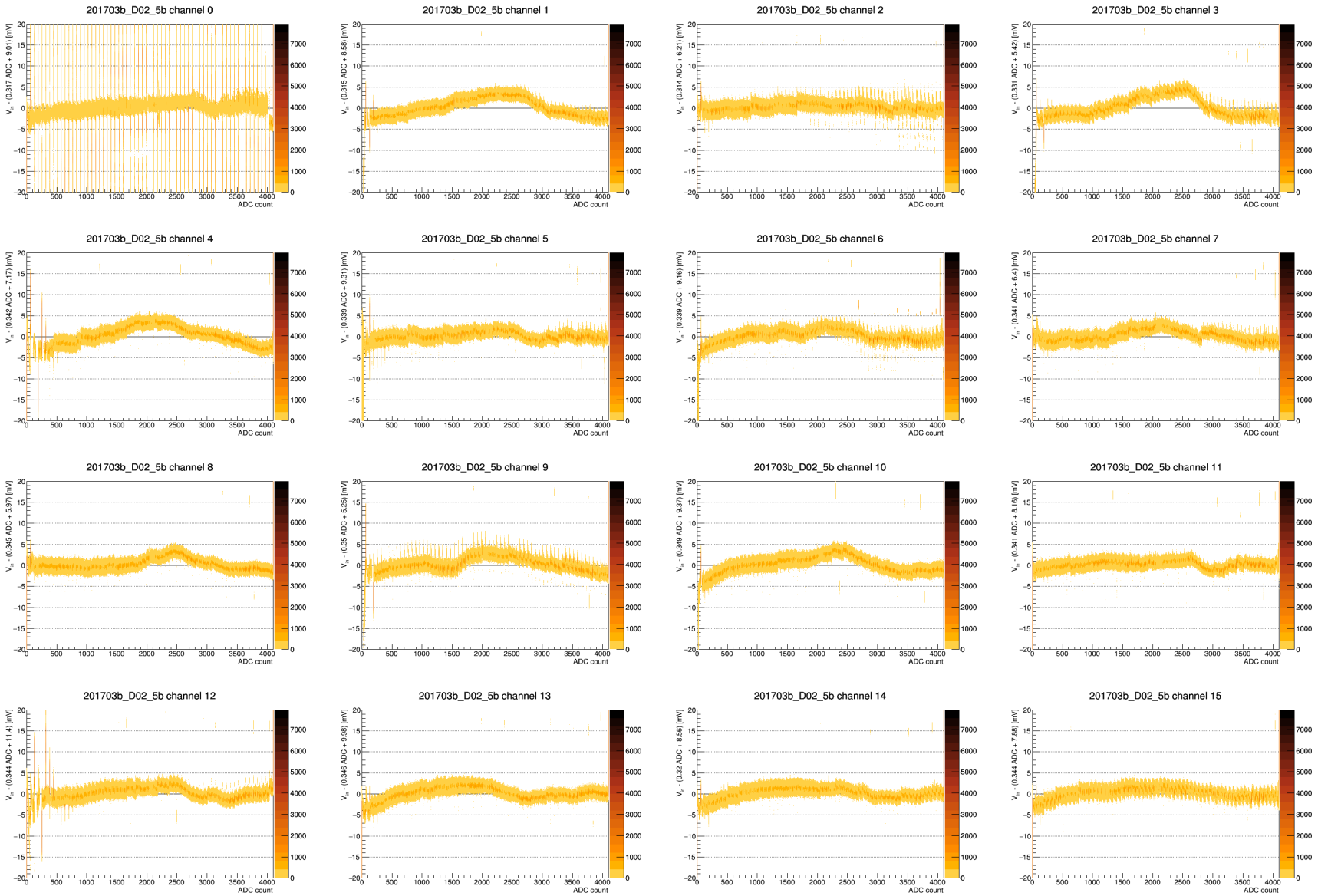
Residuals: chip D02, time 4b



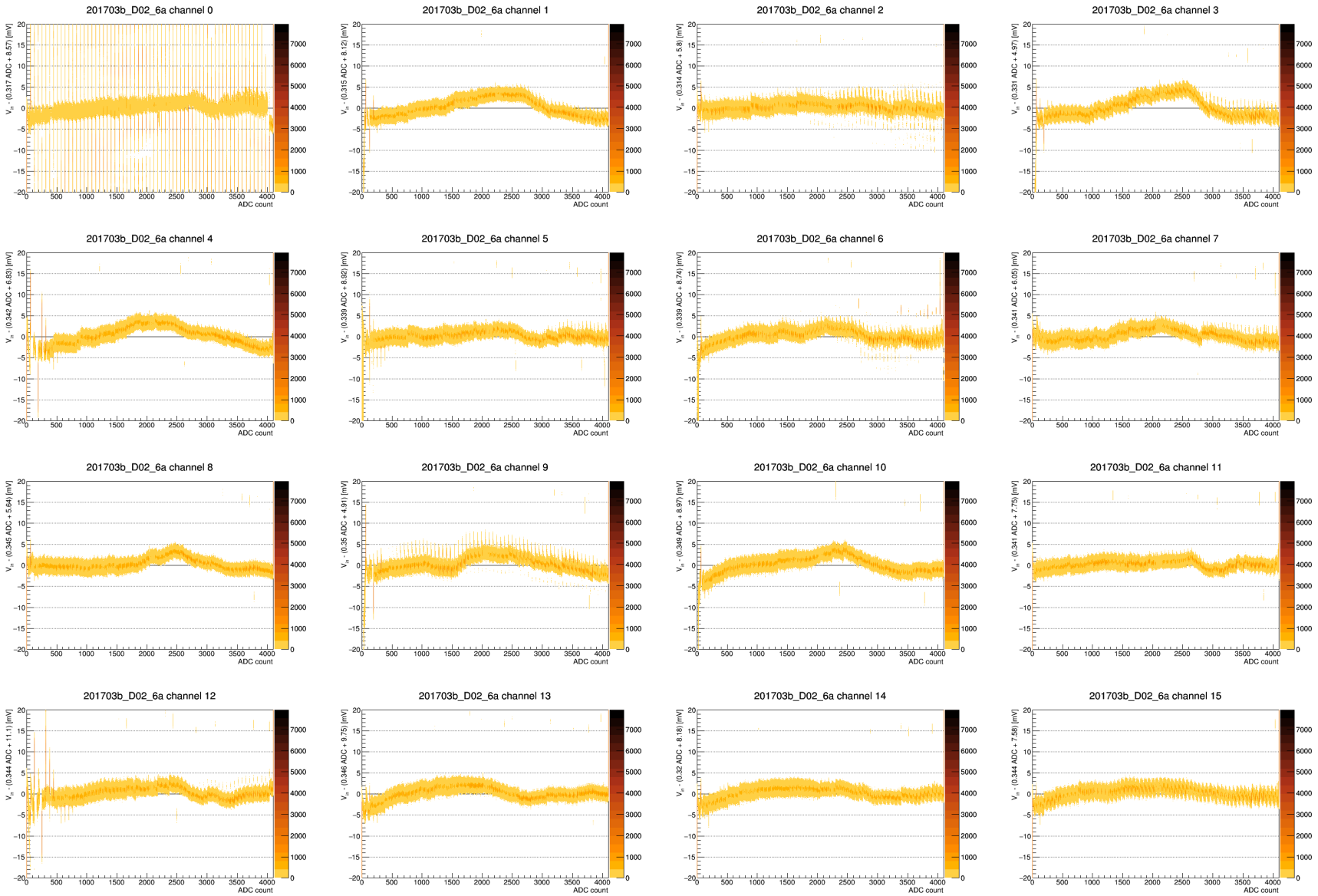
Residuals: chip D02, time 5a



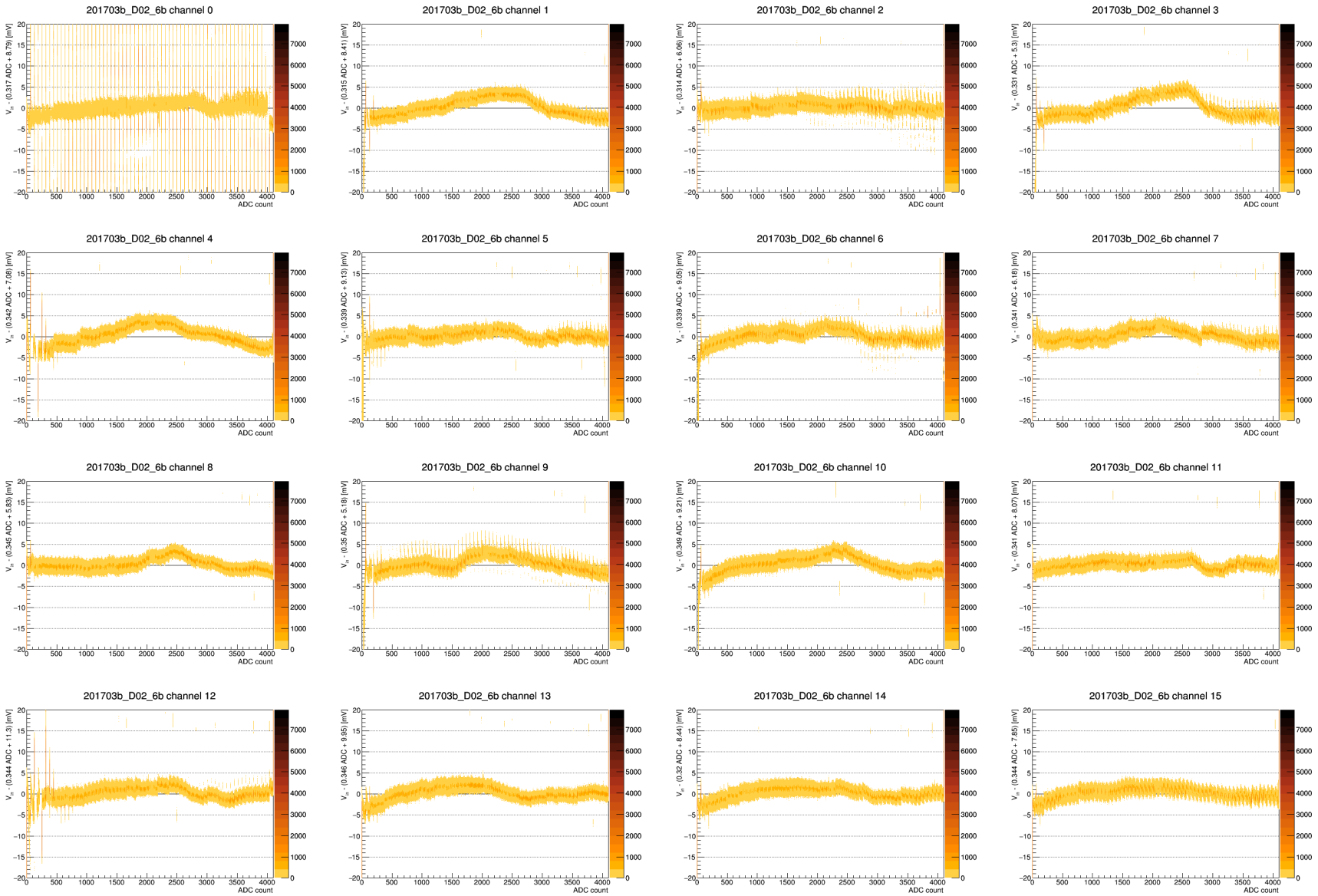
Residuals: chip D02, time 5b



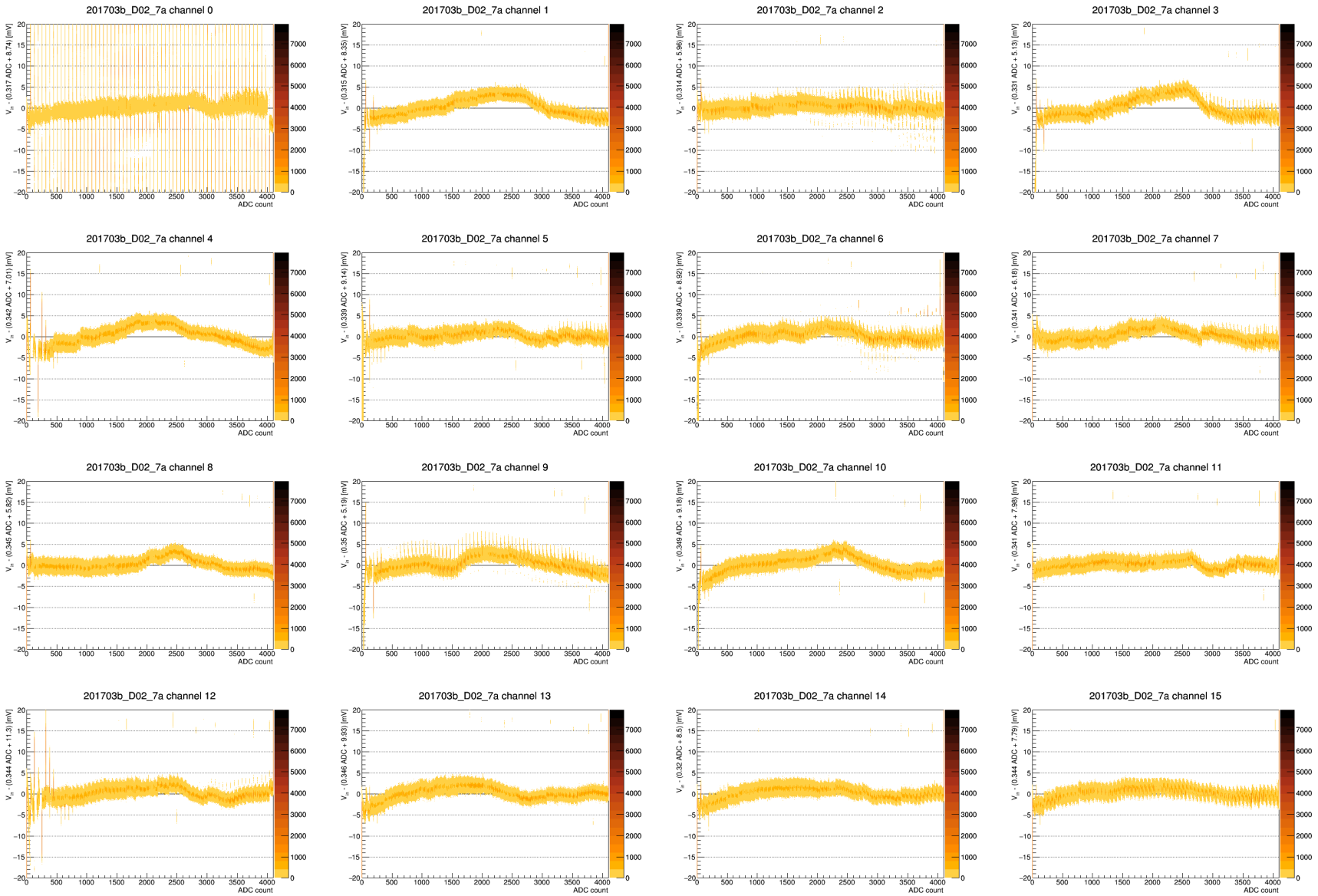
Residuals: chip D02, time 6a



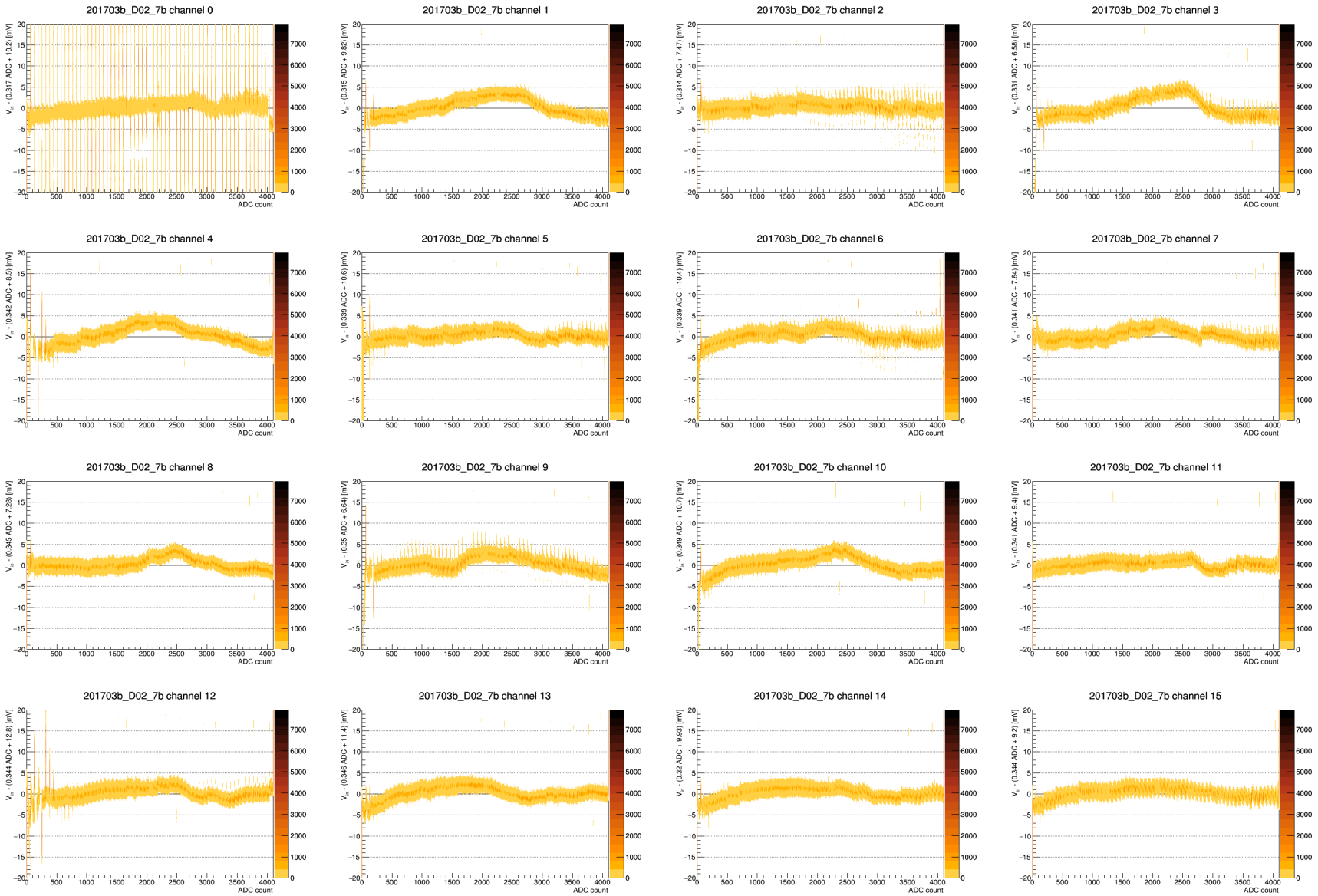
Residuals: chip D02, time 6b



Residuals: chip D02, time 7a



Residuals: chip D02, time 7b



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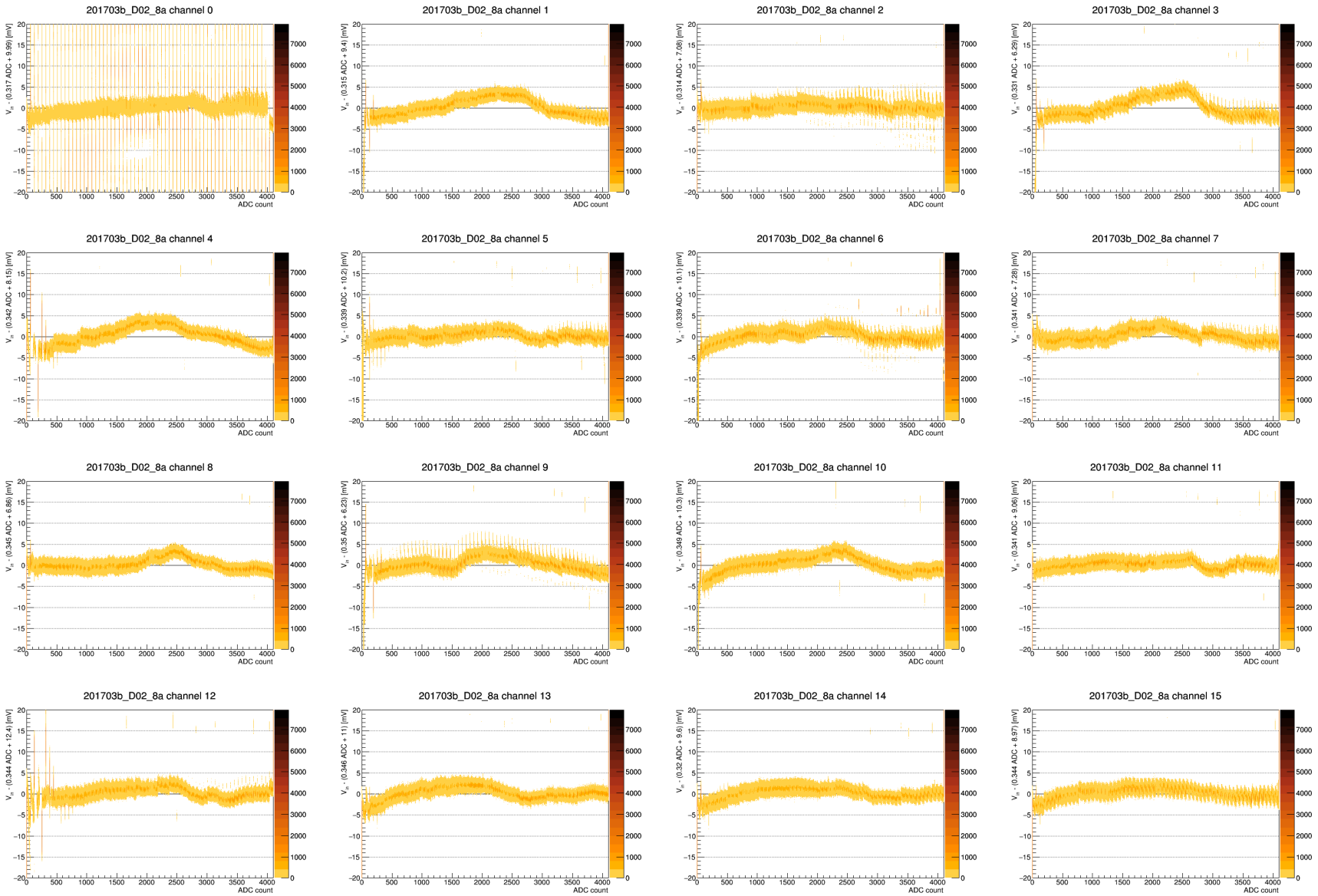

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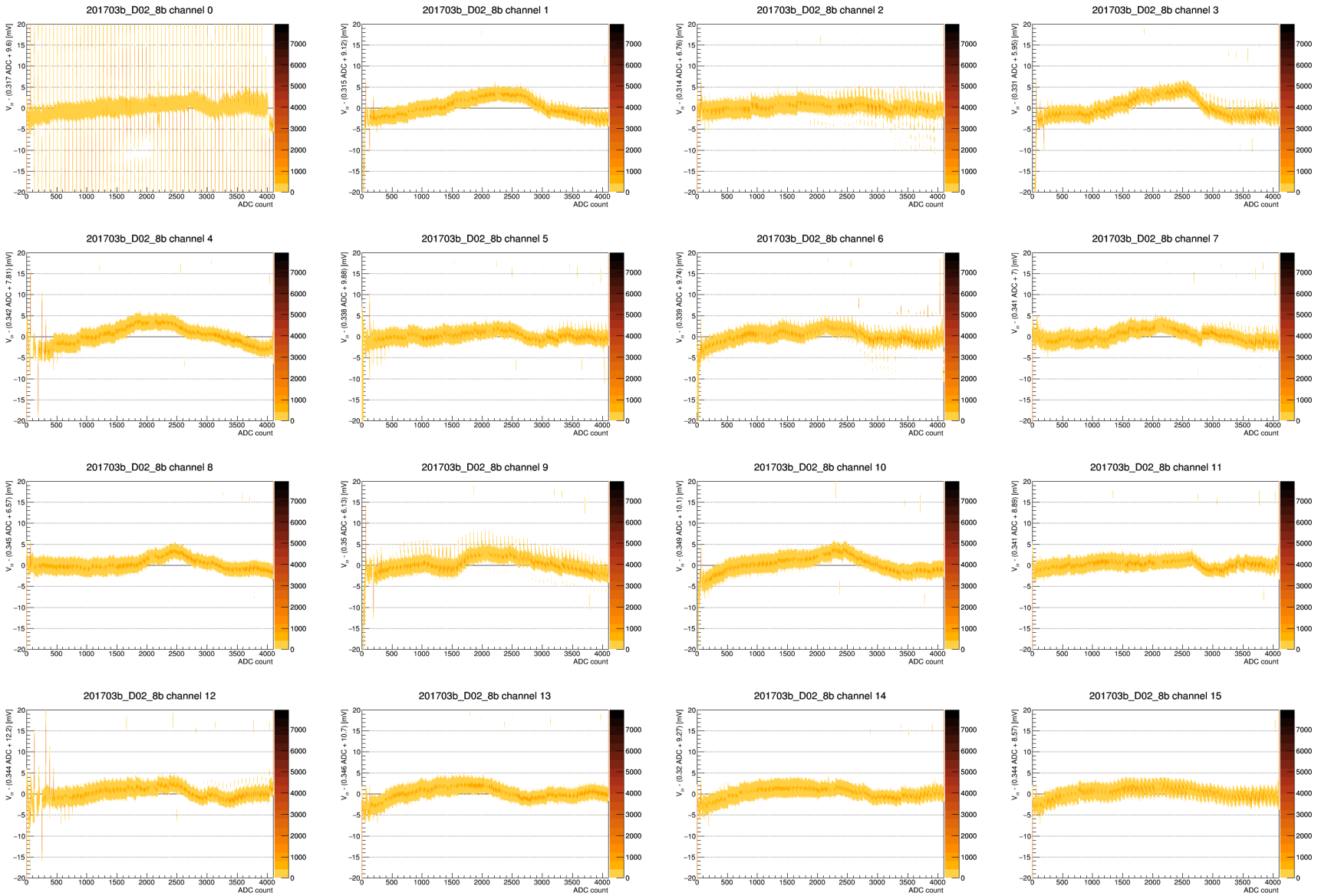

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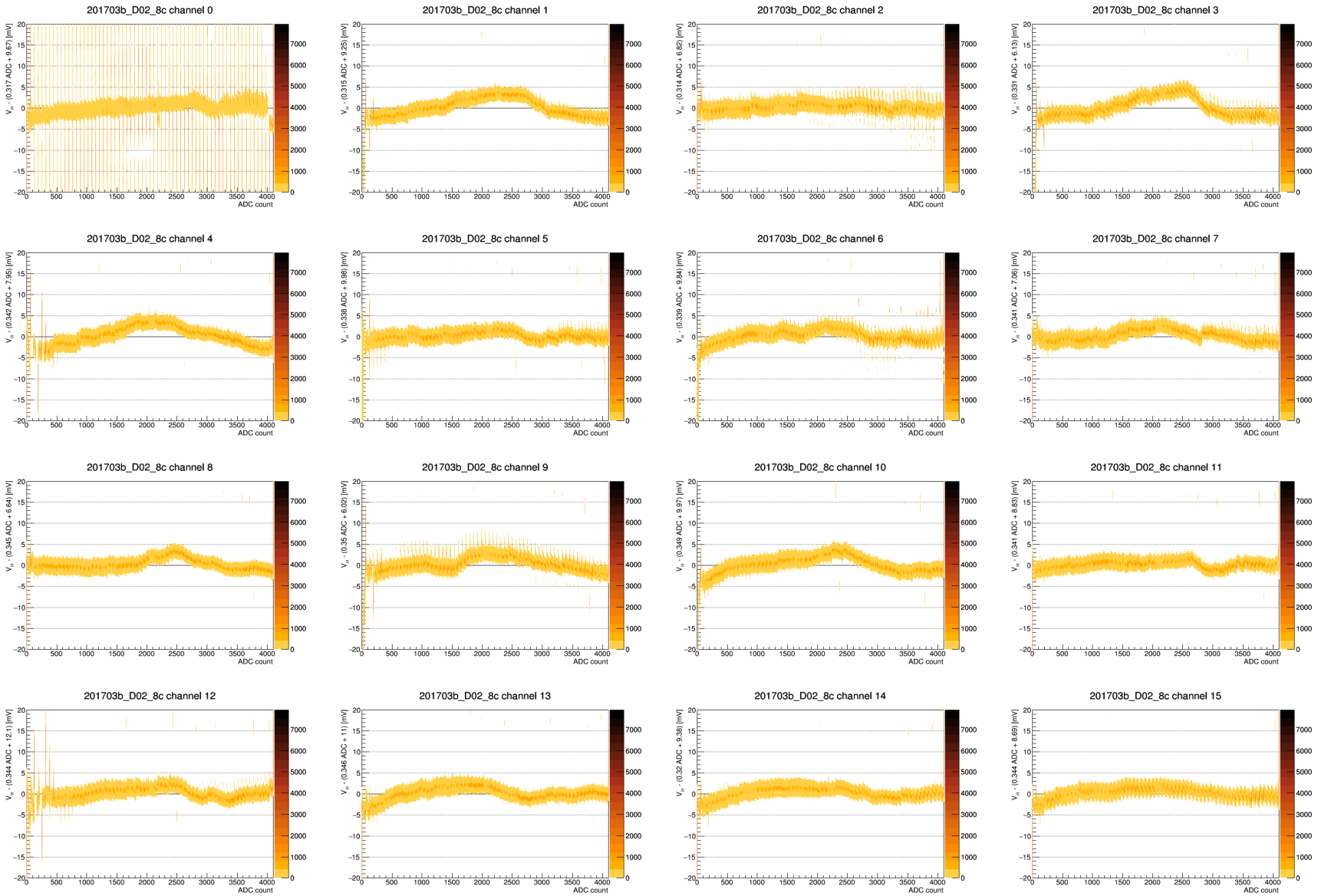
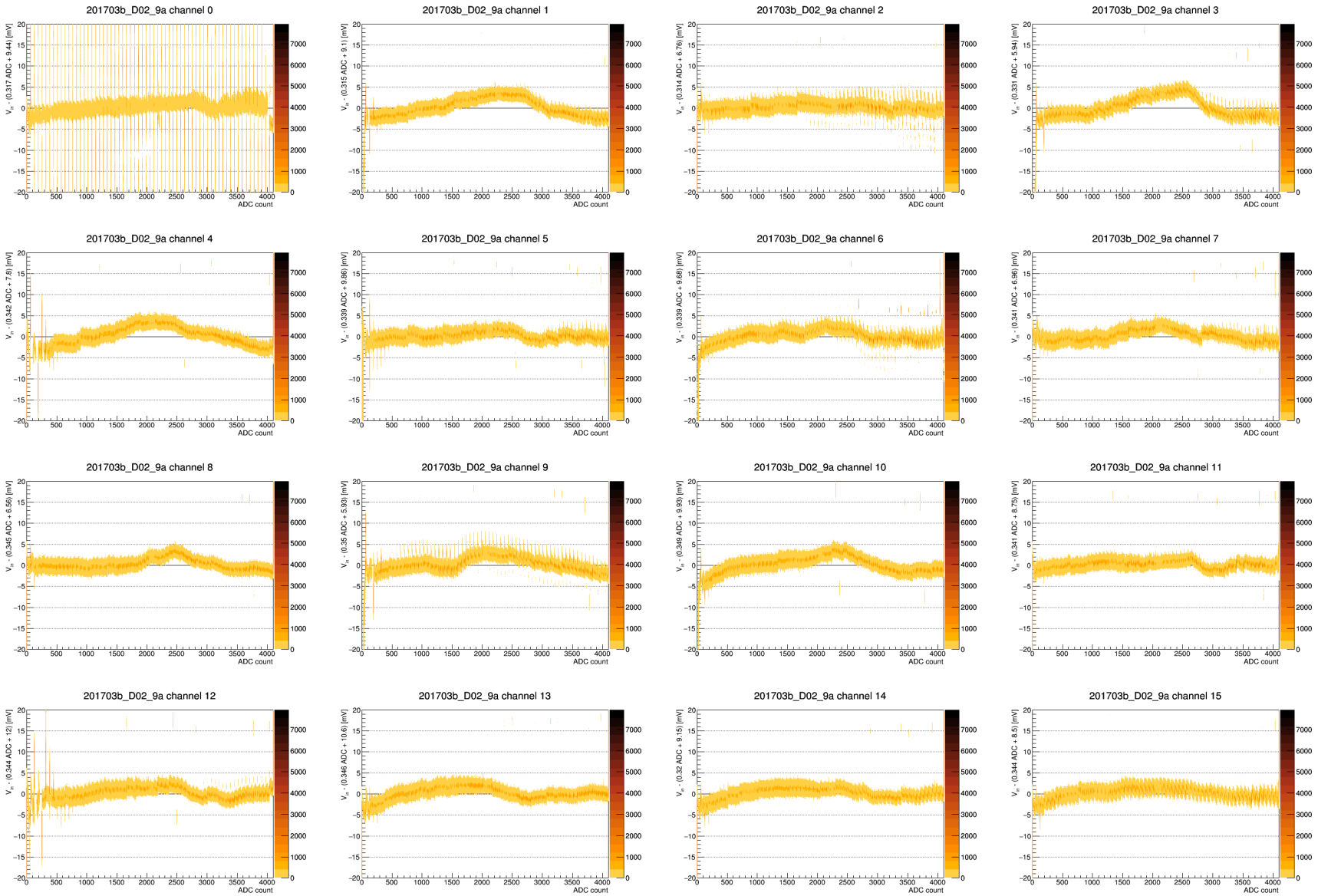


Residuals: chip D02, time 9a



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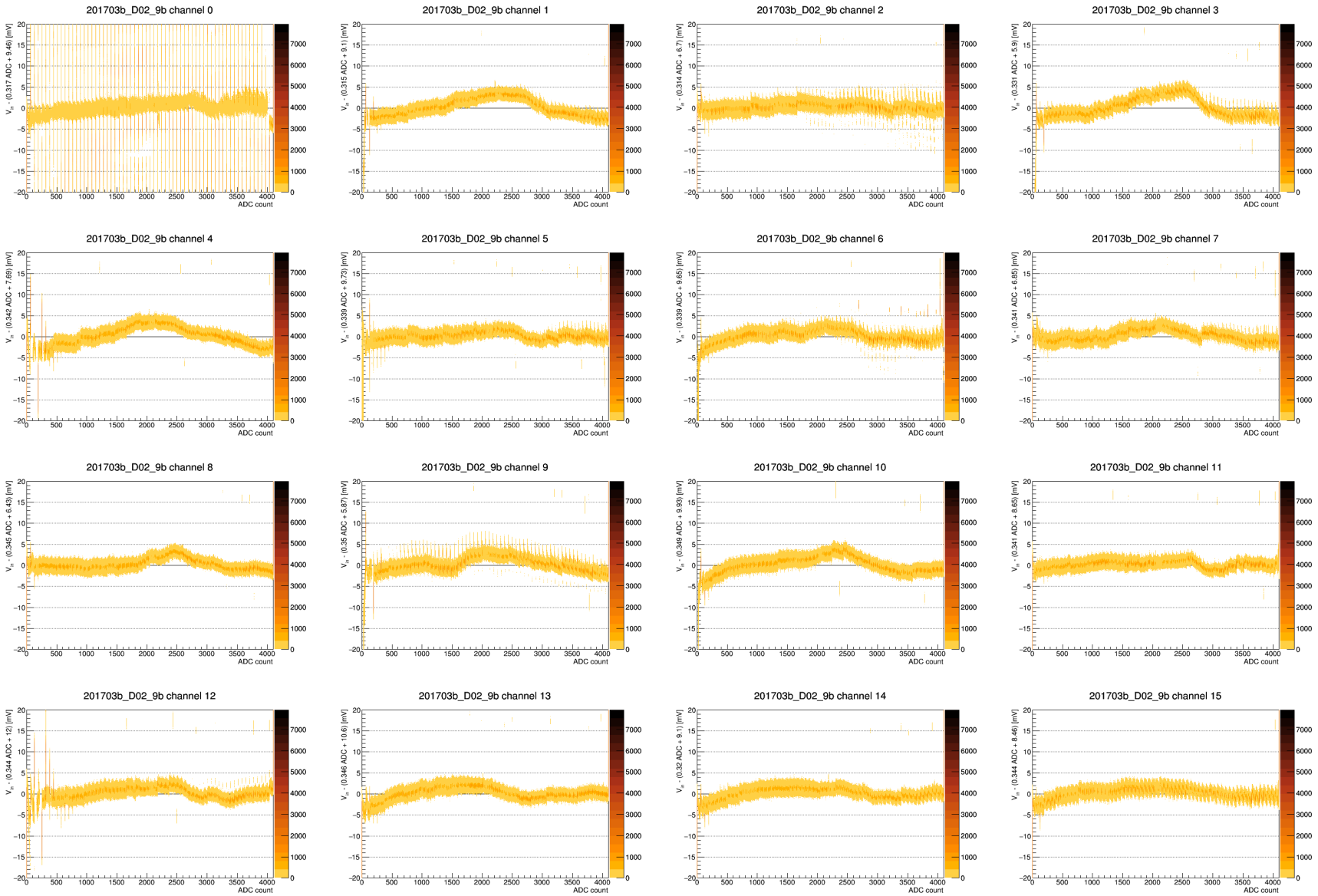

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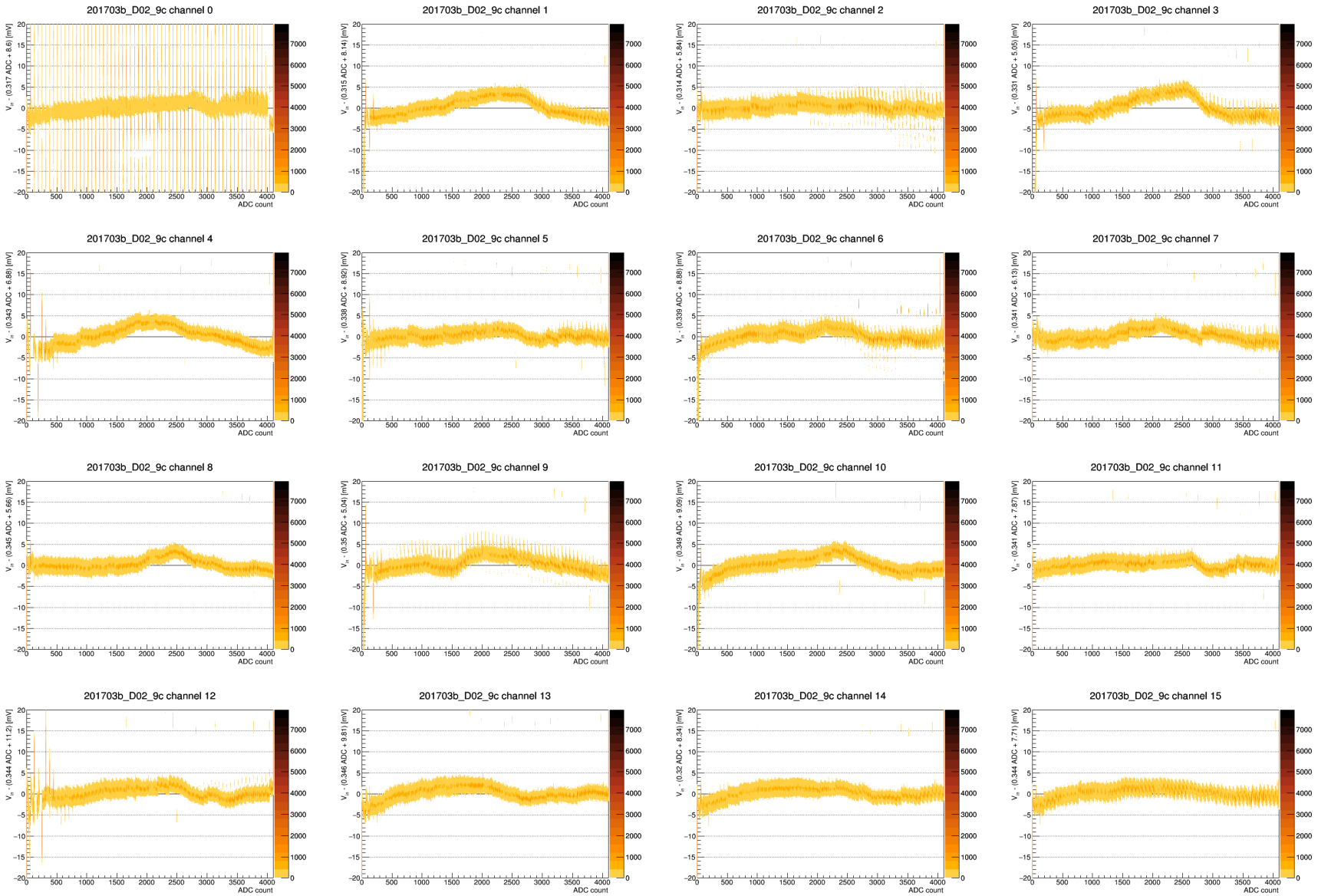
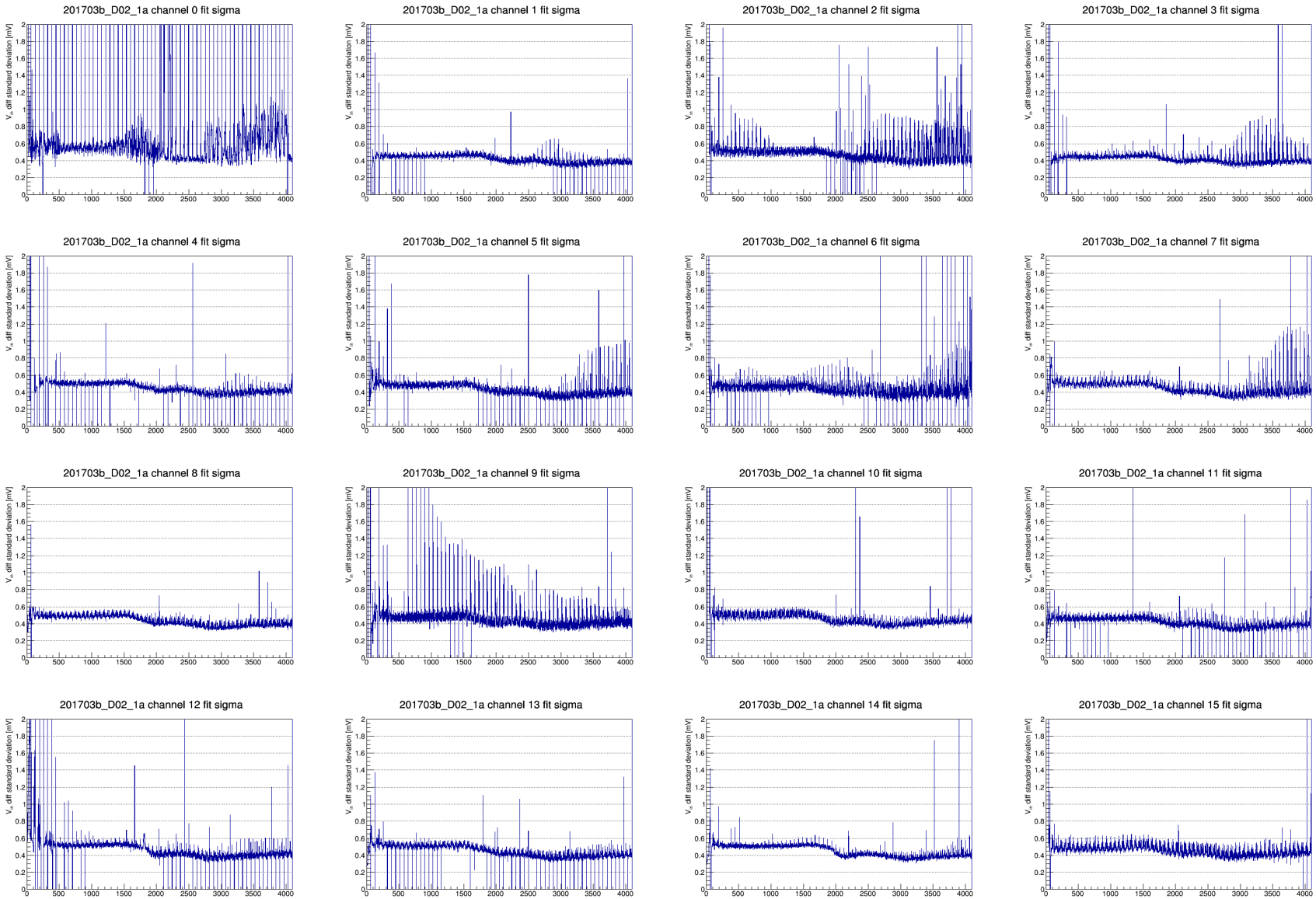
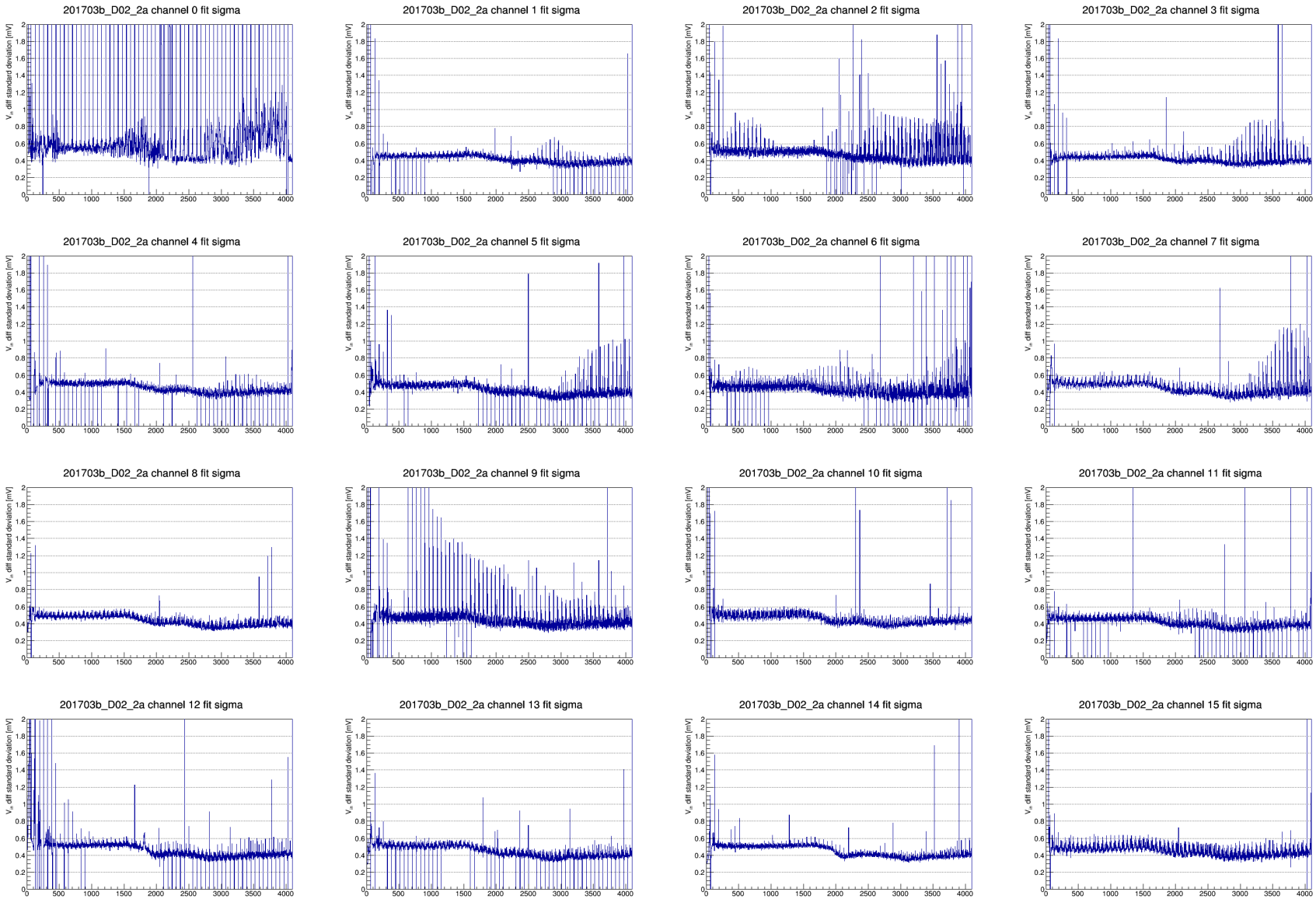


Bin RMS

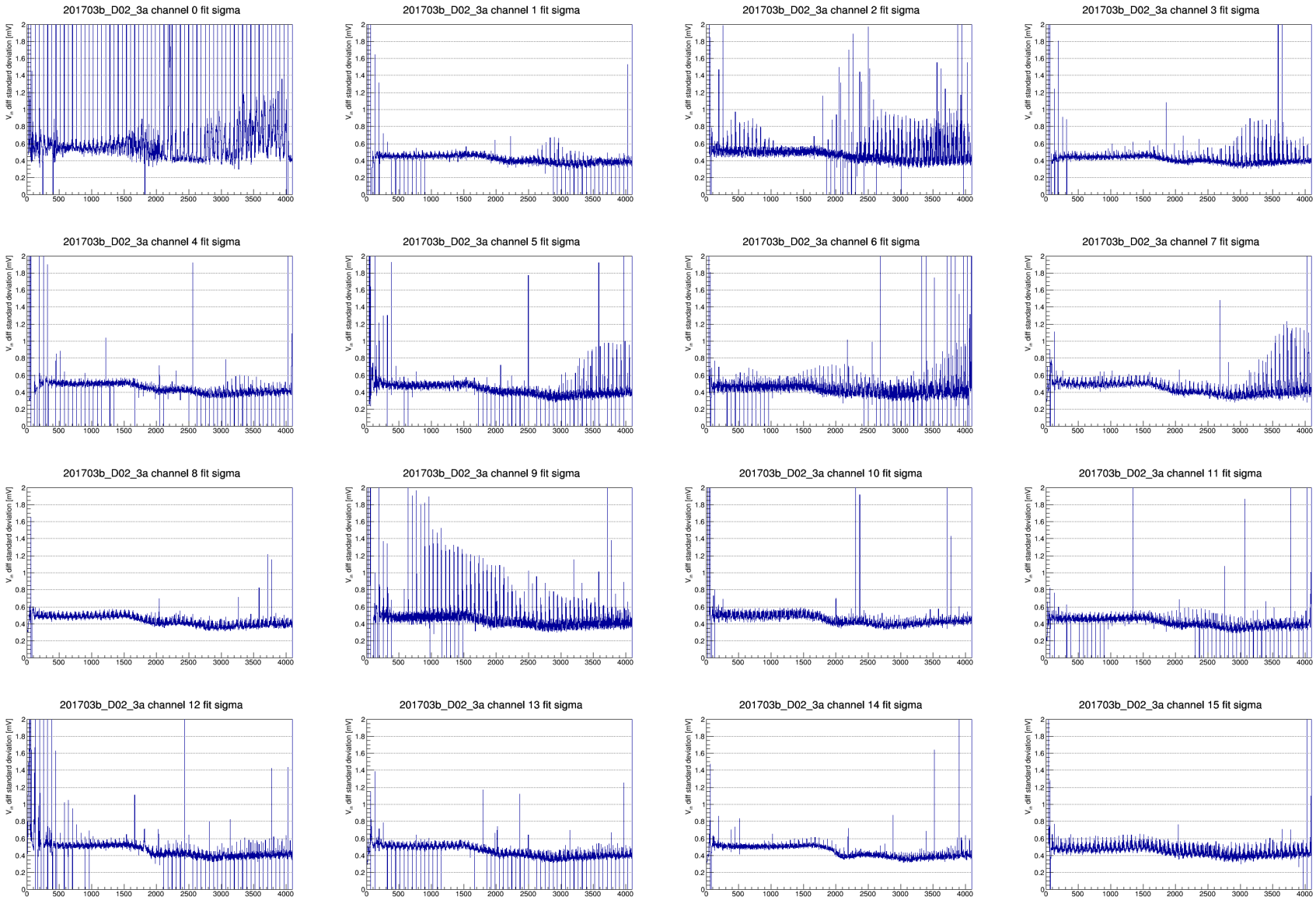
Bin RMS: chip D02, time 1a



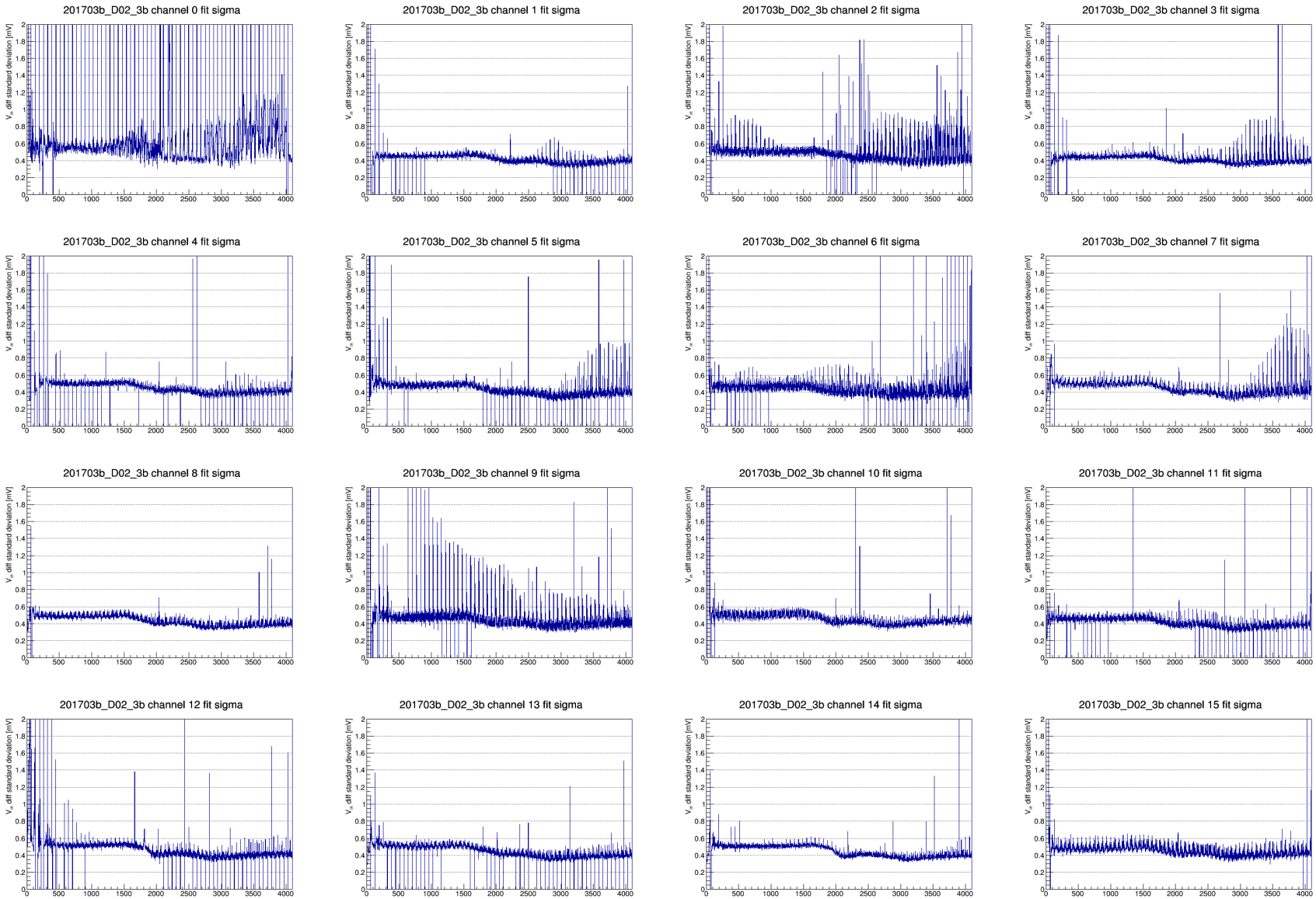
Bin RMS: chip D02, time 2a



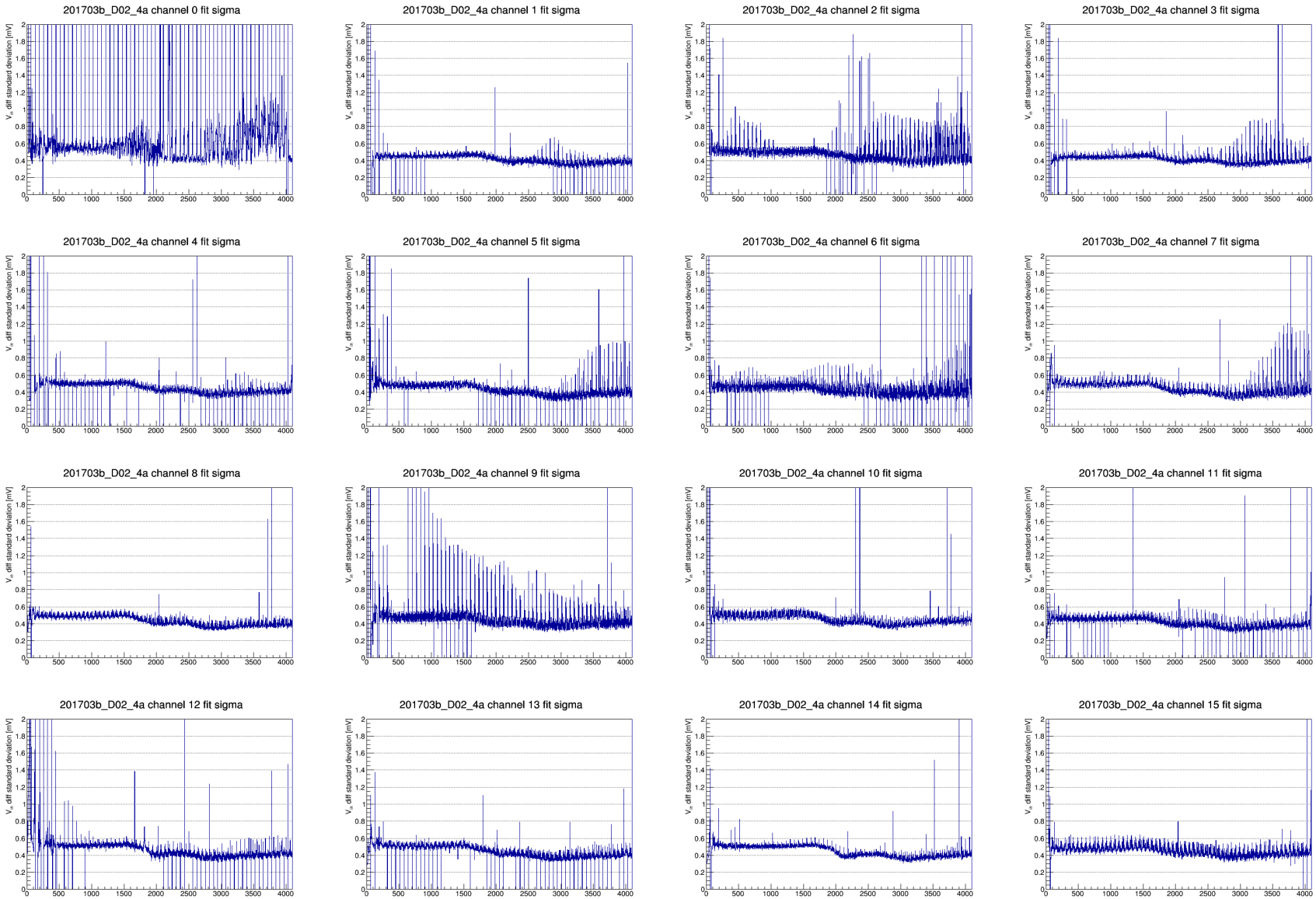
Bin RMS: chip D02, time 3a



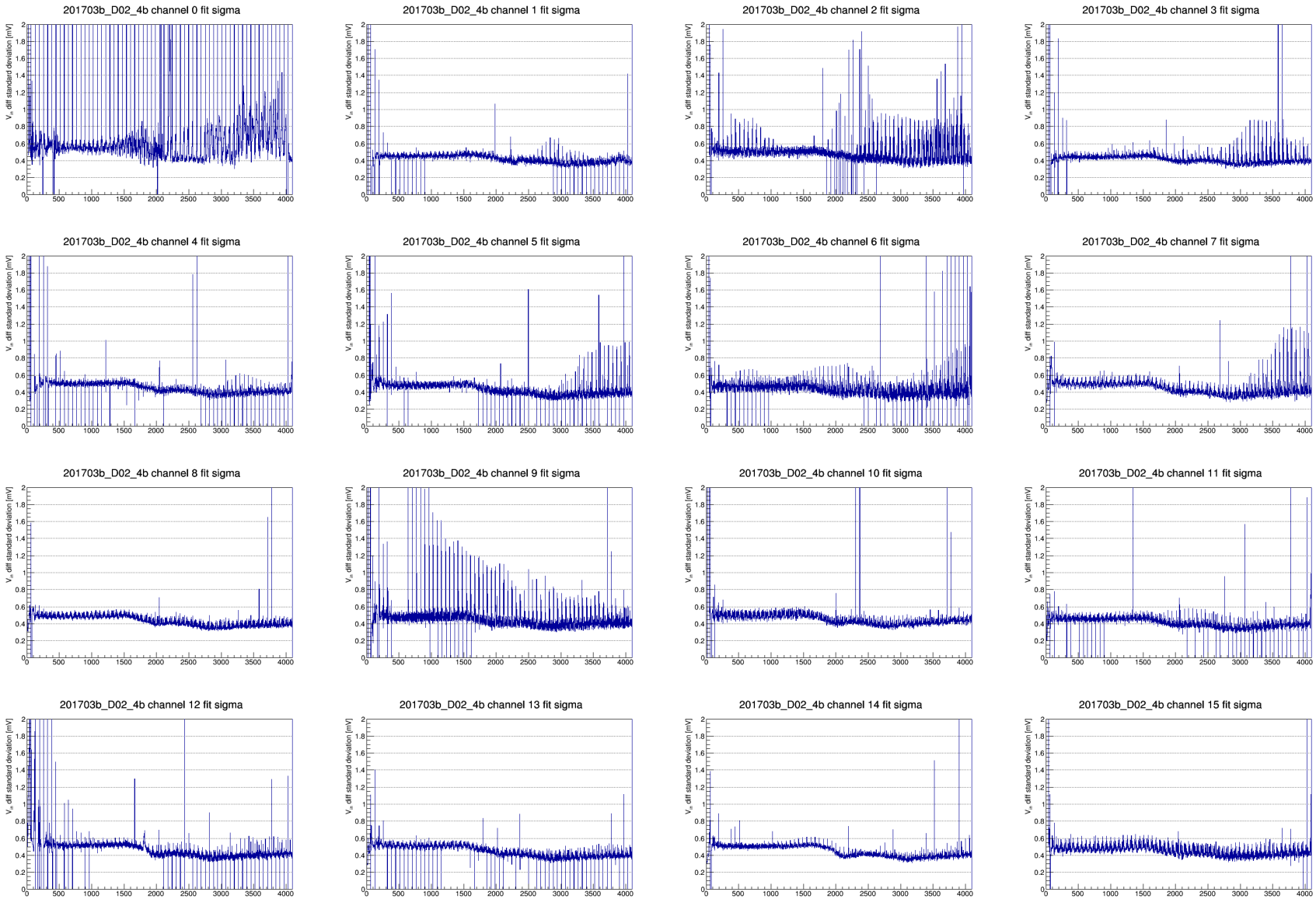
Bin RMS: chip D02, time 3b



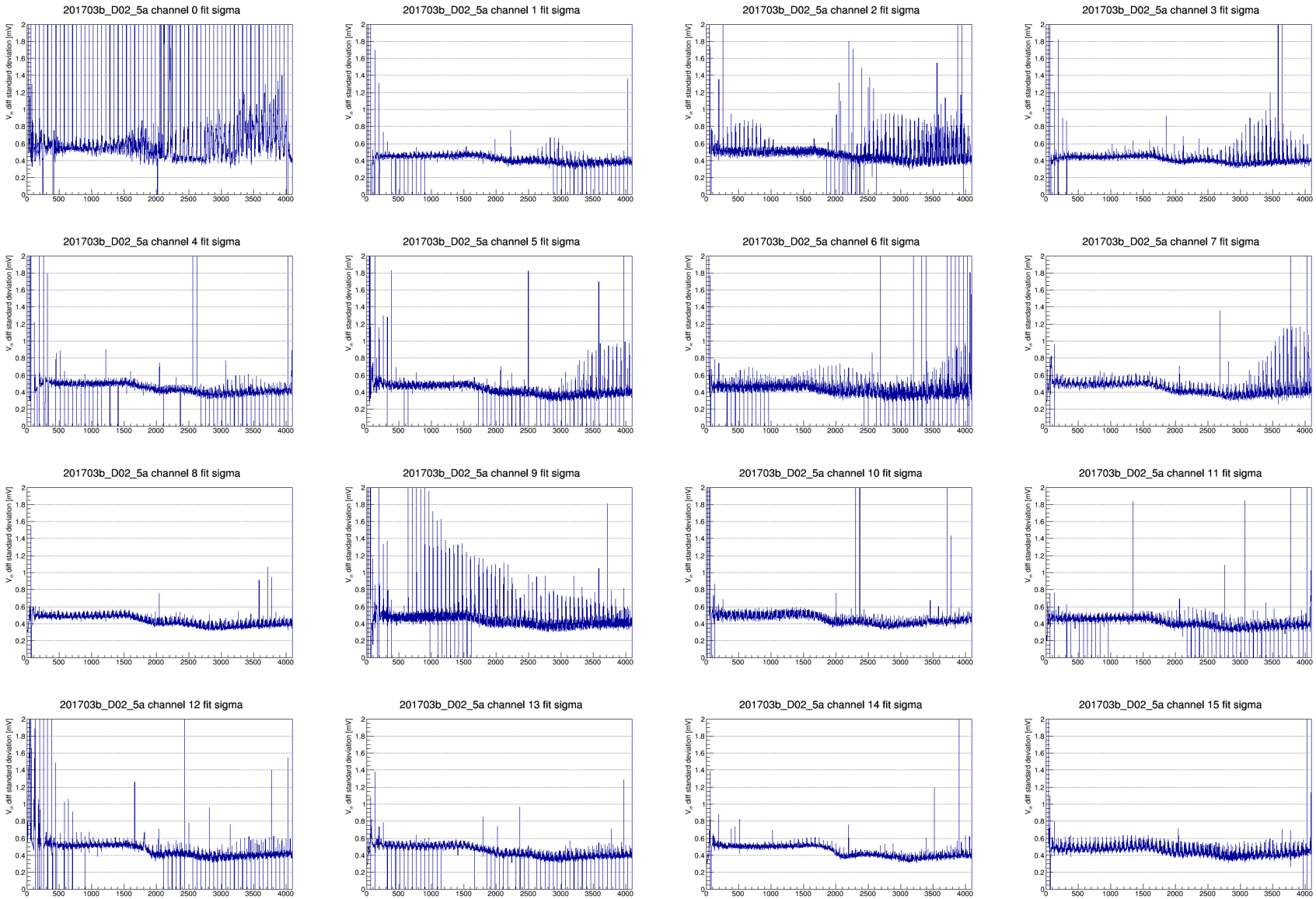
Bin RMS: chip D02, time 4a



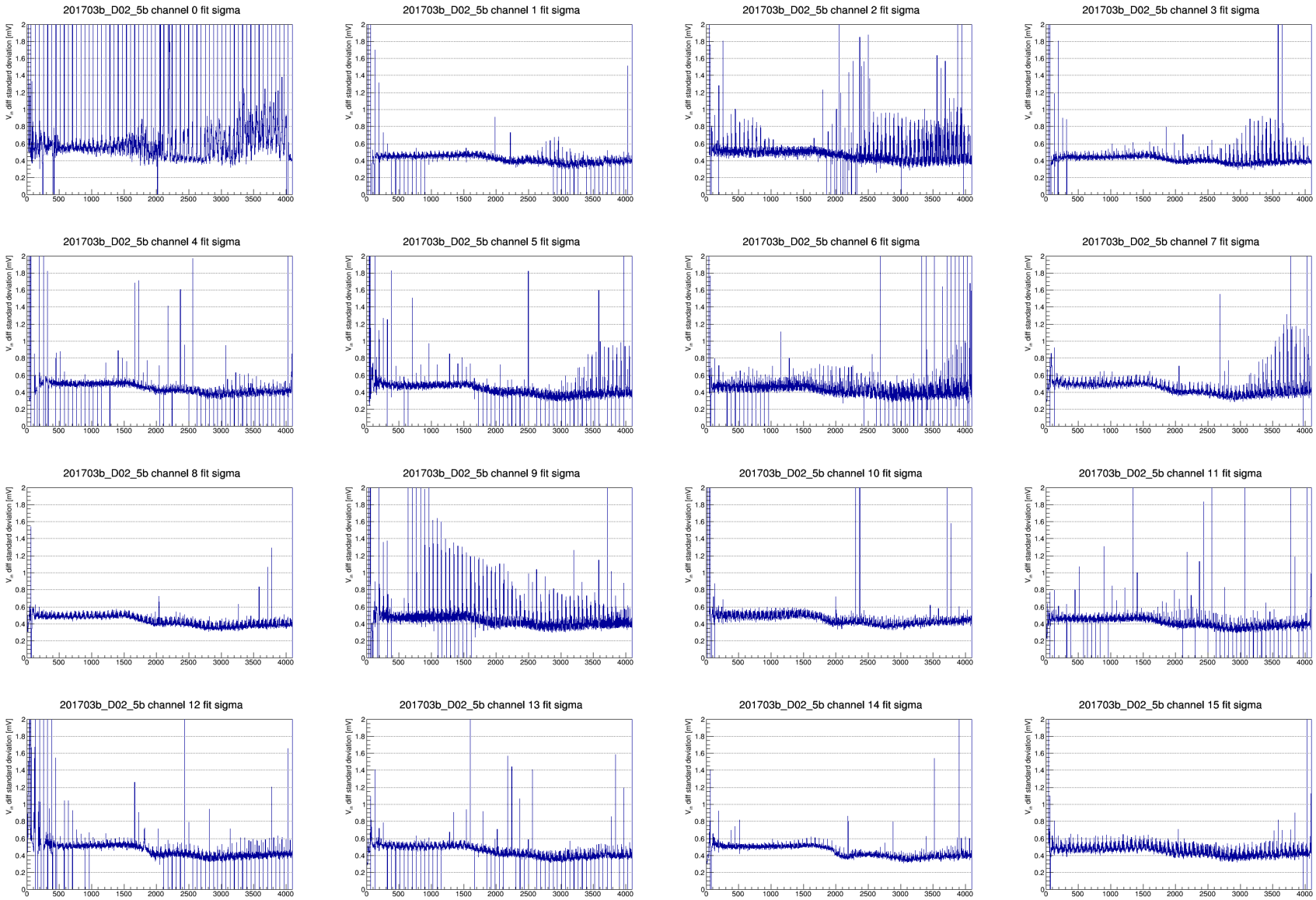
Bin RMS: chip D02, time 4b



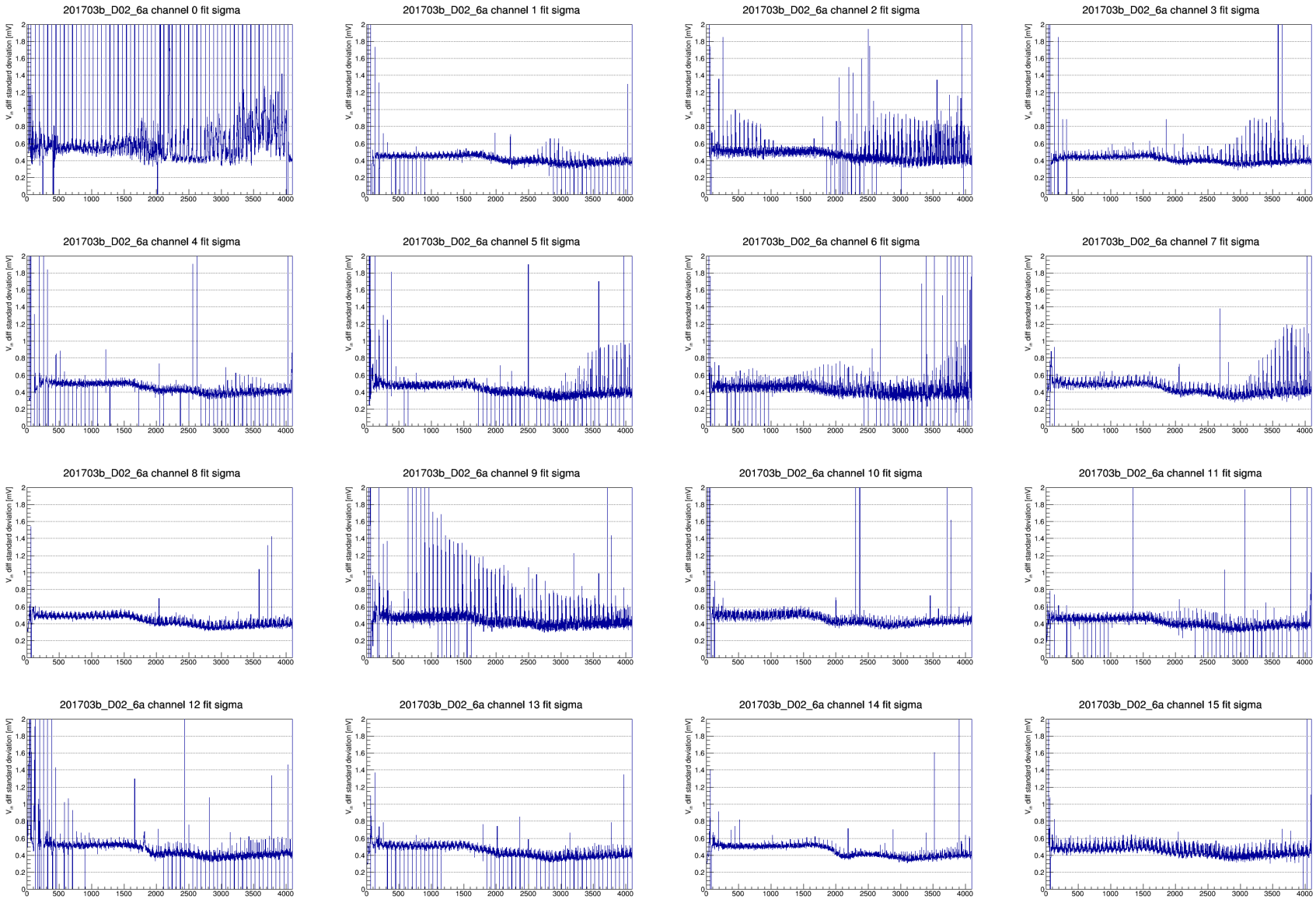
Bin RMS: chip D02, time 5a



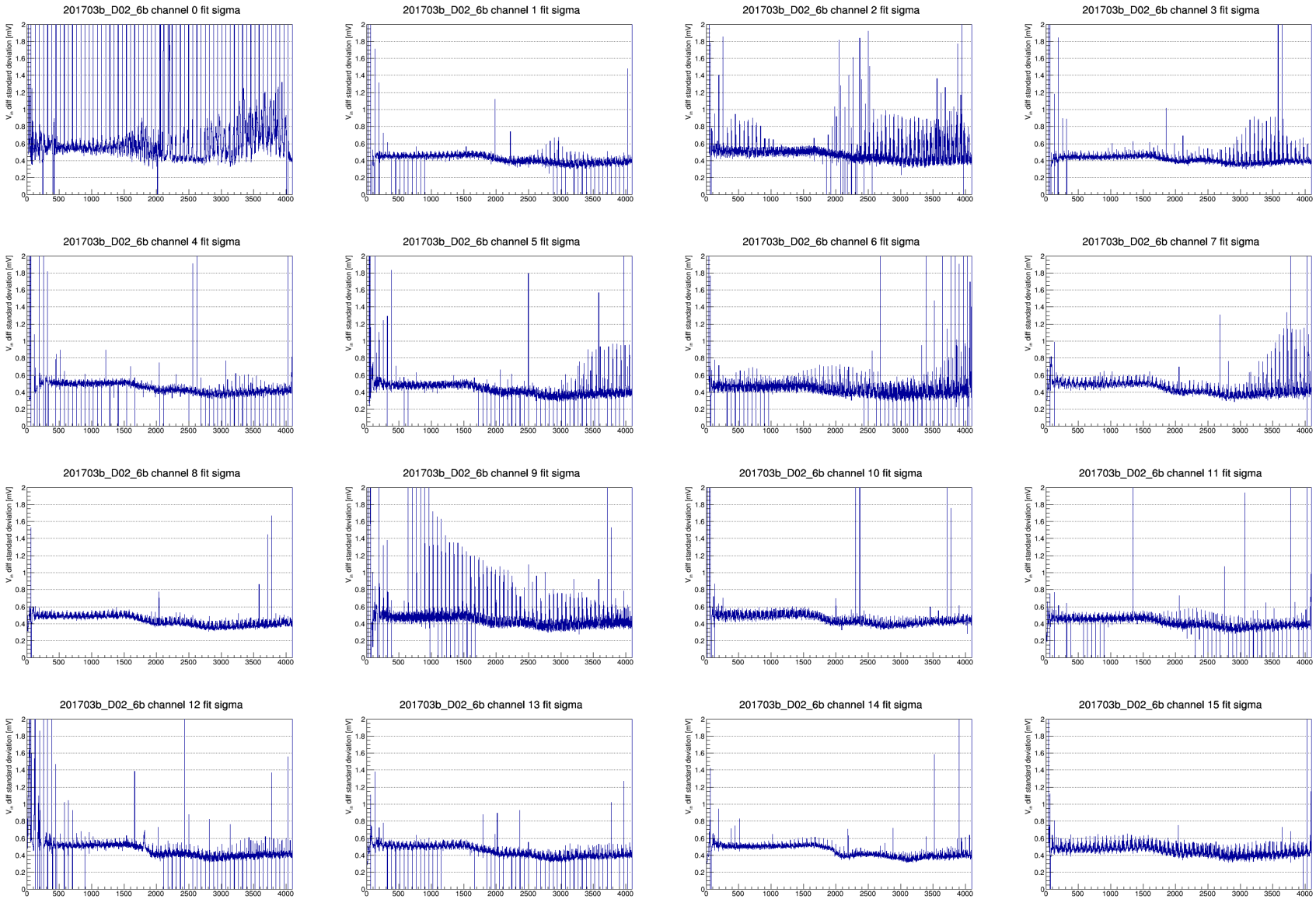
Bin RMS: chip D02, time 5b



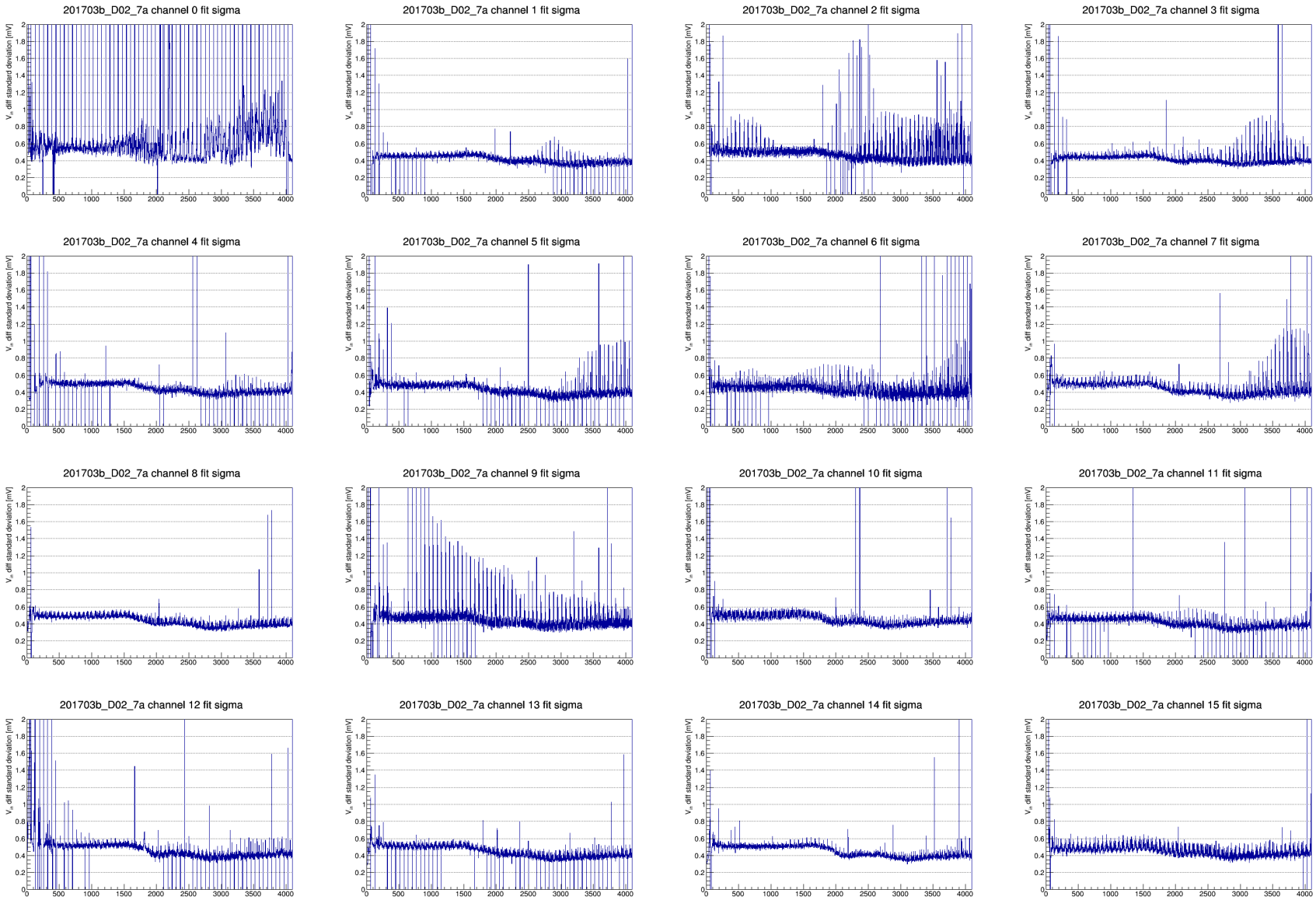
Bin RMS: chip D02, time 6a



Bin RMS: chip D02, time 6b



Bin RMS: chip D02, time 7a



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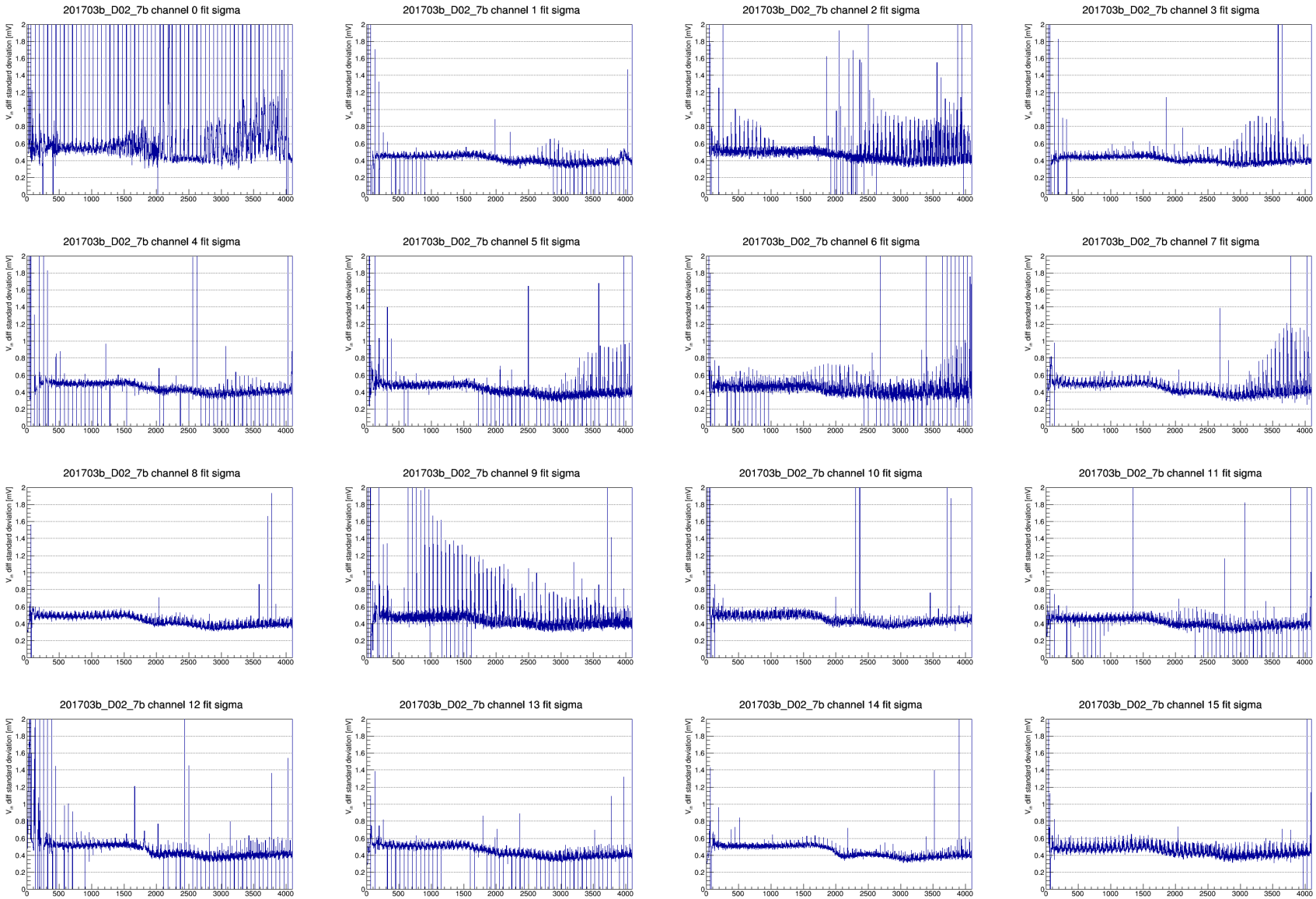

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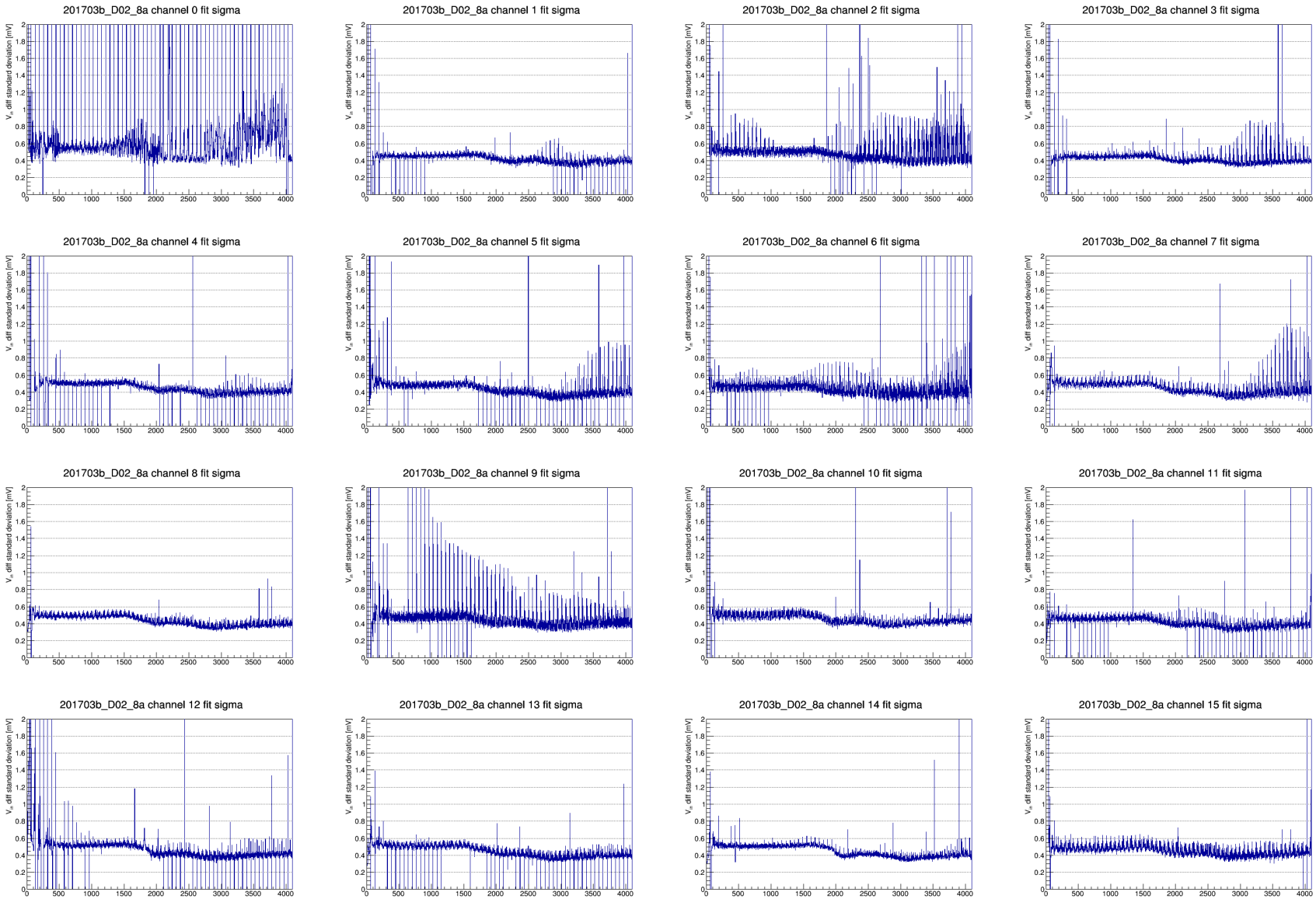

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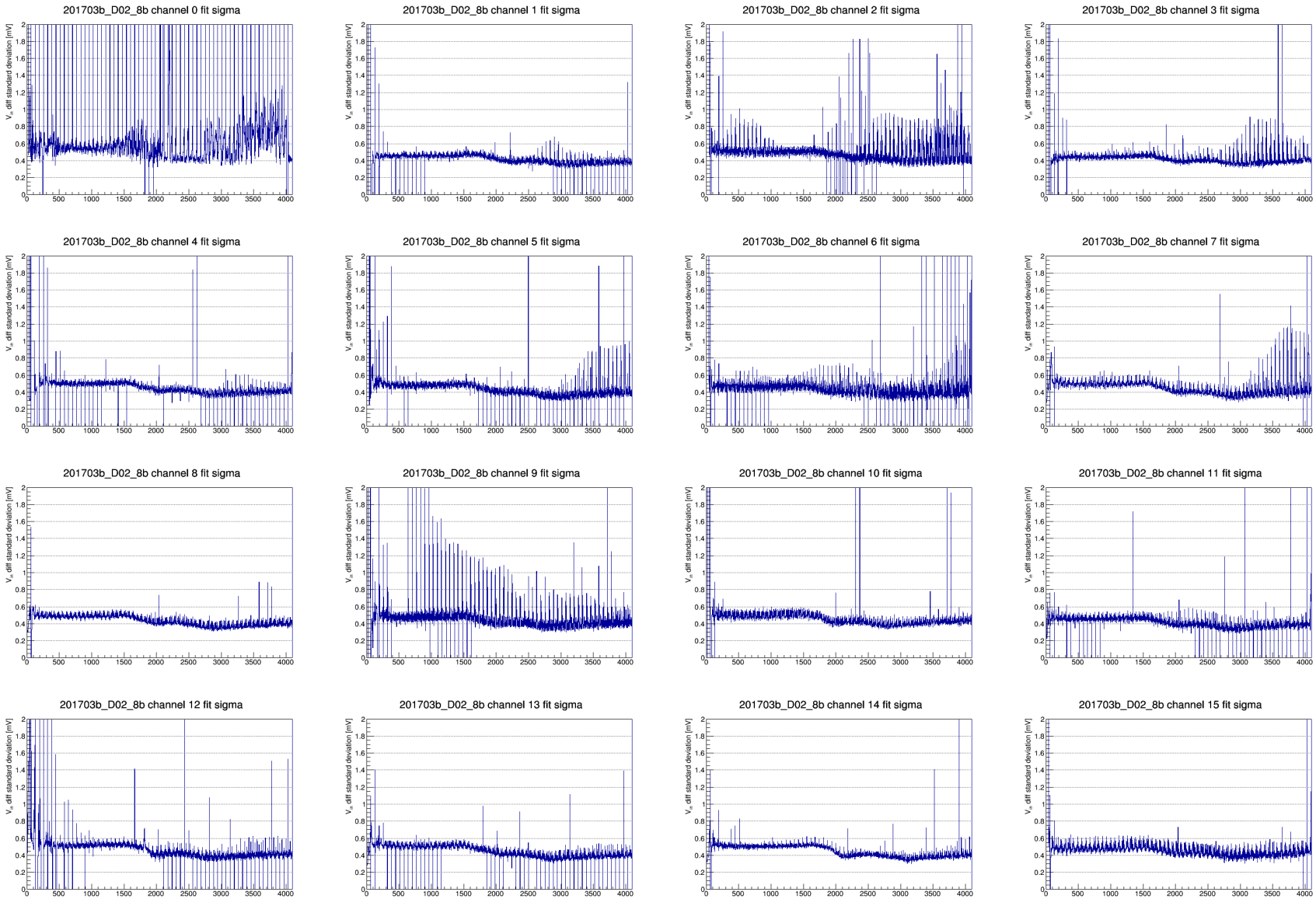

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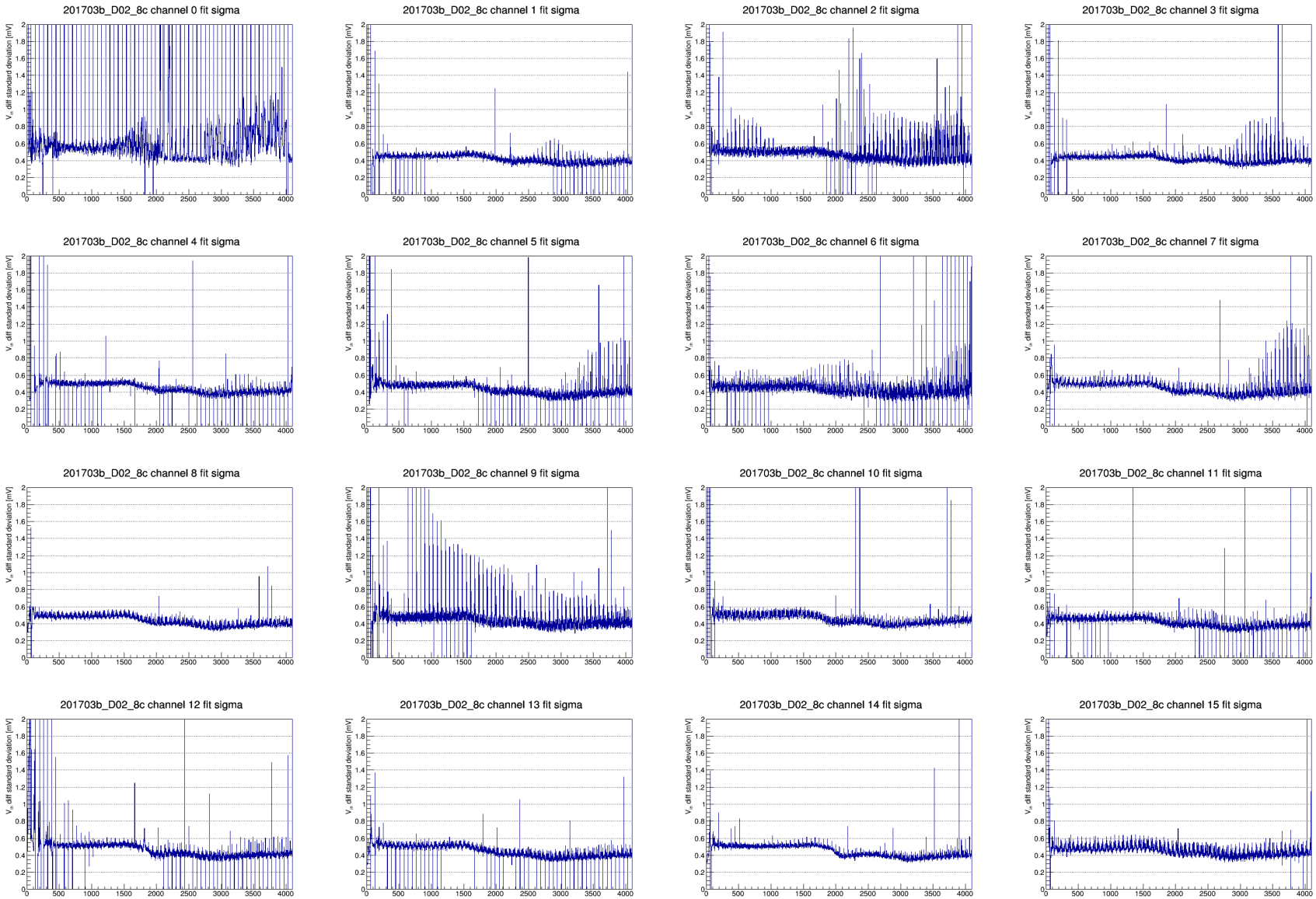

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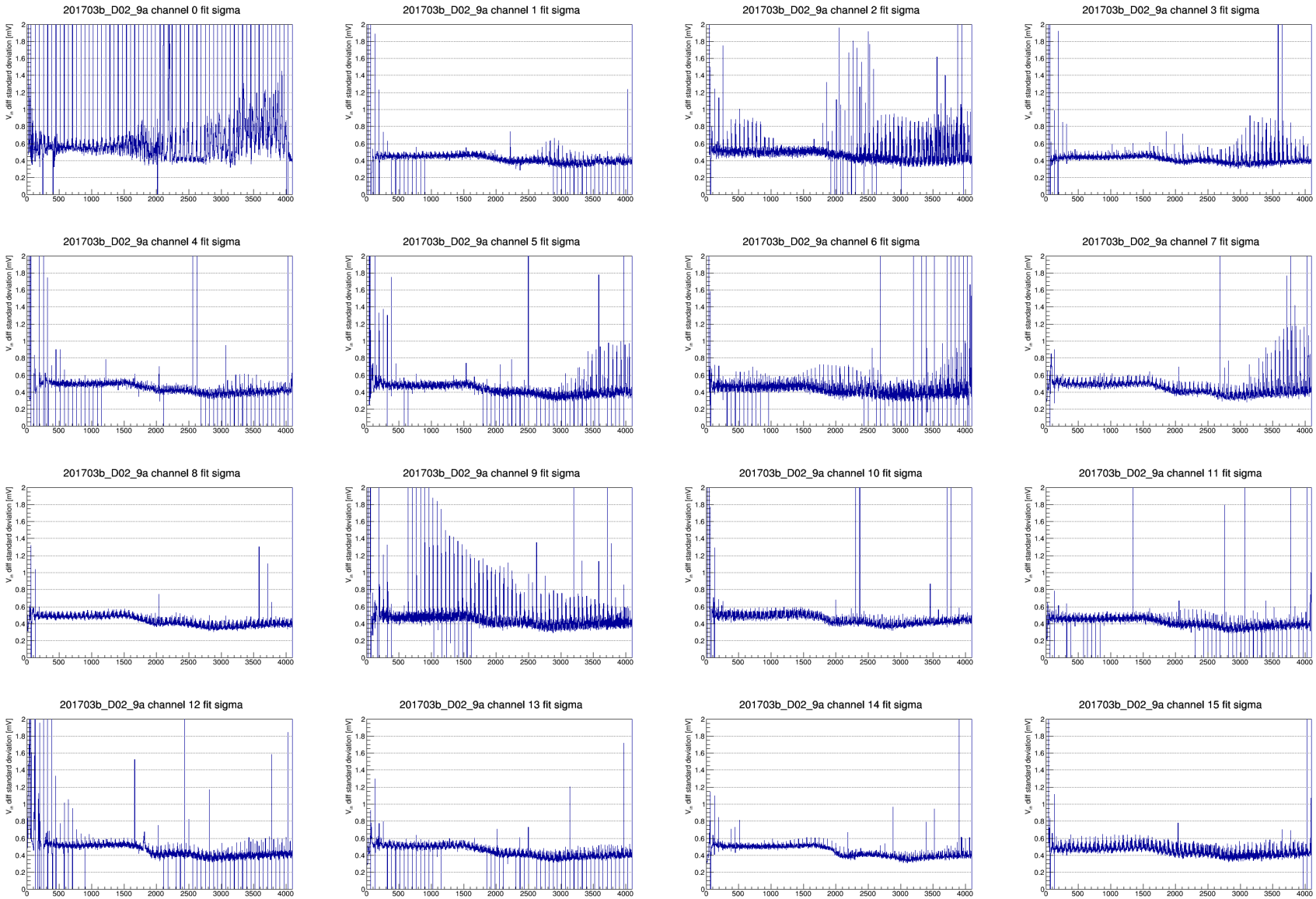

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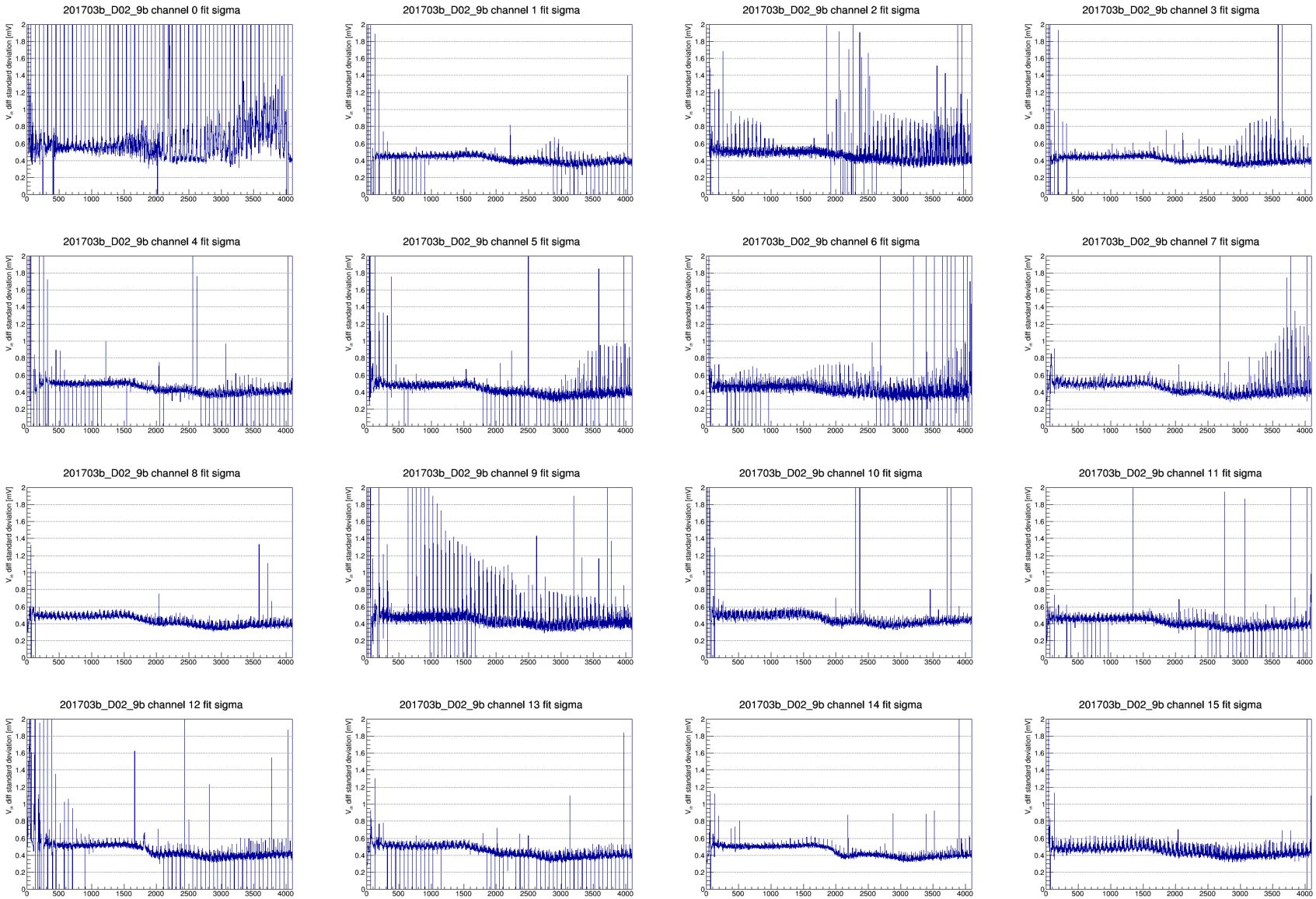

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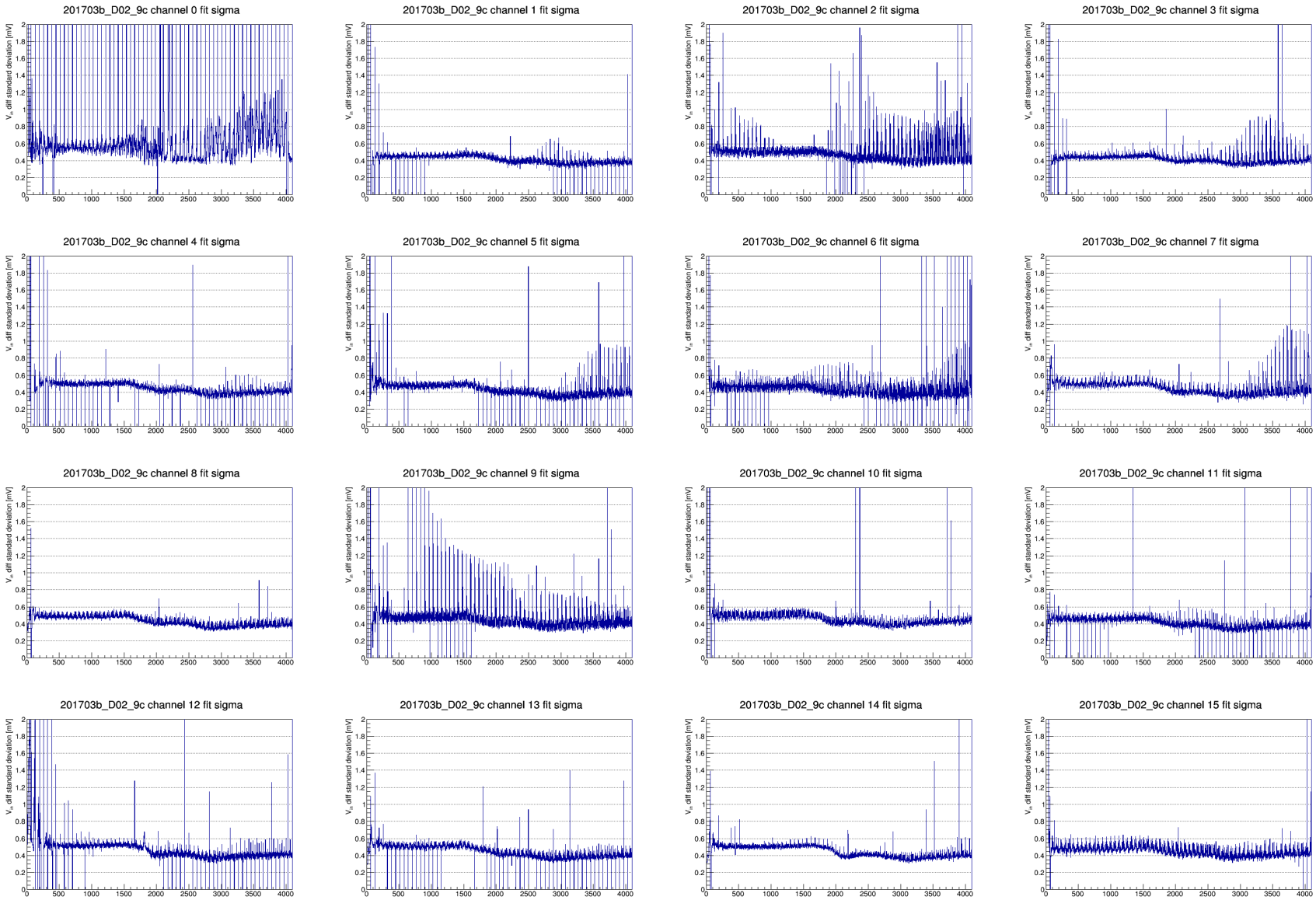
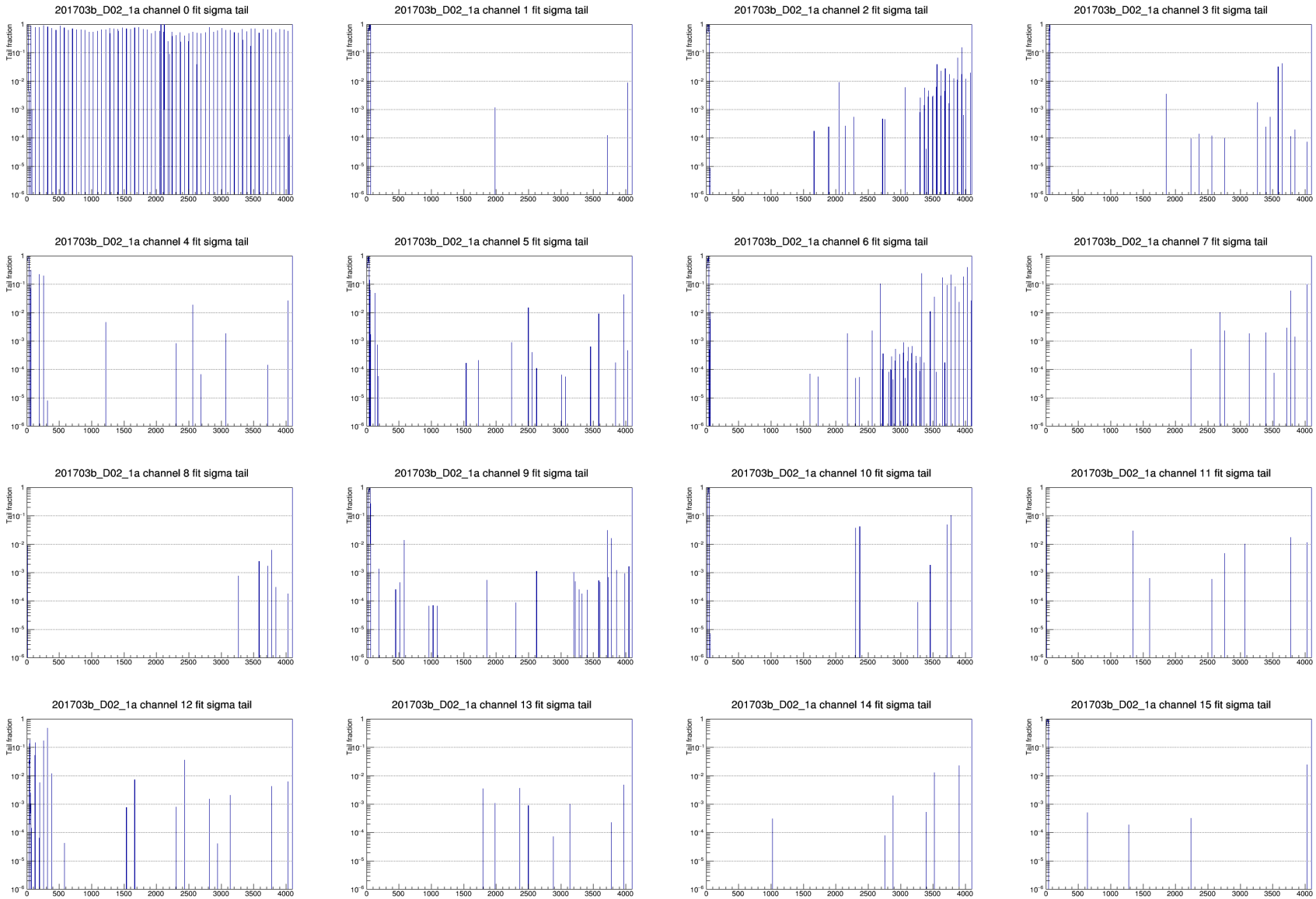
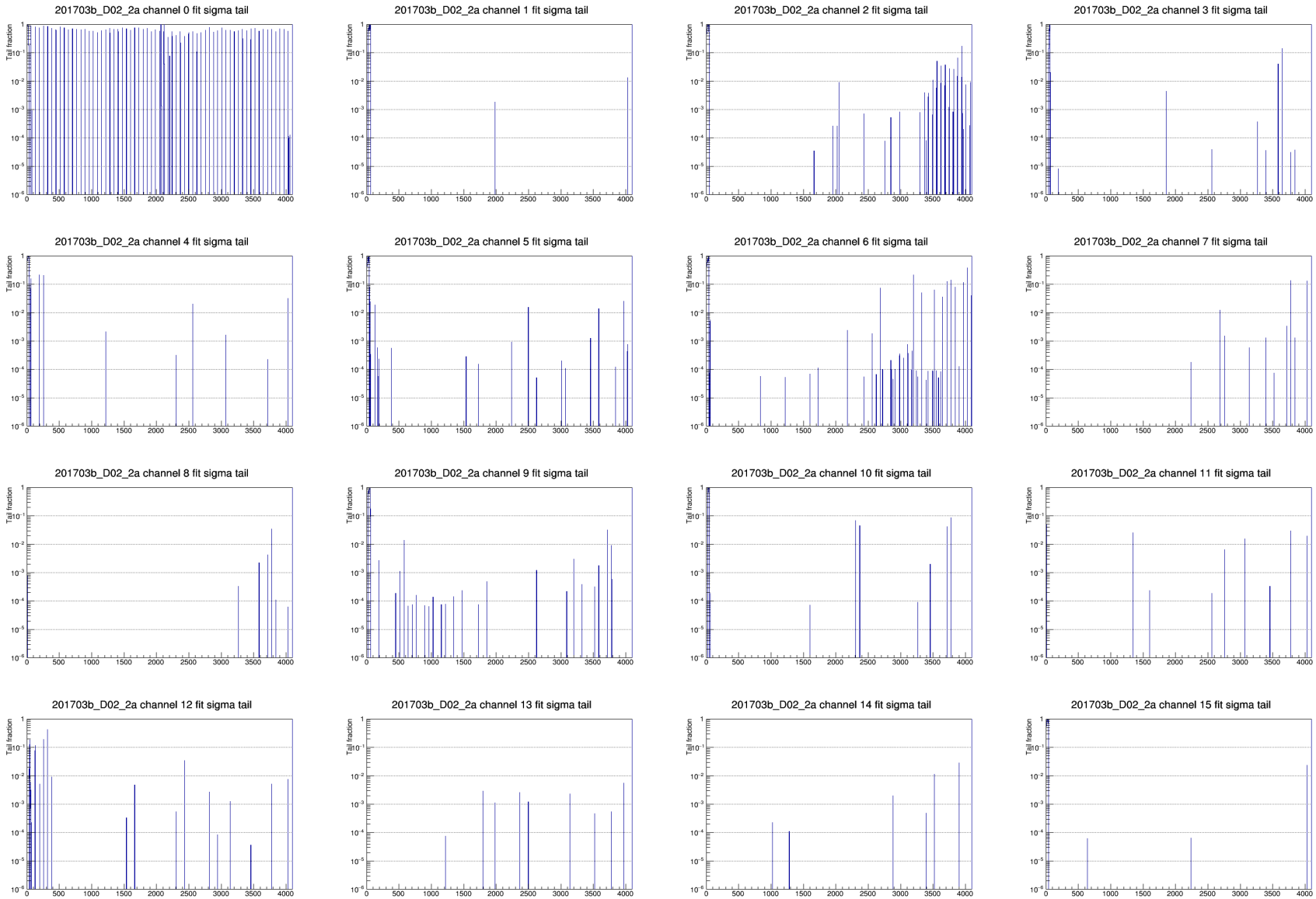


Tails

Tails: chip D02, time 1a



Tails: chip D02, time 2a



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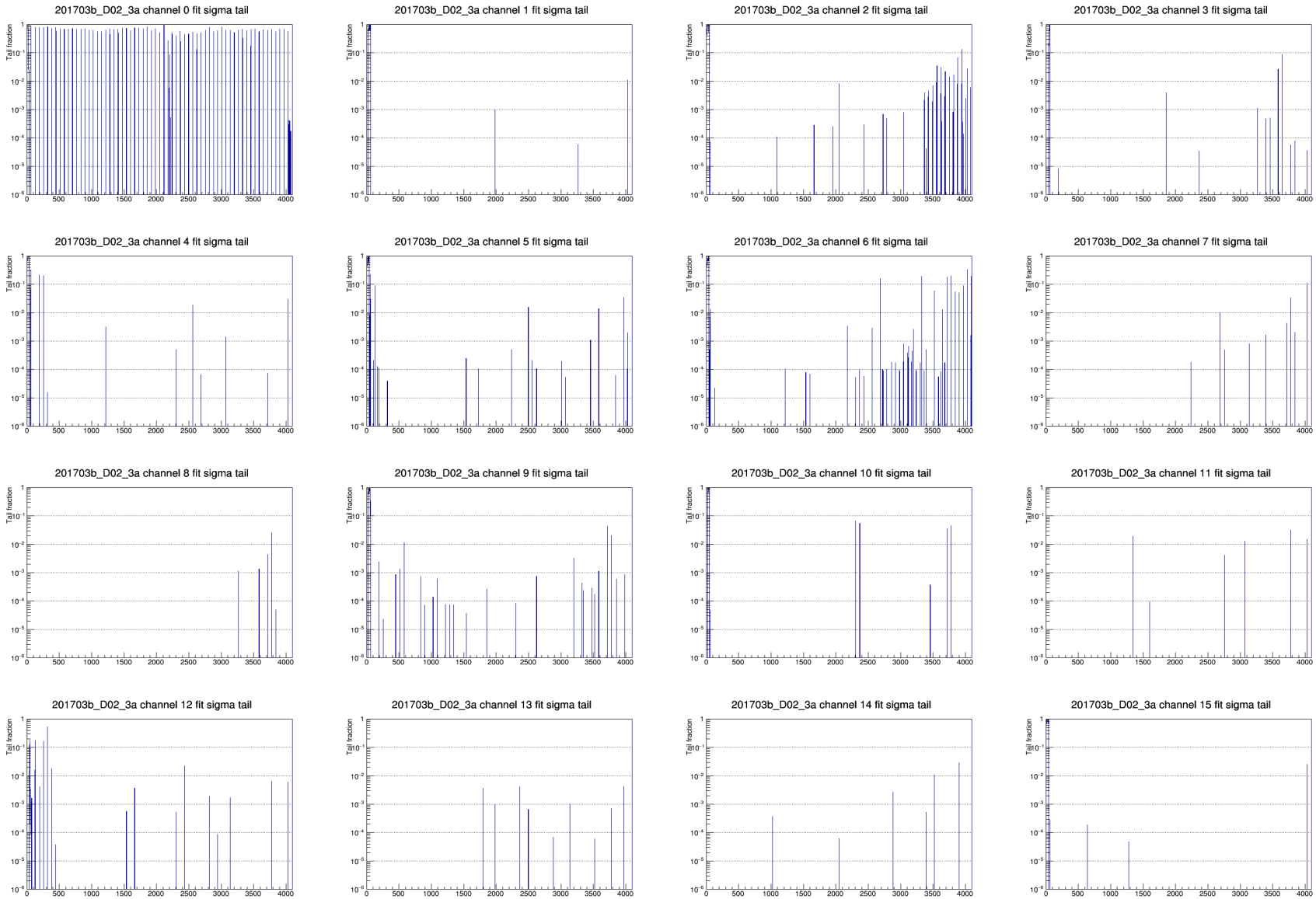

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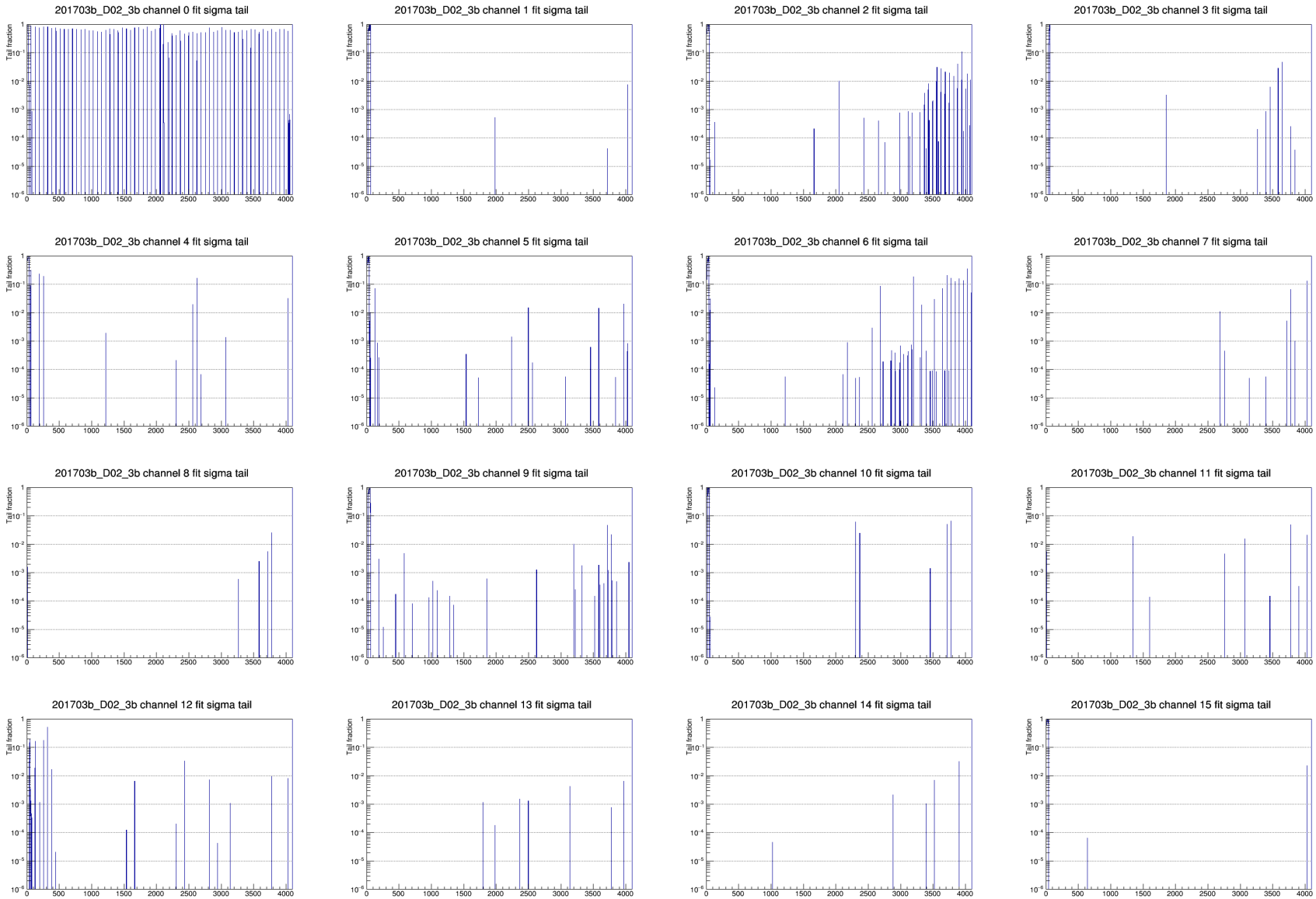

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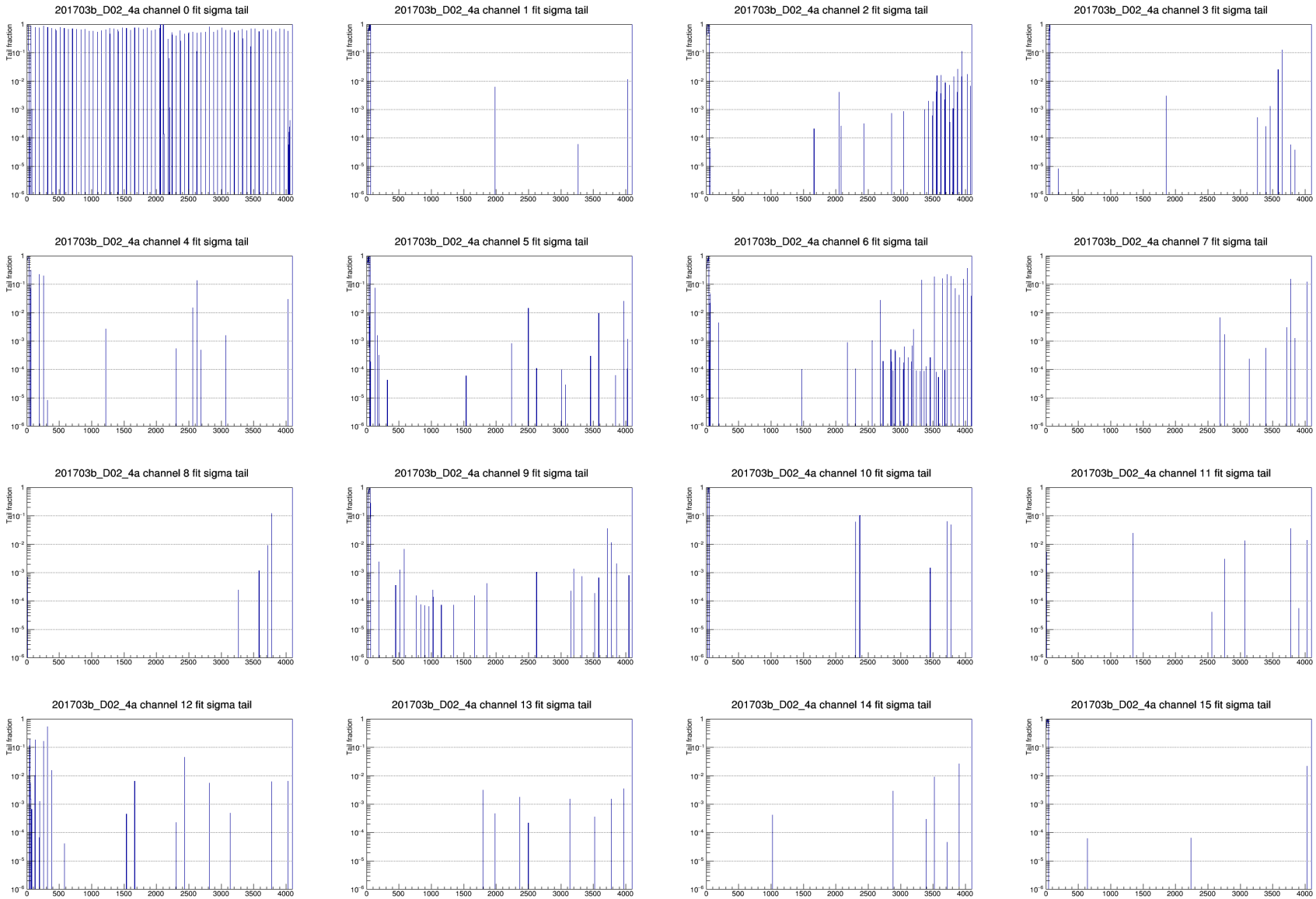

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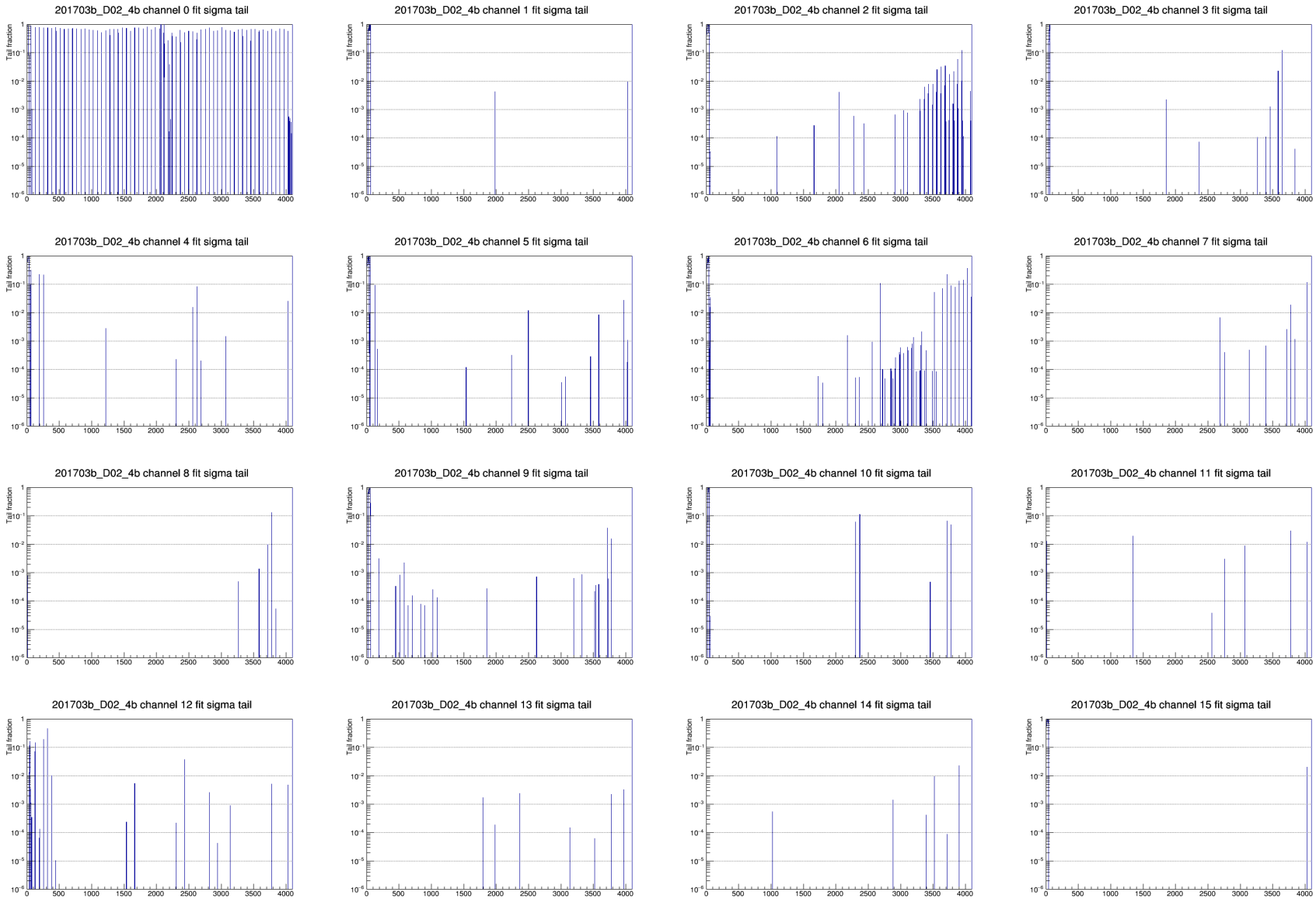

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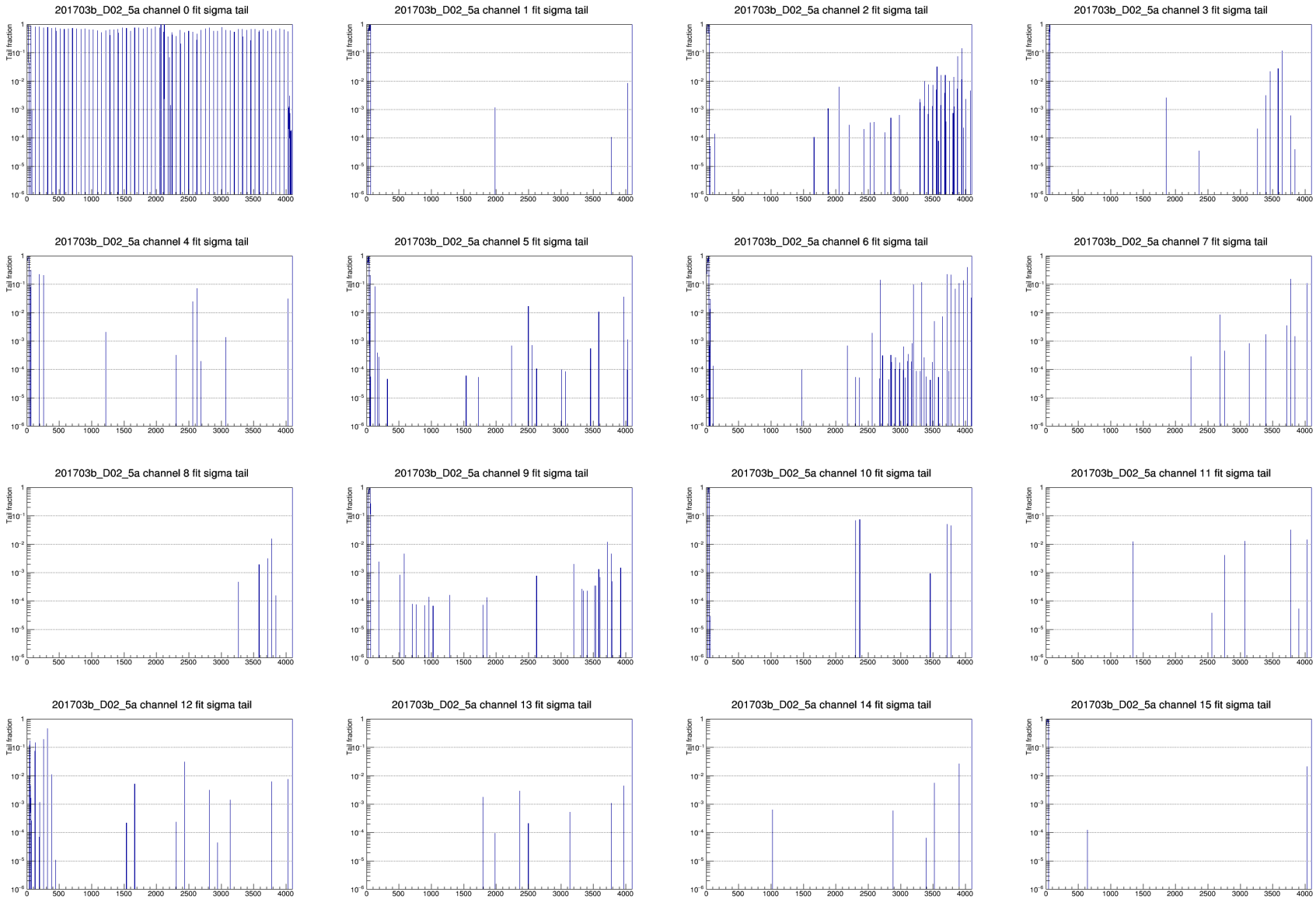
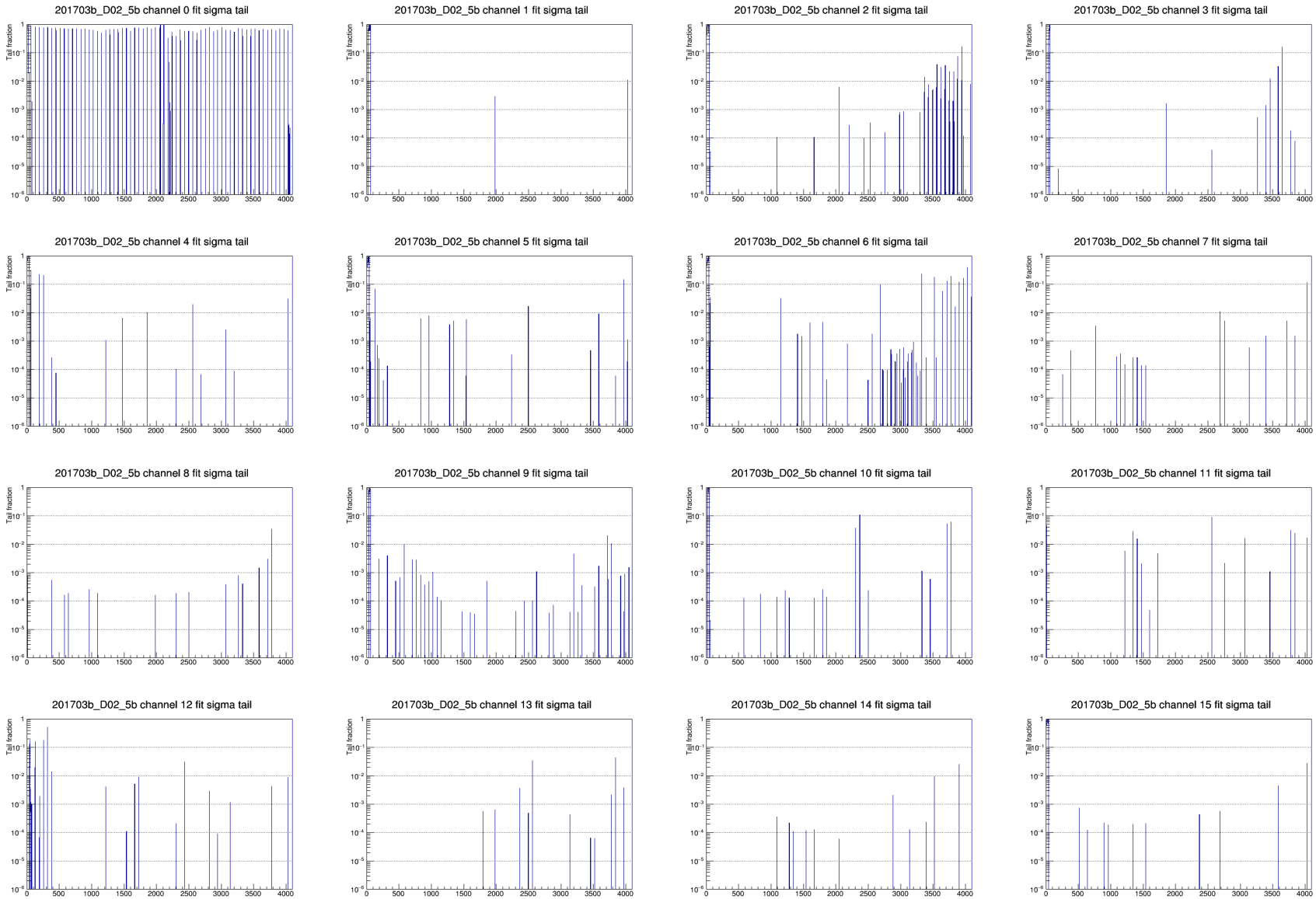


Tails: chip D02, time 5b



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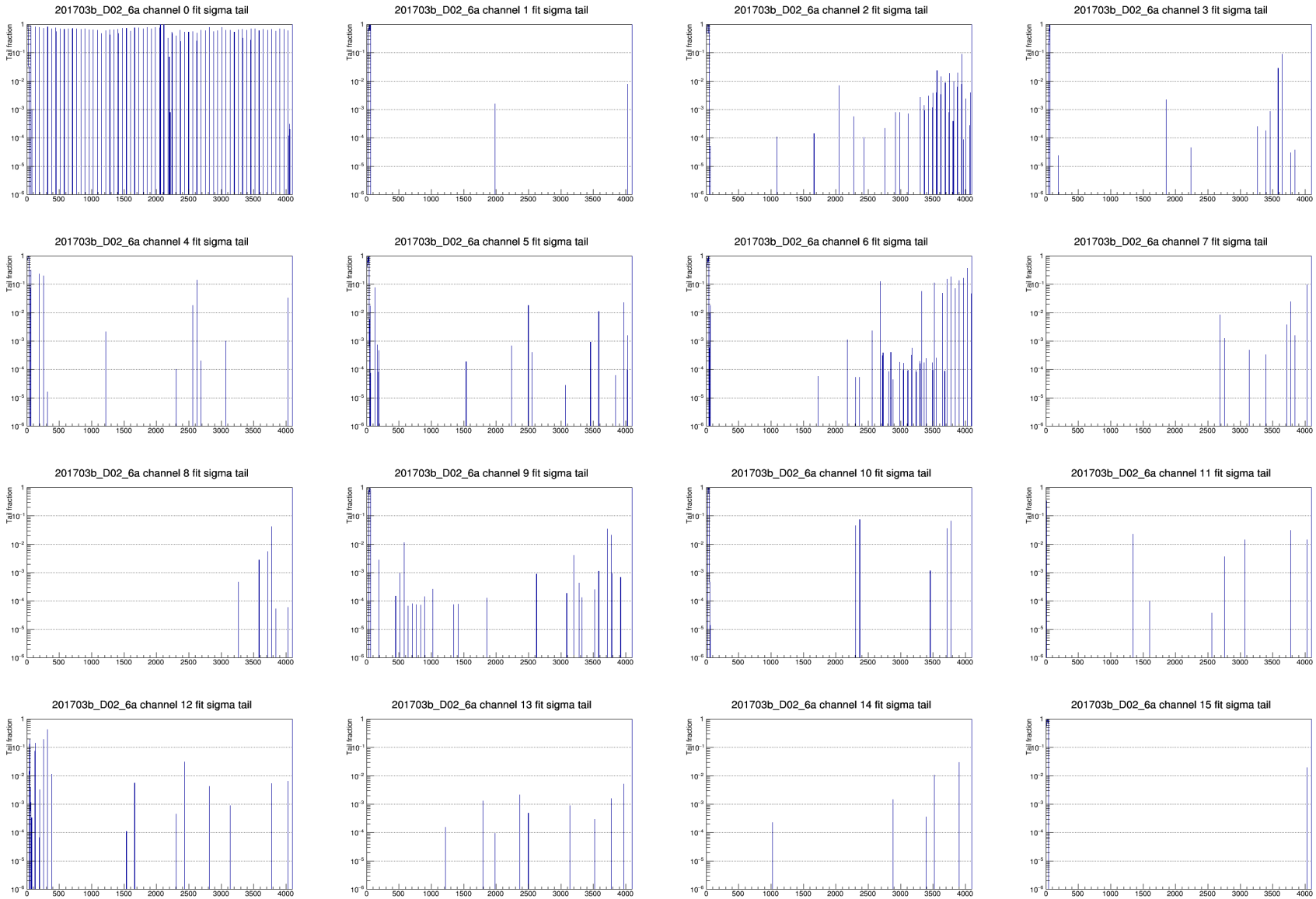

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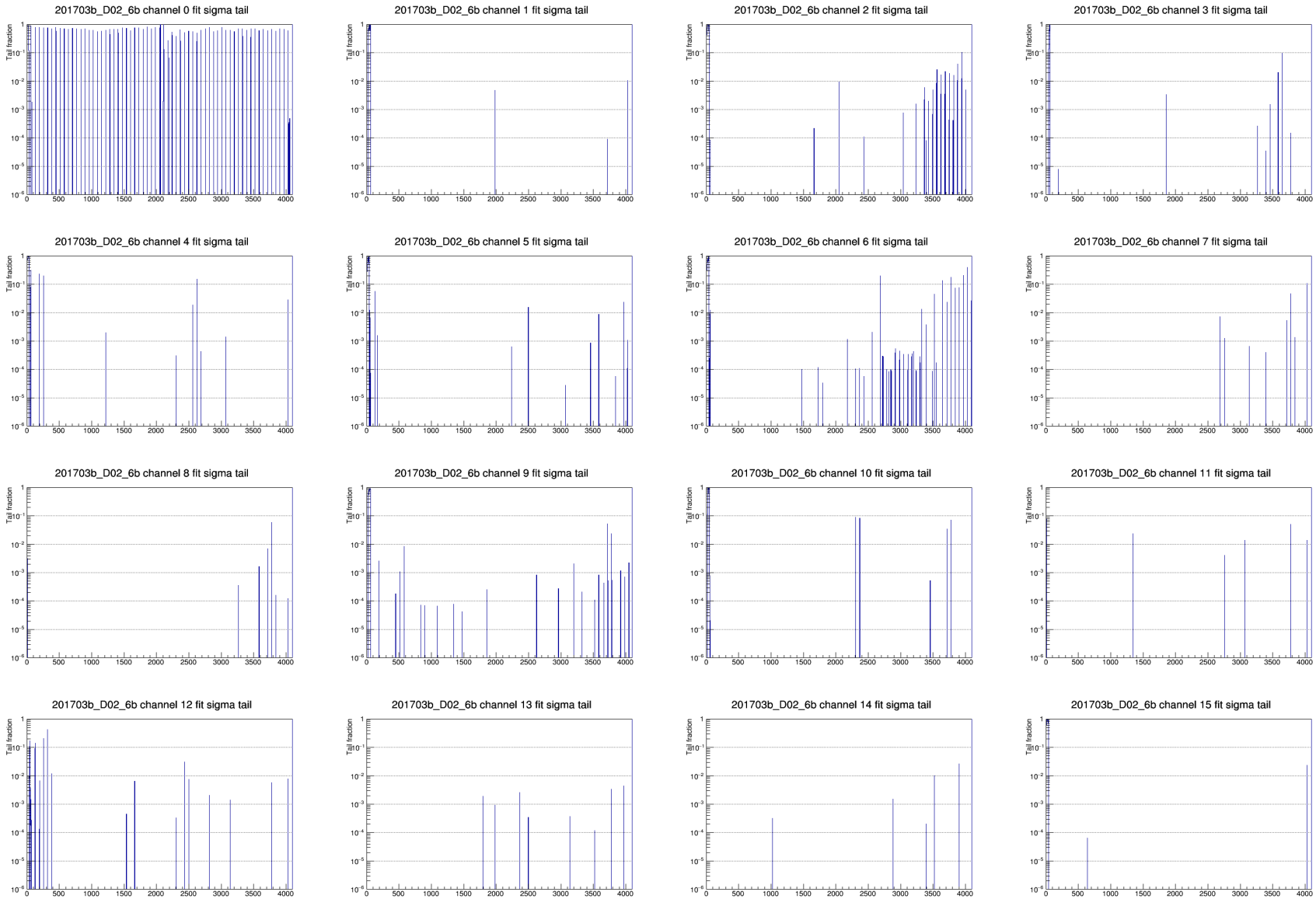

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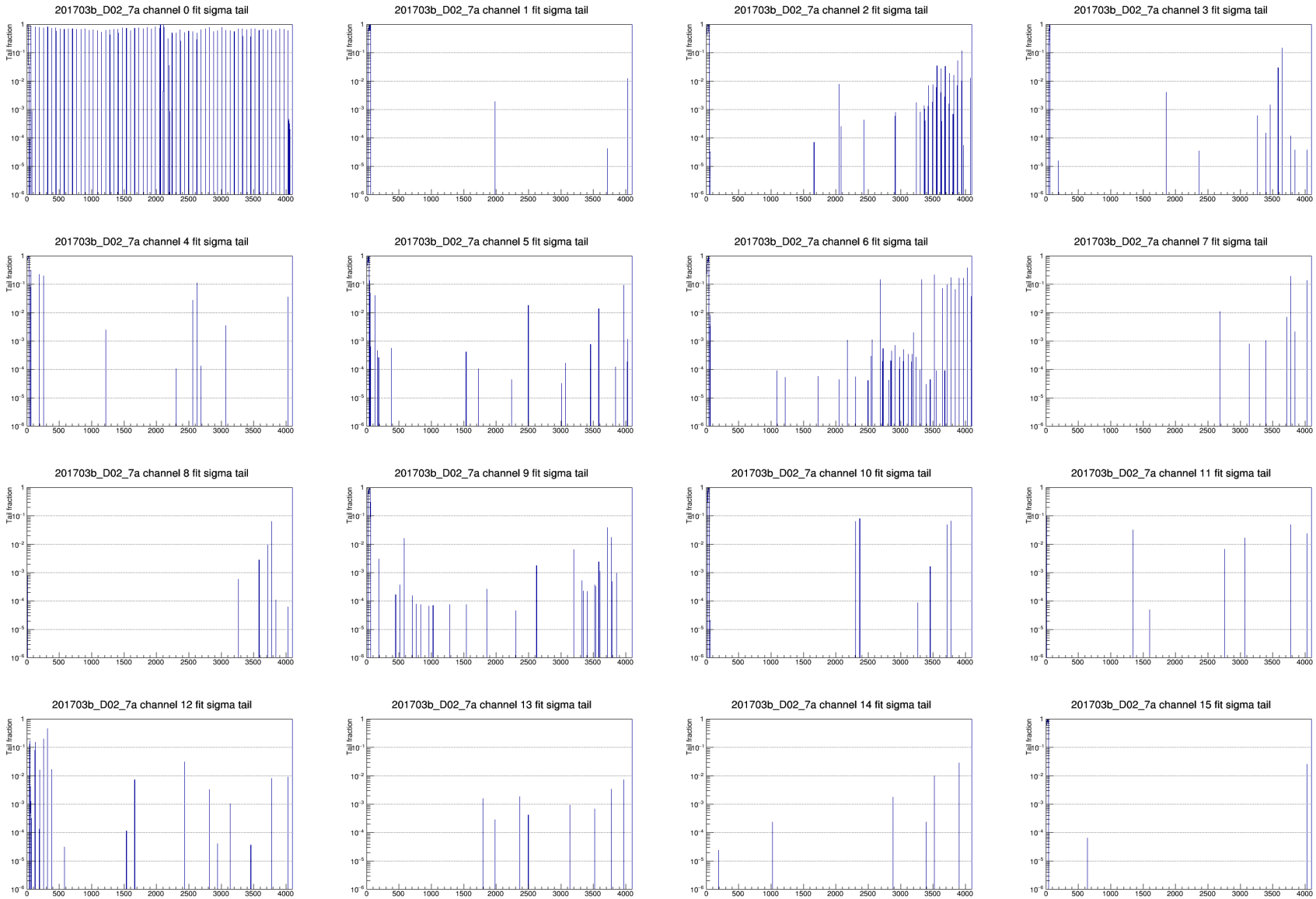
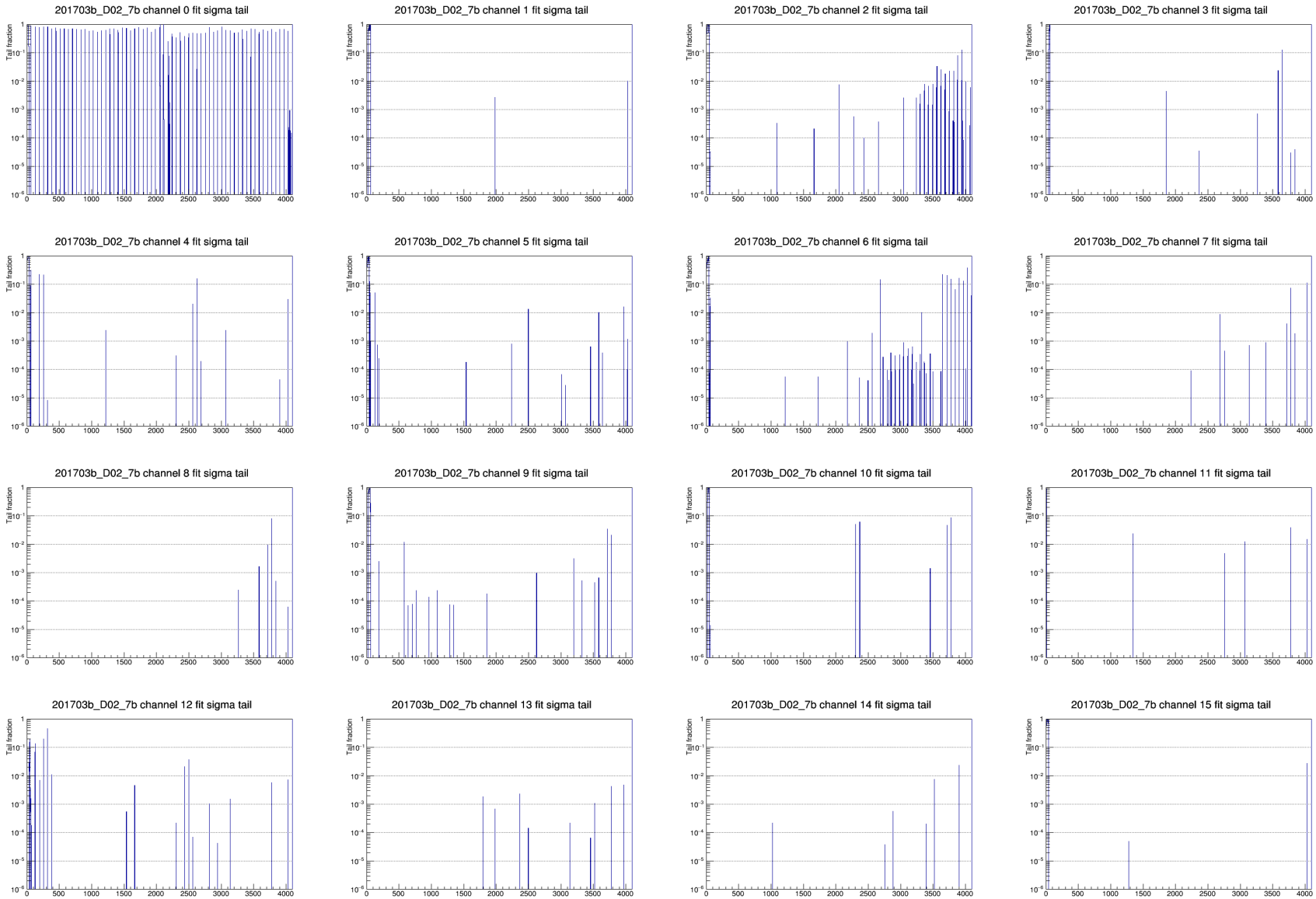


Tails: chip D02, time 7b



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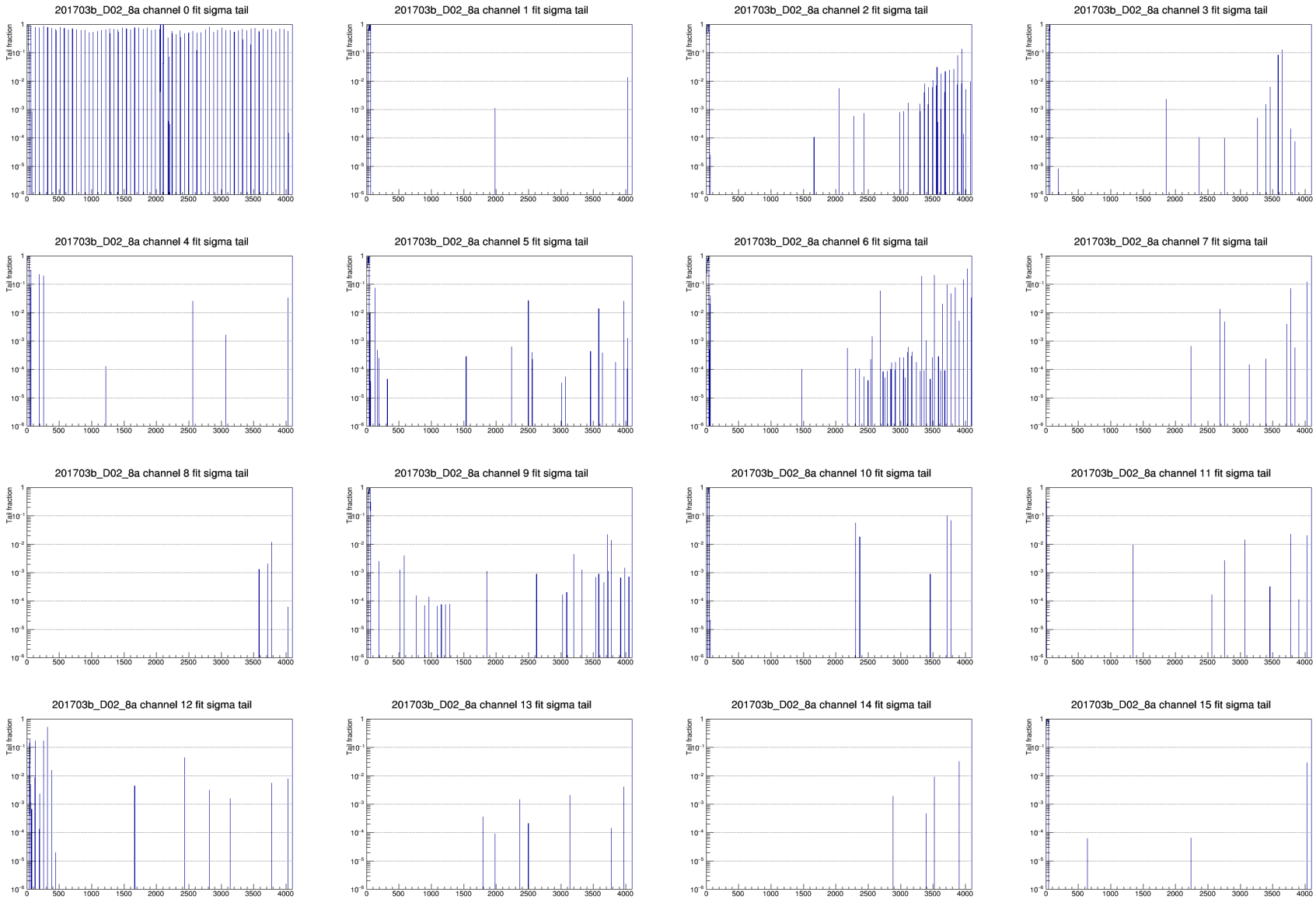

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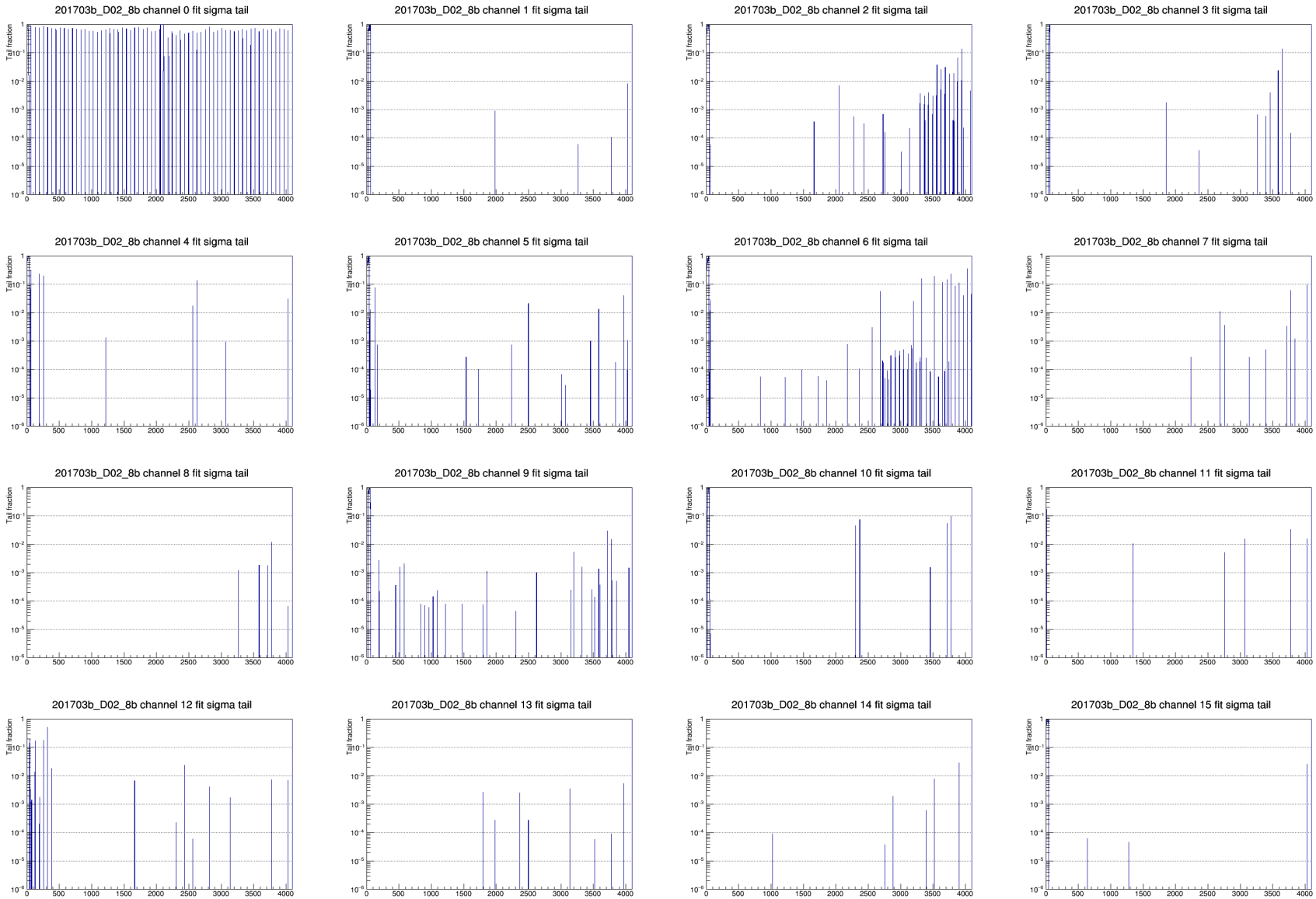

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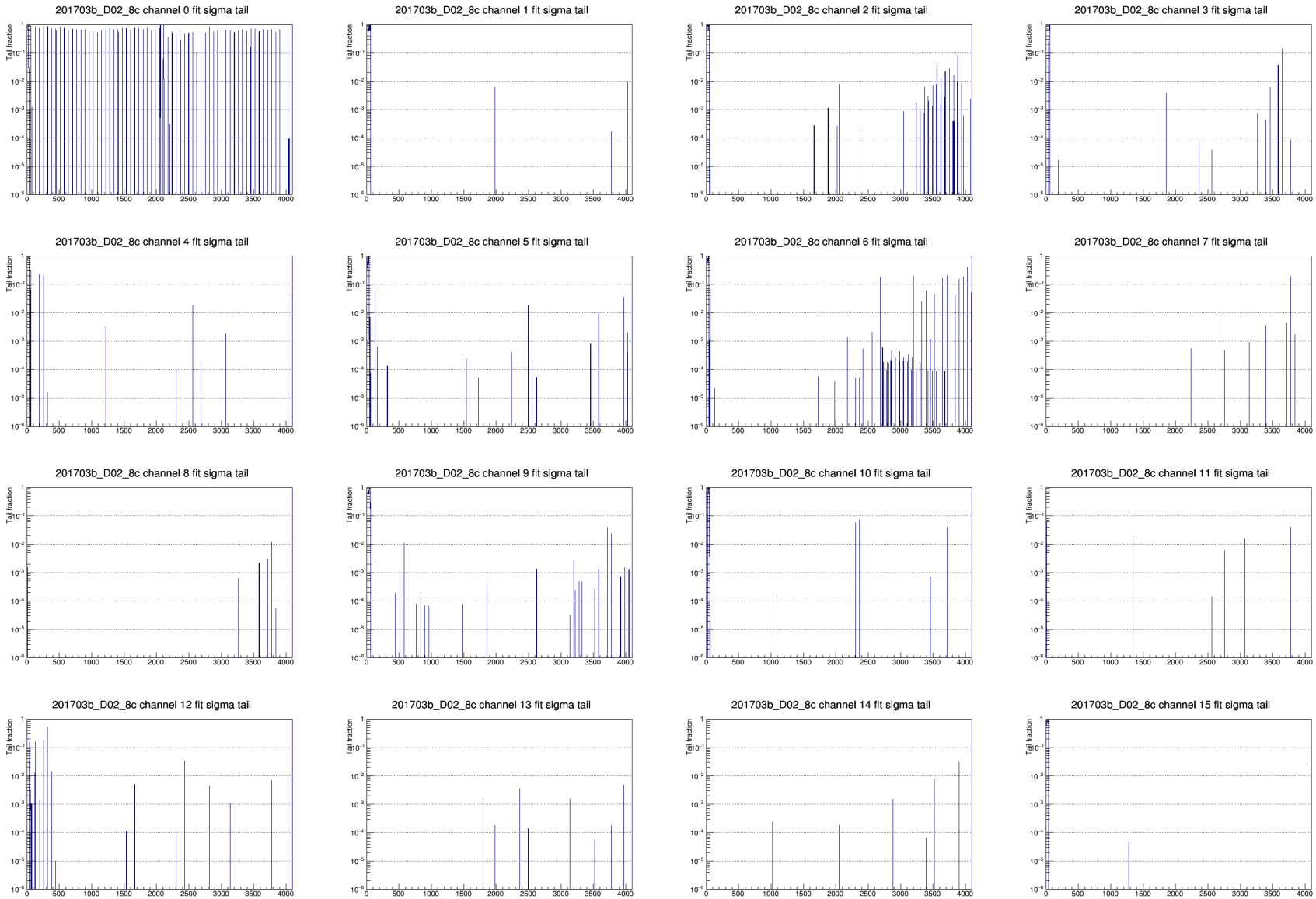
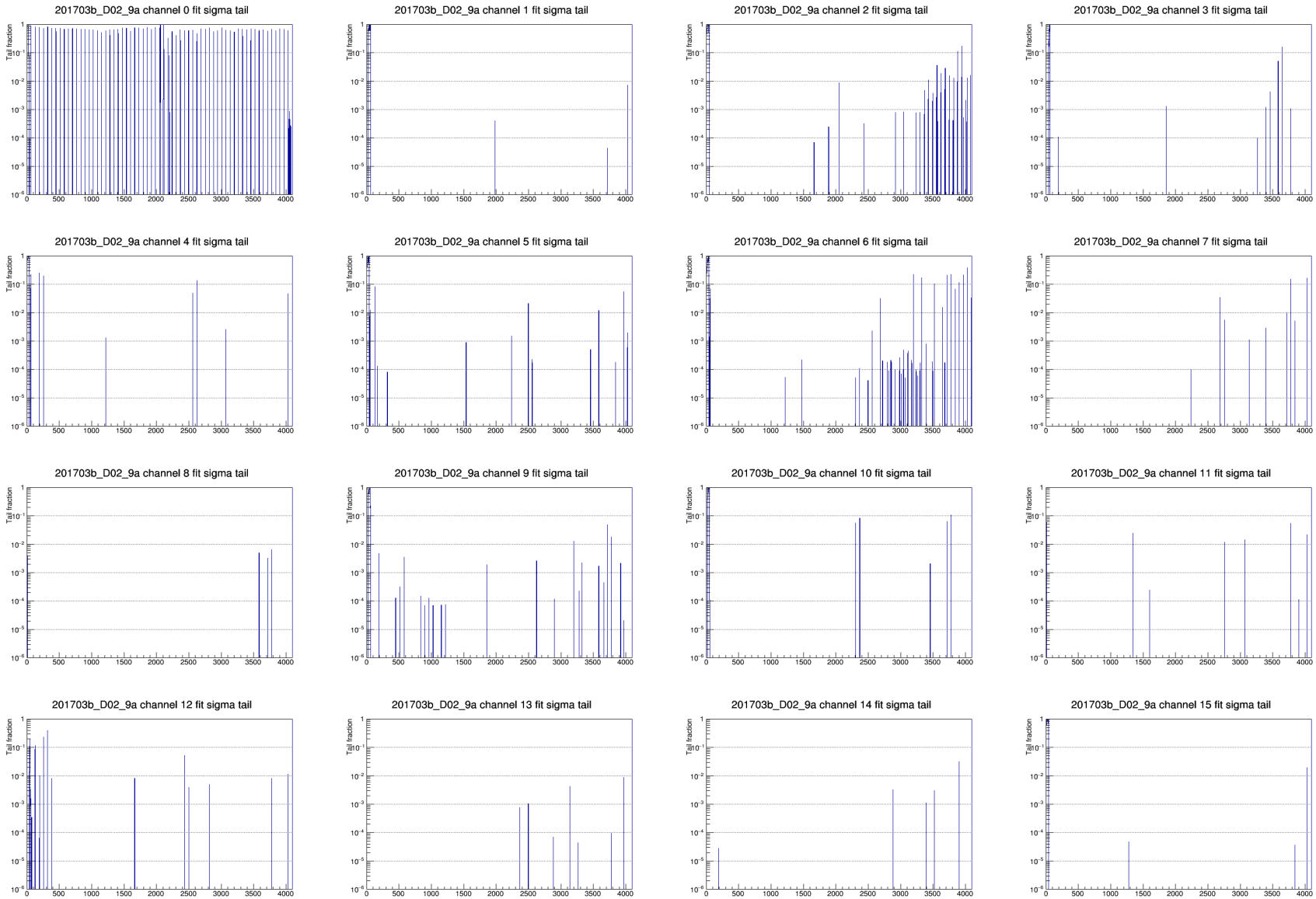


Tails: chip D02, time 9a



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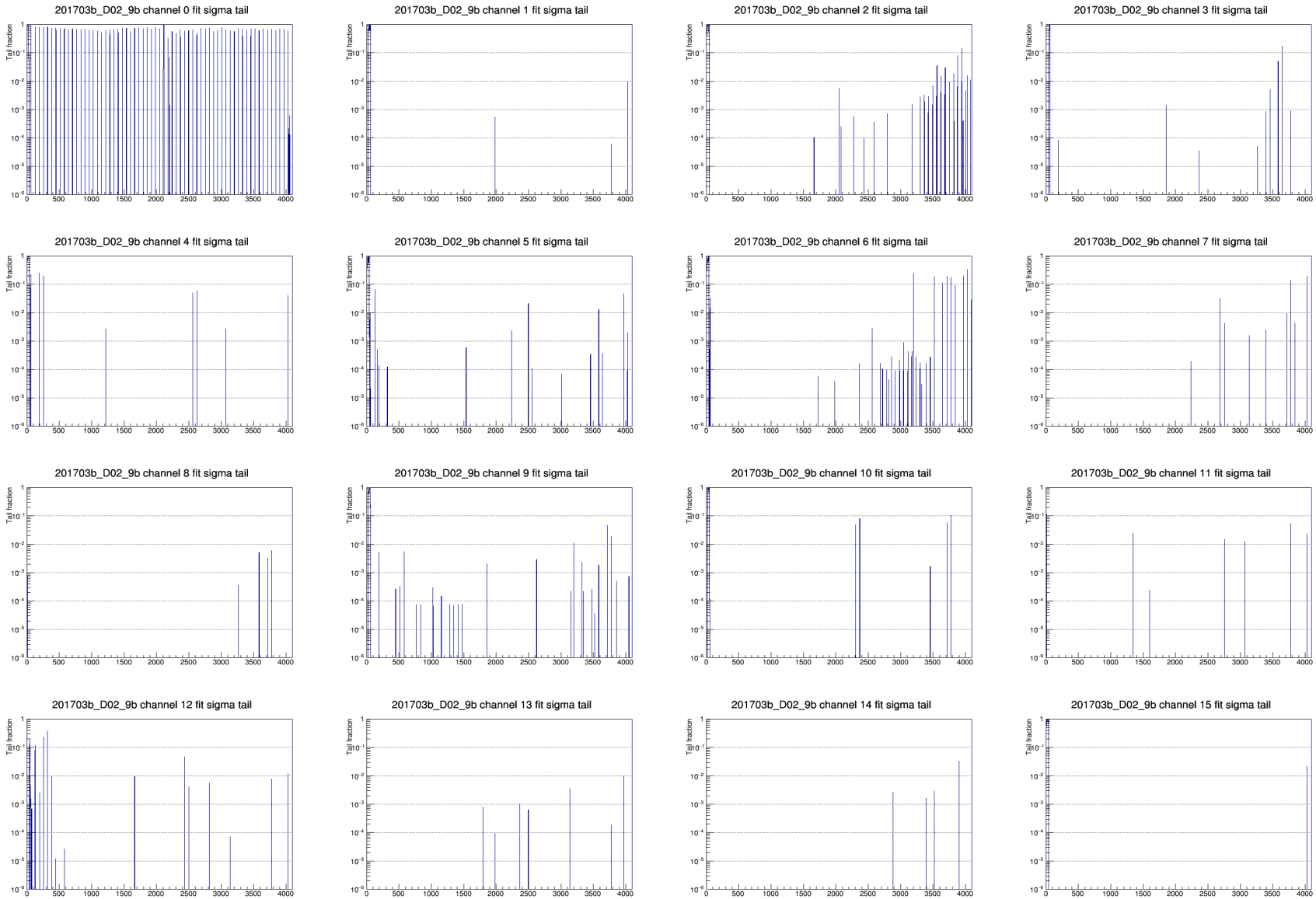

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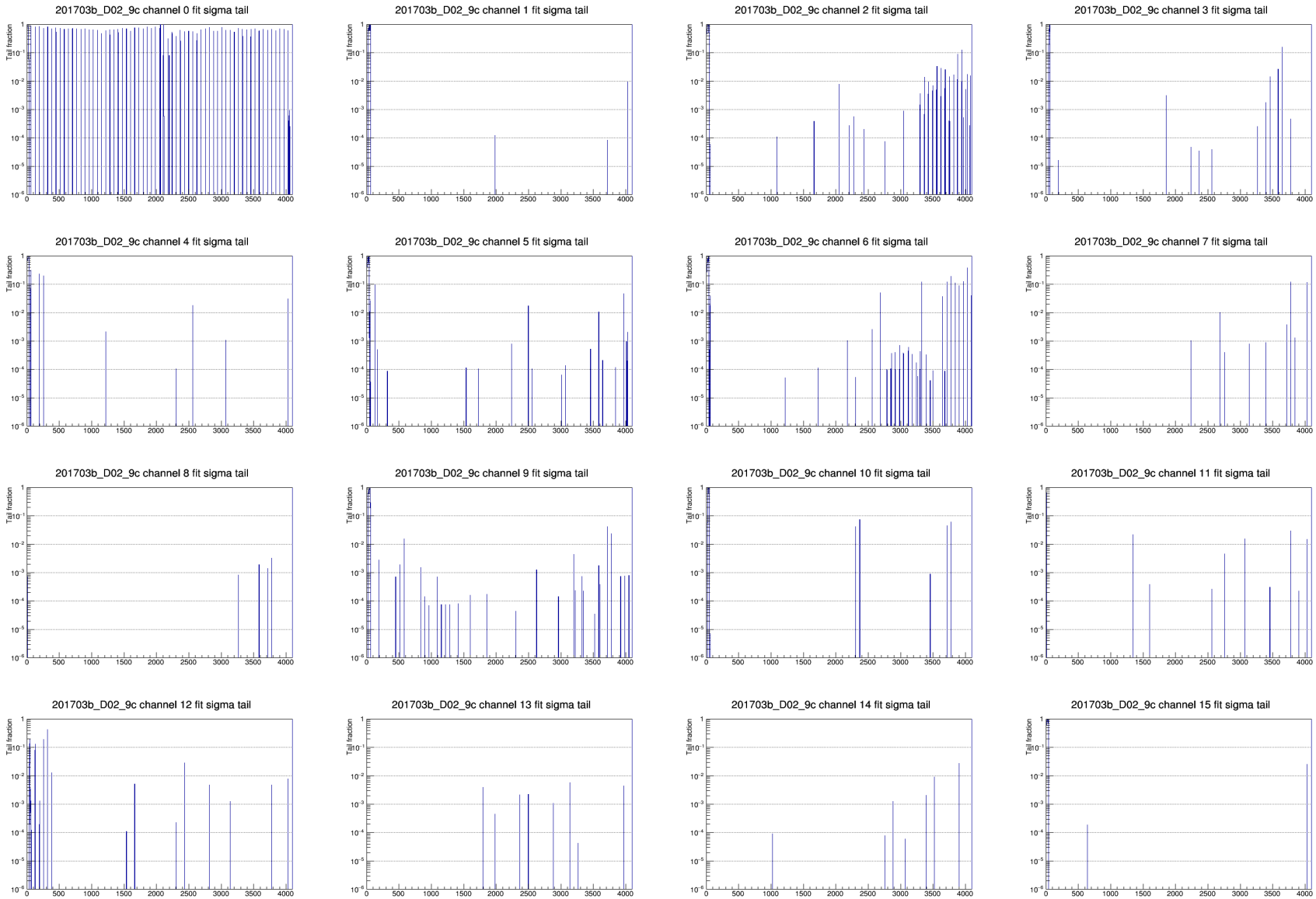
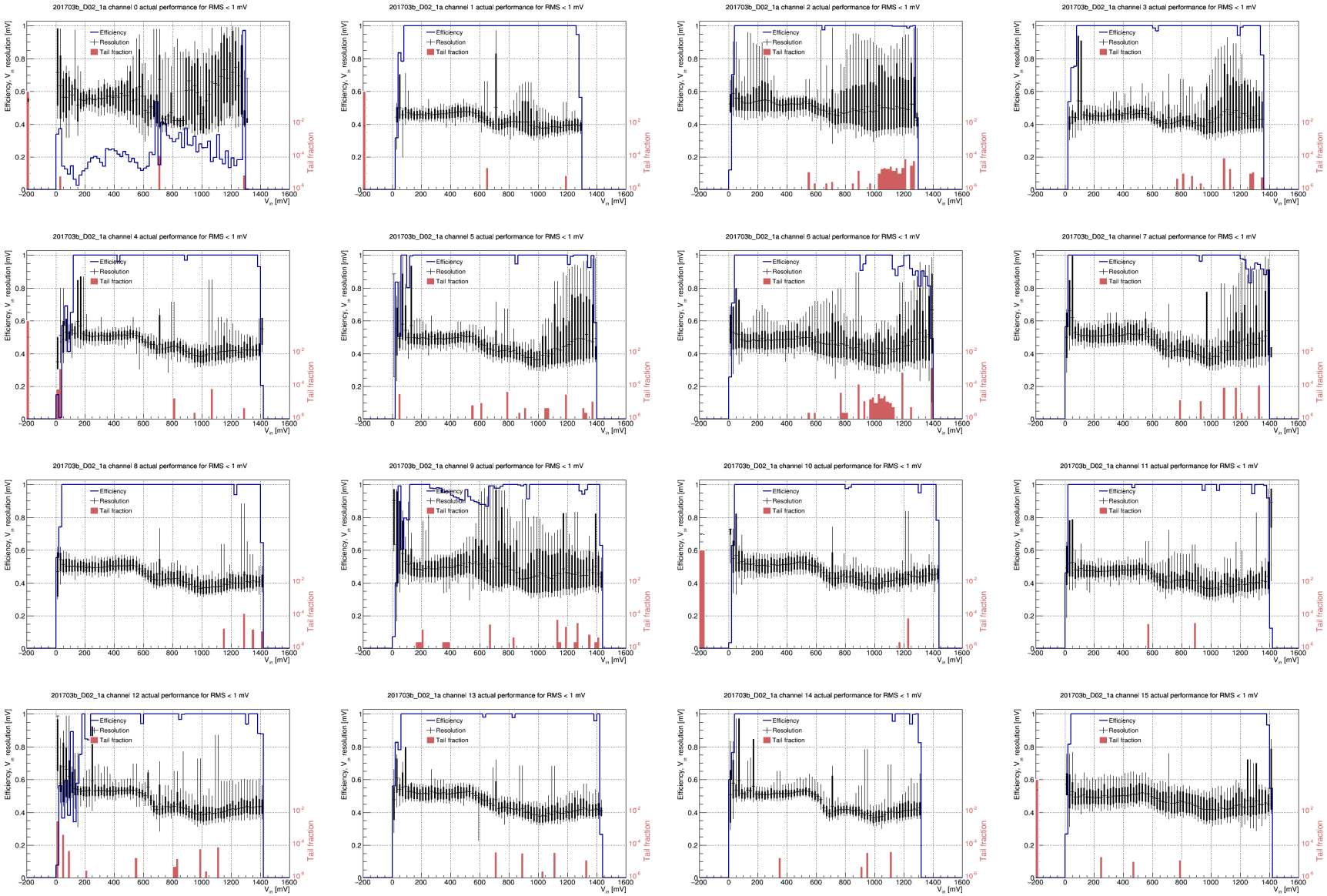
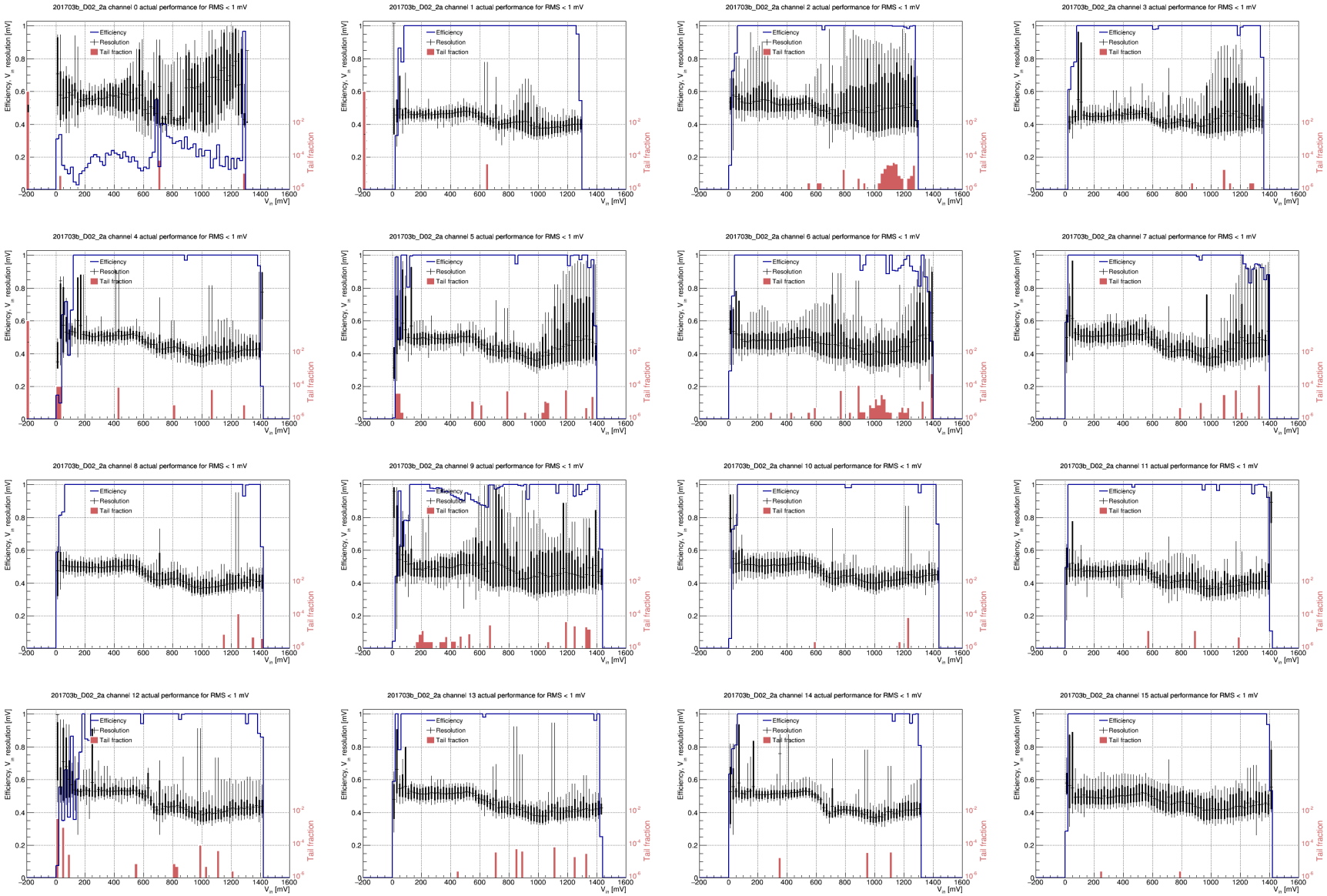


Performance

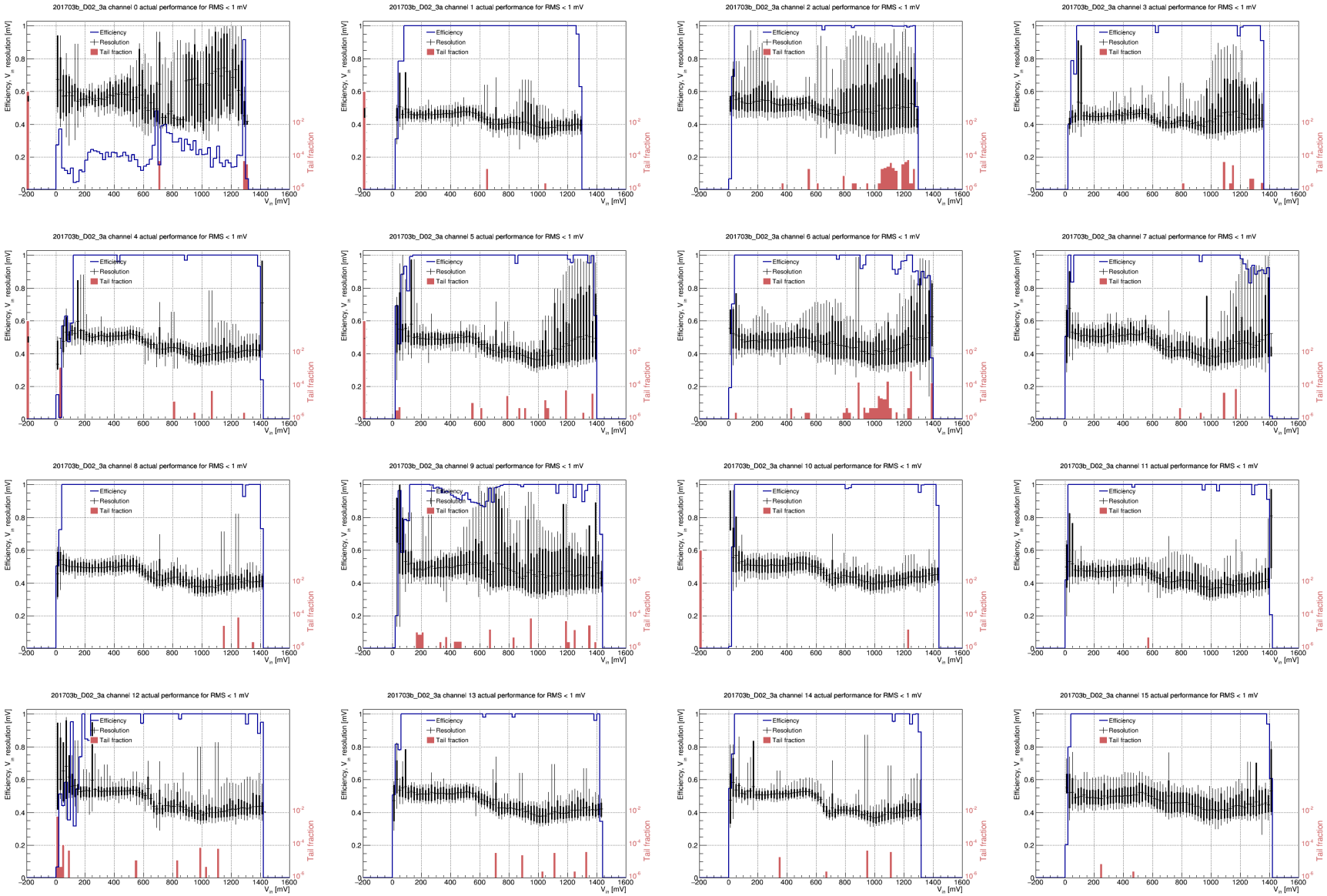
Performance: chip D02, time 1a



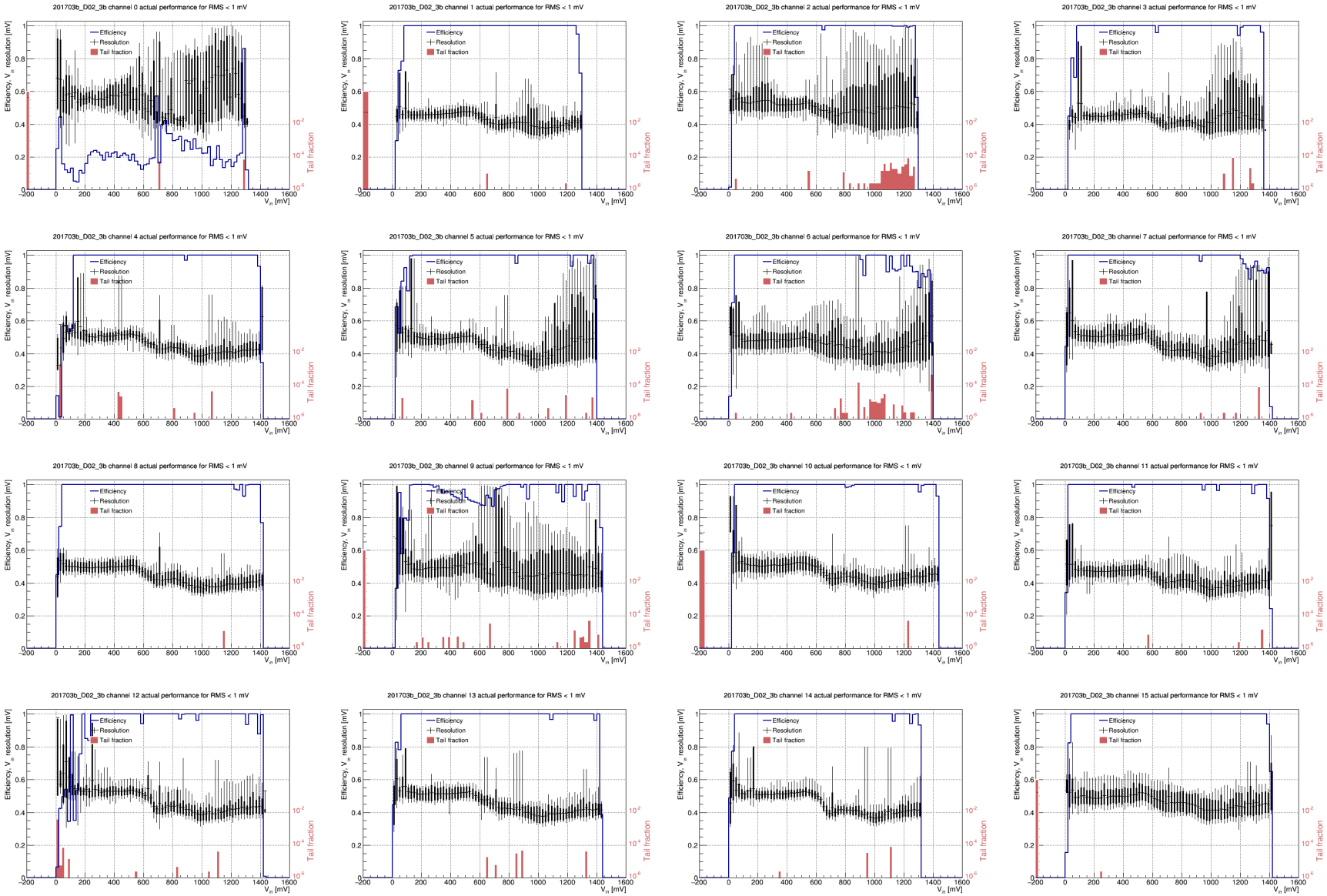
Performance: chip D02, time 2a



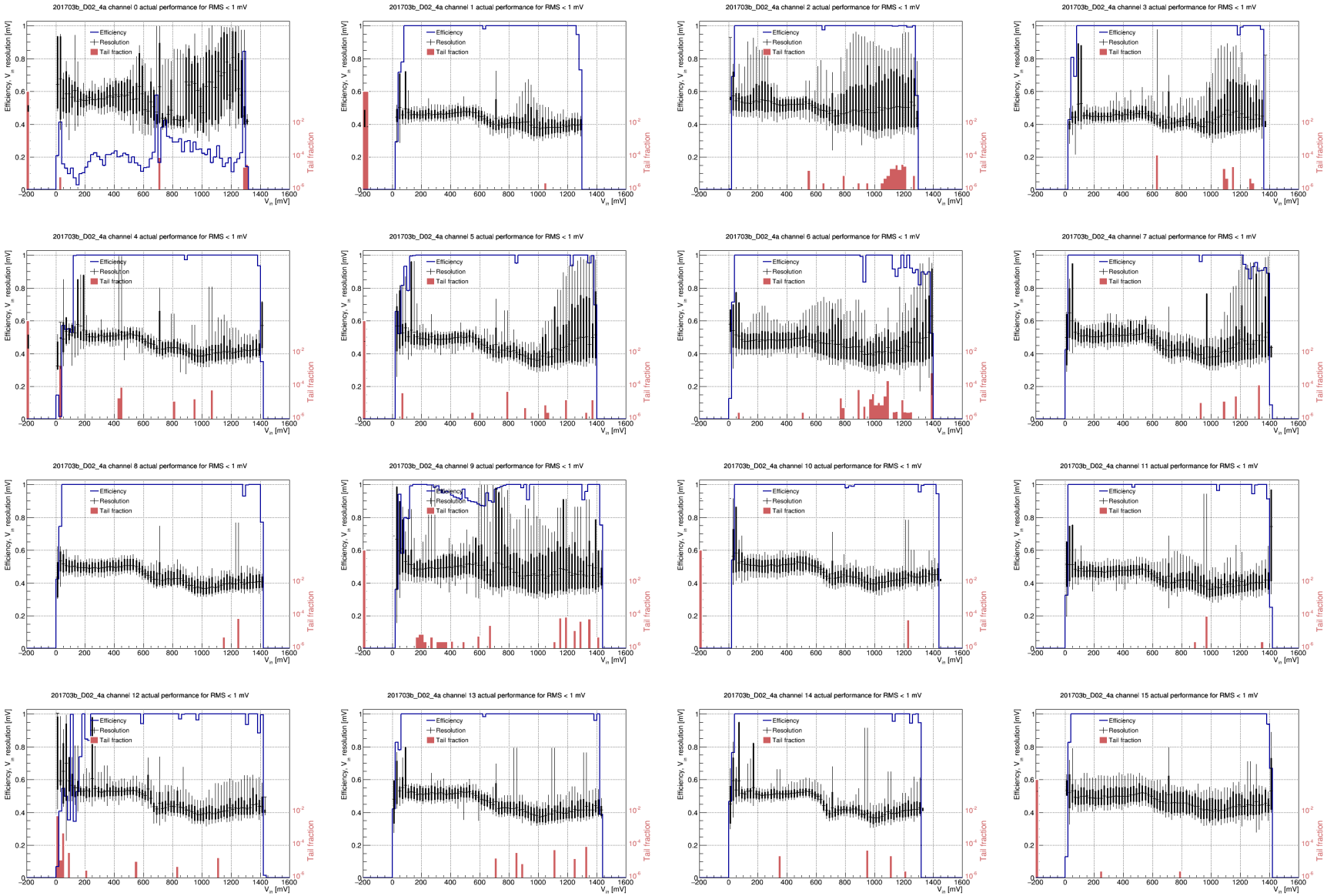
Performance: chip D02, time 3a



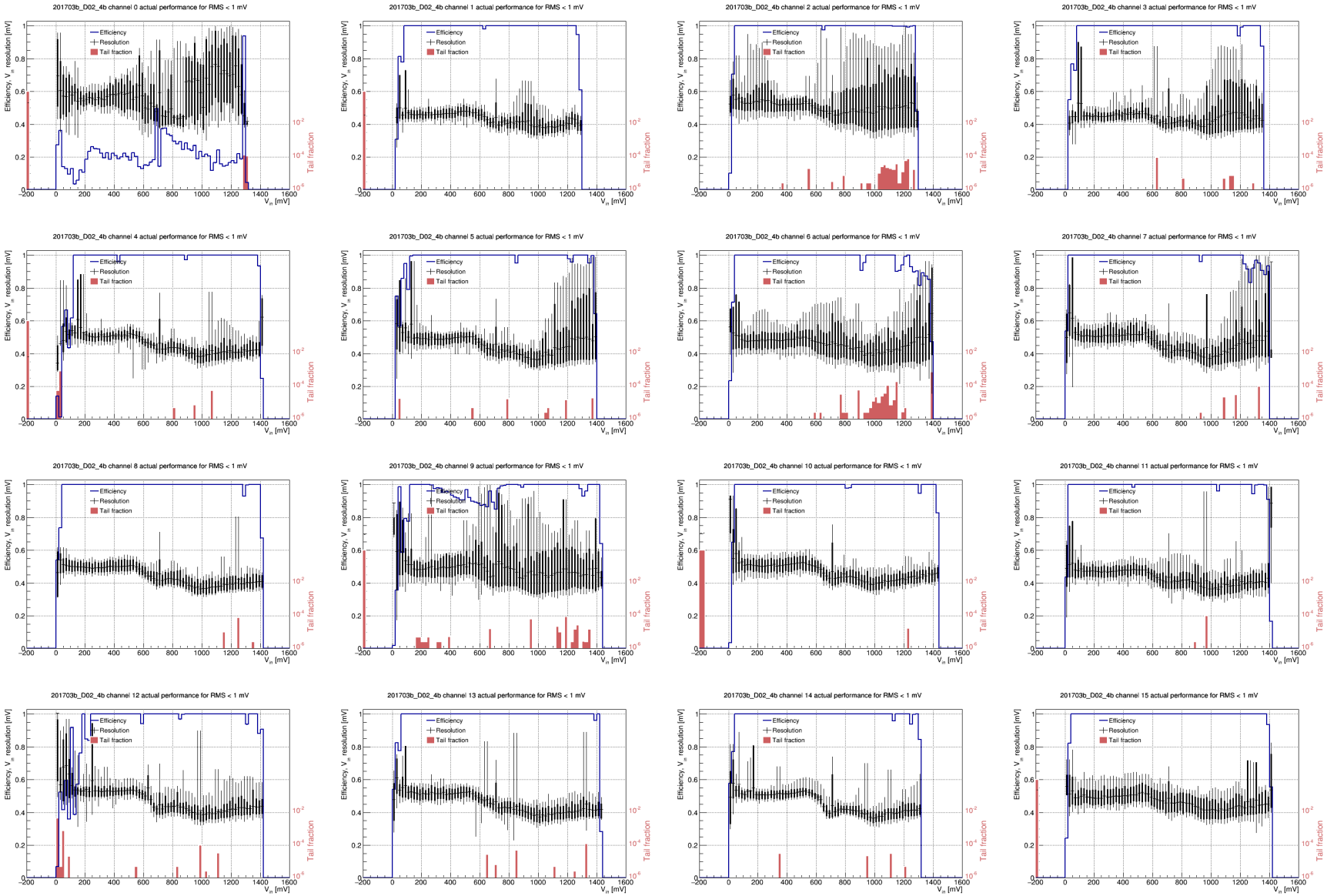
Performance: chip D02, time 3b



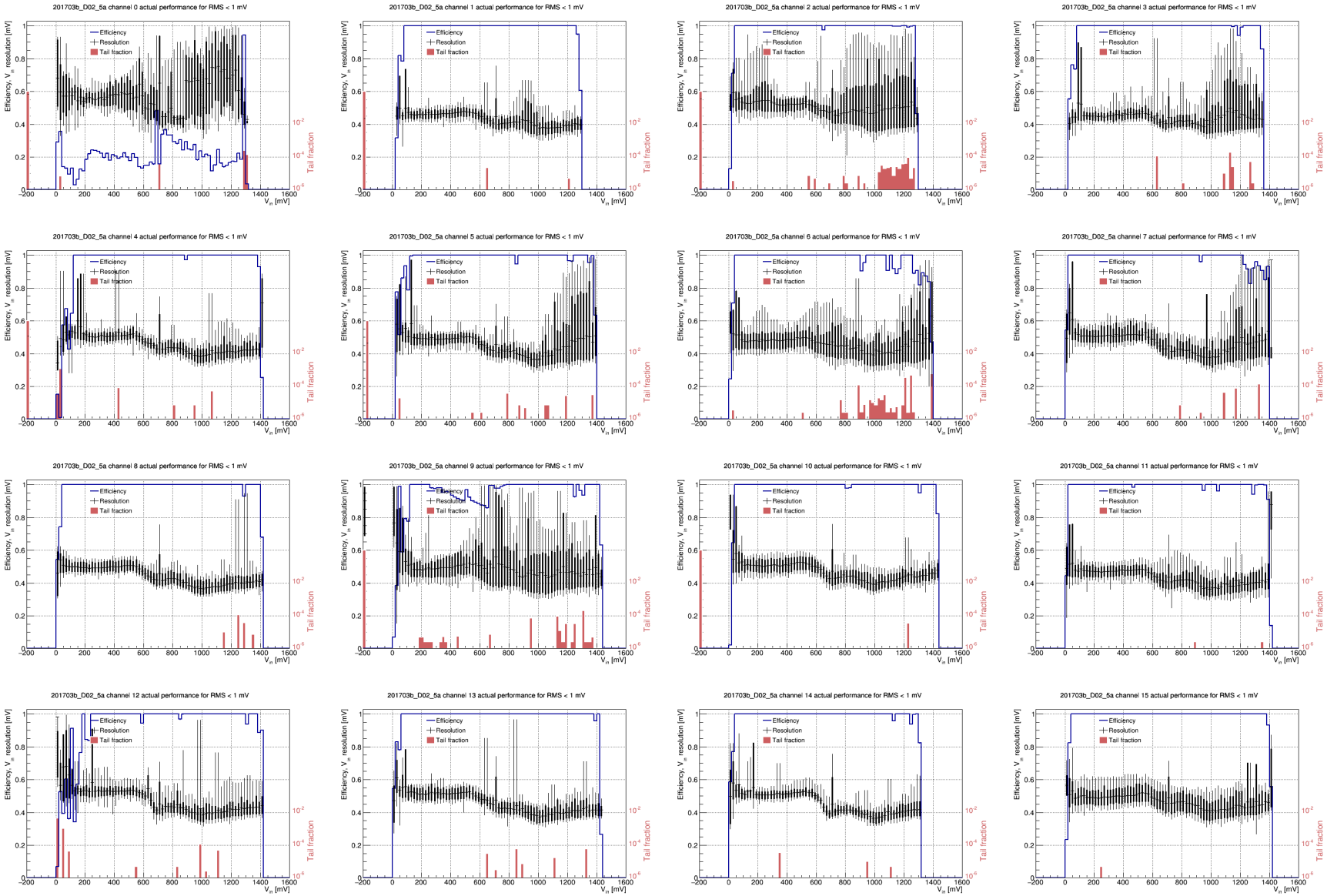
Performance: chip D02, time 4a



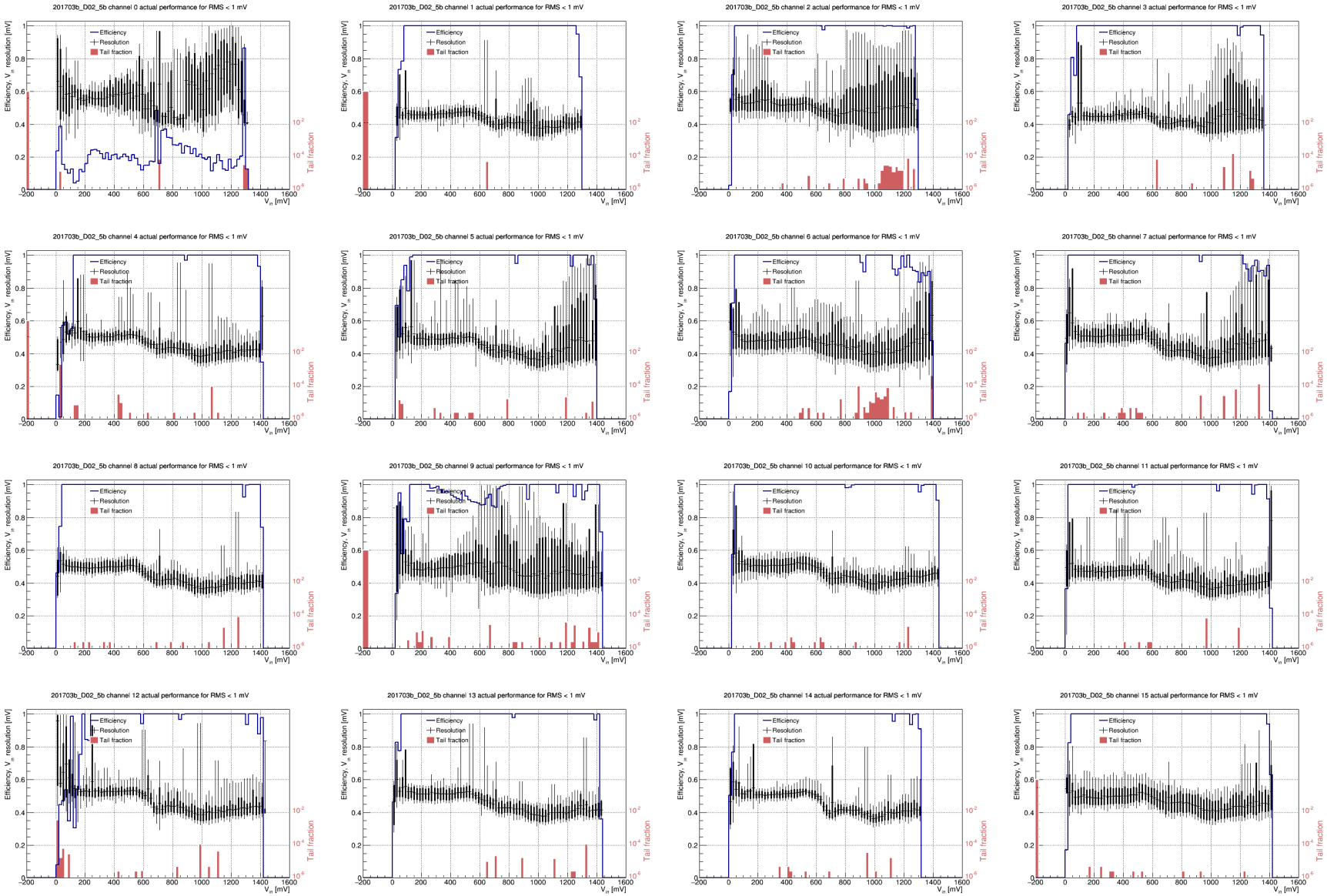
Performance: chip D02, time 4b



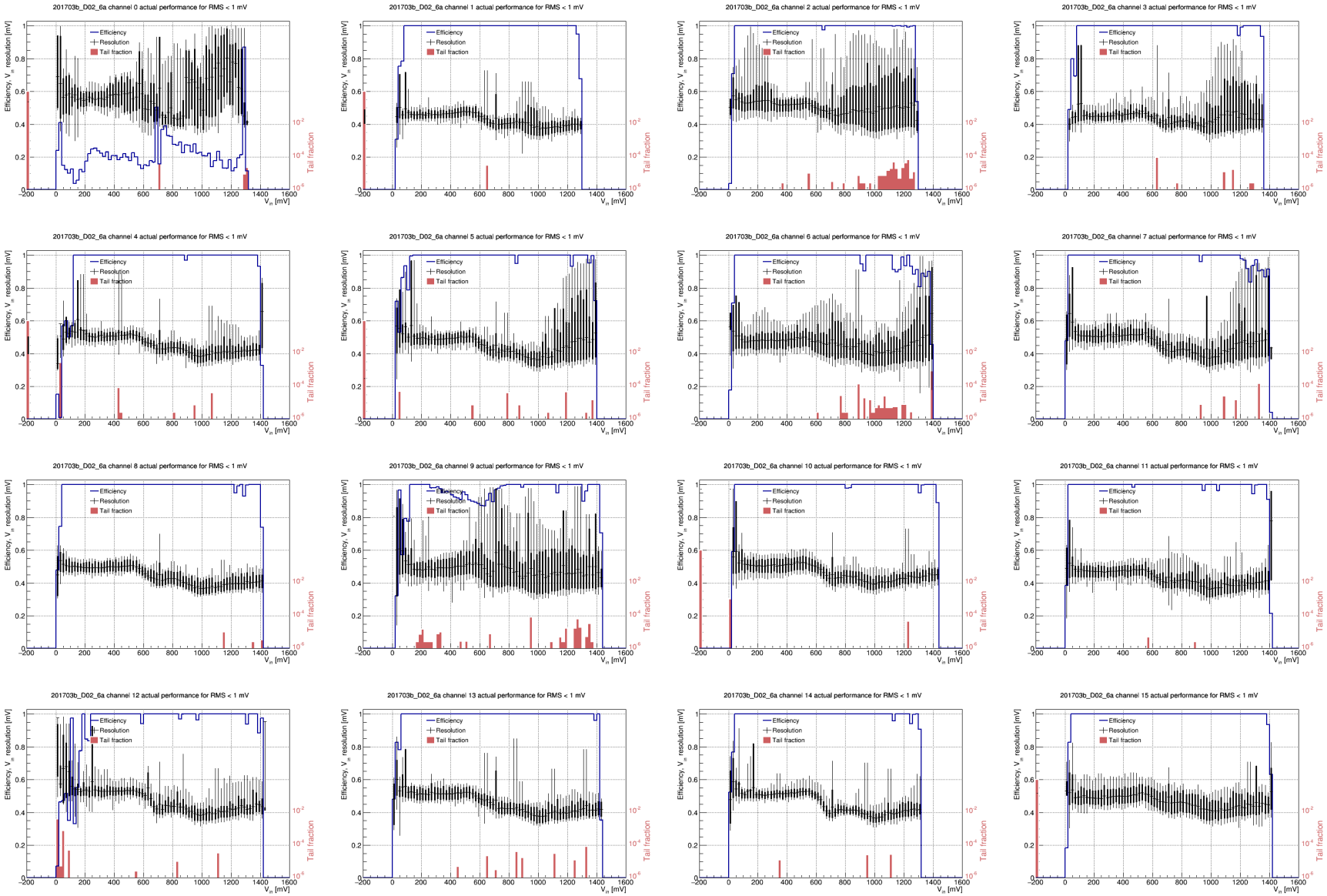
Performance: chip D02, time 5a



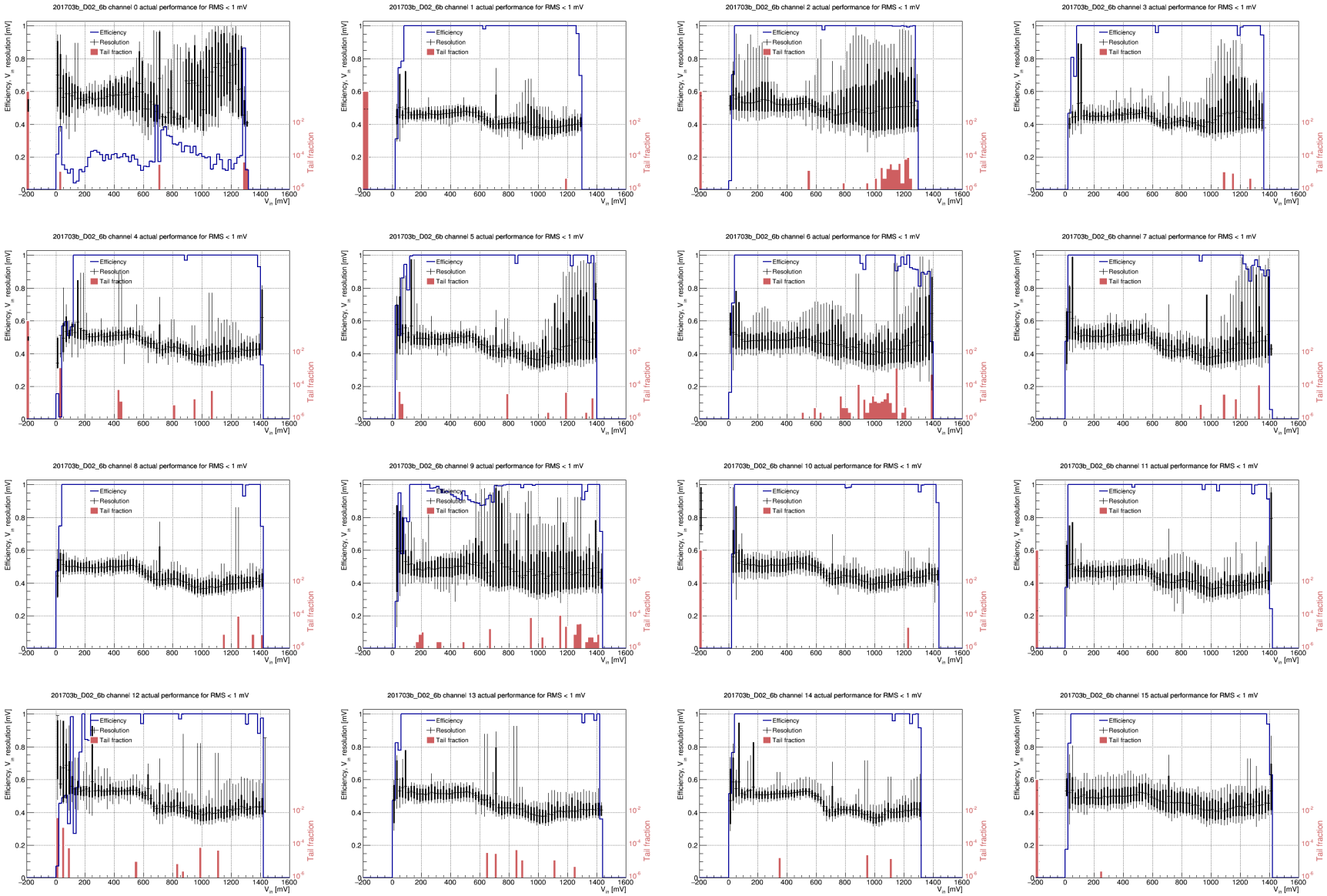
Performance: chip D02, time 5b



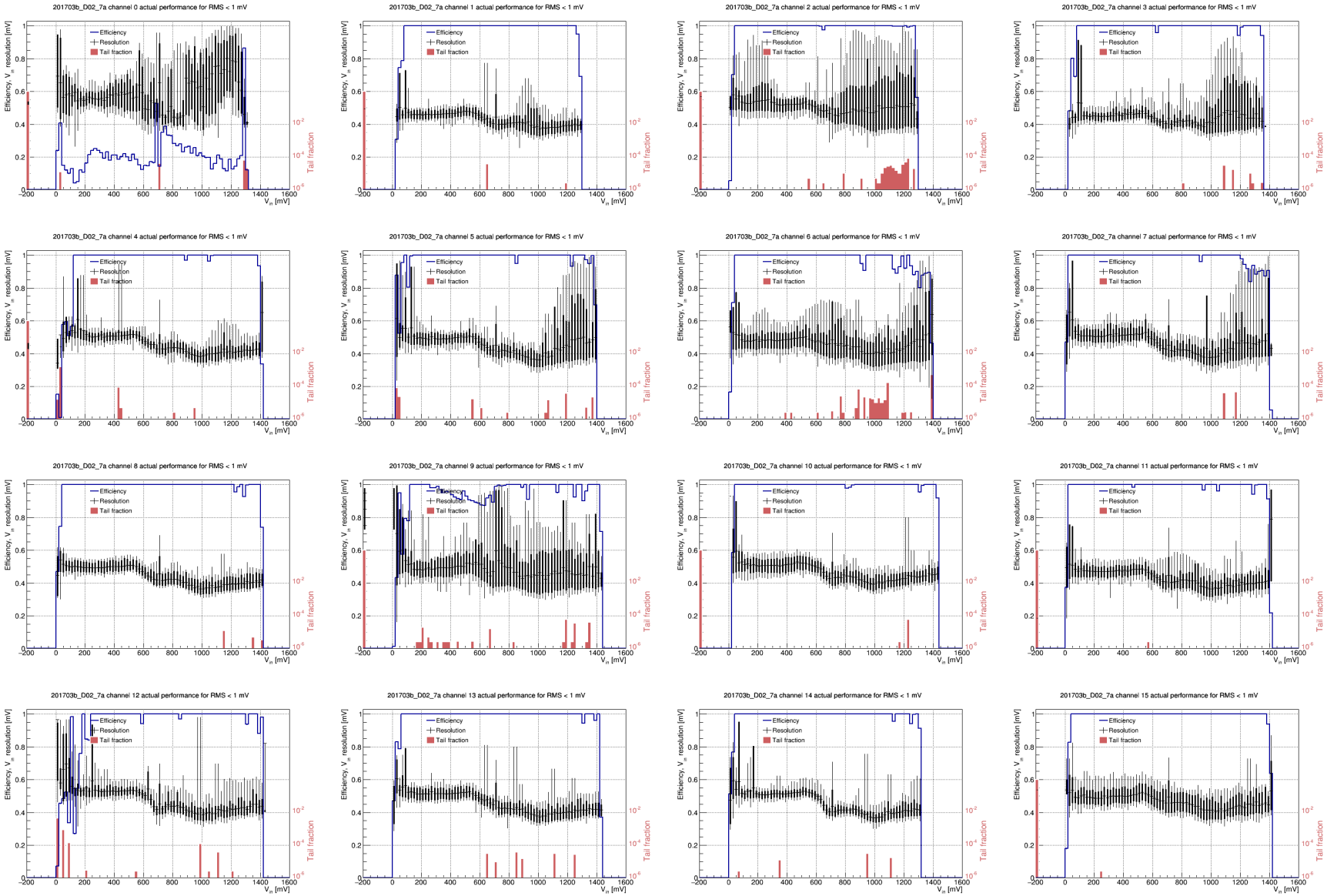
Performance: chip D02, time 6a



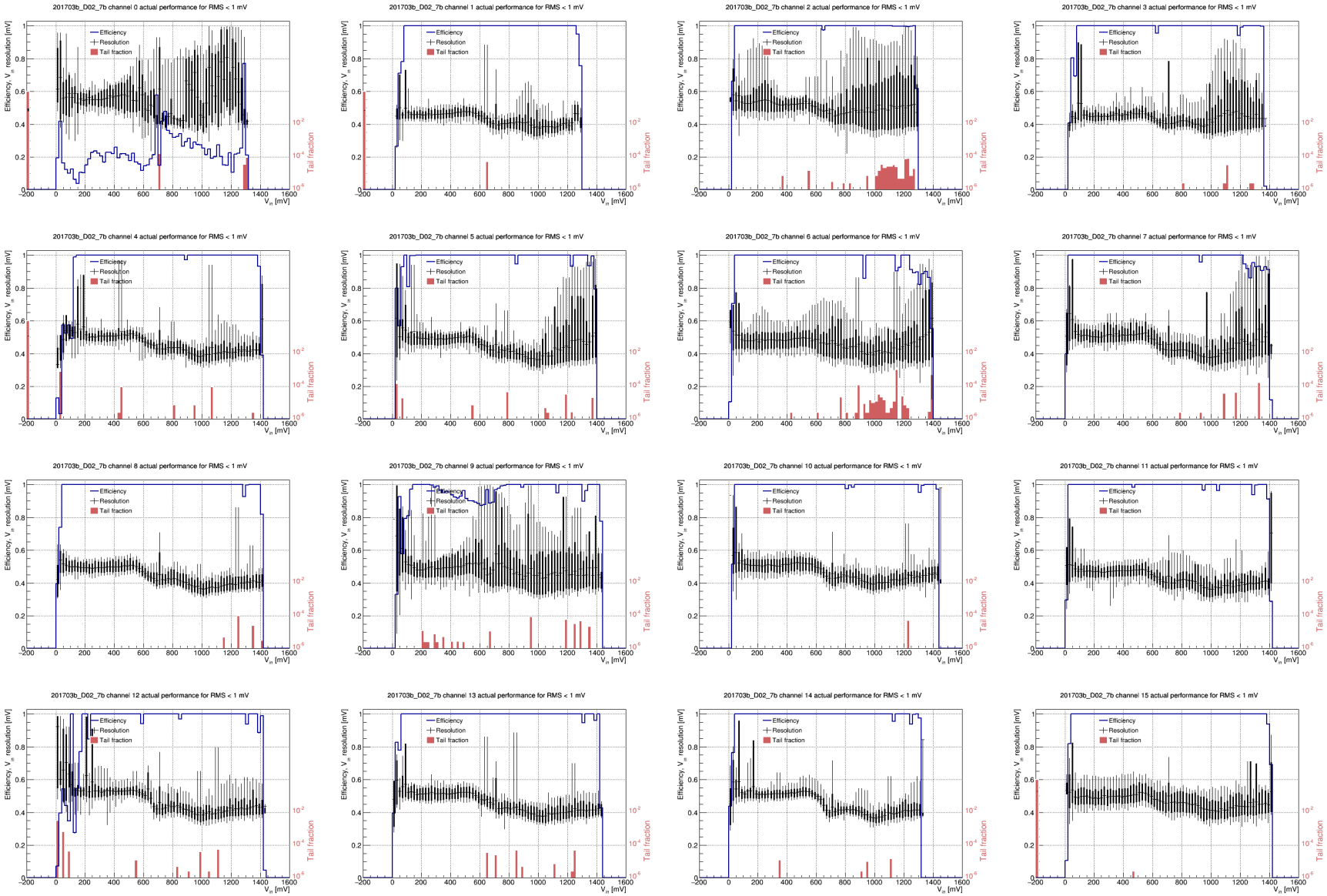
Performance: chip D02, time 6b



Performance: chip D02, time 7a



Performance: chip D02, time 7b



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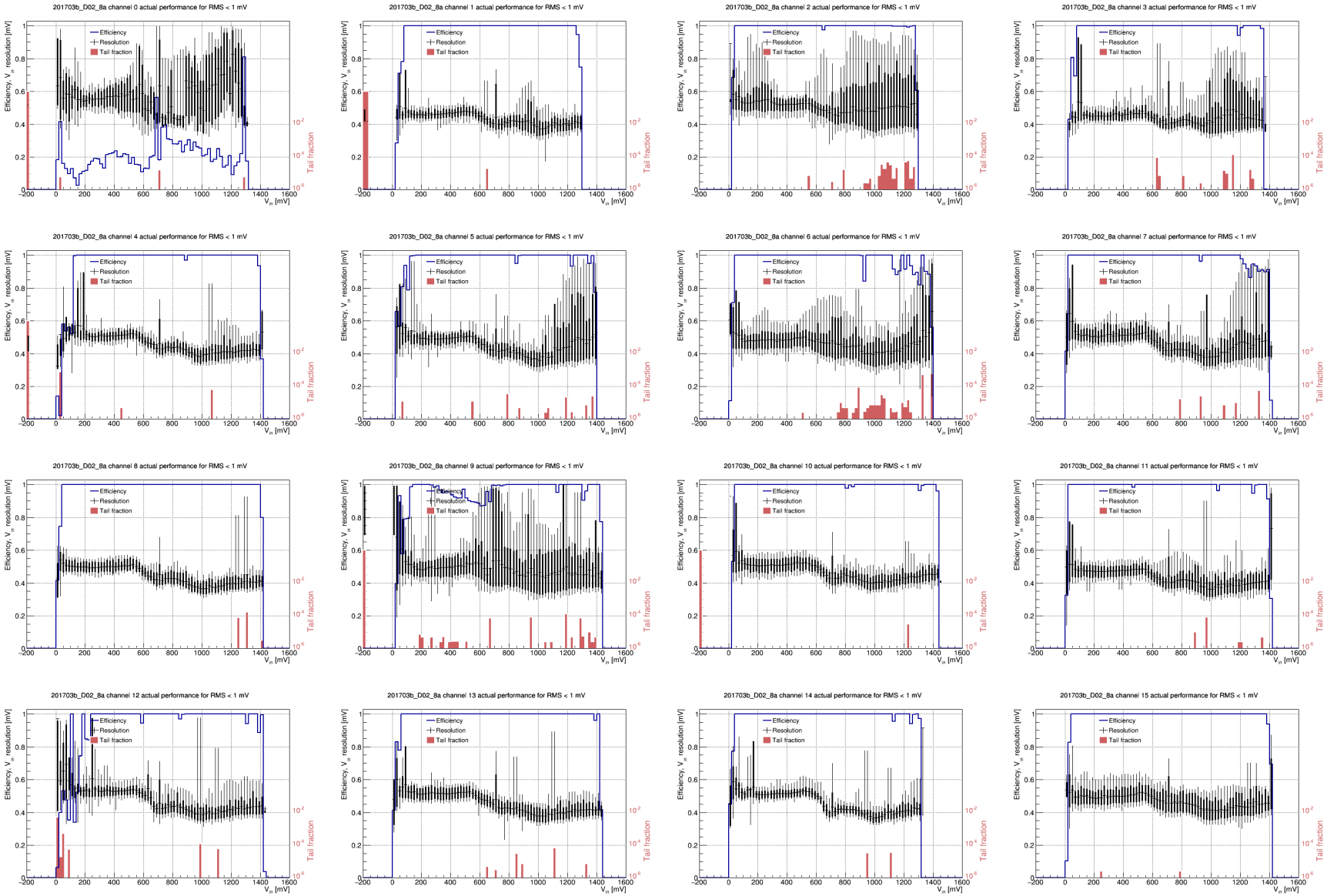

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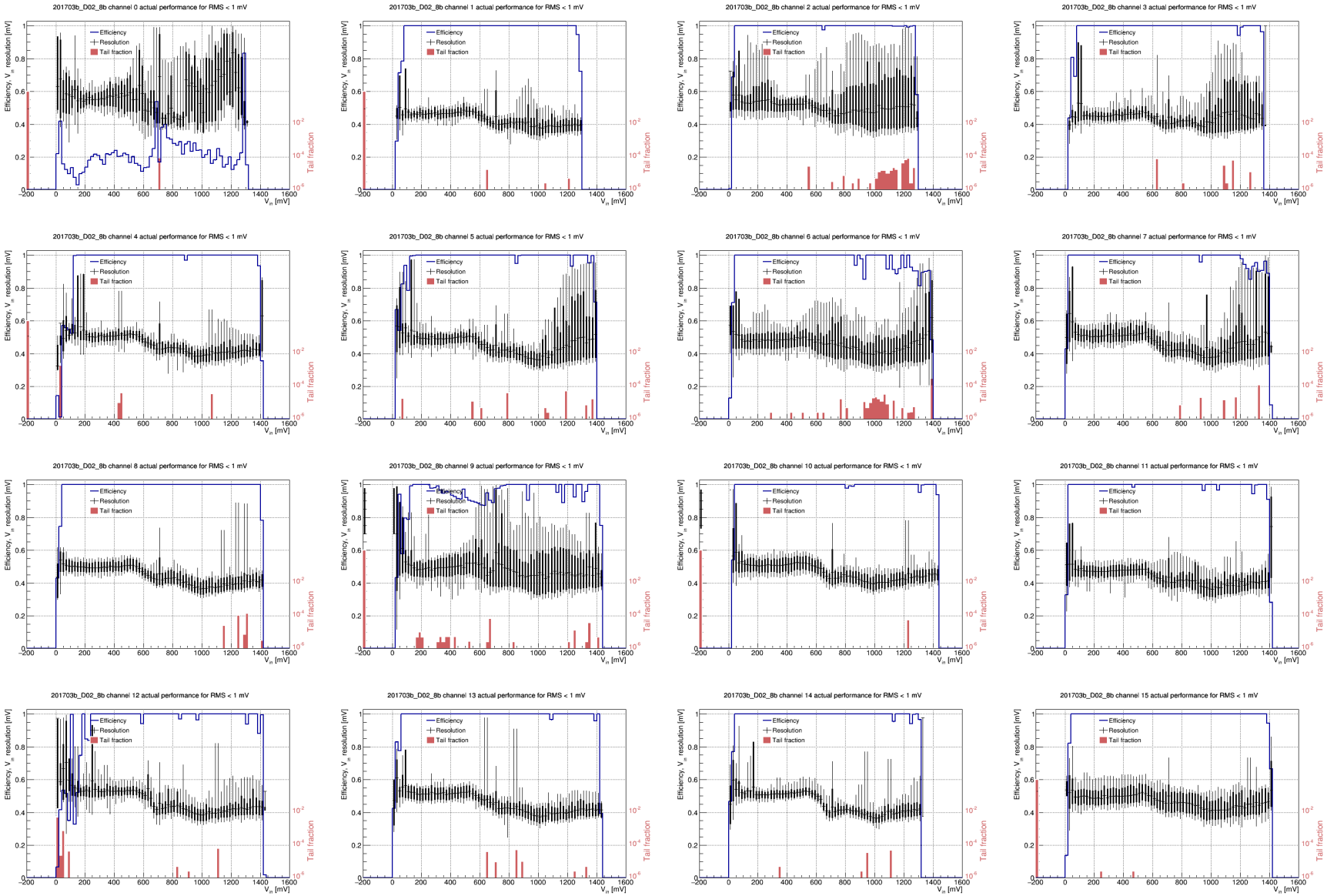

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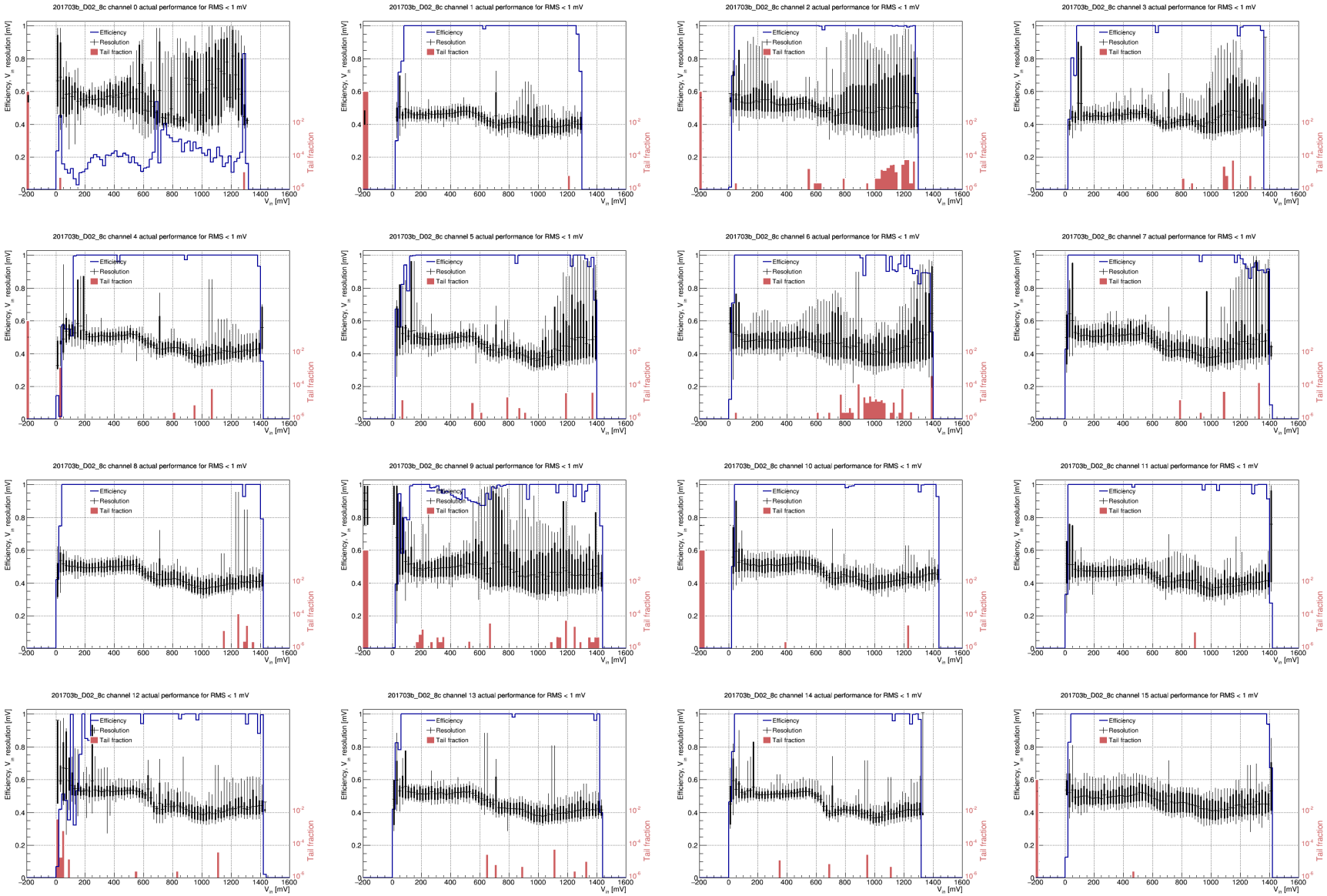
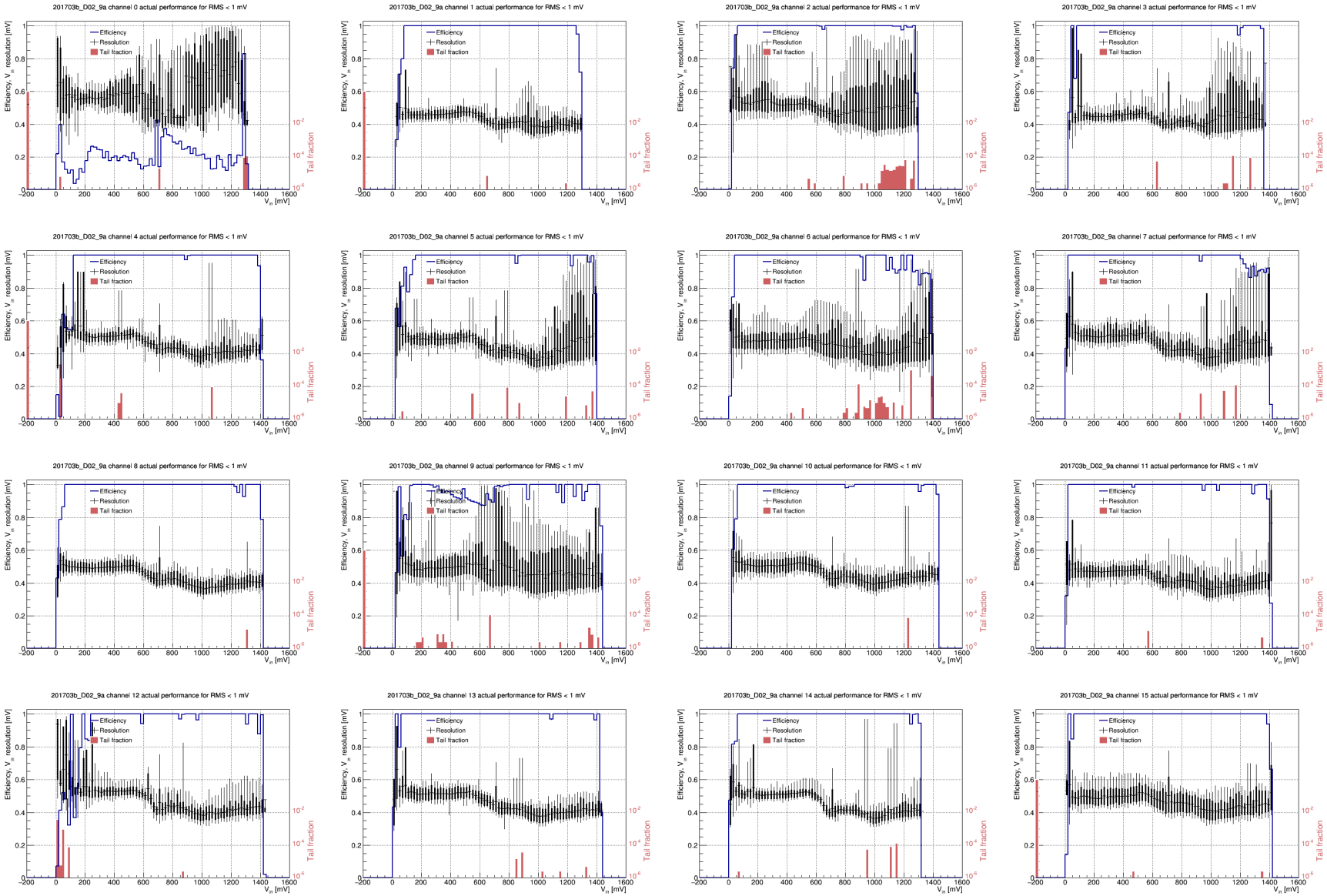
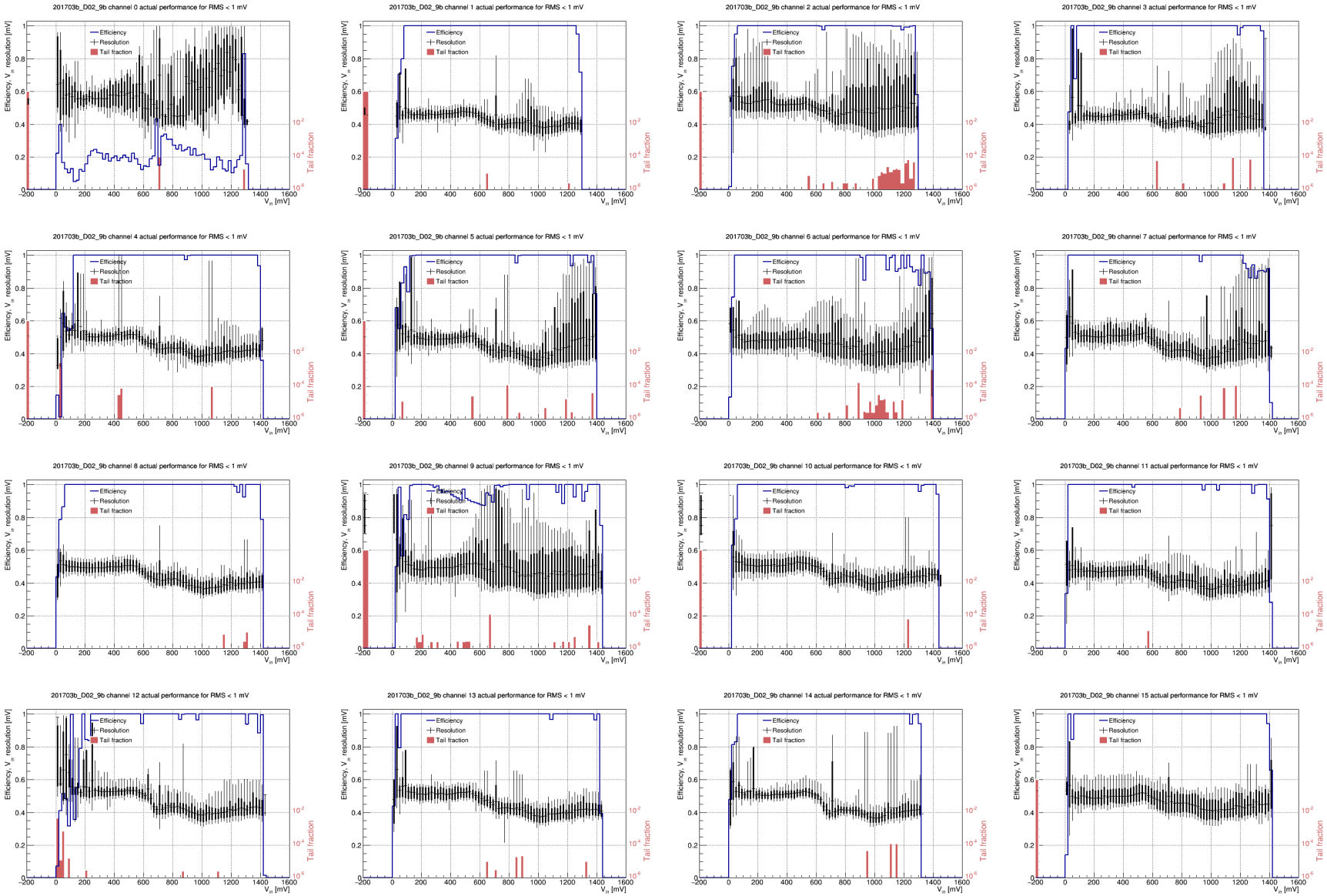


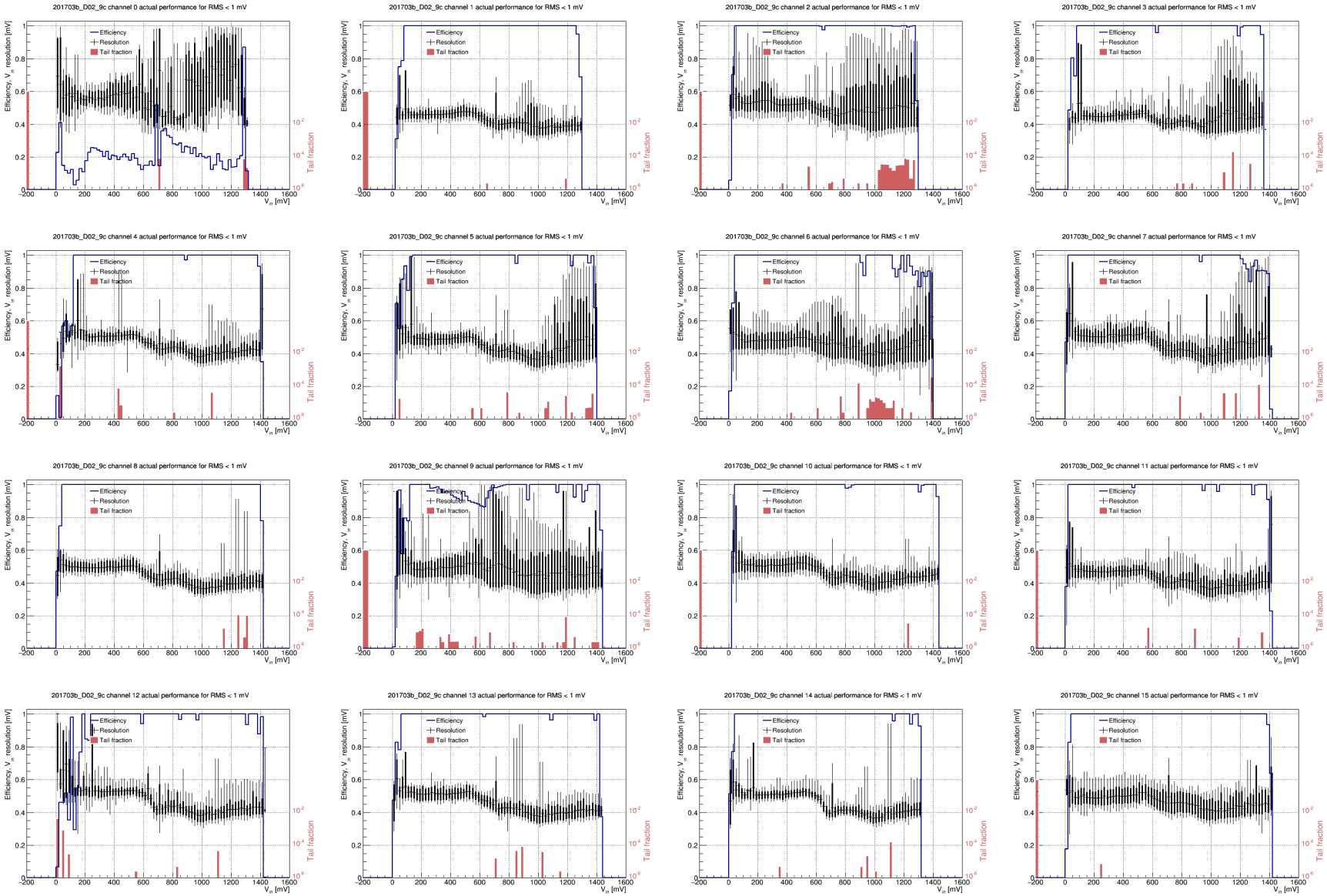
Performance: chip D02, time 9a



Performance: chip D02, time 9b

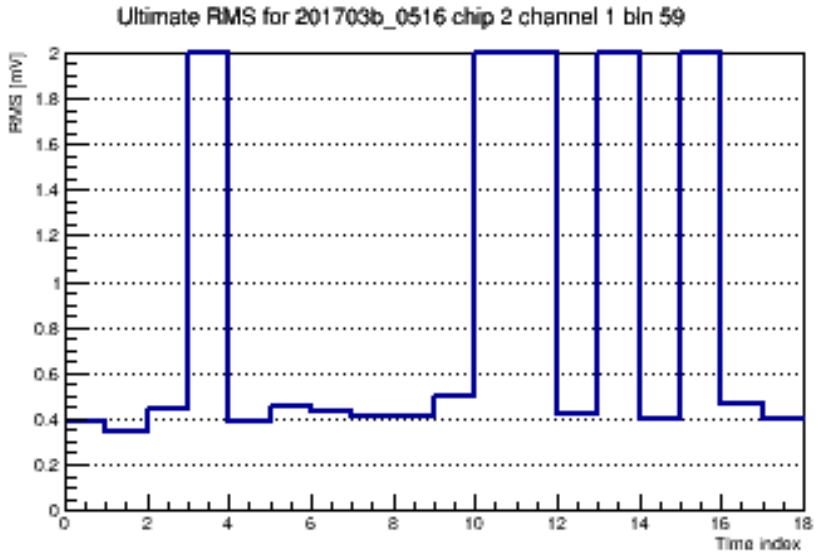


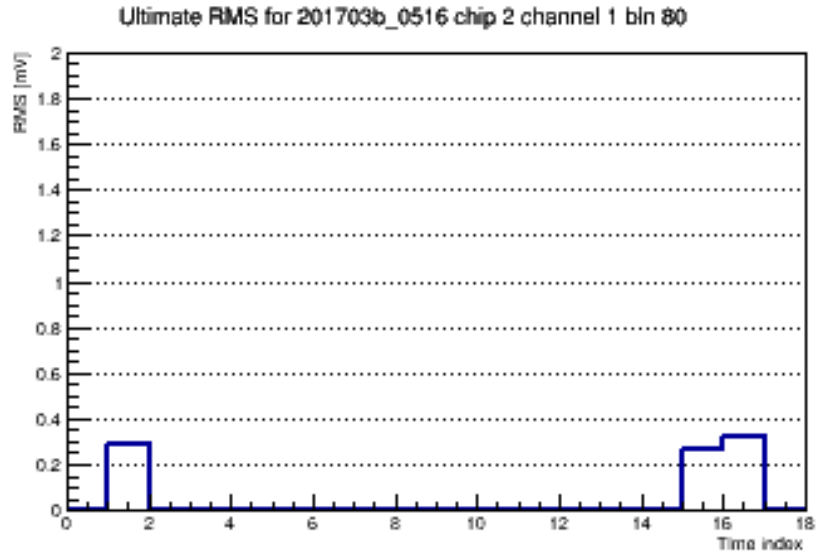
Performance: chip D02, time 9c

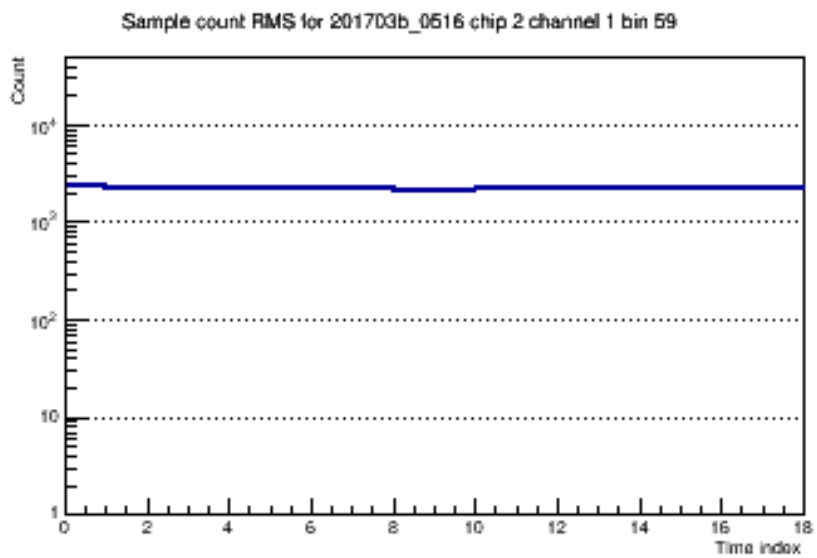


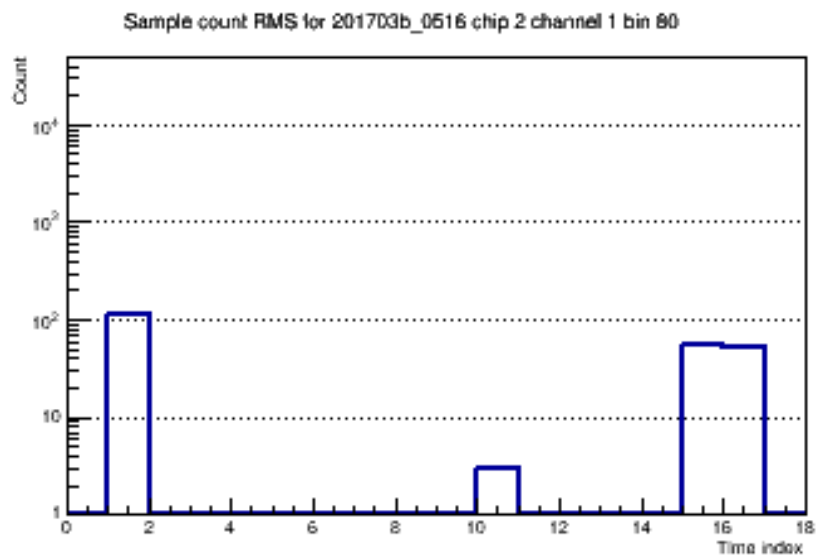
Appendix 3: Time variation

Time varying bins 1

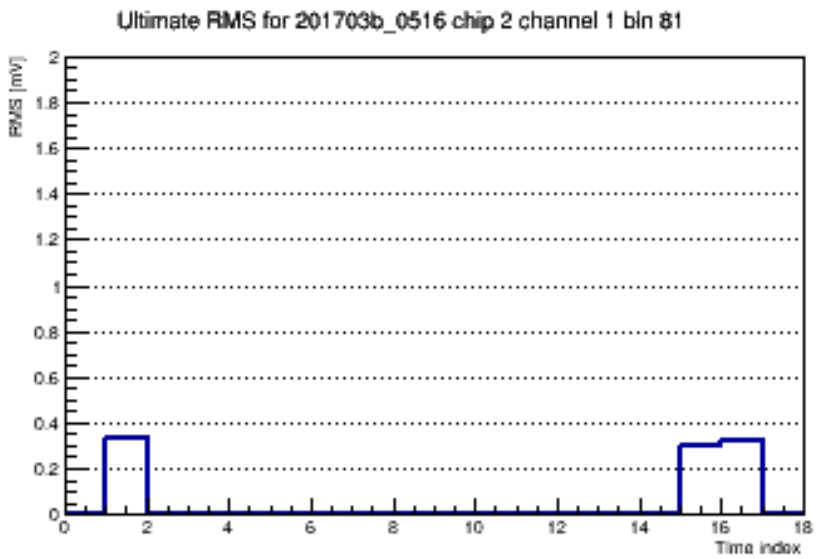


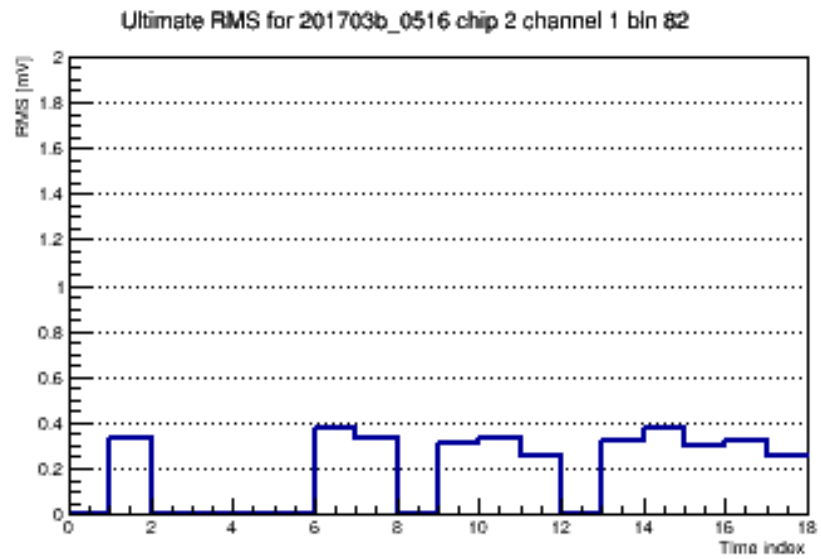


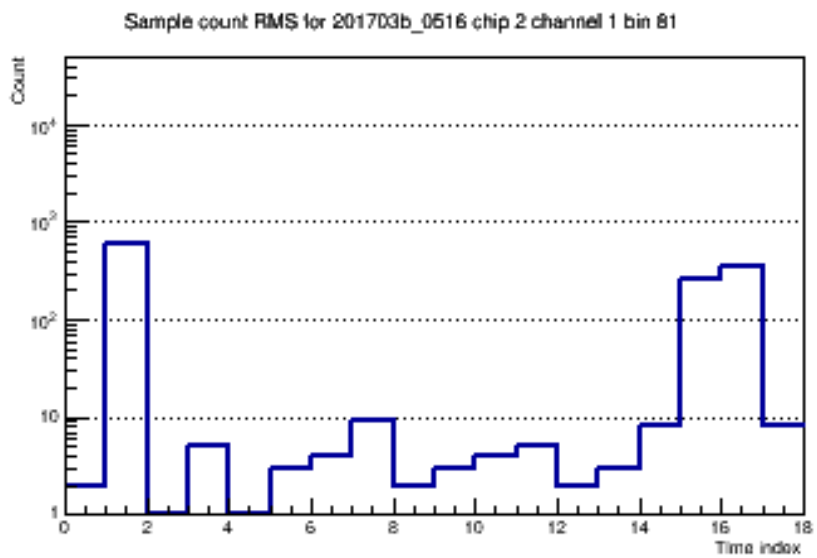


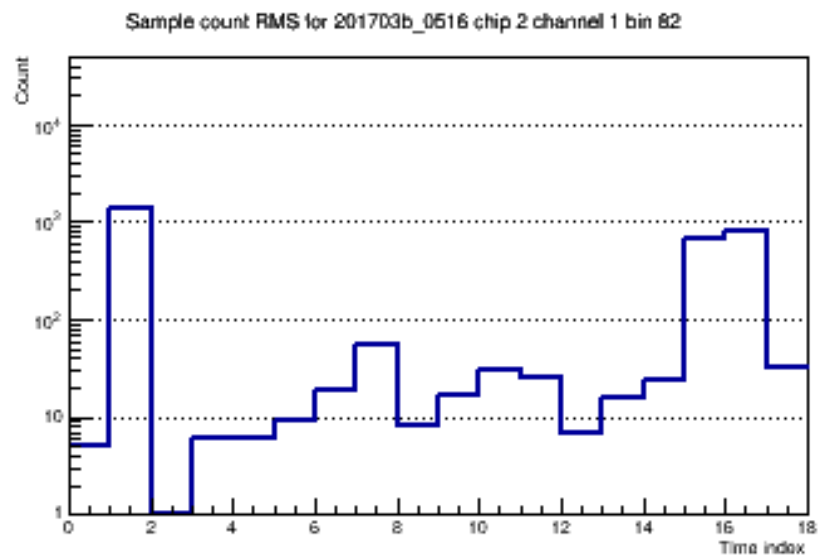


Time varying bins 2

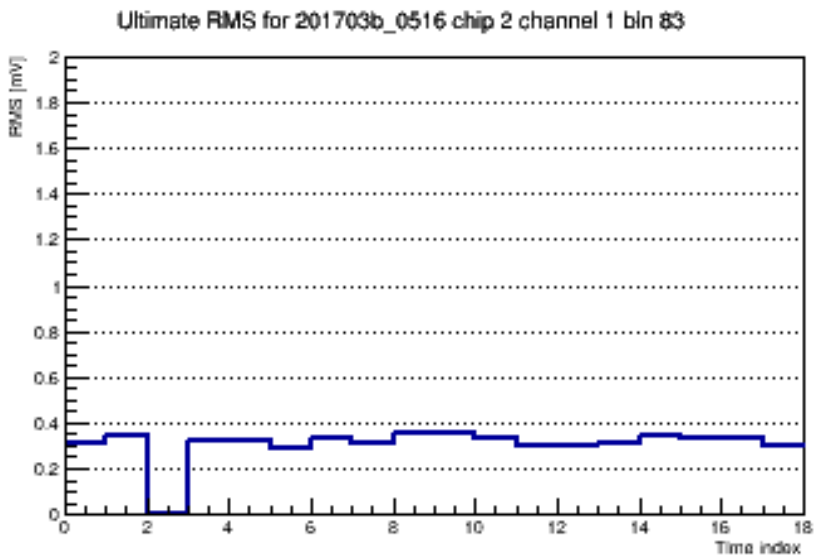


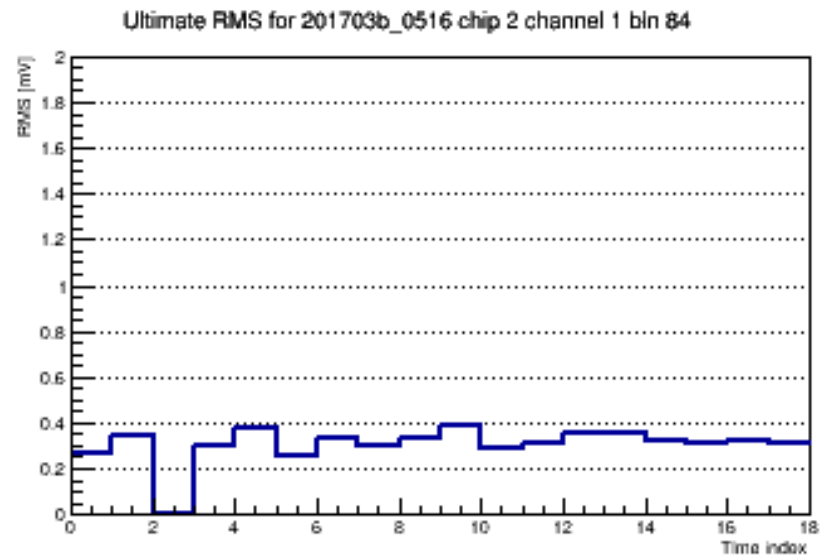


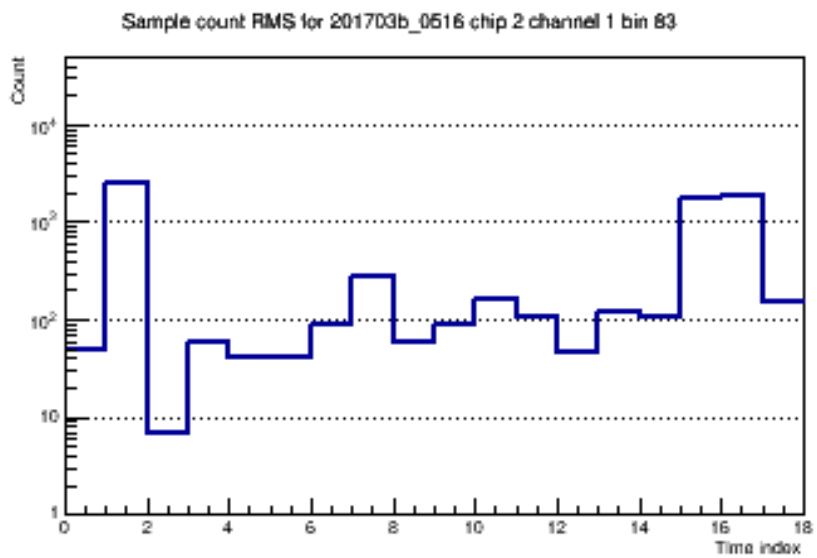


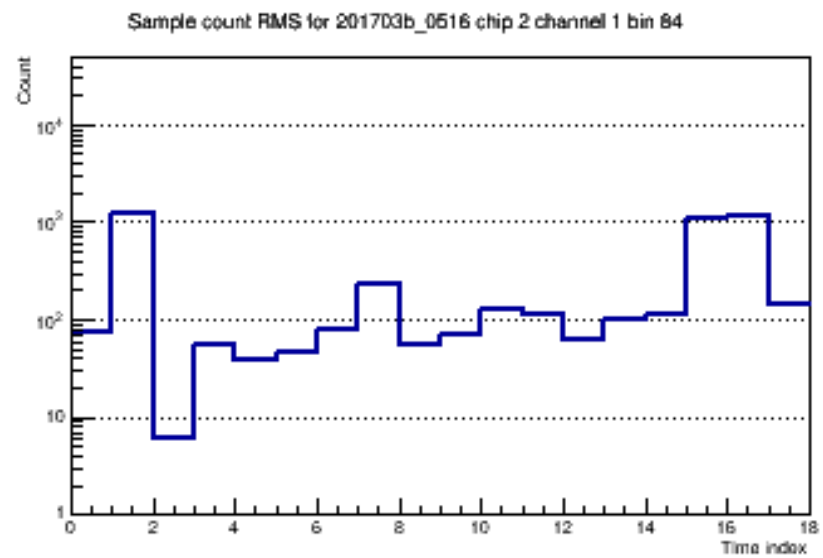


Time varying bins 3

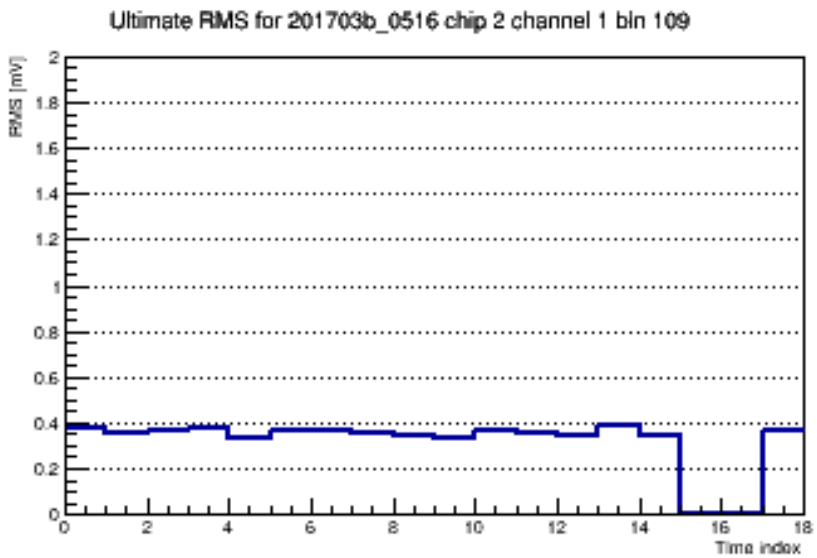


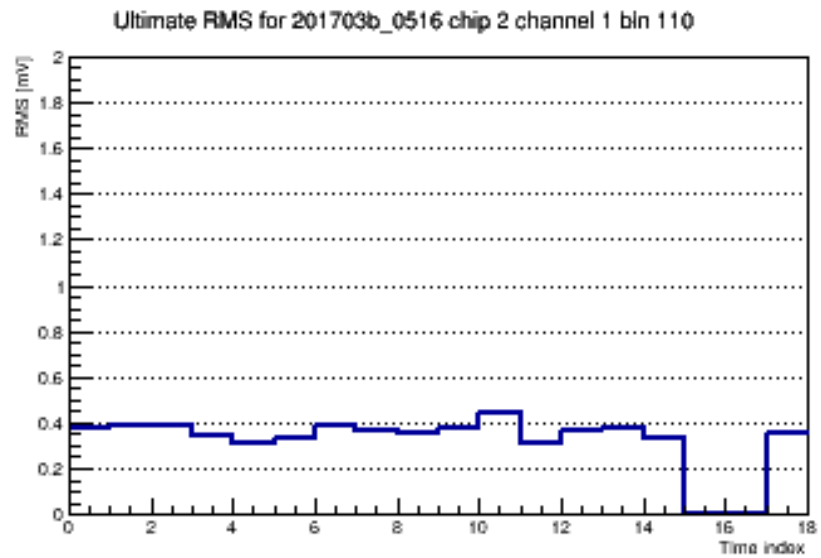


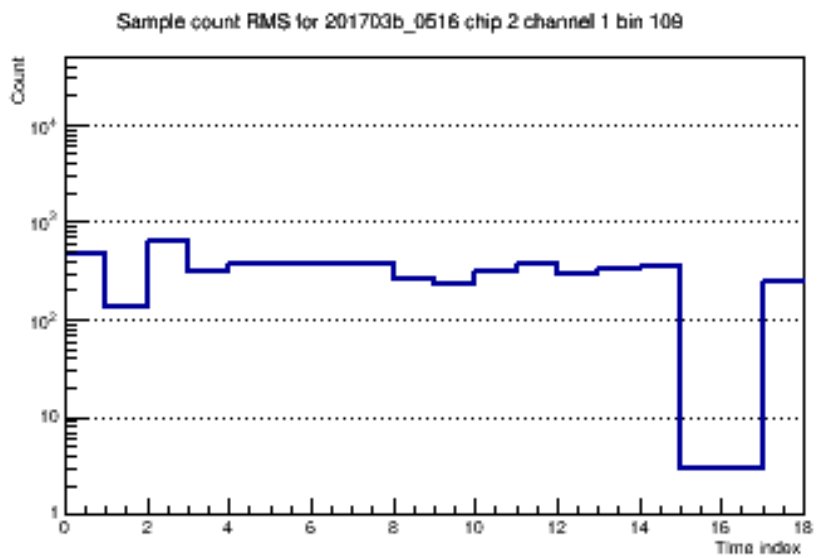


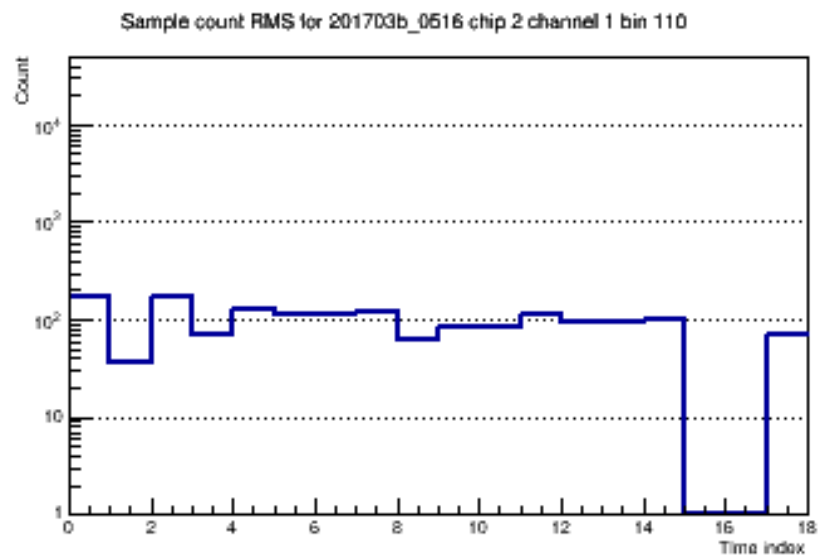


Time varying bins 4

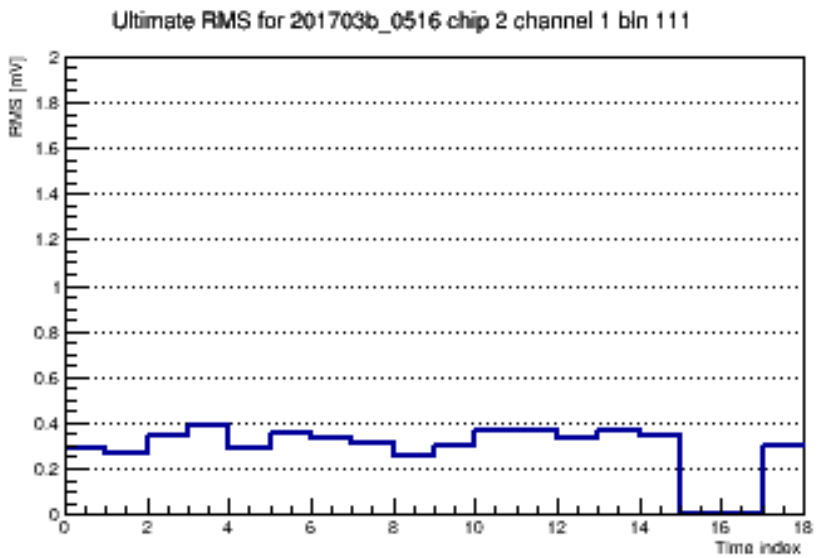


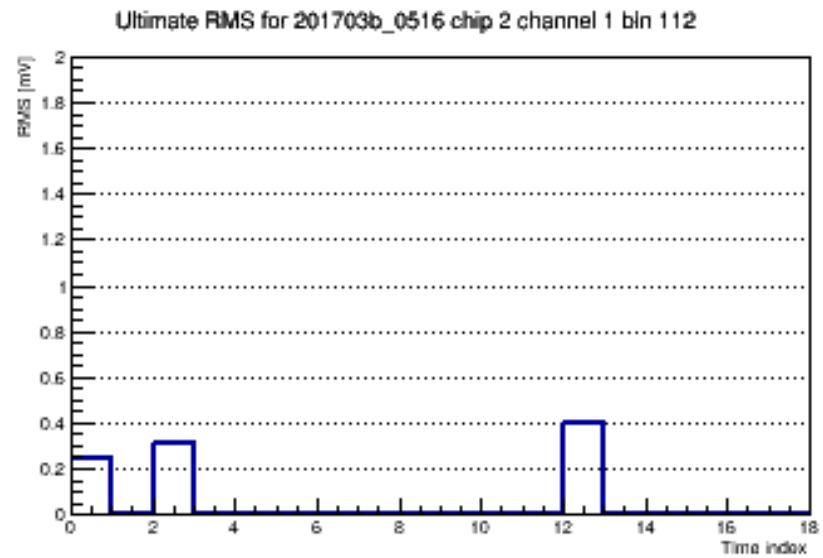


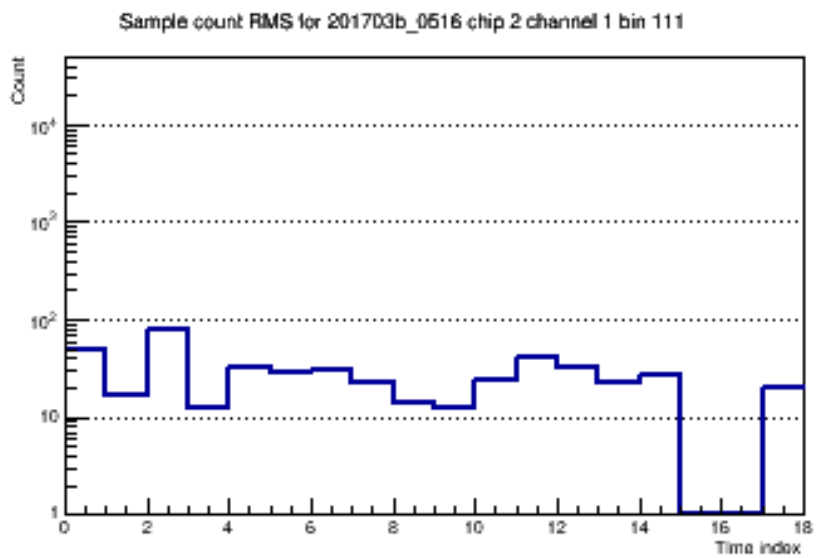


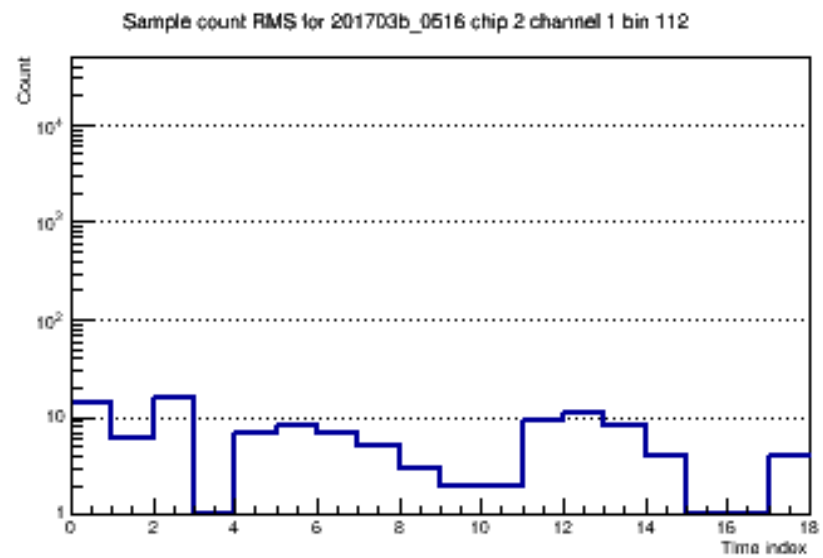


Time varying bins 5

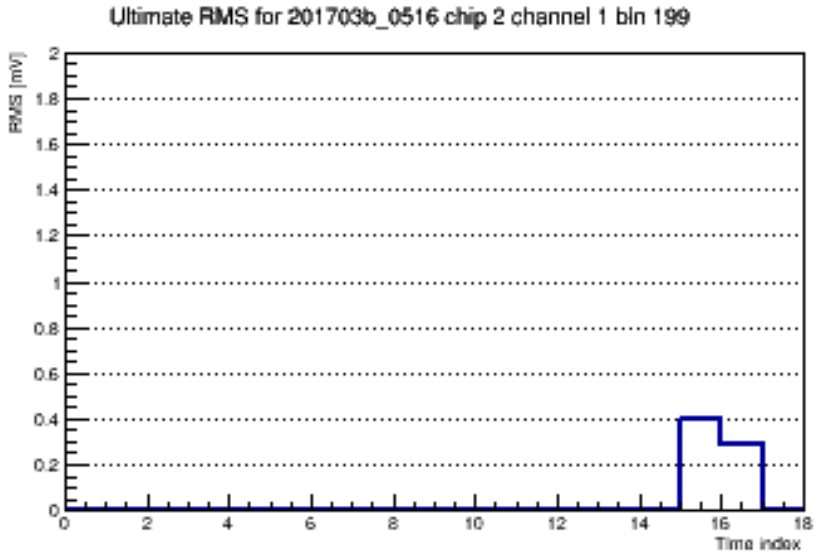


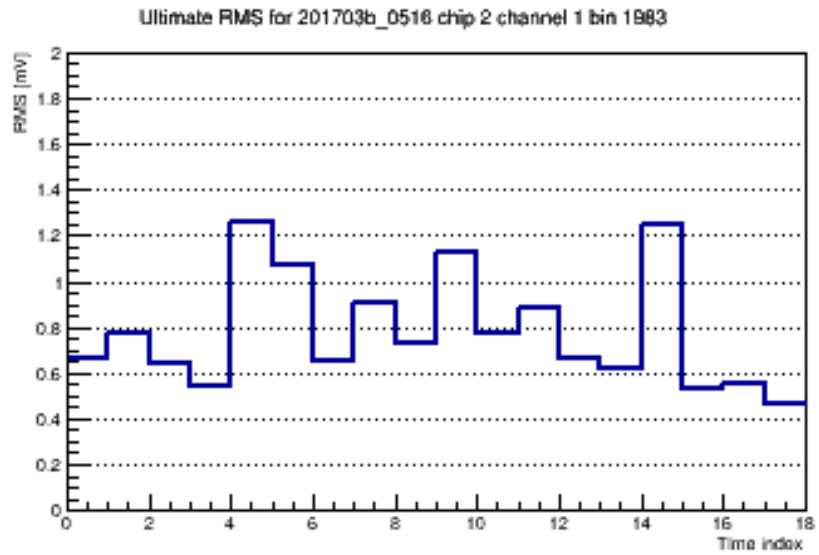


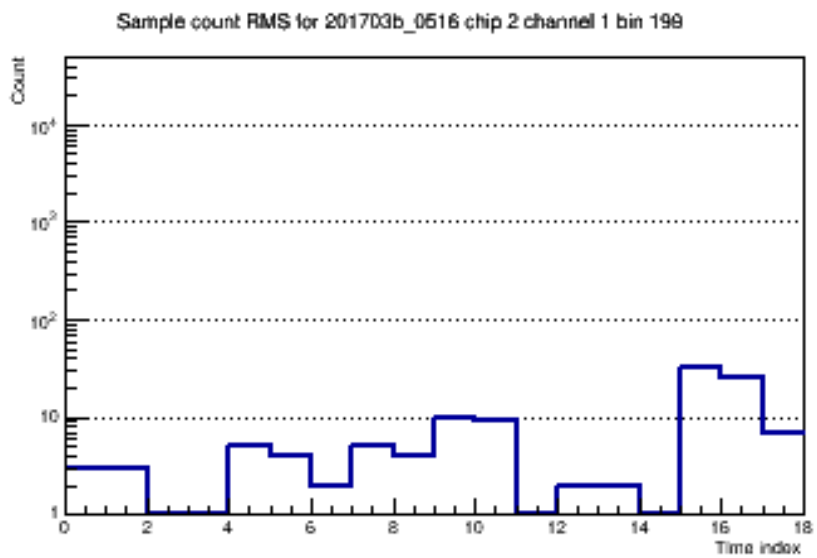


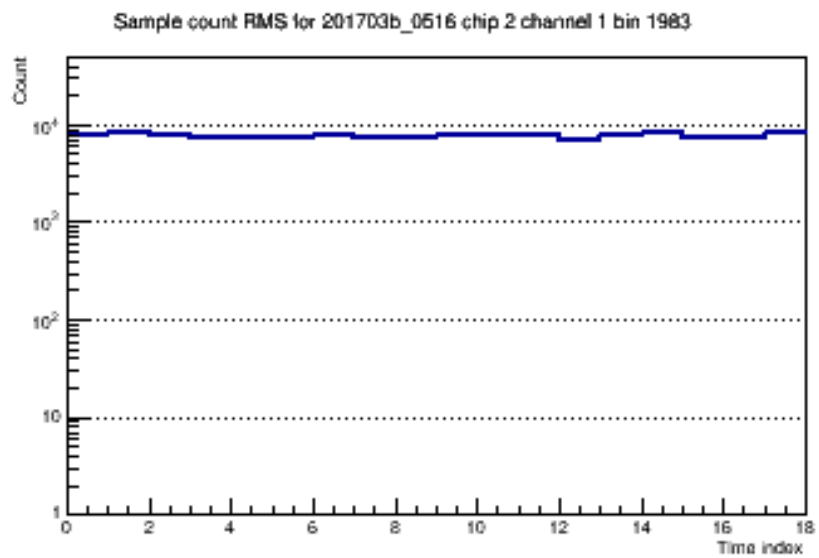


Time varying bins 6

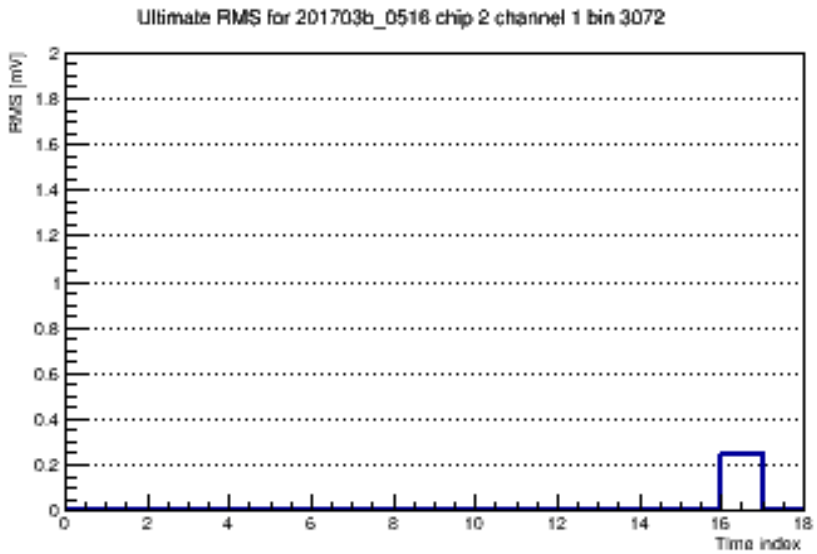


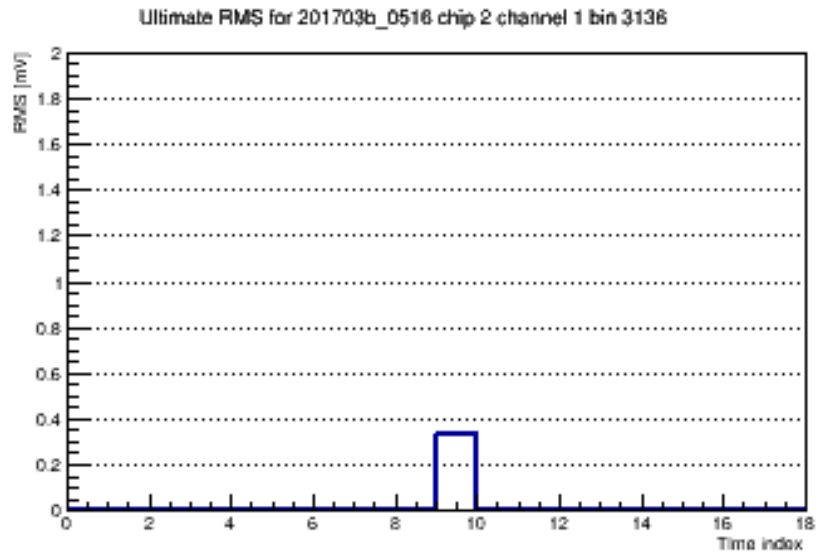


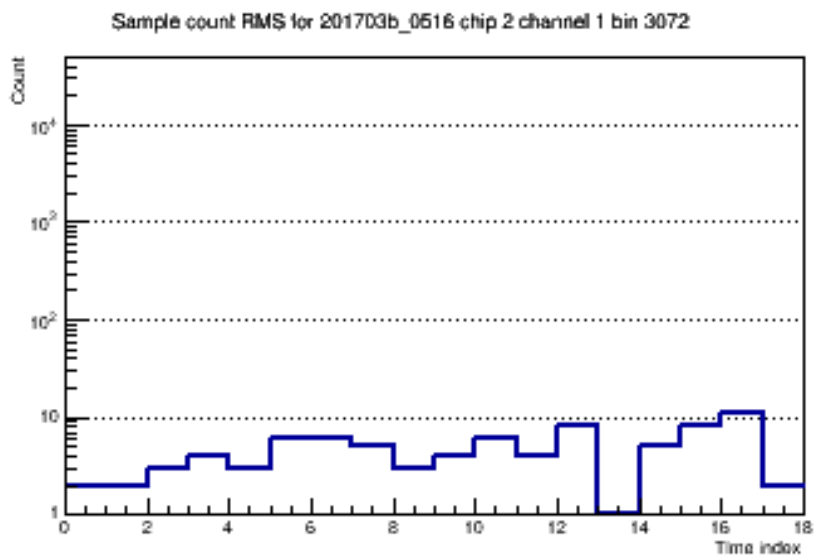


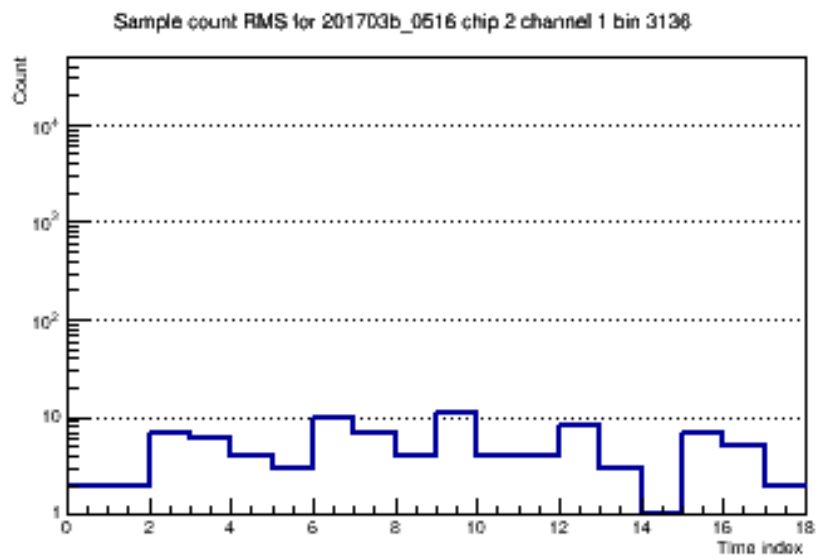


Time varying bins 7

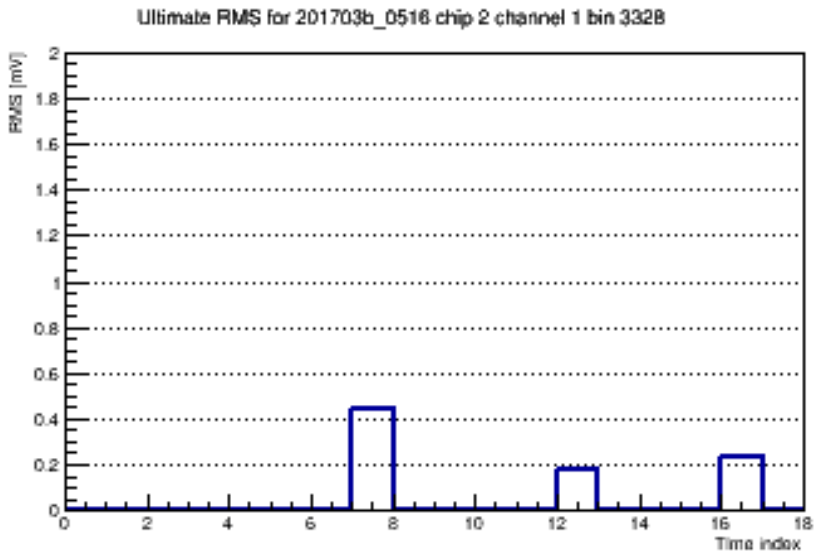


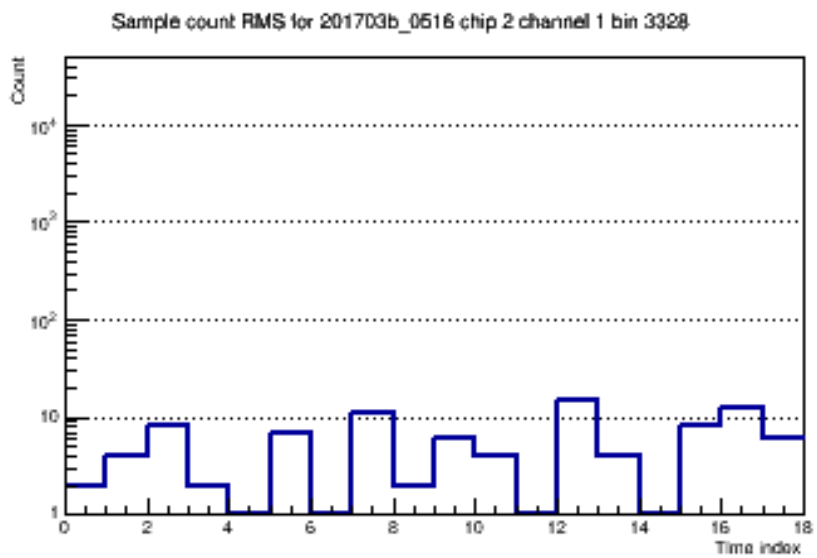




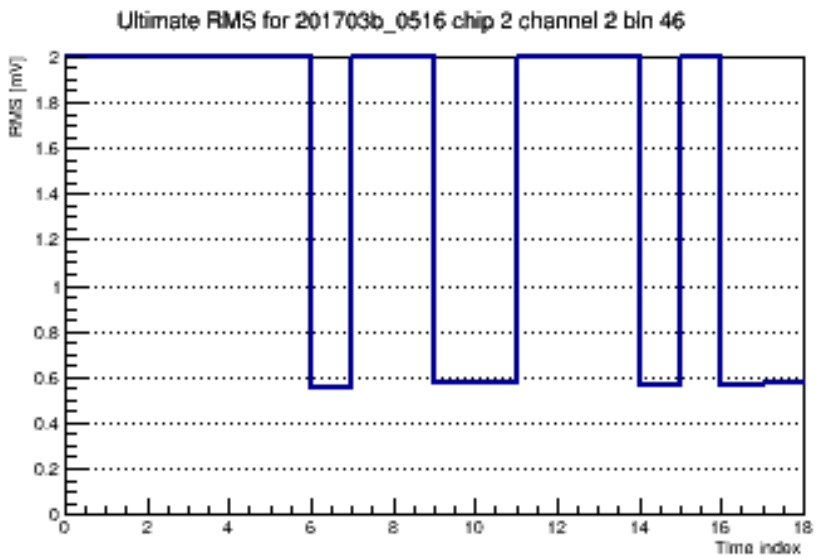


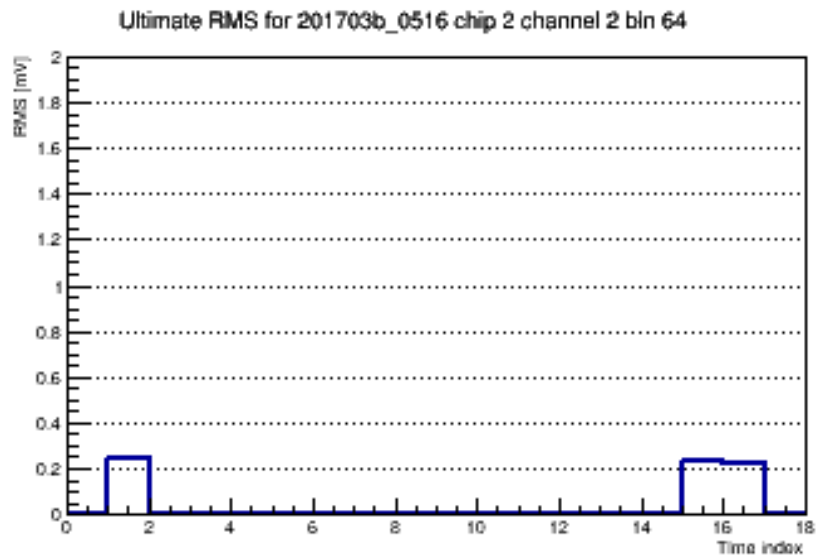
Time varying bins 8

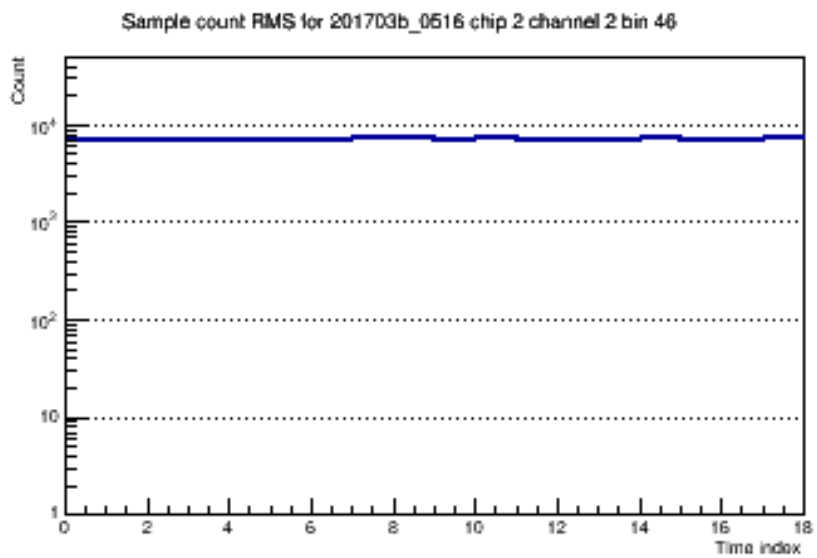


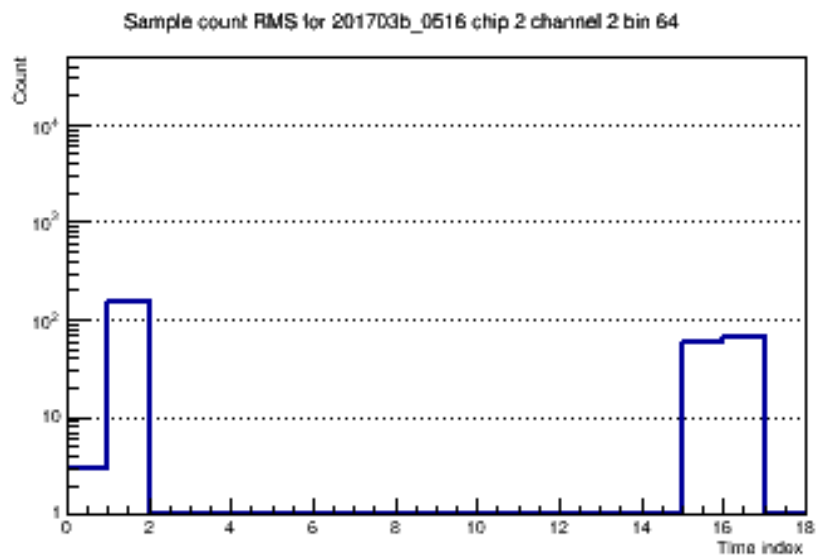


Time varying bins 9

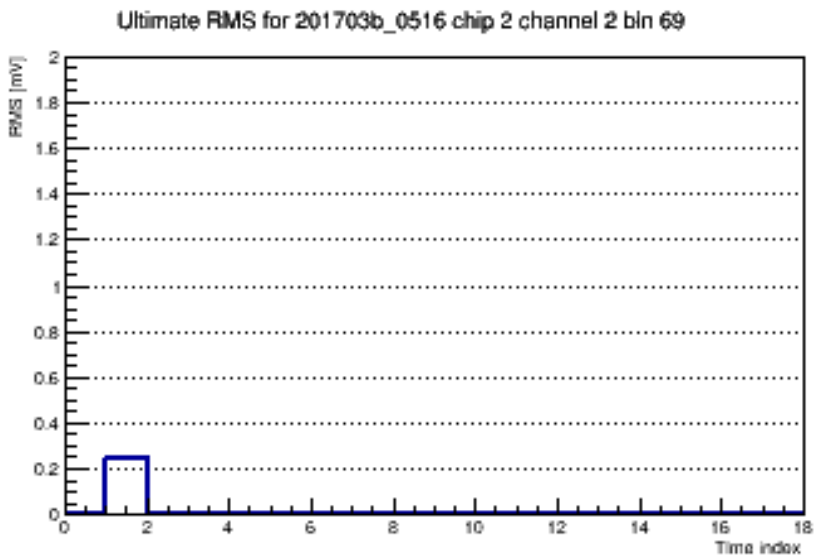


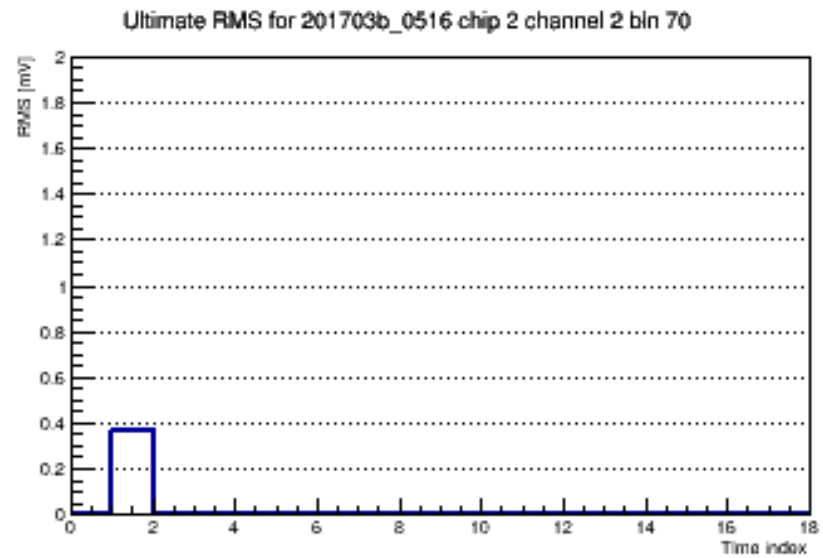


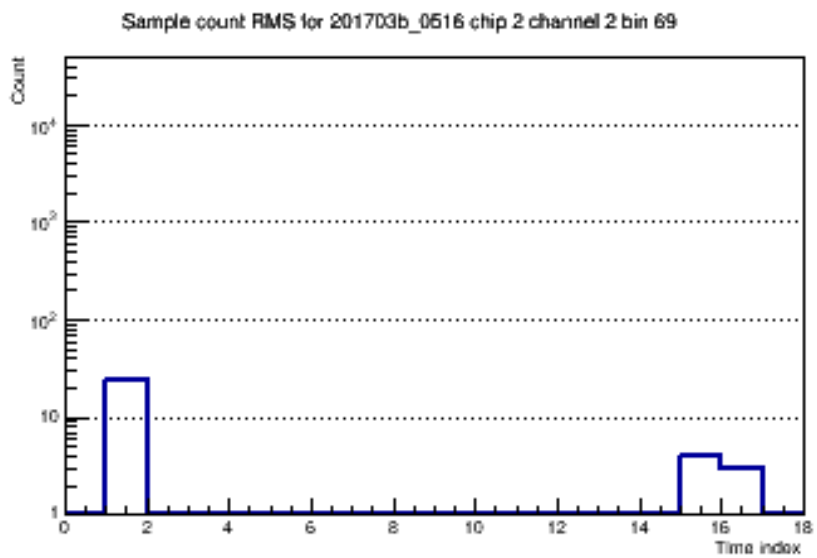


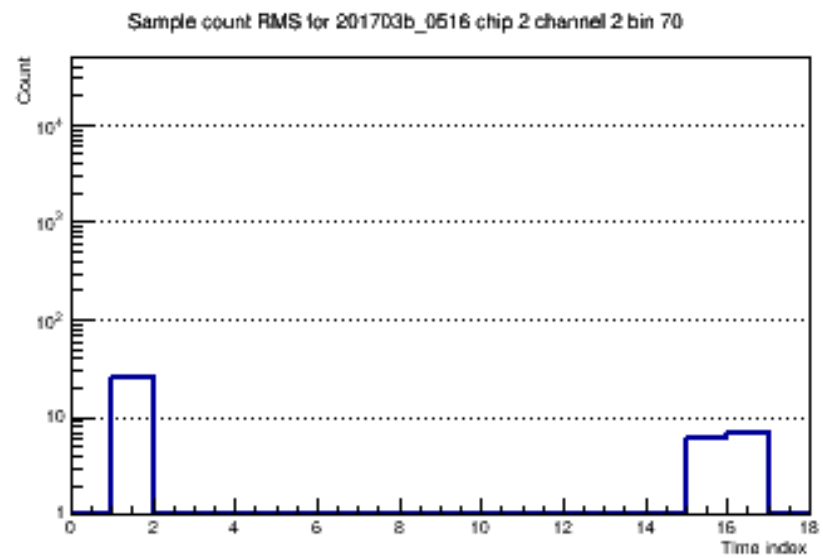


Time varying bins 10

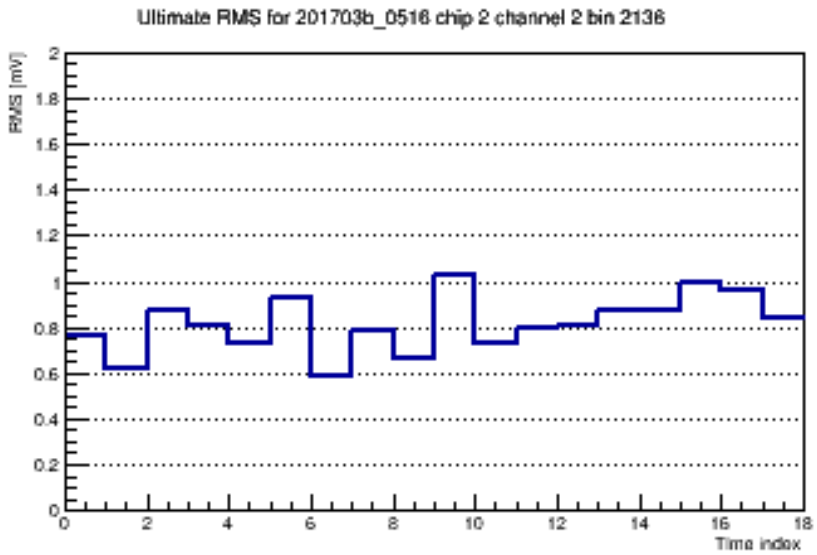


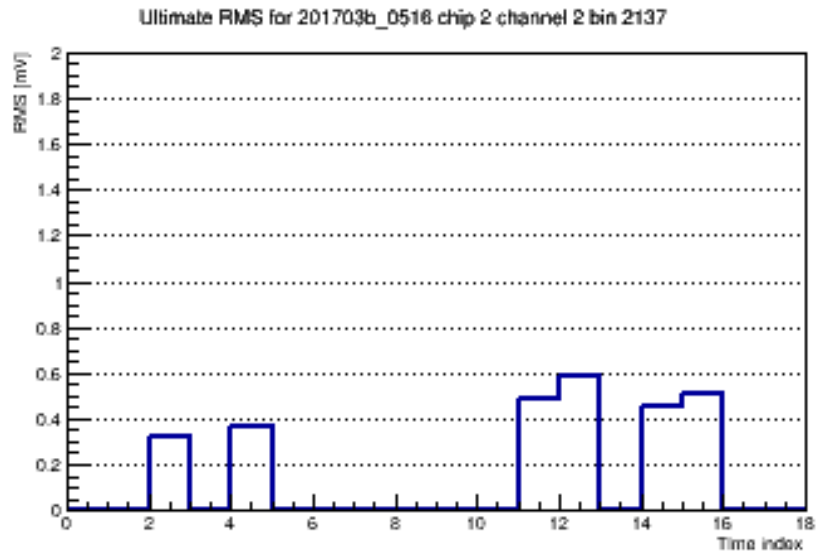


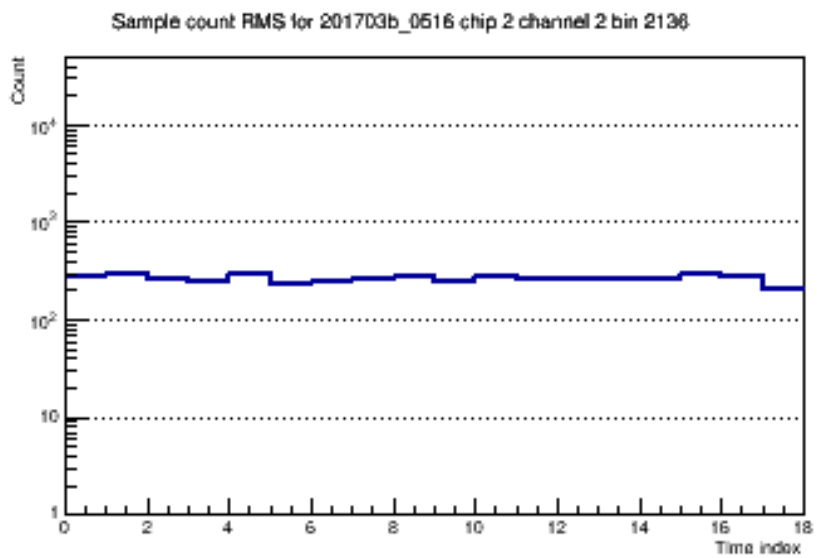


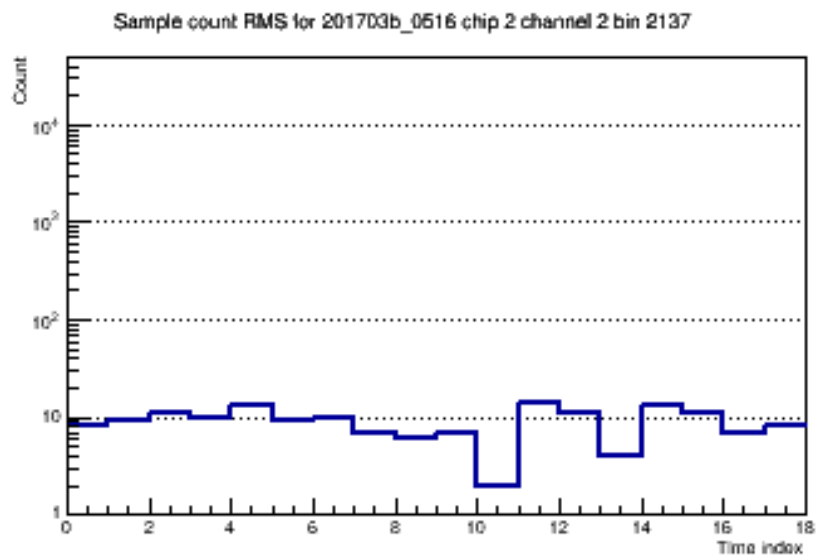


Time varying bins 11

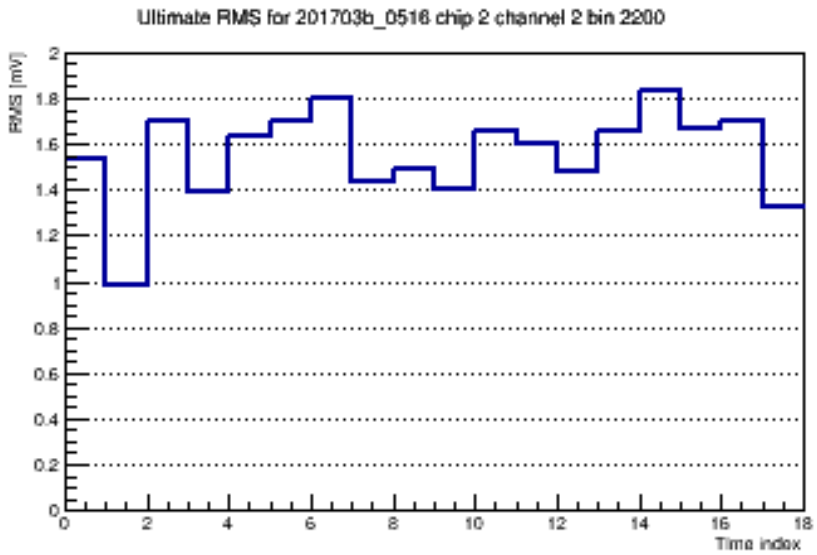


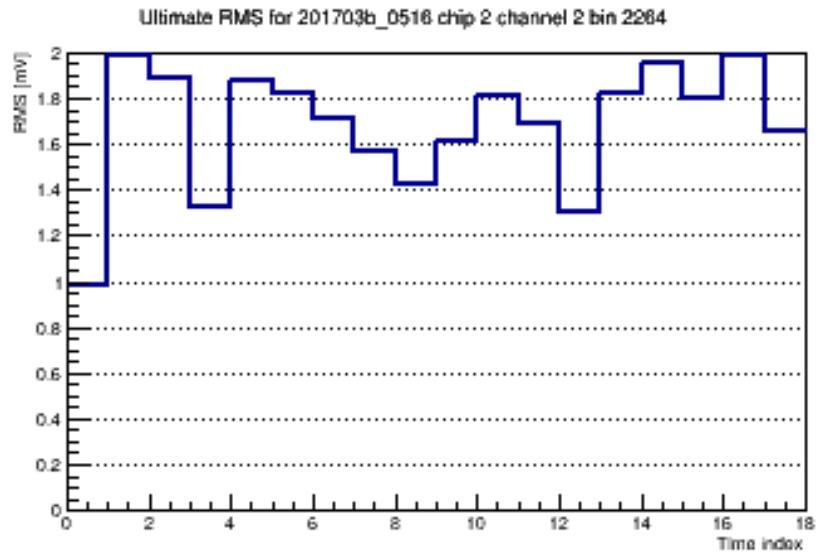


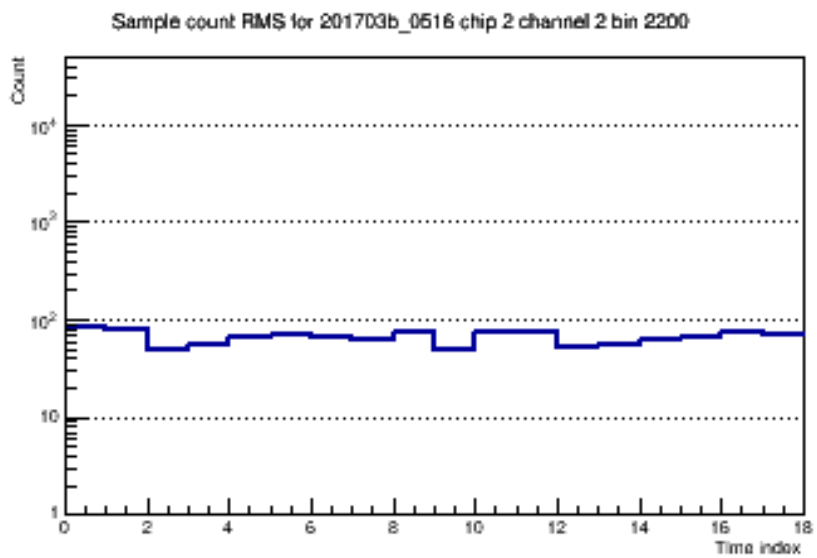


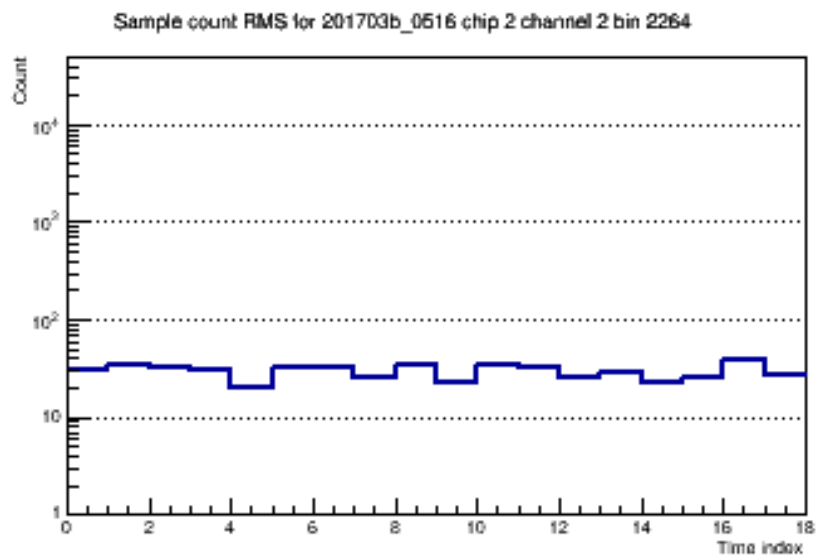


Time varying bins 12

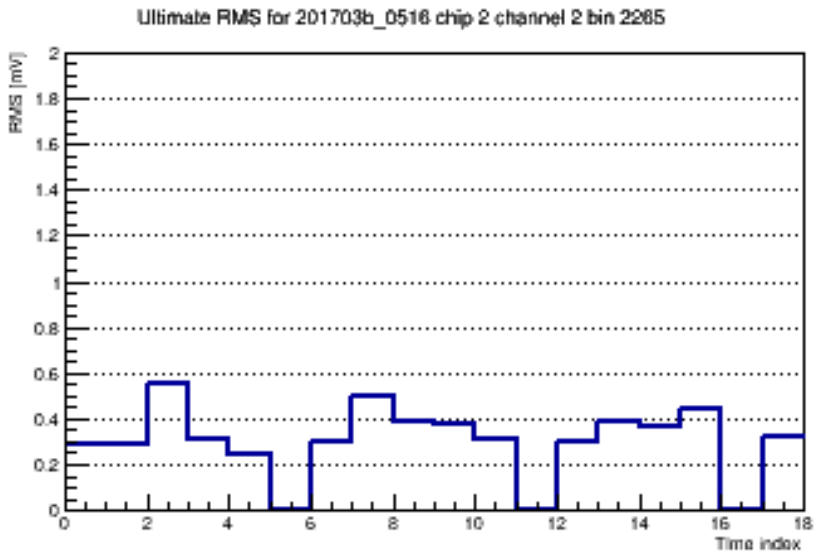


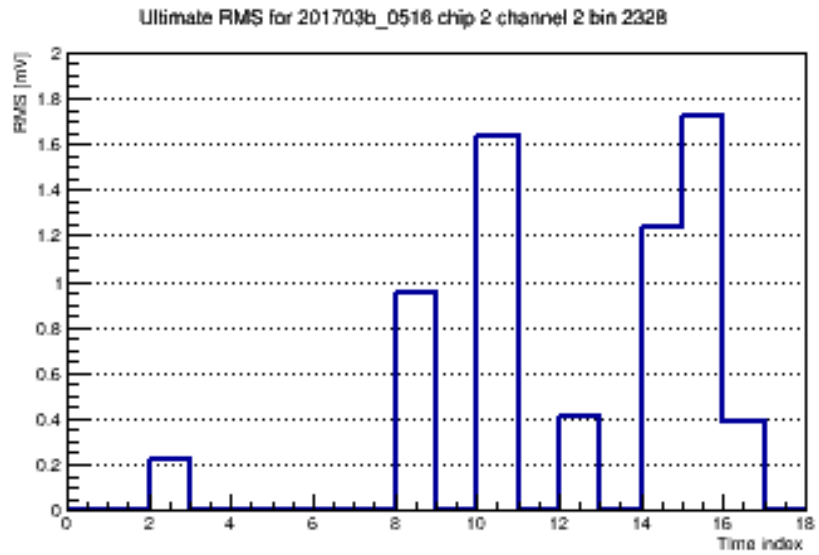


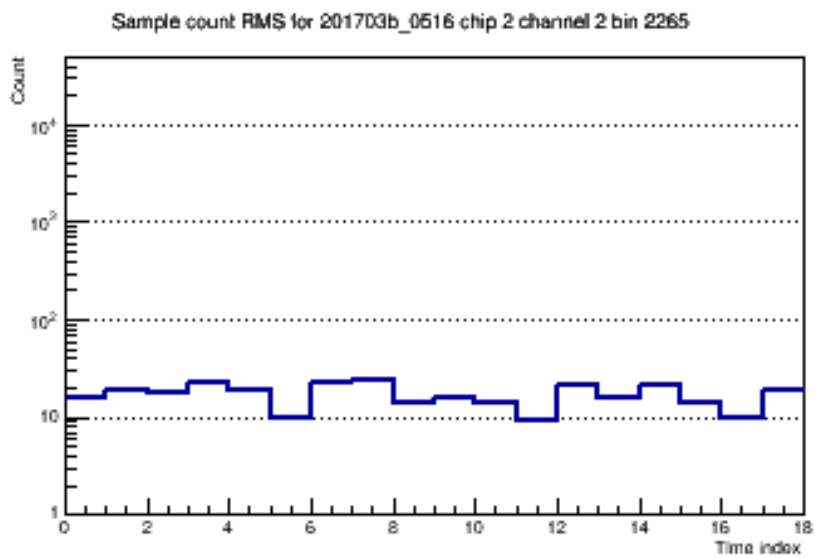


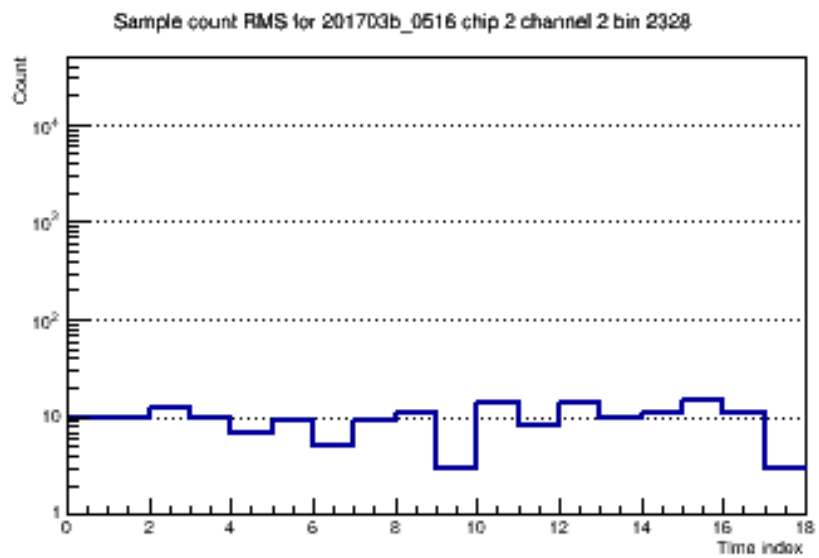


Time varying bins 13

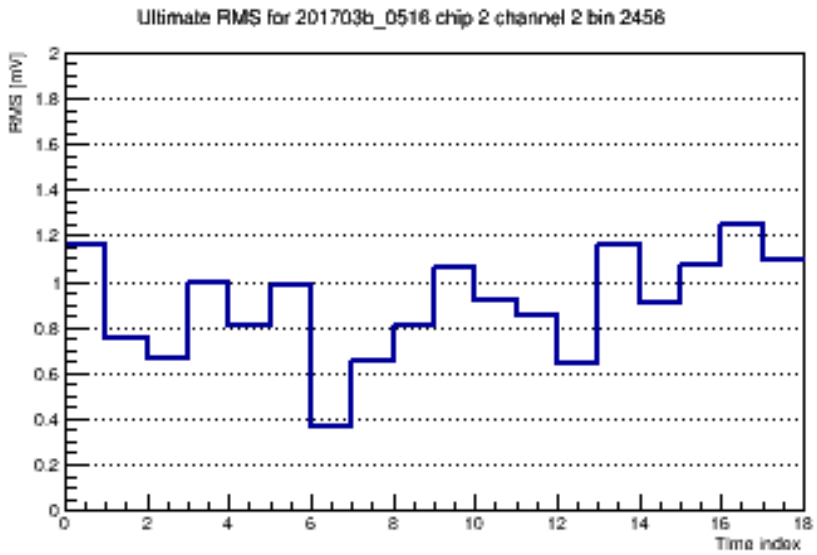


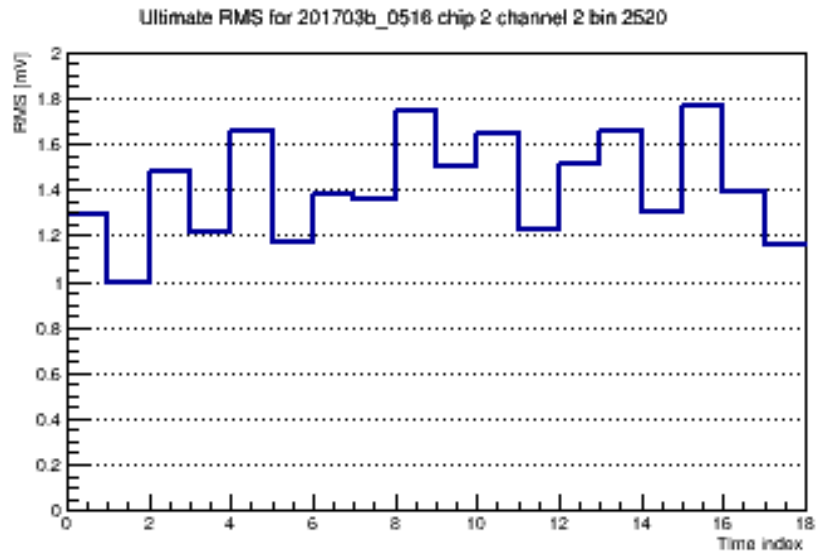


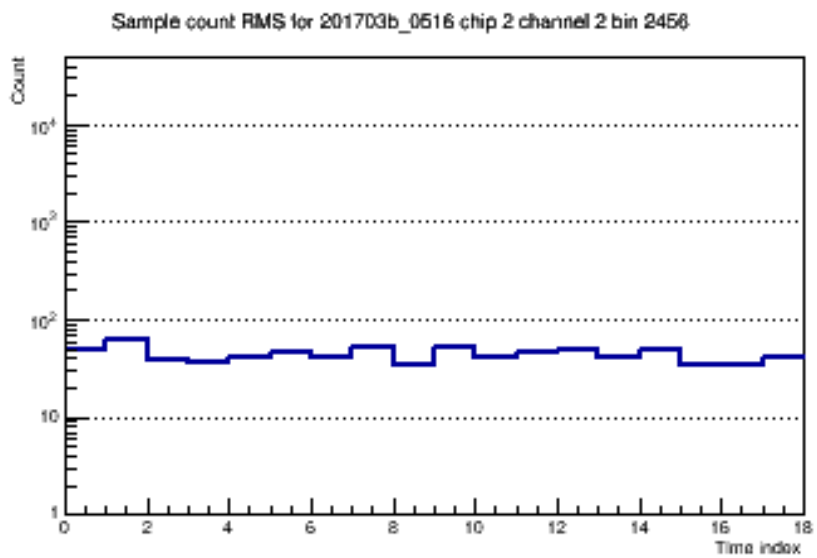


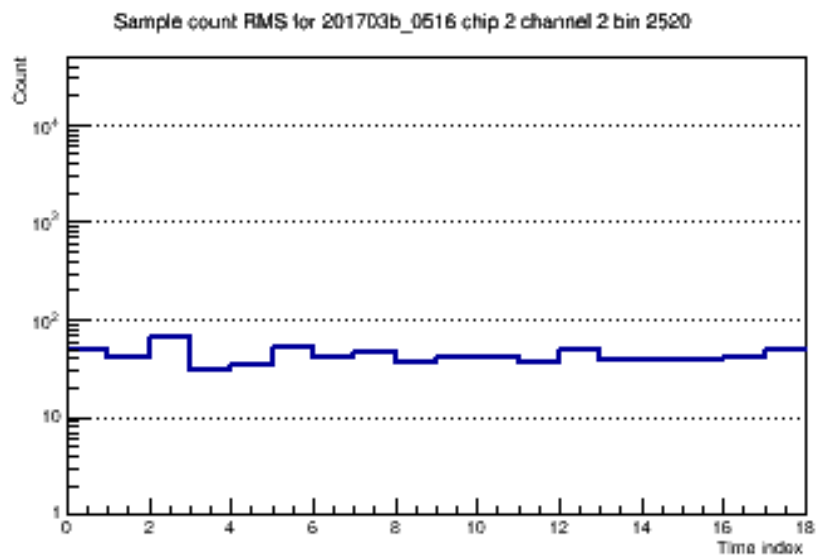


Time varying bins 14

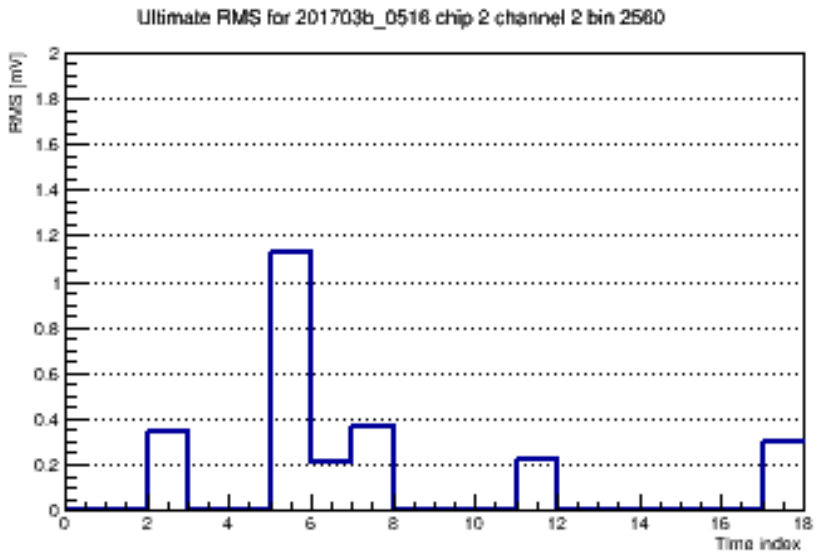


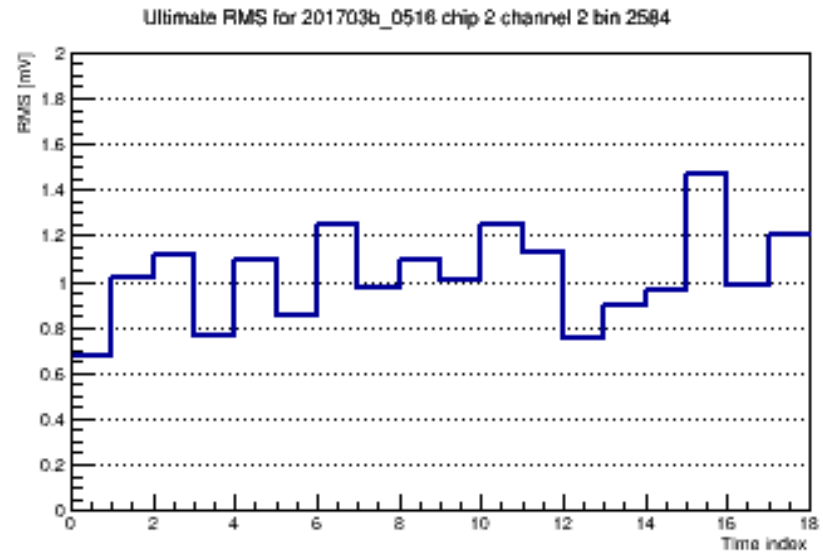


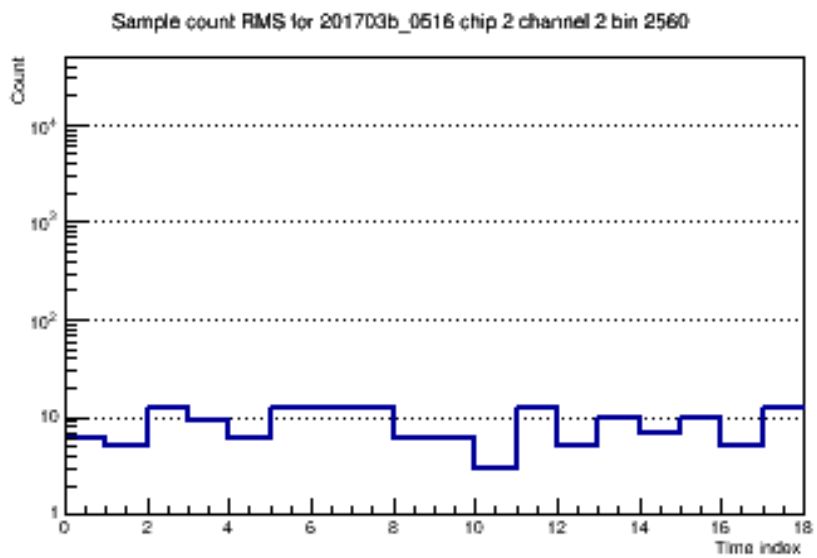


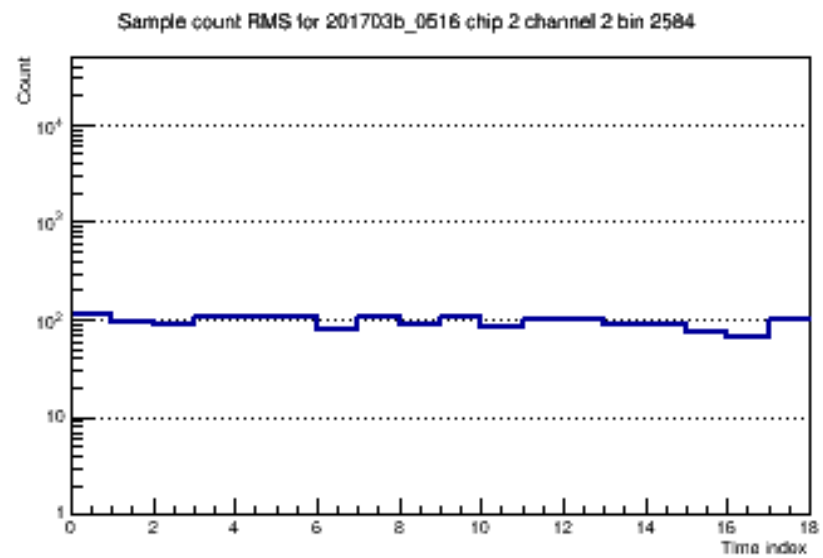


Time varying bins 15

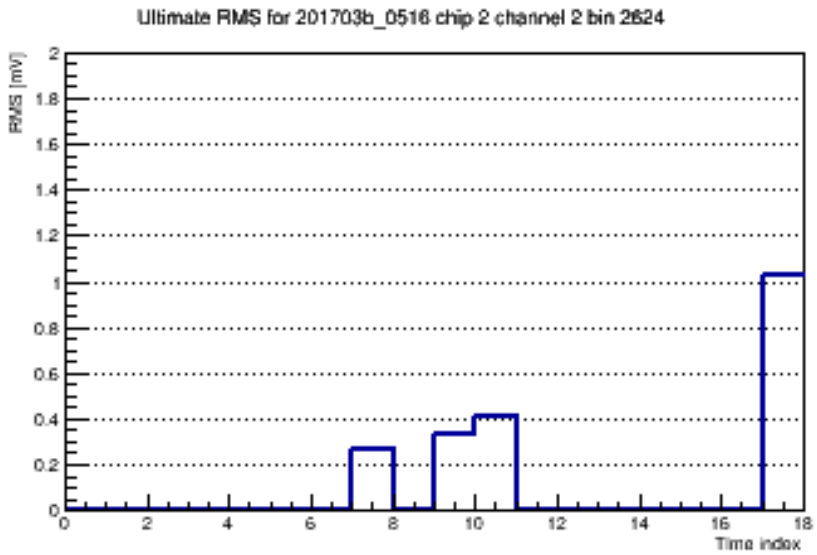


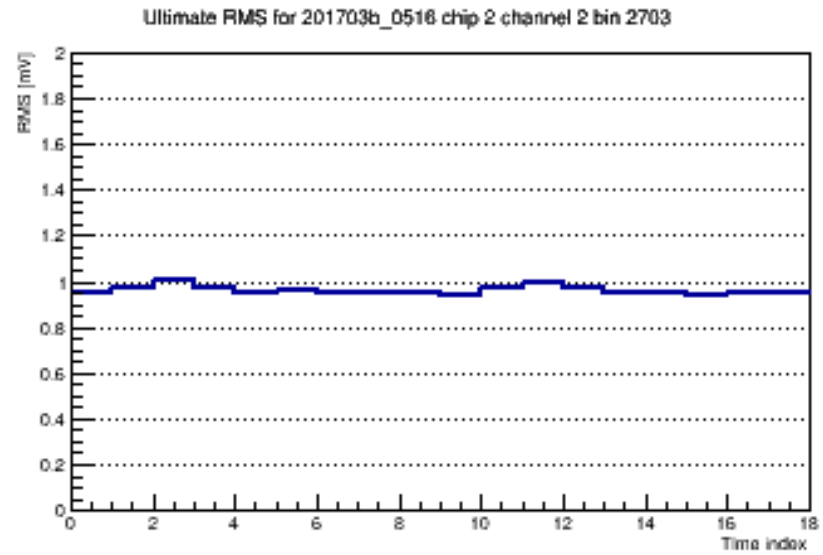


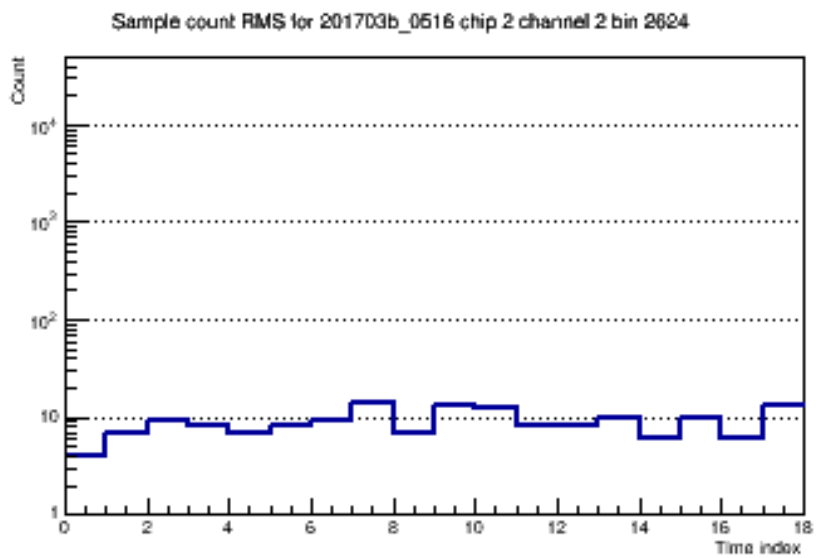


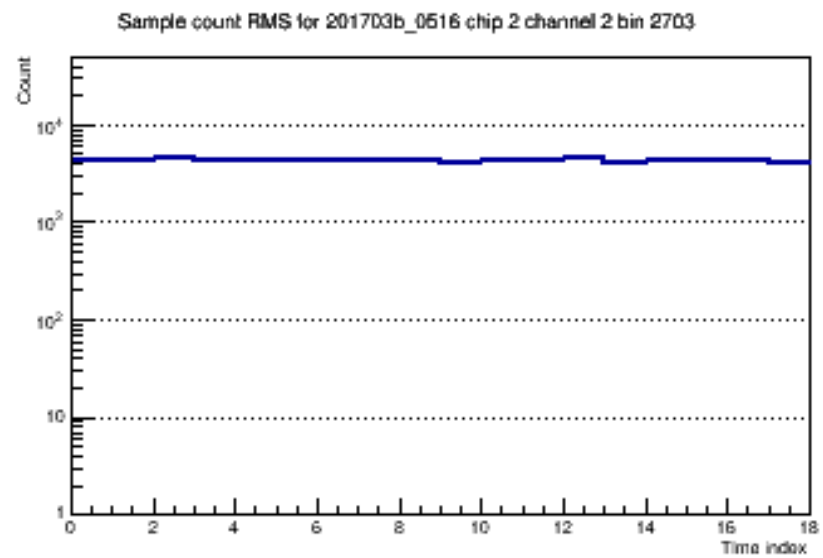


Time varying bins 16

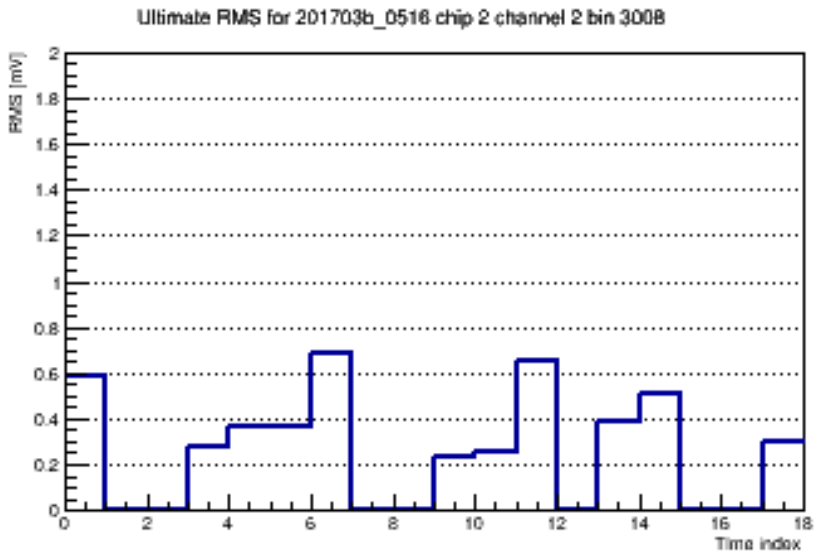


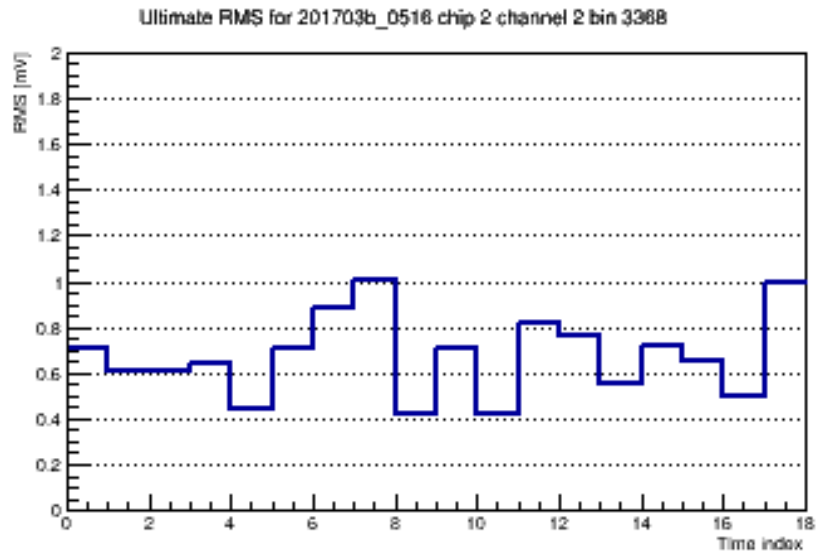


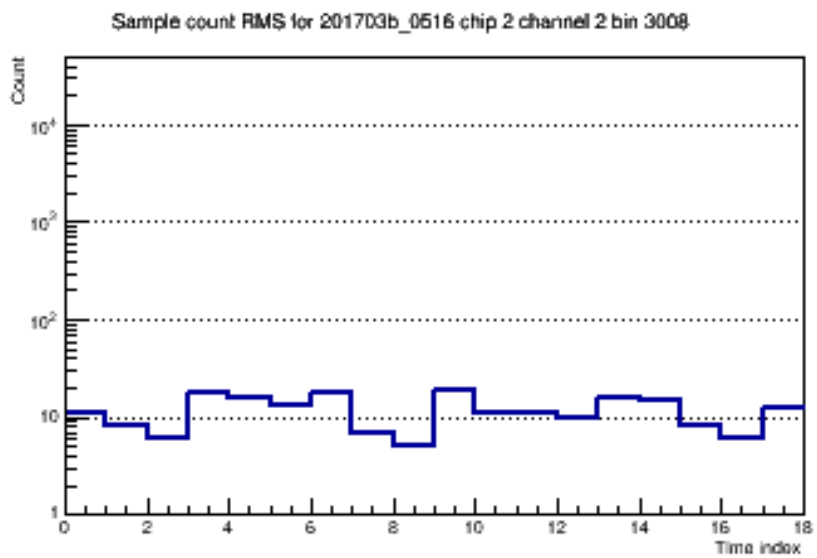


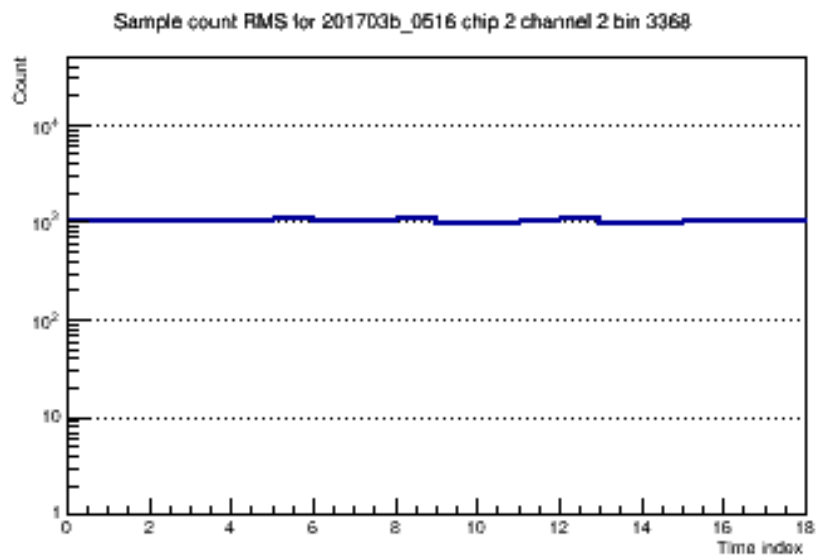


Time varying bins 17

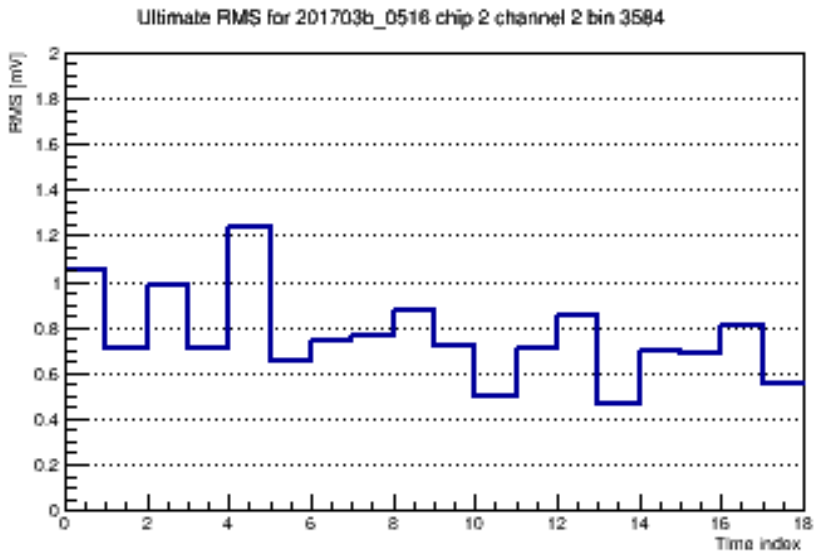


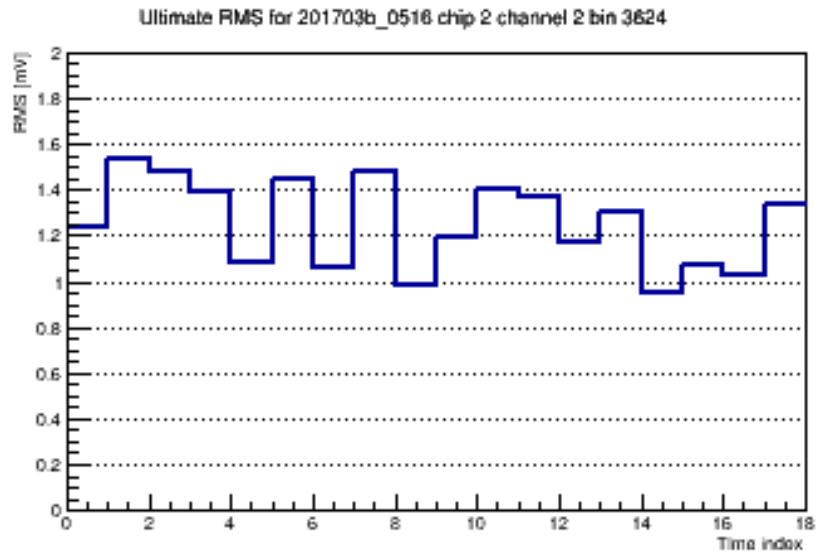


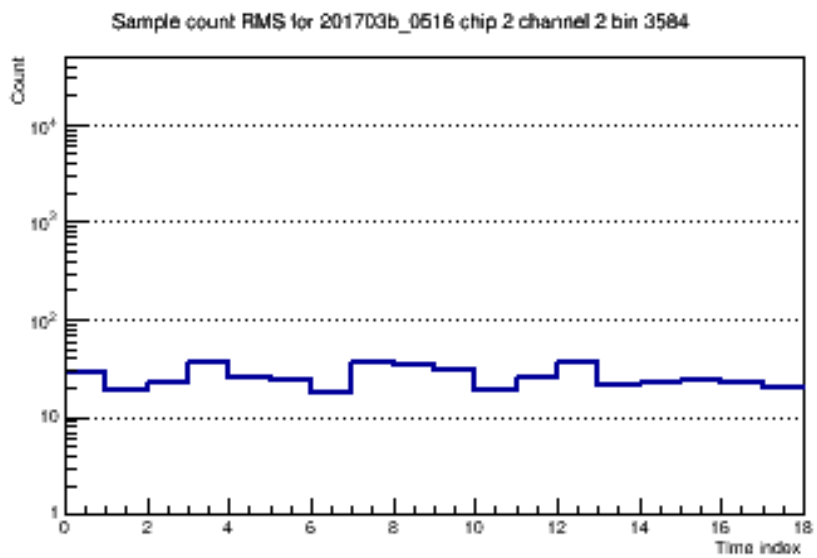


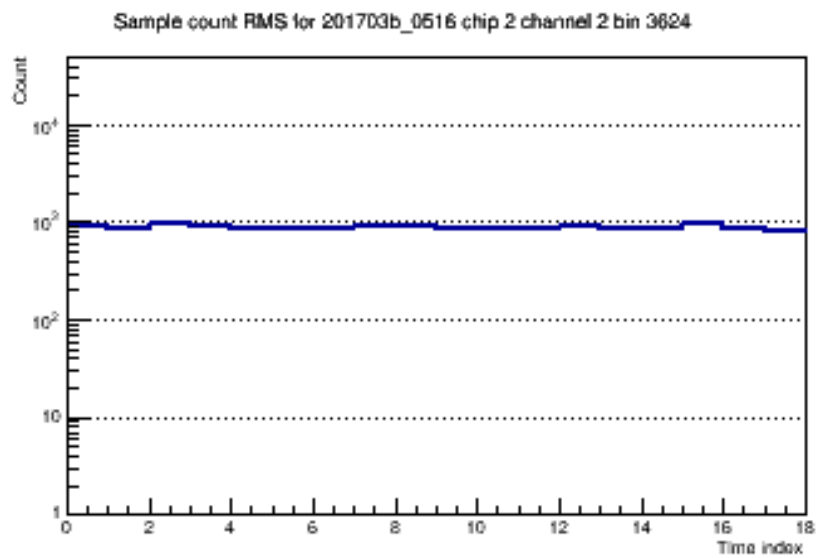


Time varying bins 18

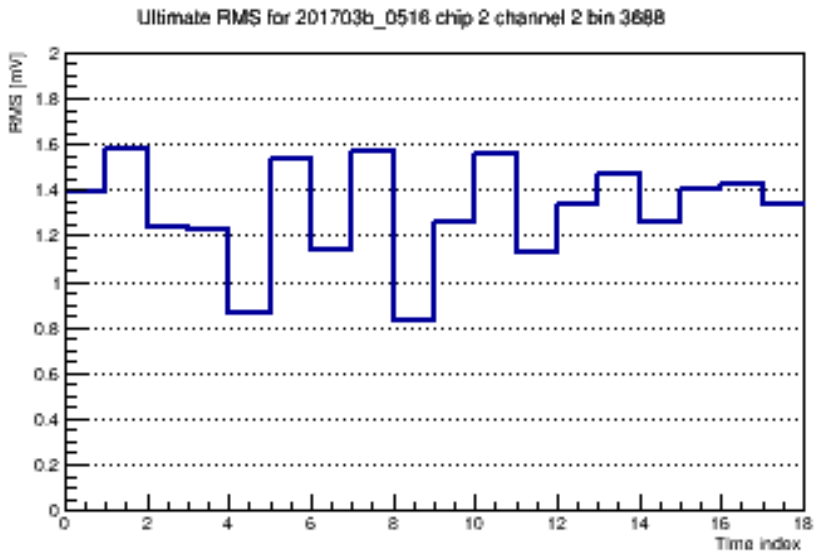


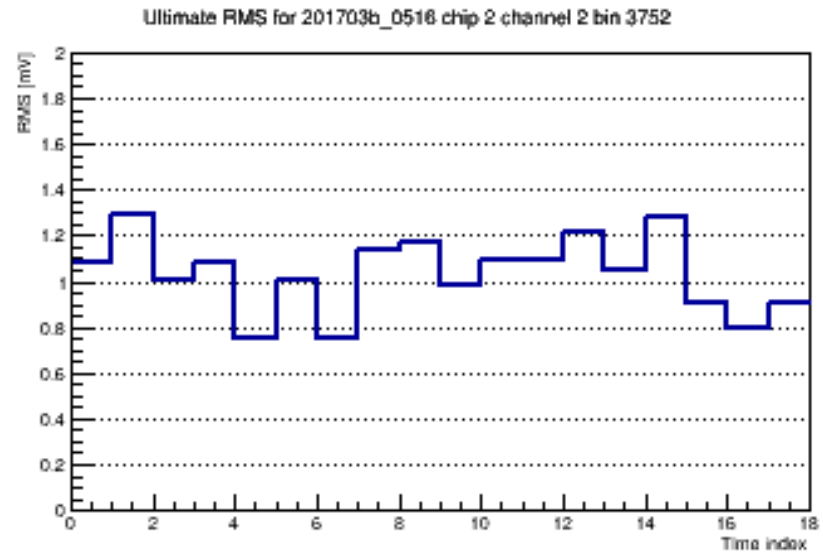


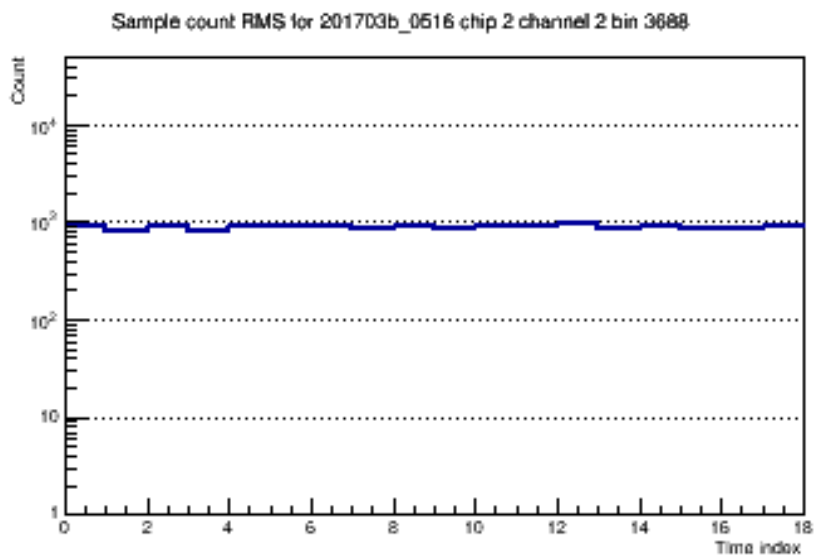


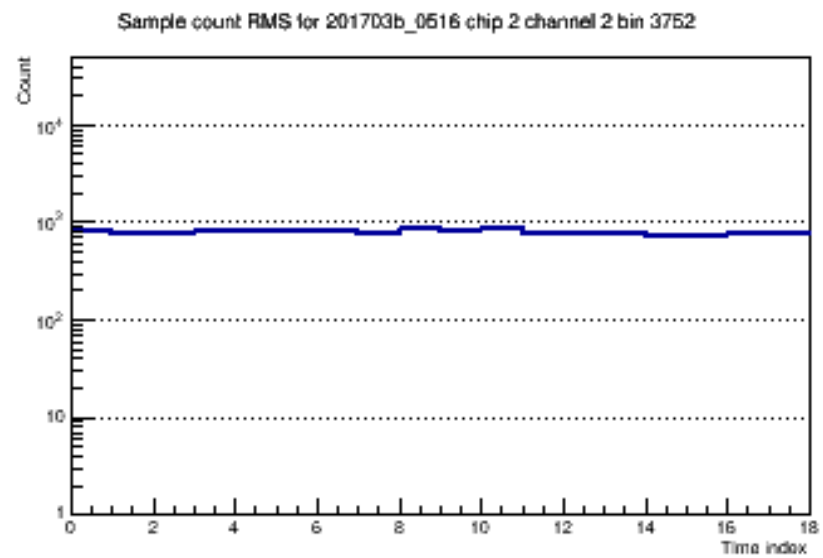


Time varying bins 19

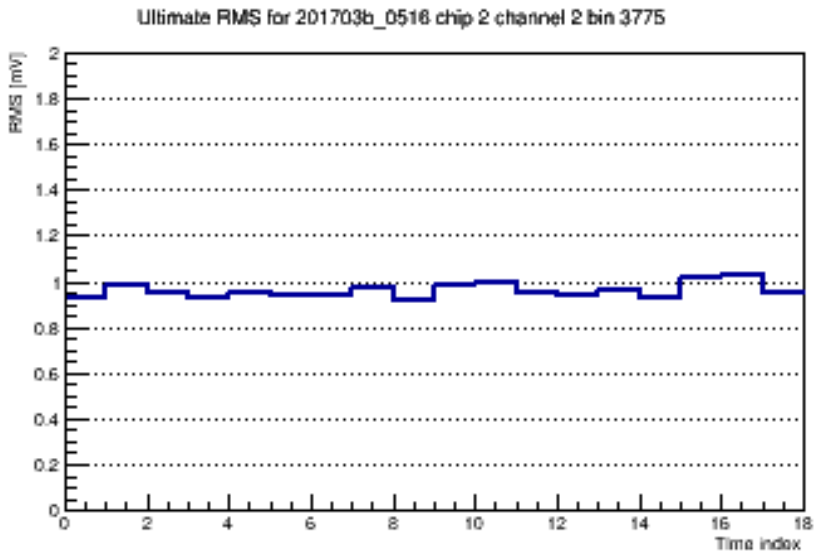


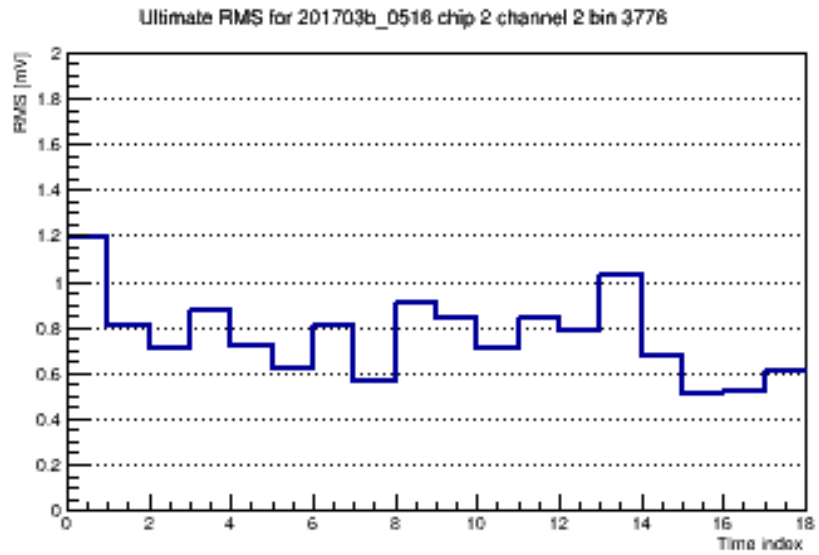


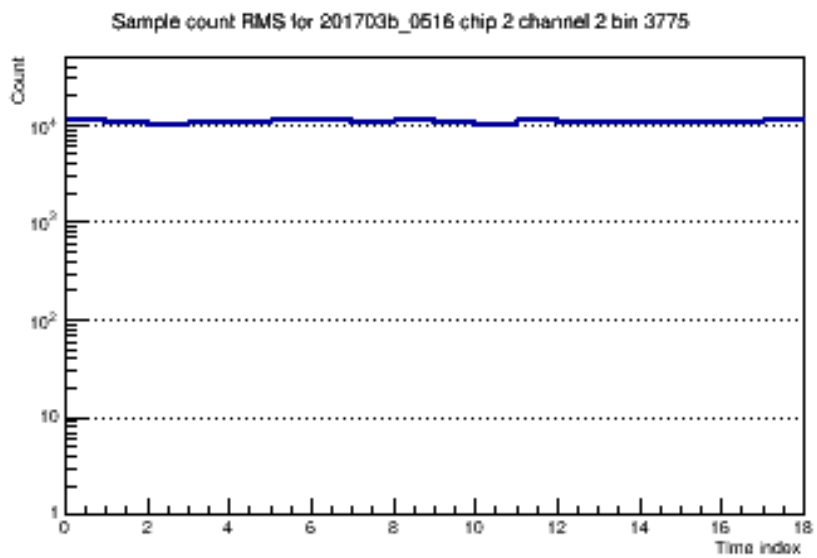


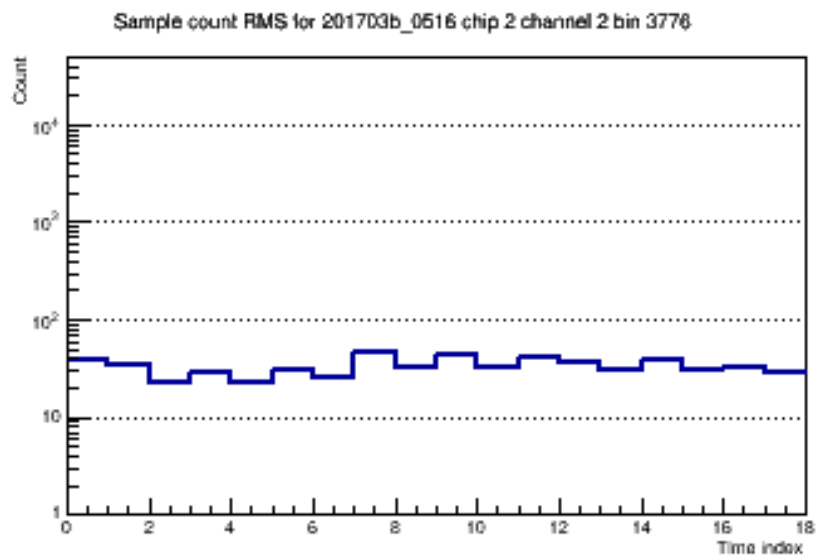


Time varying bins 20

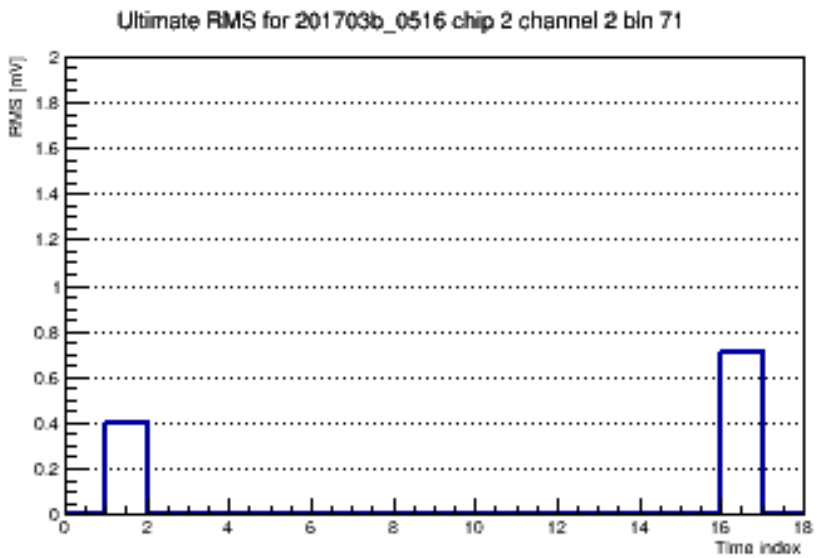


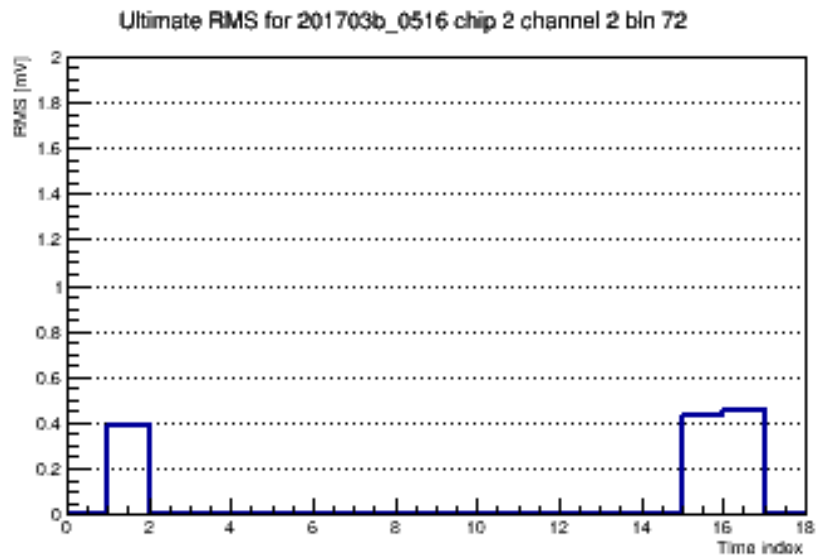


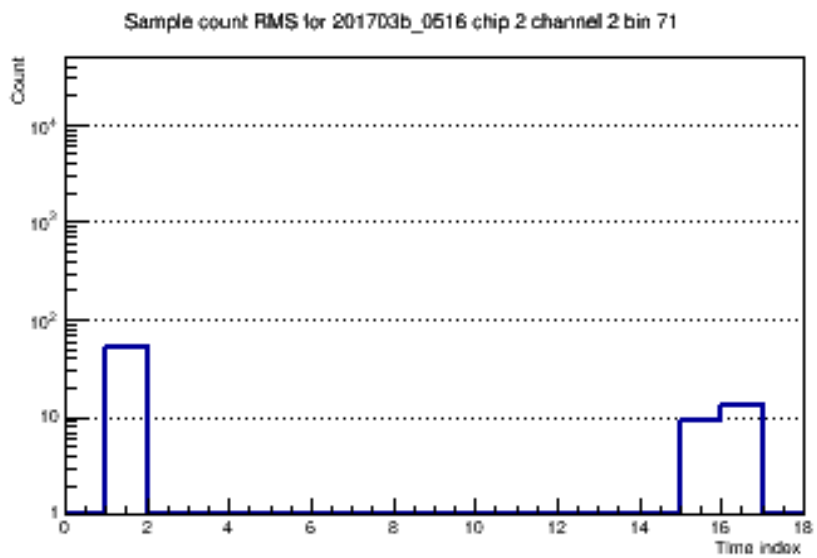


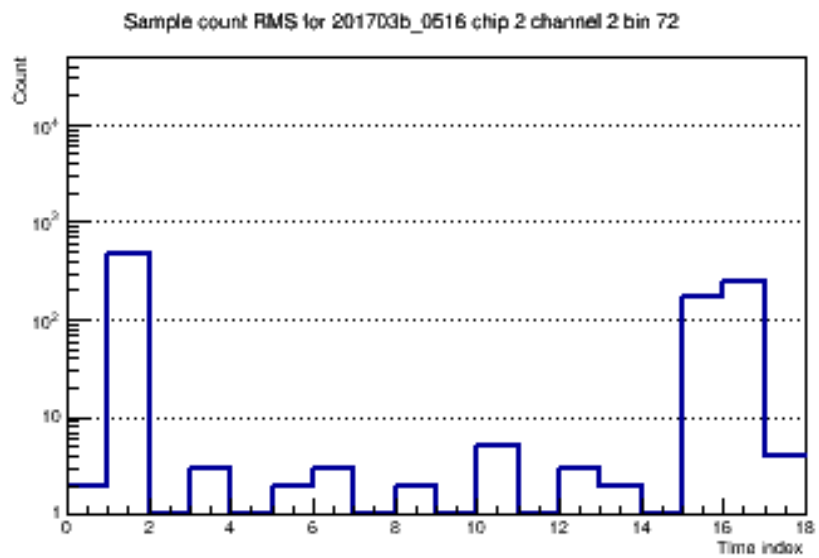


Time varying bins 21

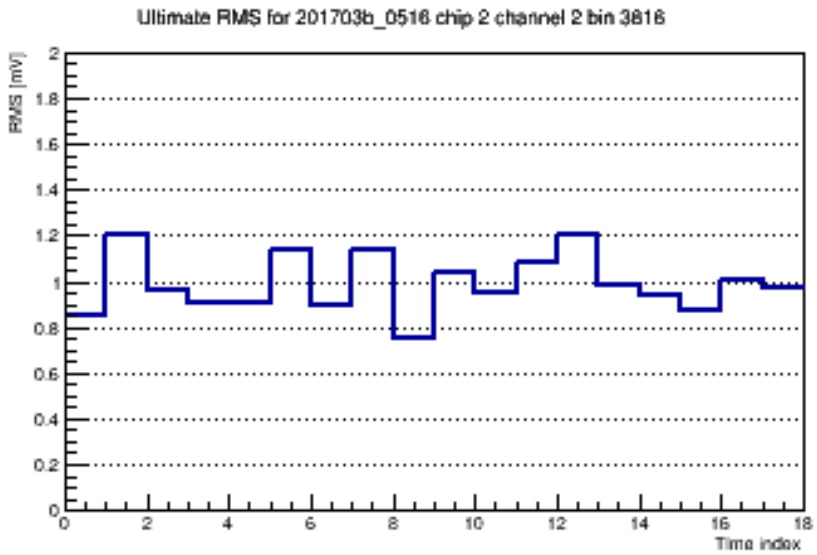


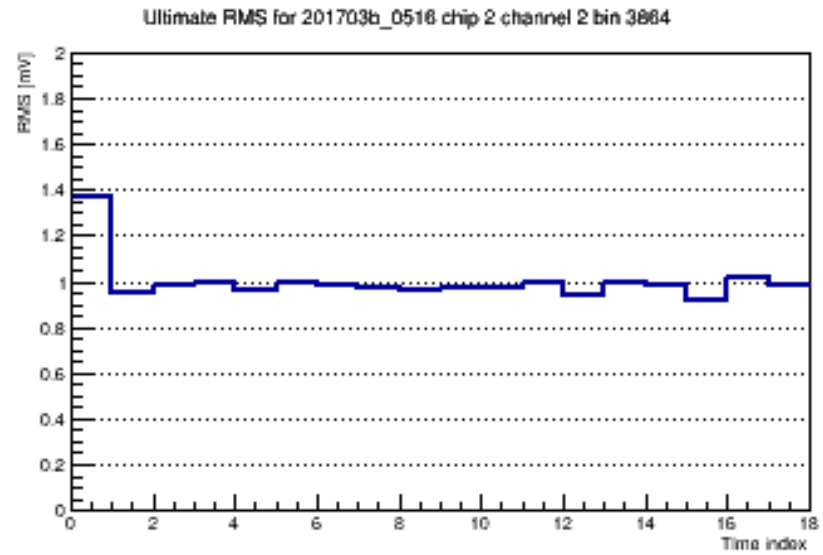


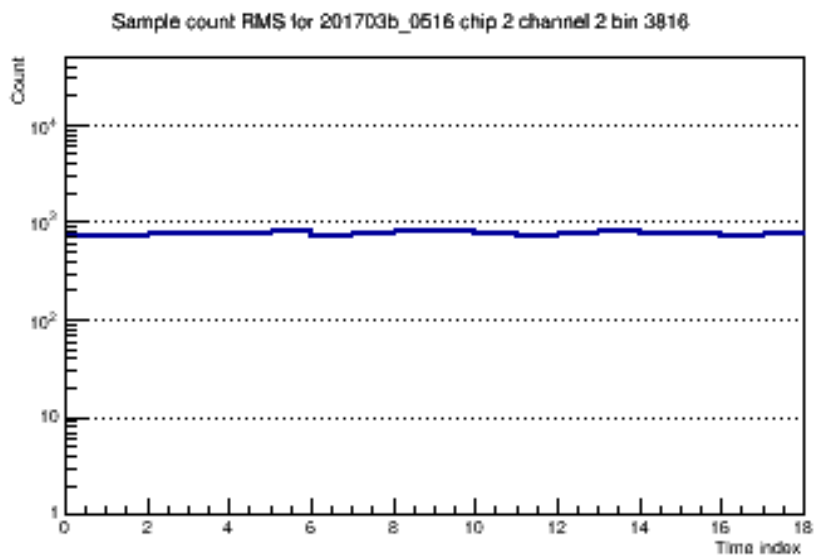


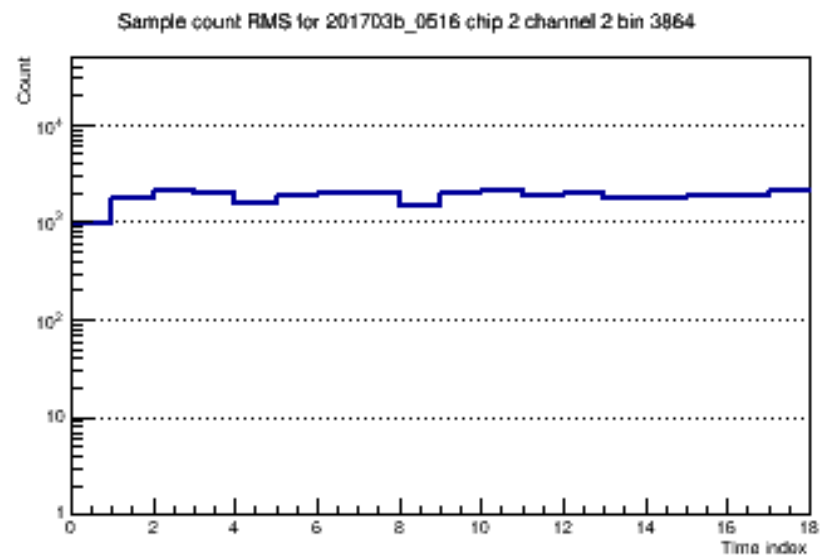


Time varying bins 22

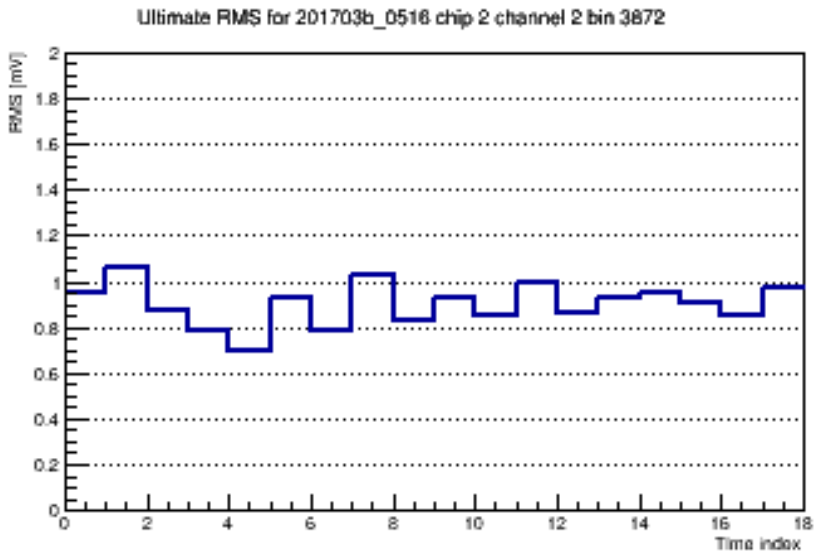


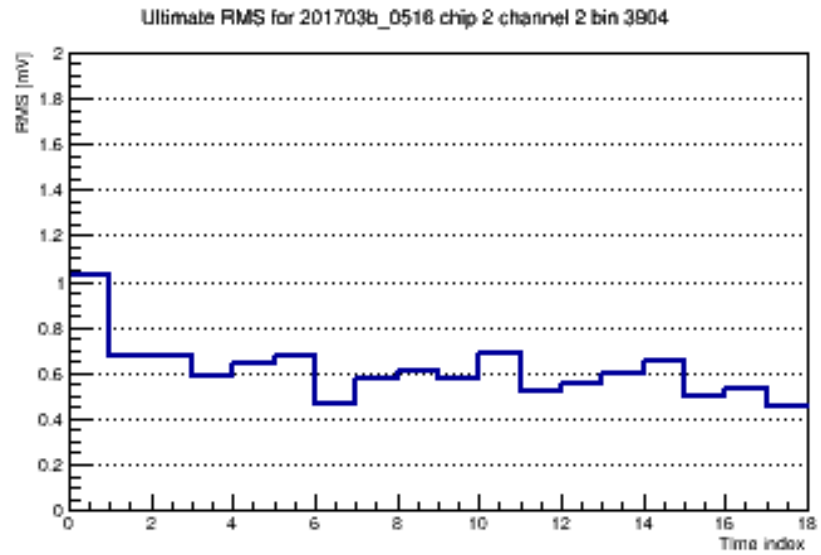


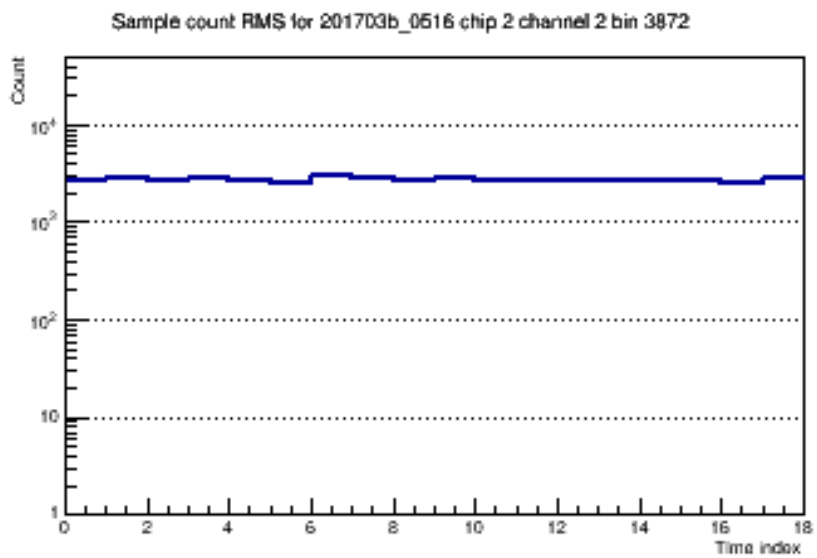


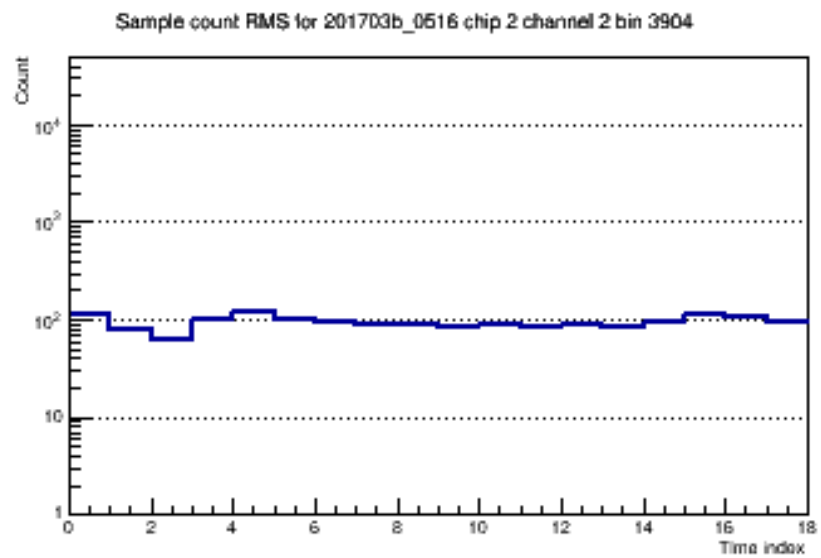


Time varying bins 23

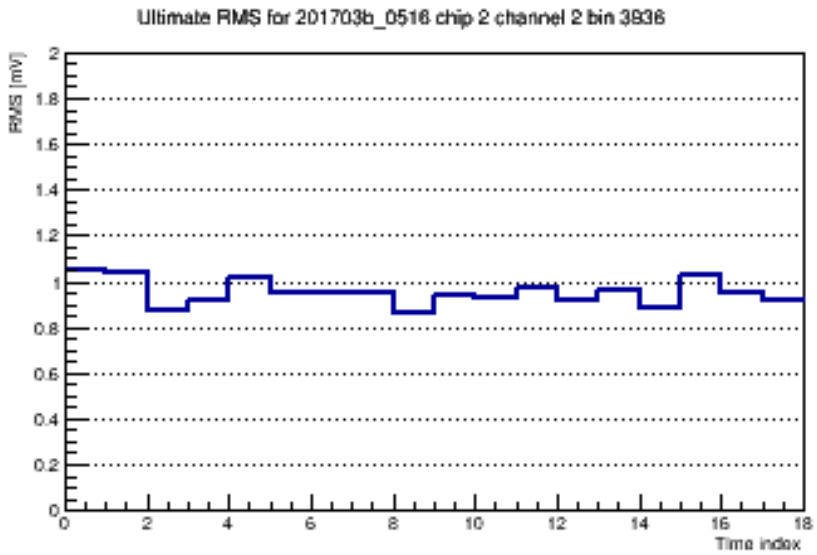


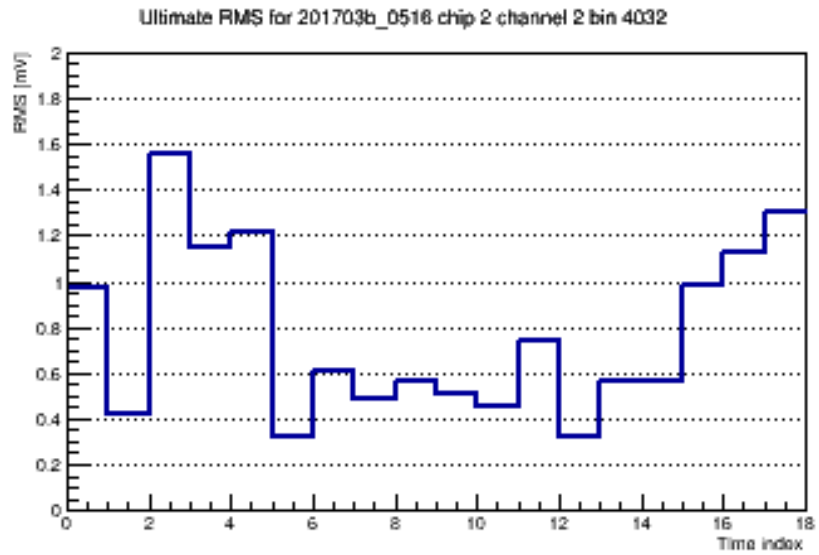


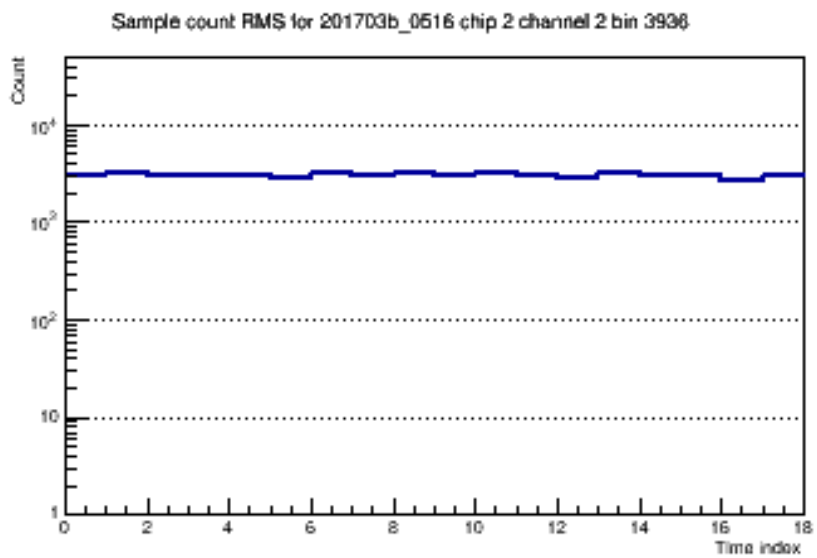


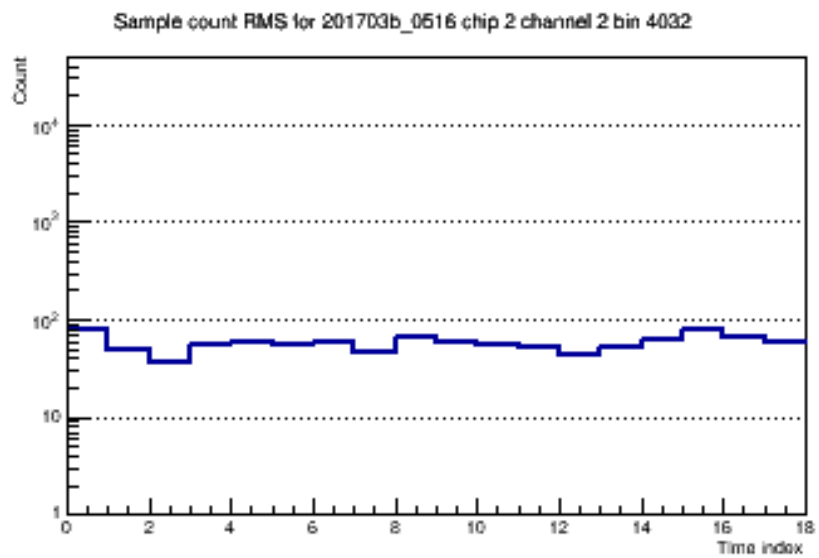


Time varying bins 24

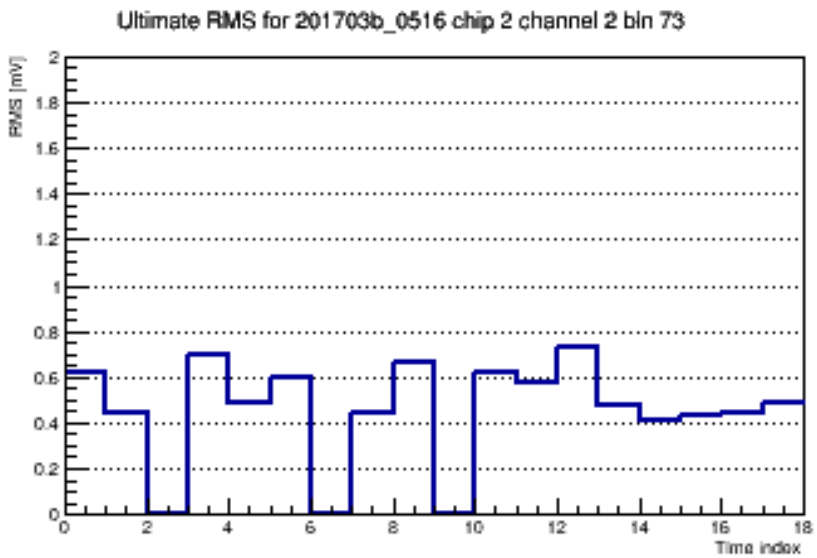


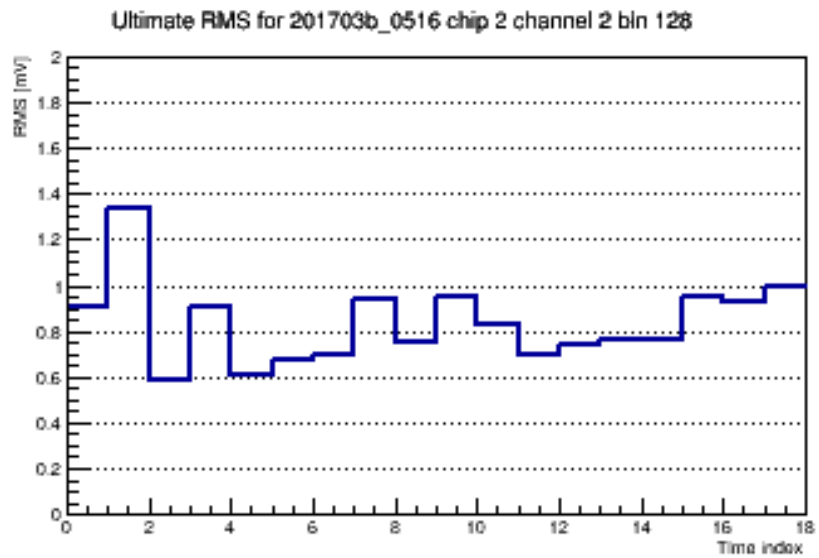


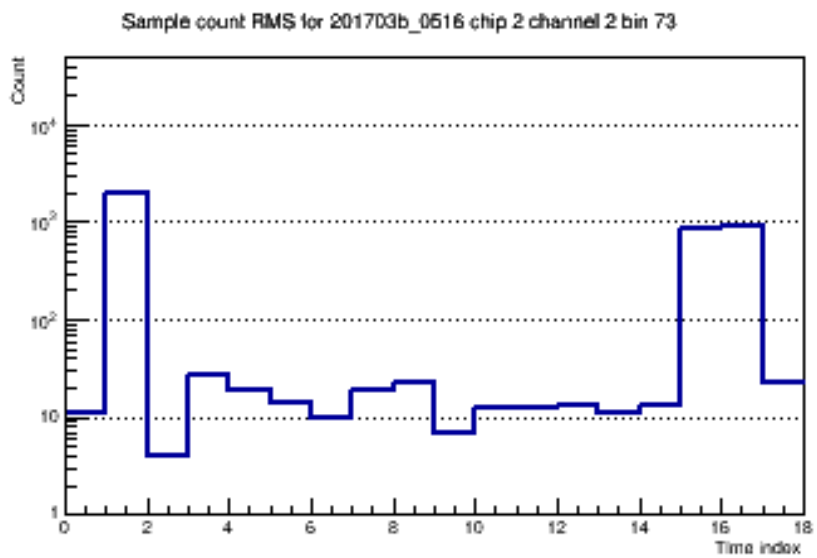


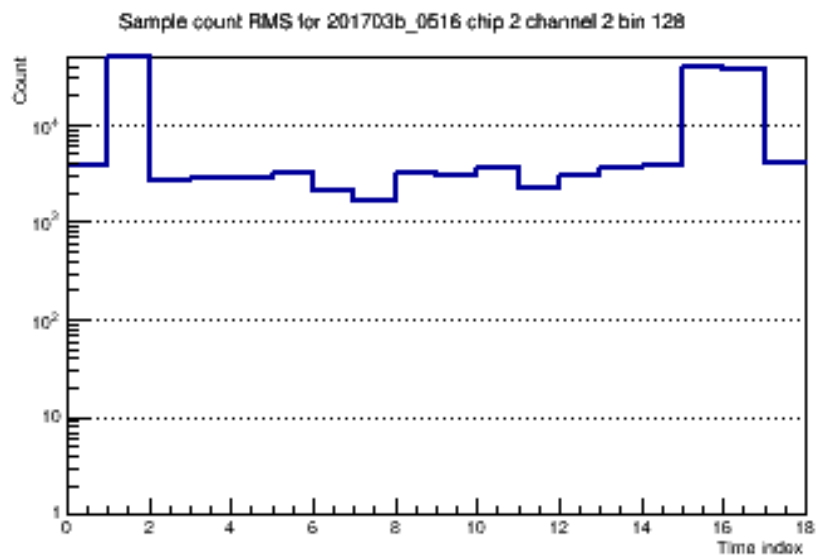


Time varying bins 25

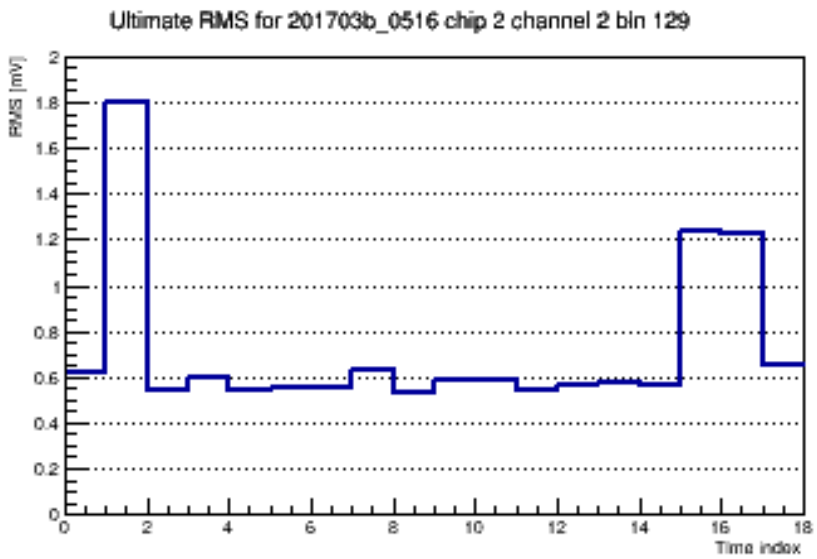


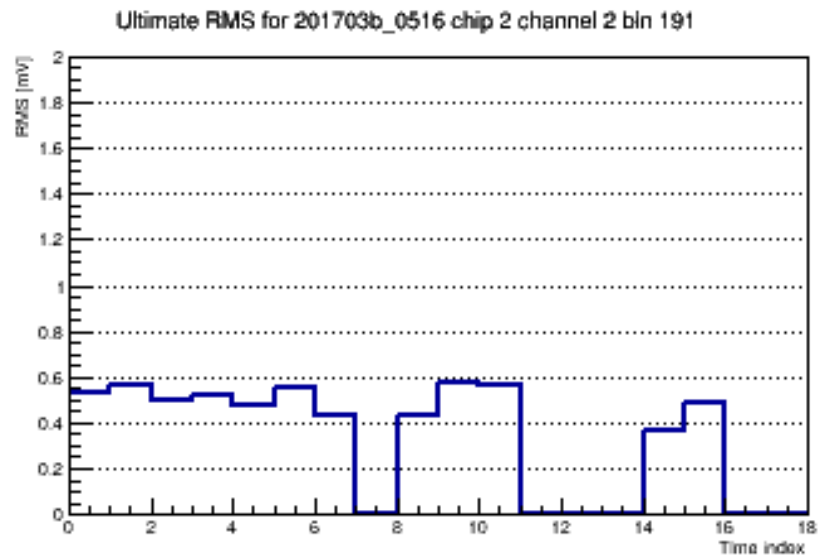


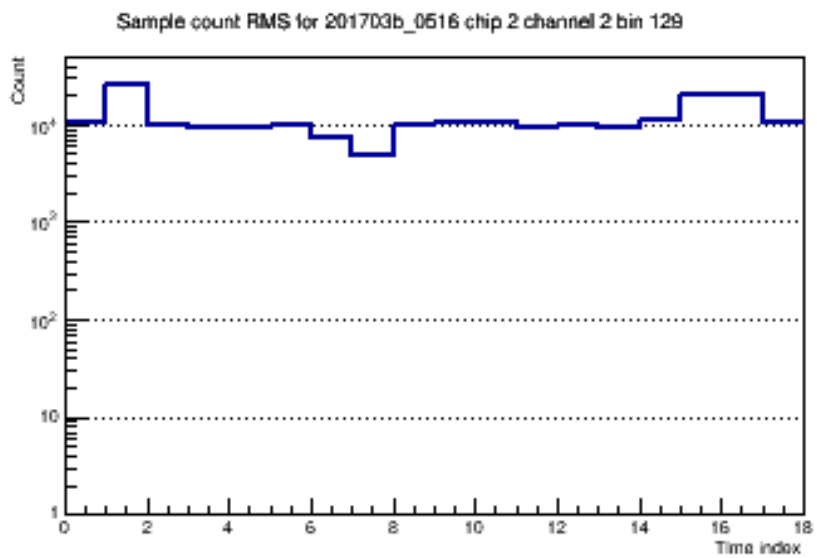


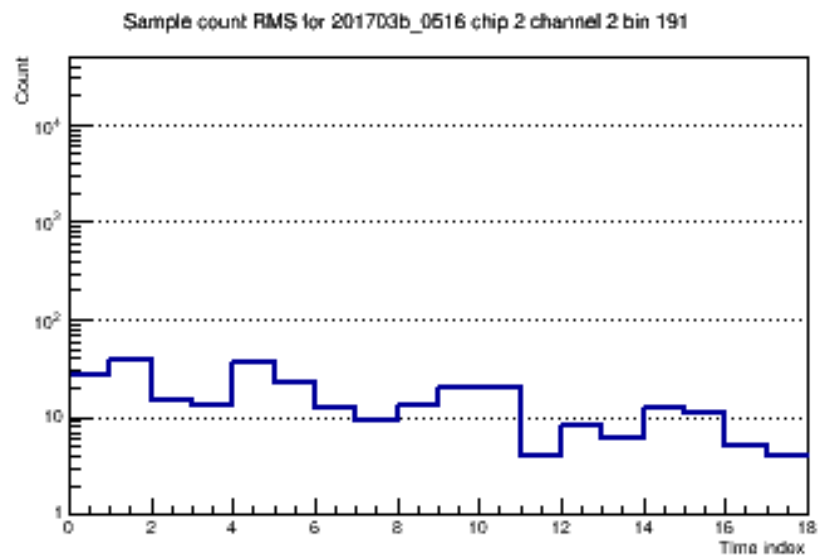


Time varying bins 26

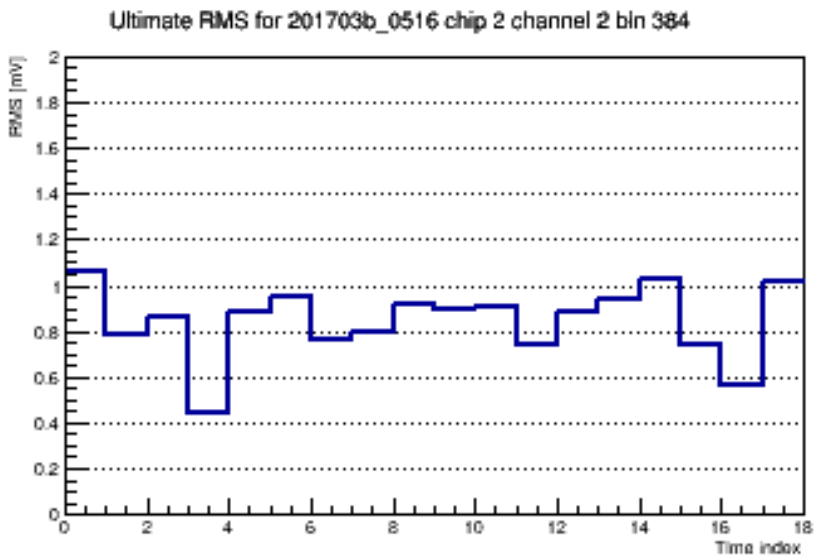


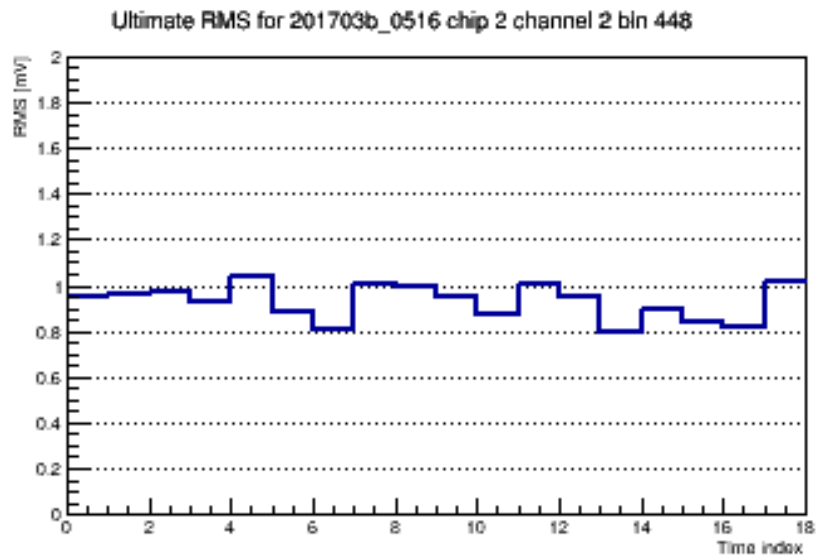


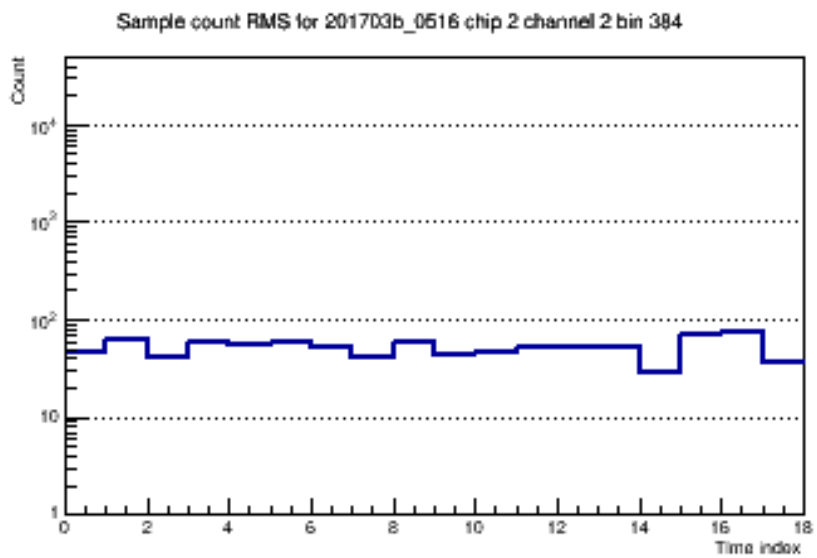


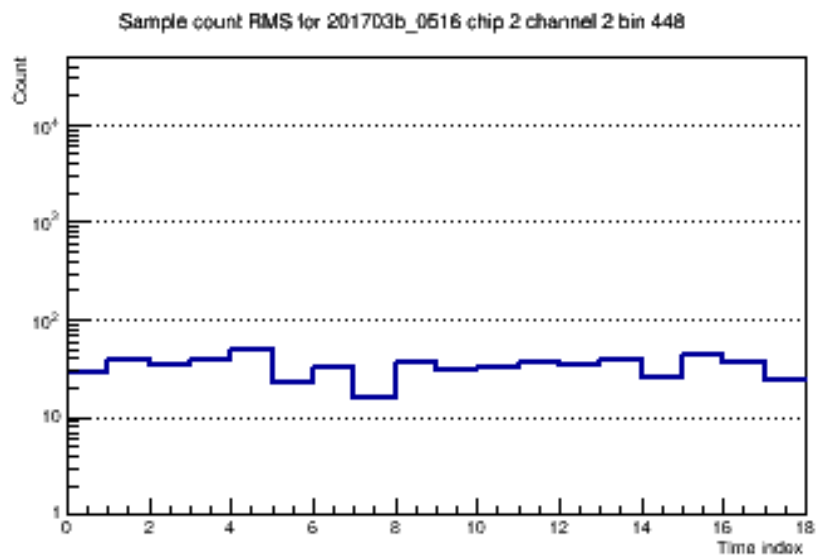


Time varying bins 27

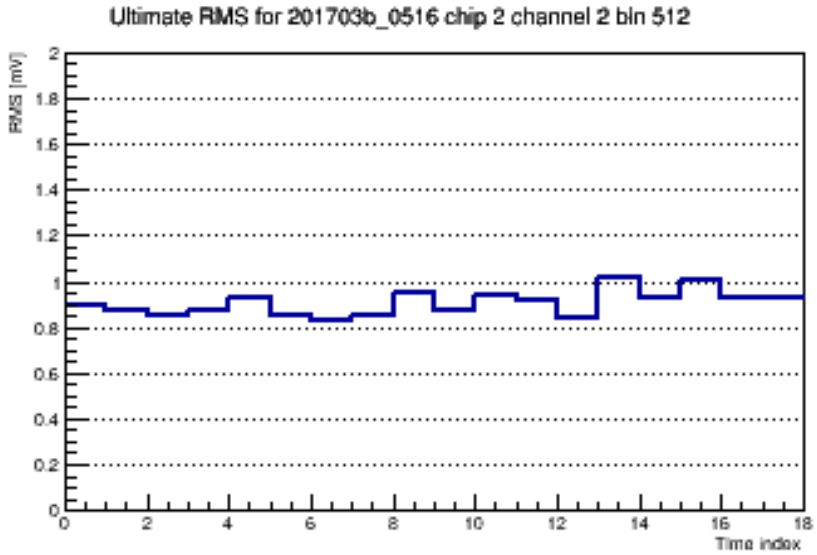


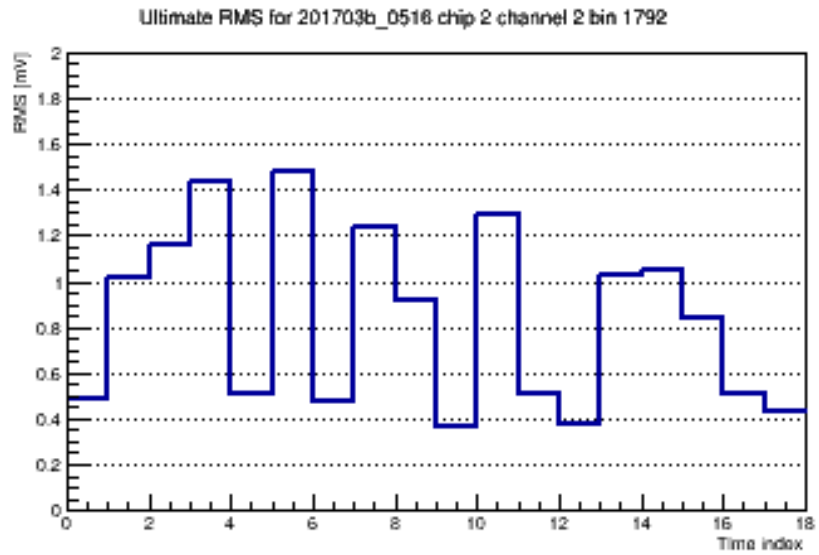


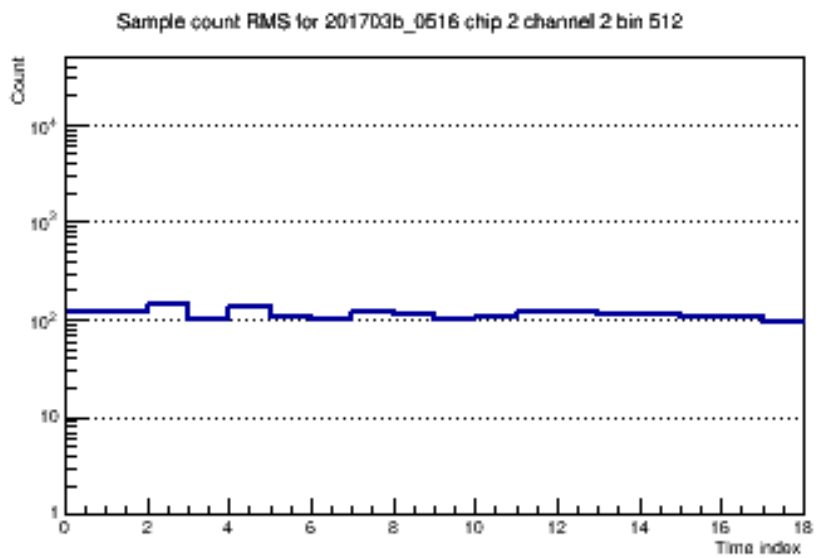


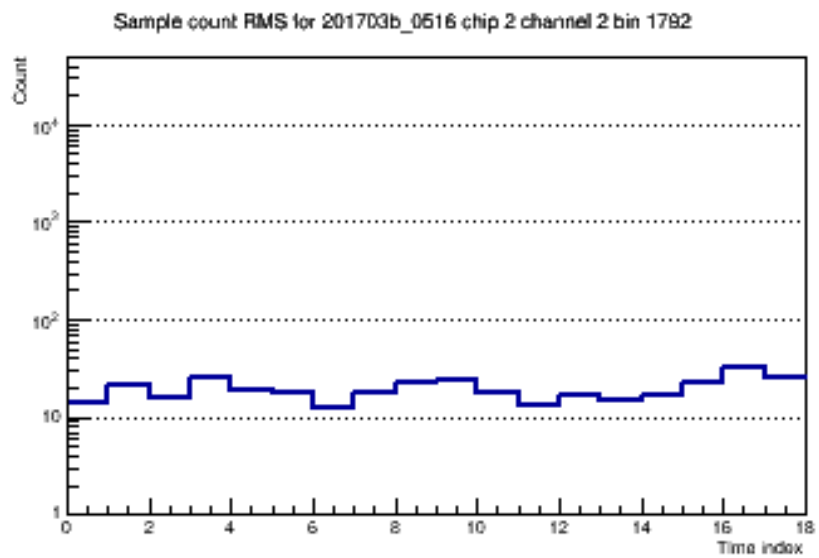


Time varying bins 28

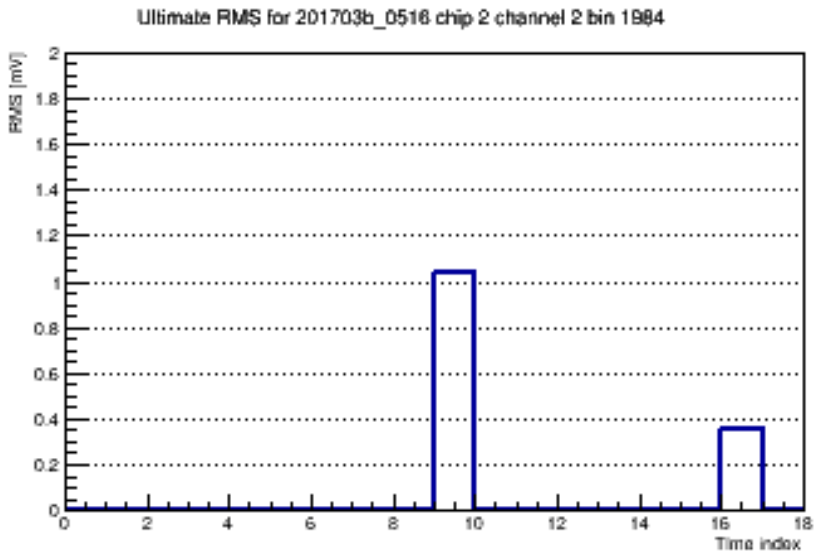


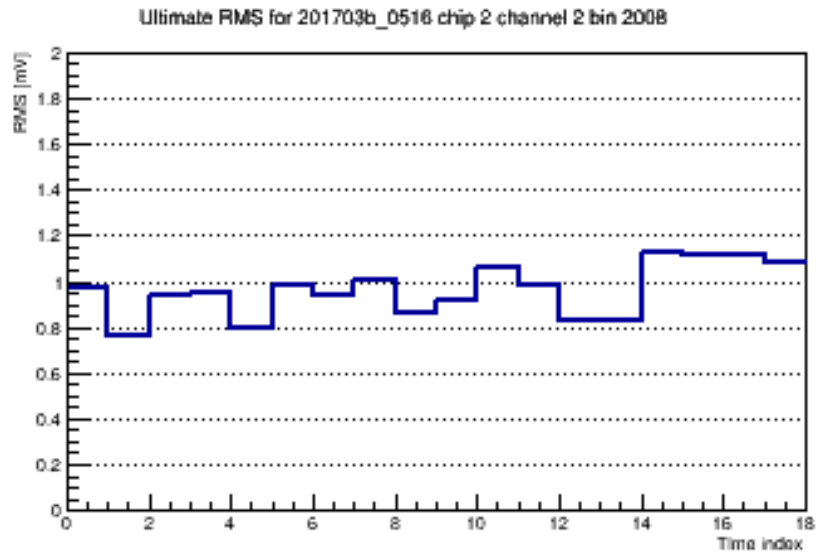


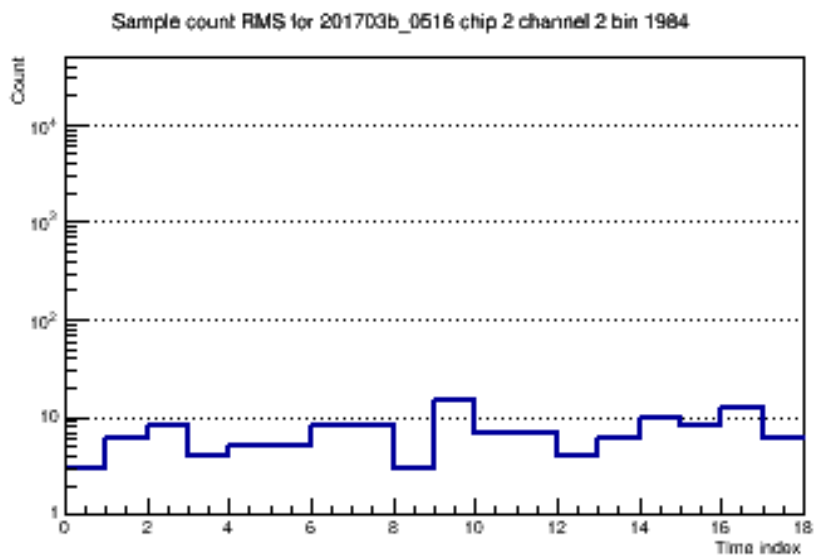


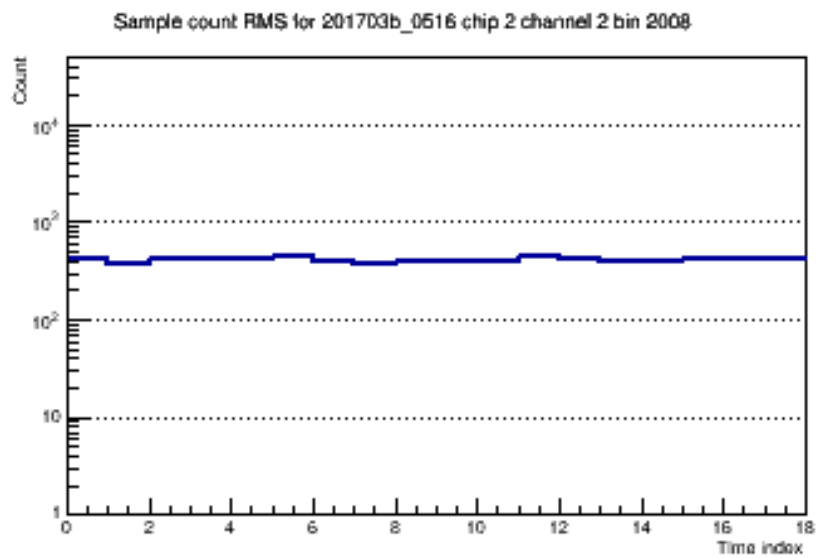


Time varying bins 29

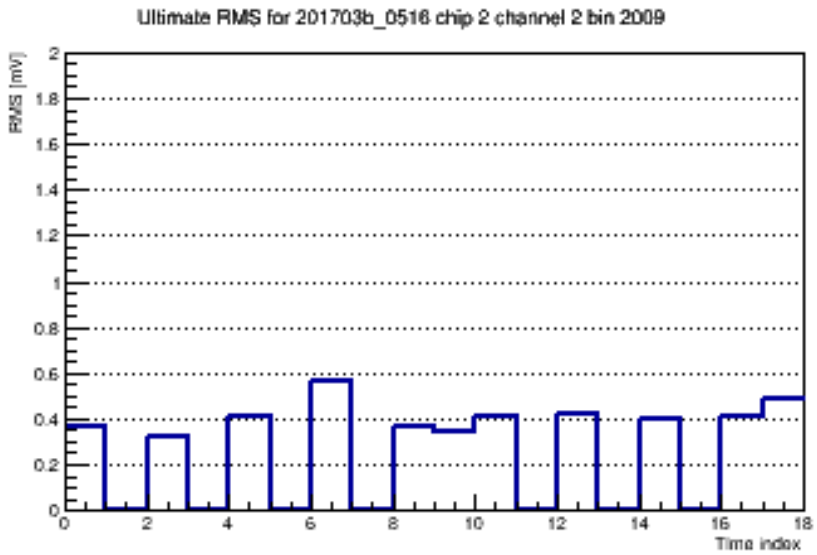


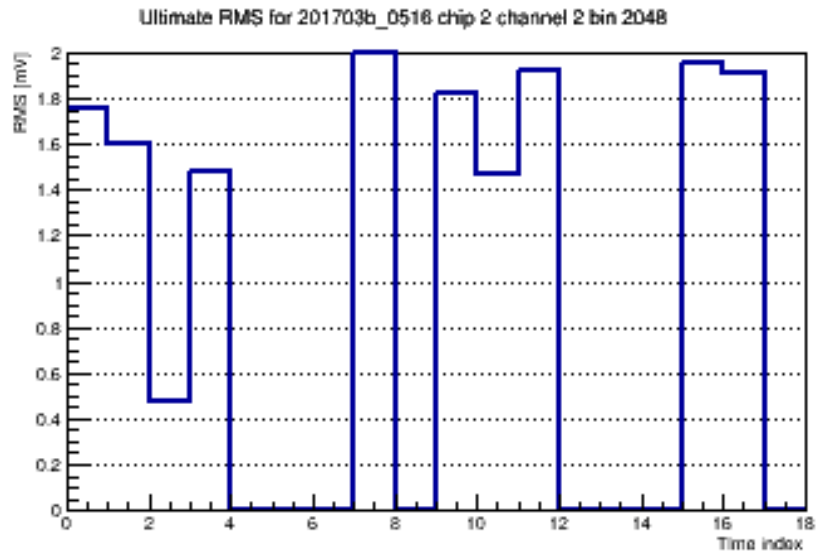


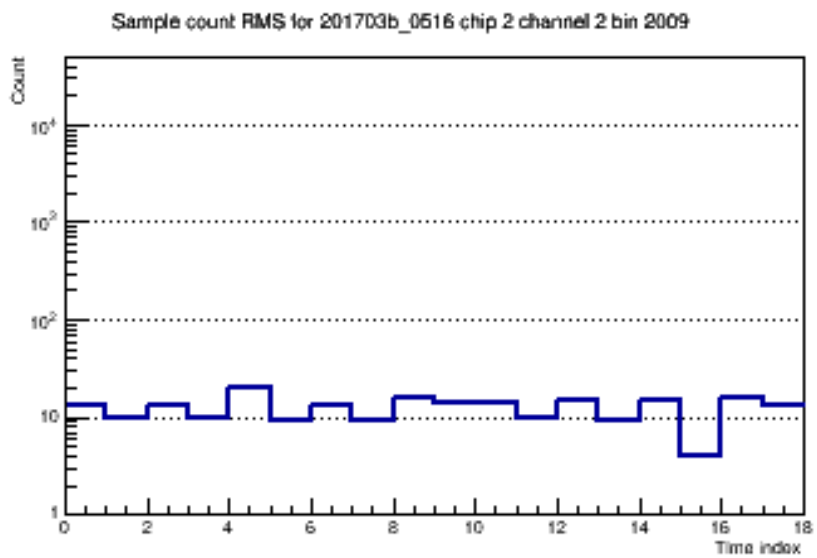


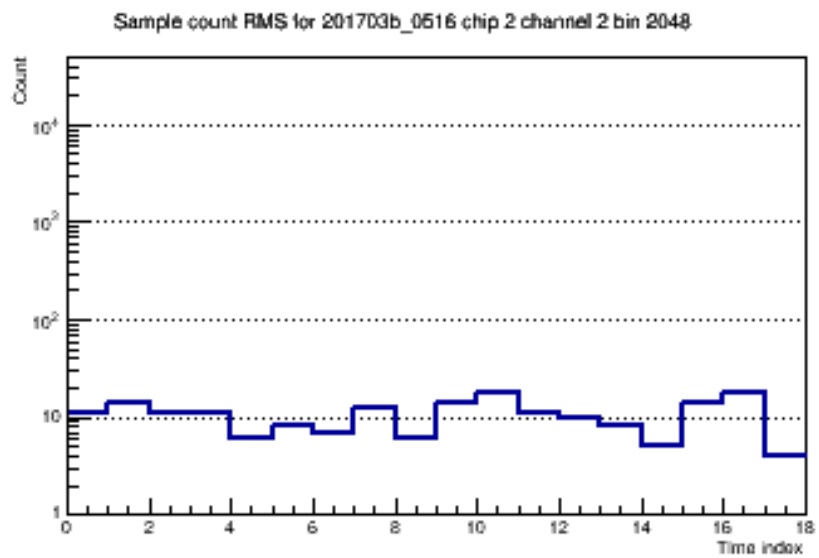


Time varying bins 30

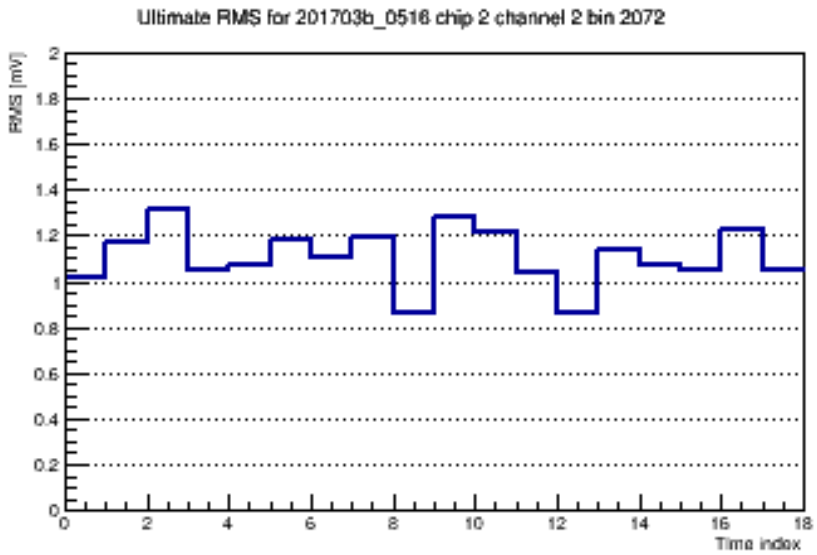


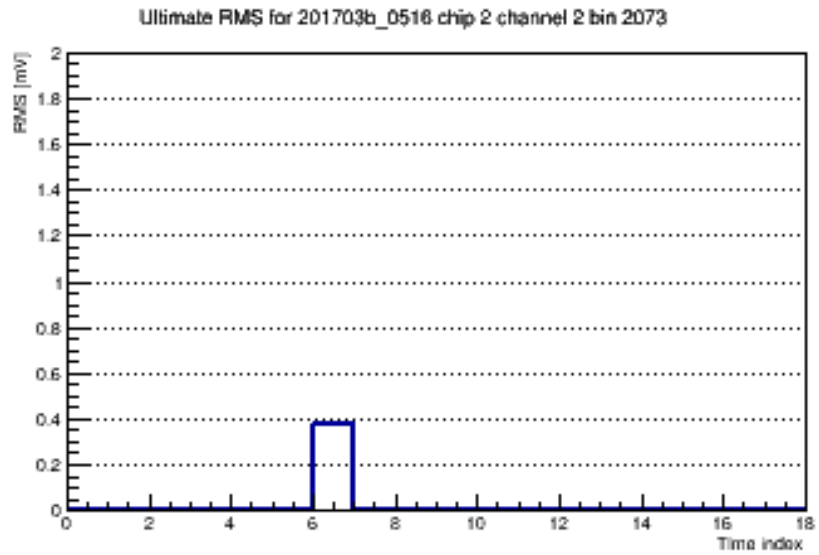


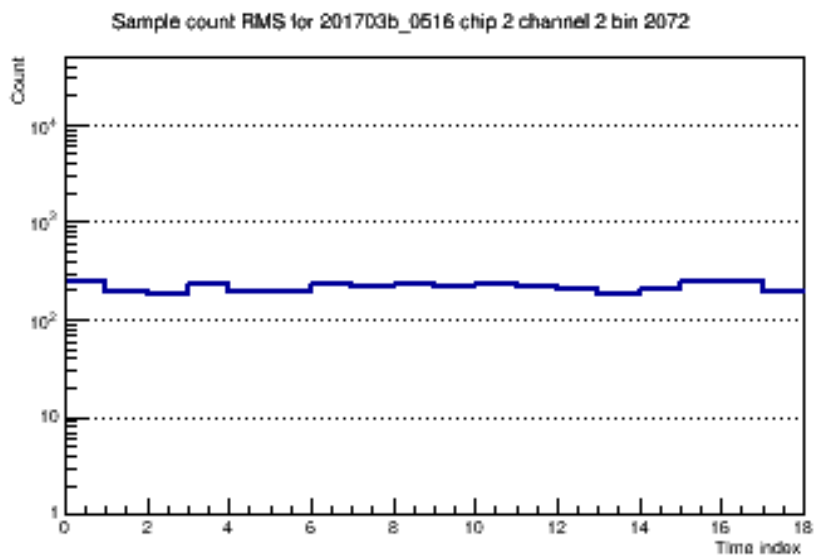


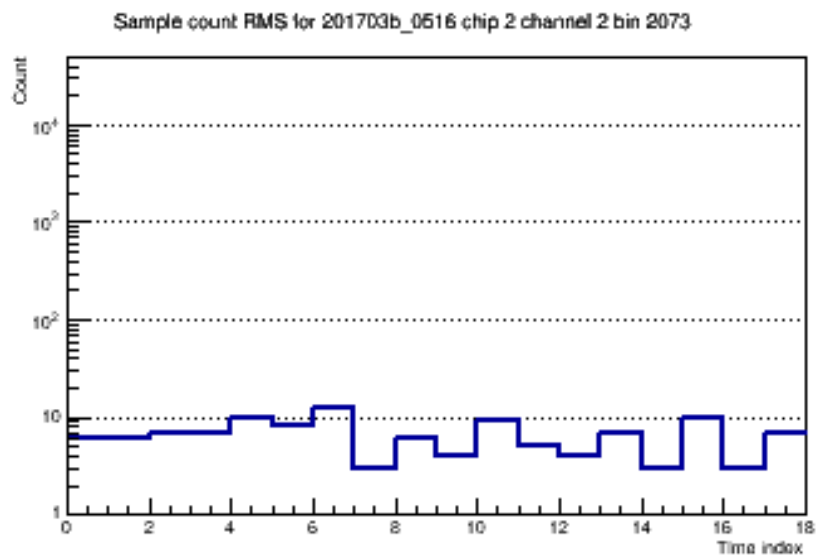


Time varying bins 31

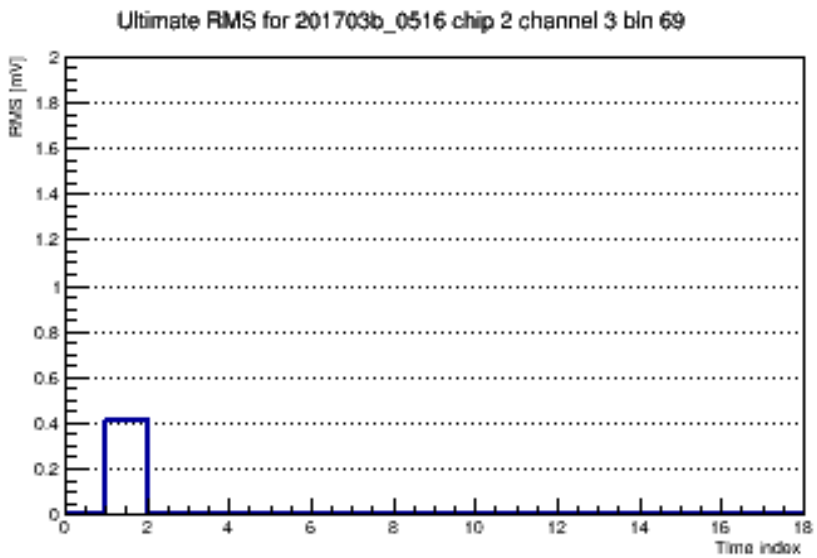


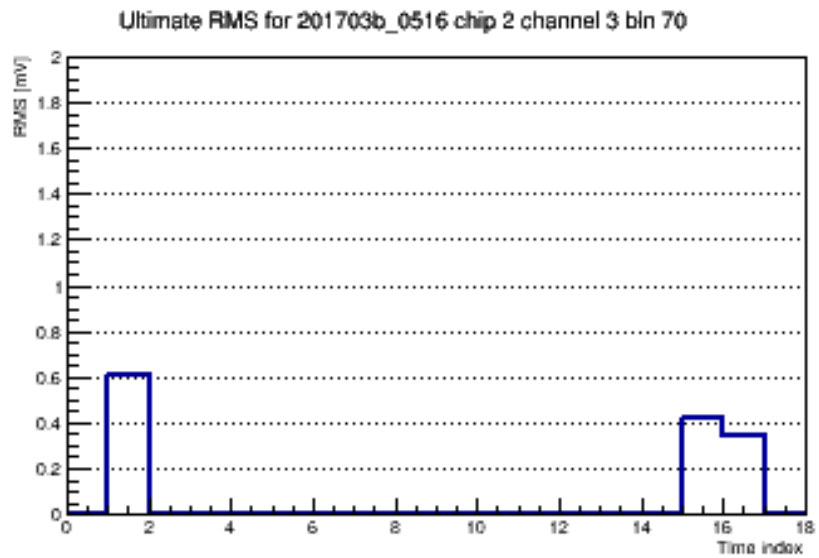


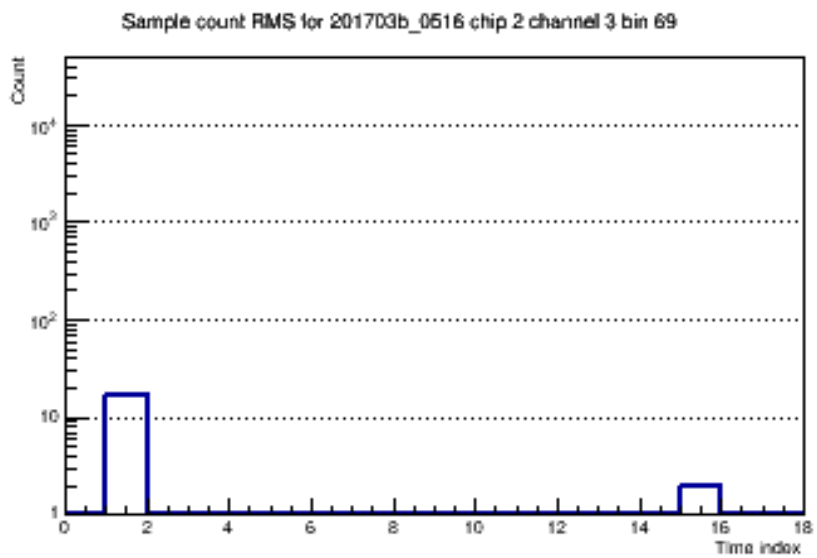


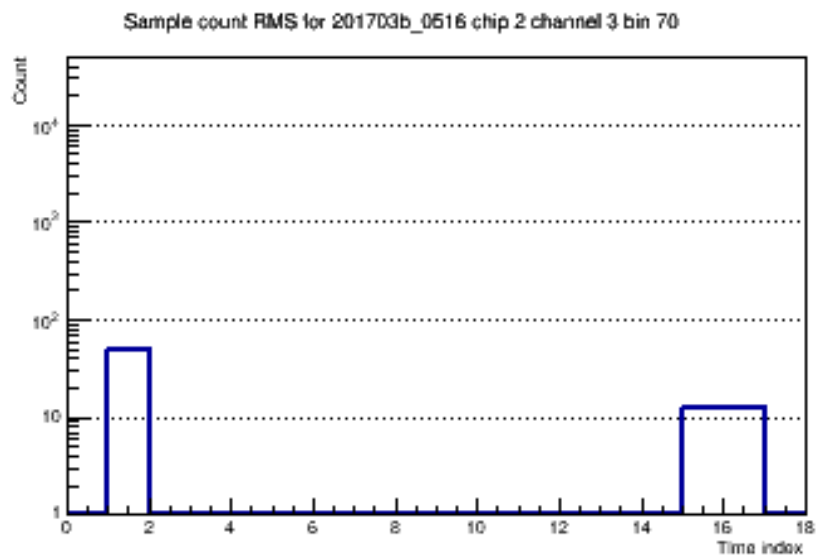


Time varying bins 32

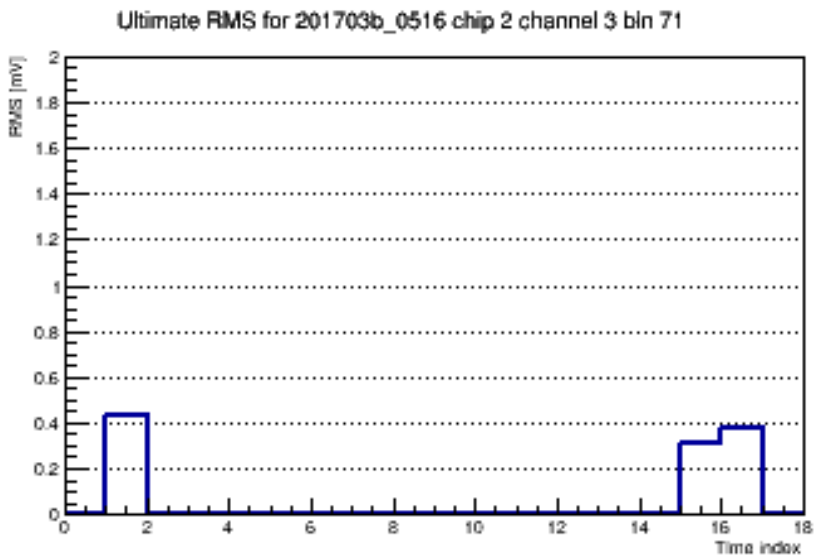


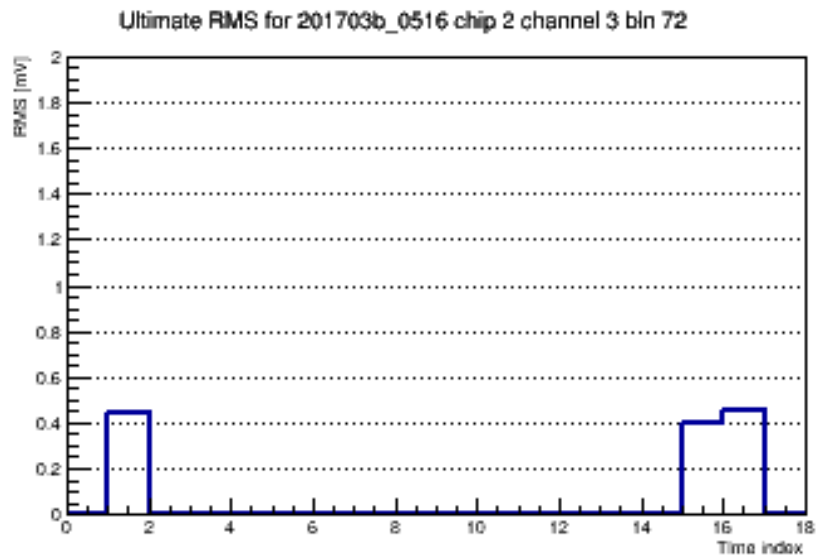


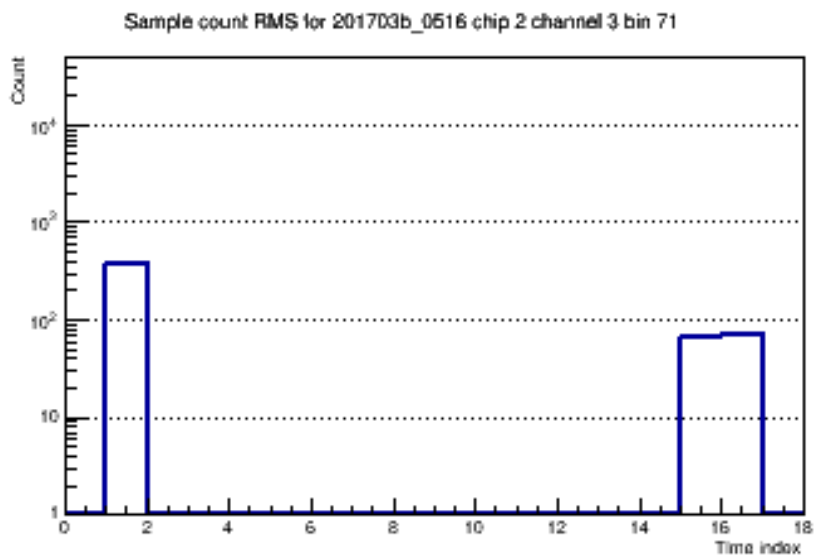


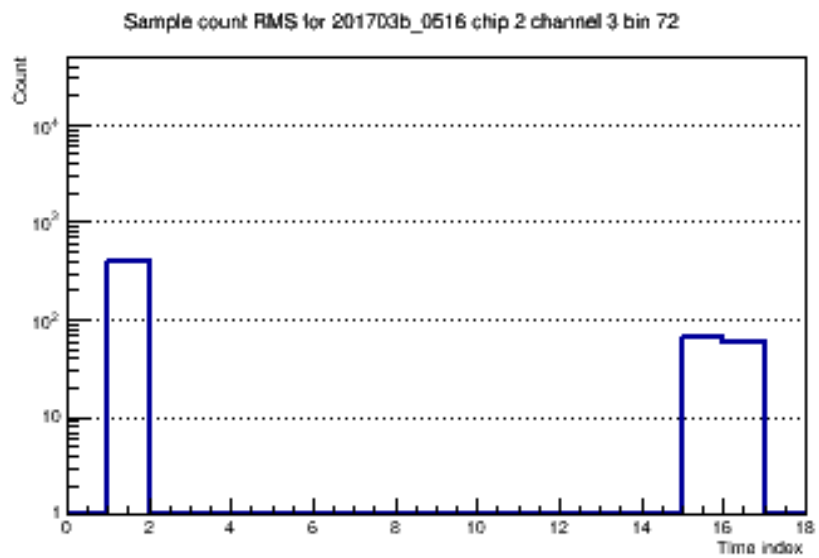


Time varying bins 33

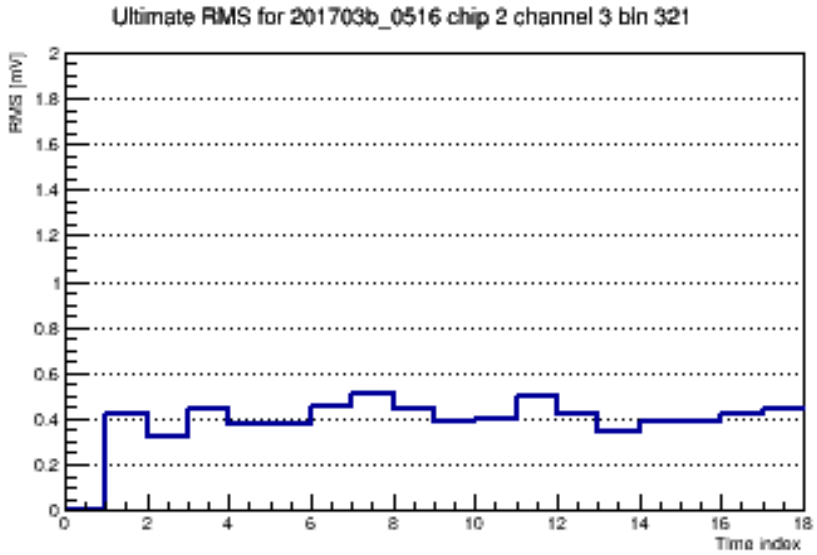


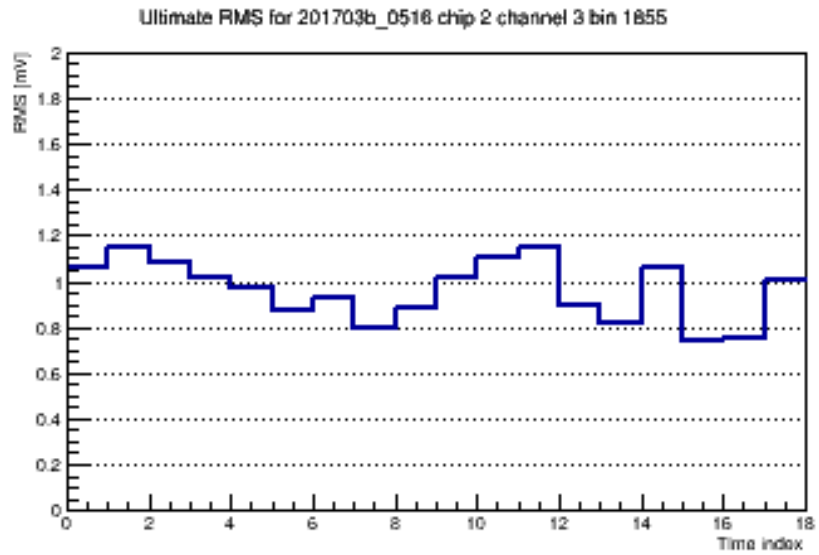


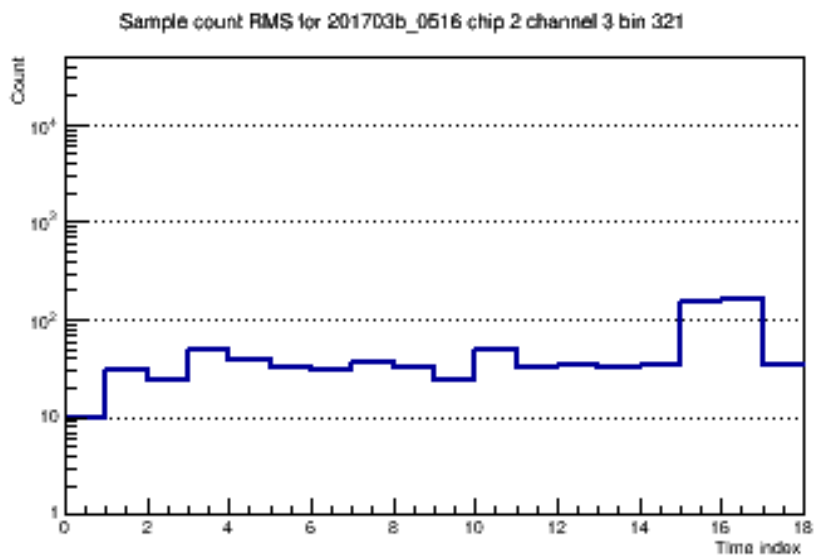


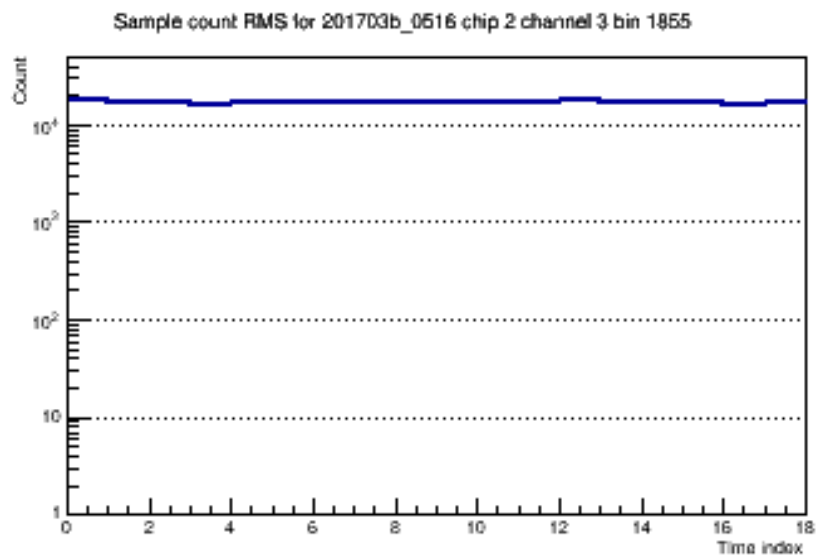


Time varying bins 34

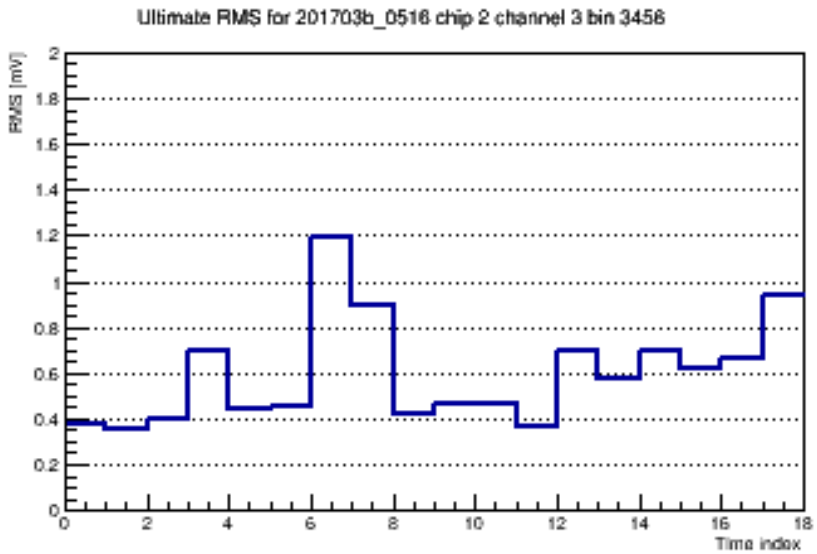


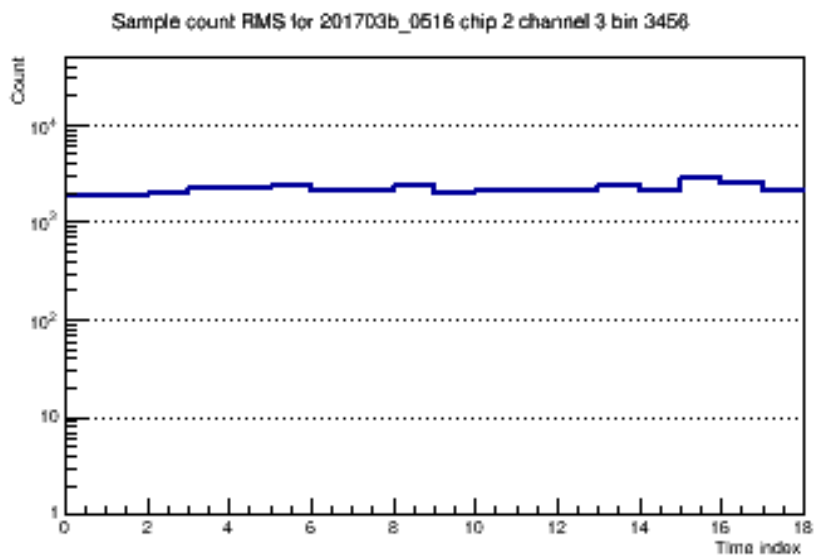




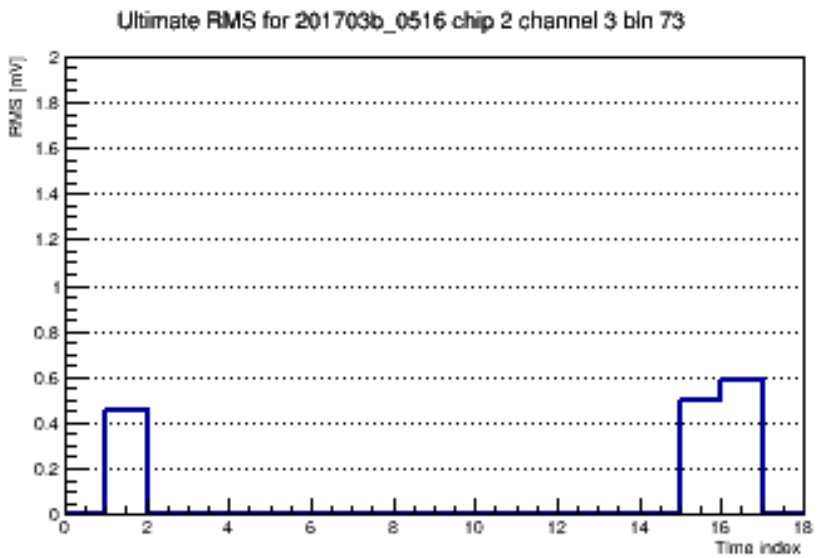


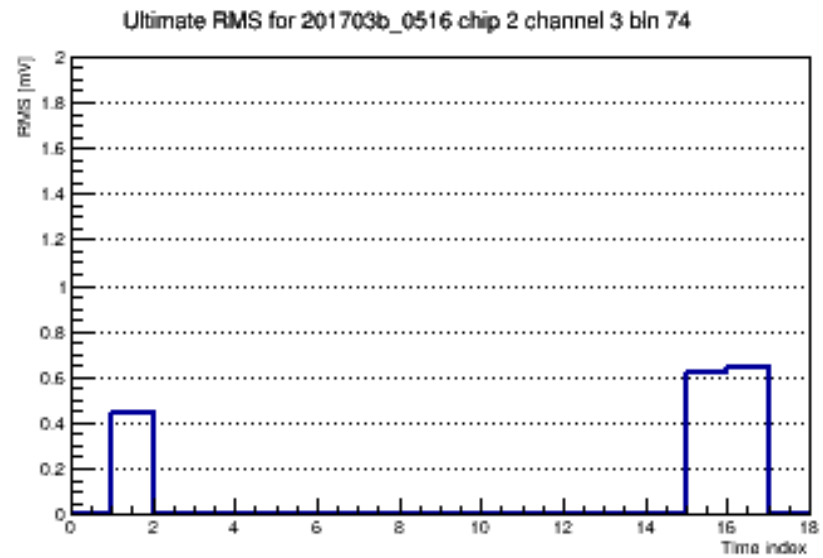
Time varying bins 35

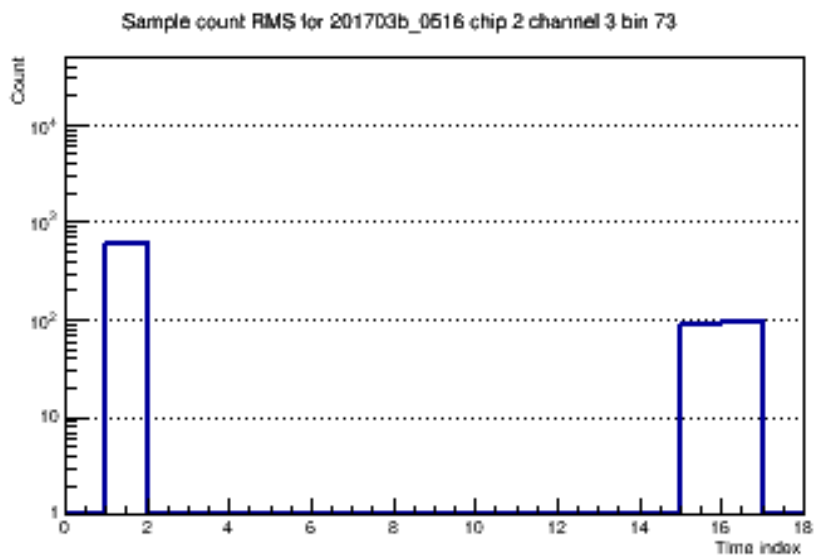


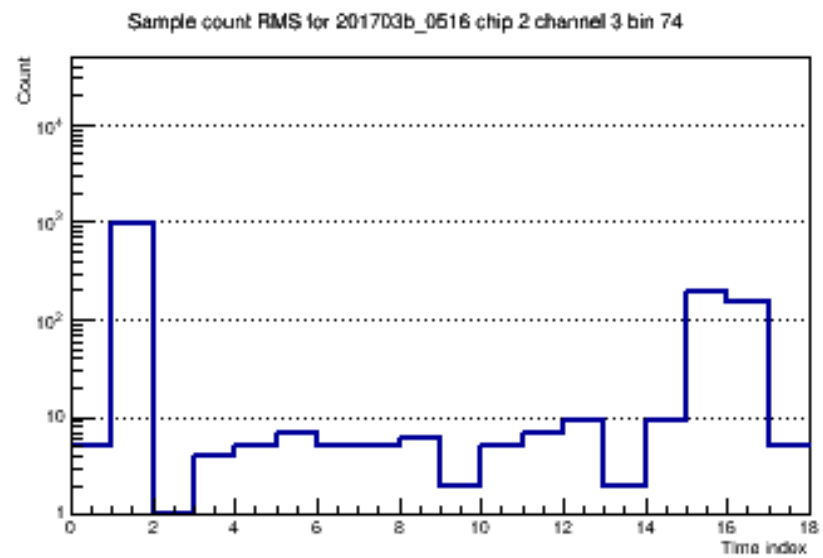


Time varying bins 36

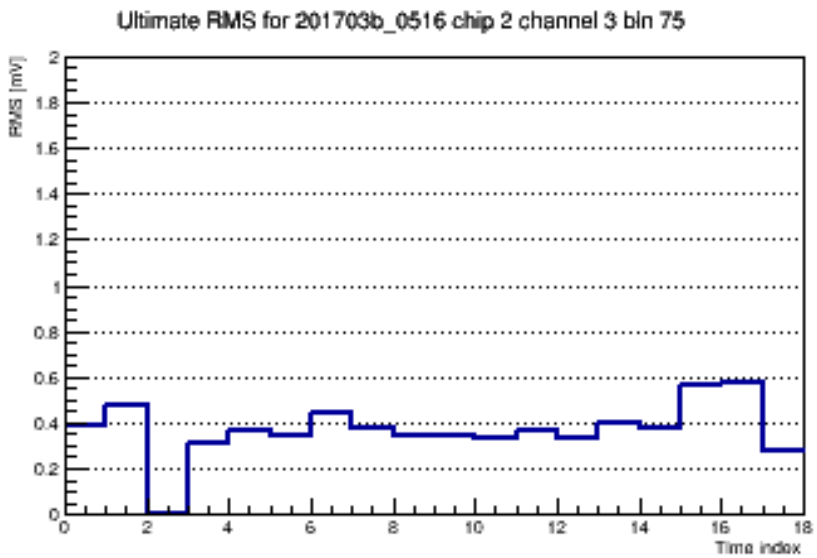


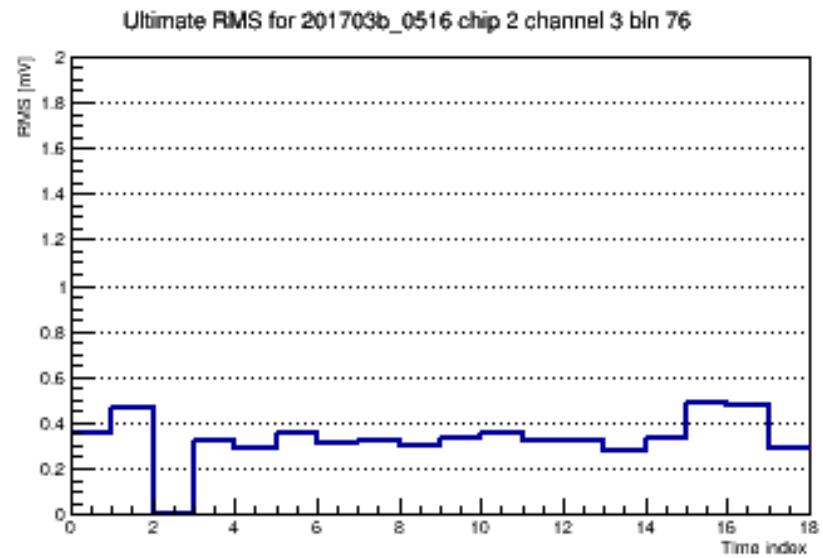


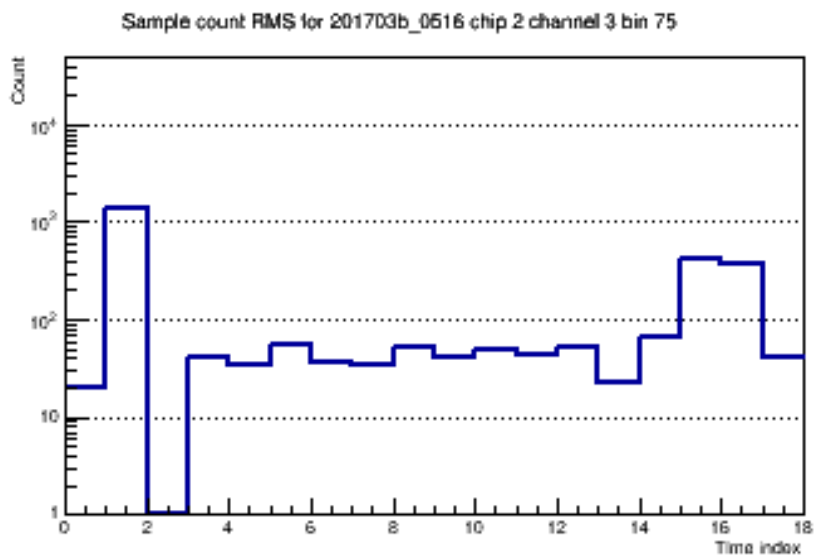


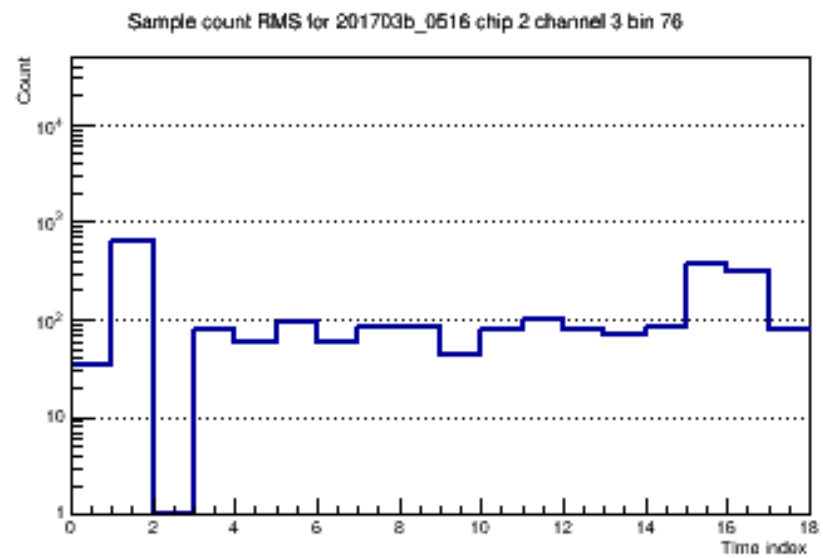


Time varying bins 37

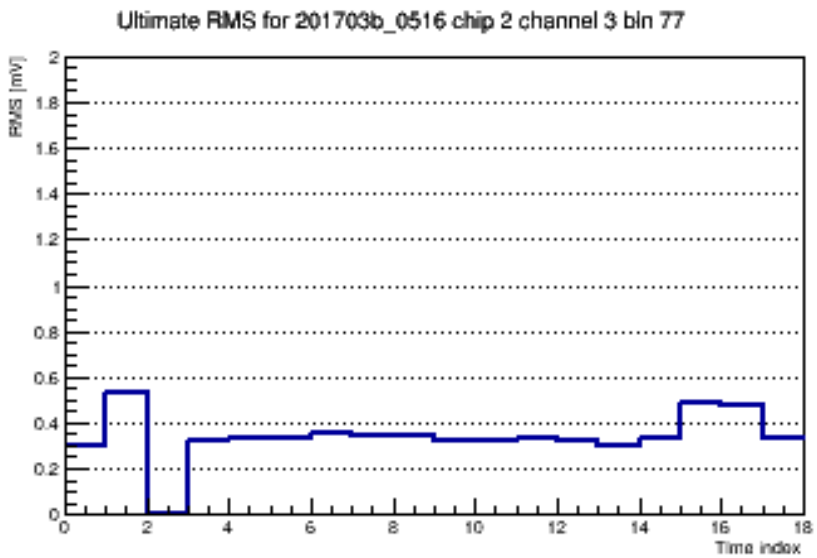


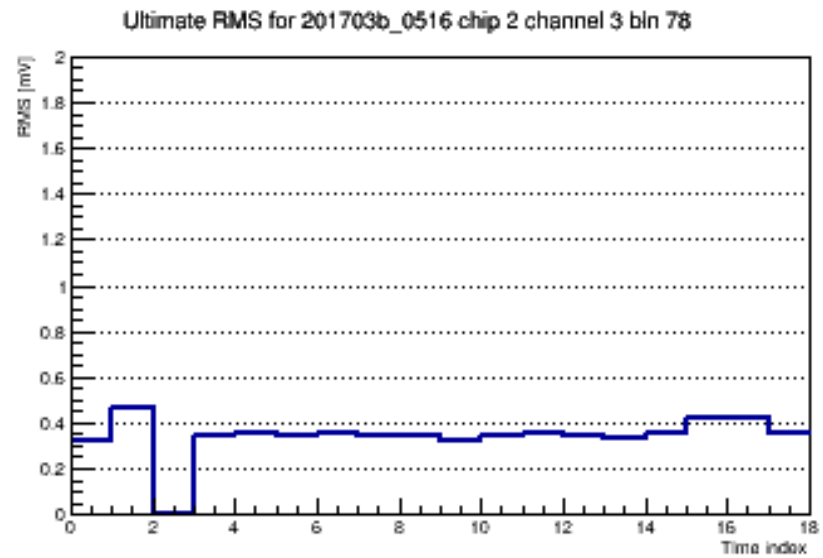


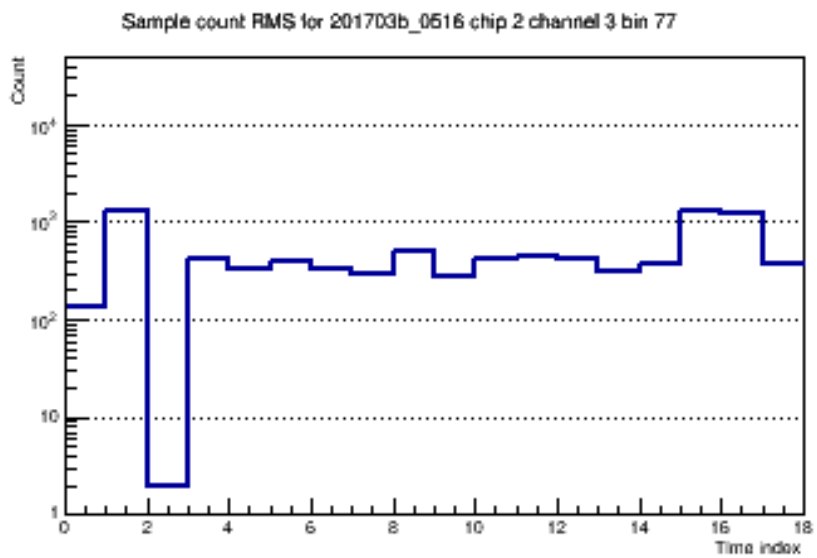


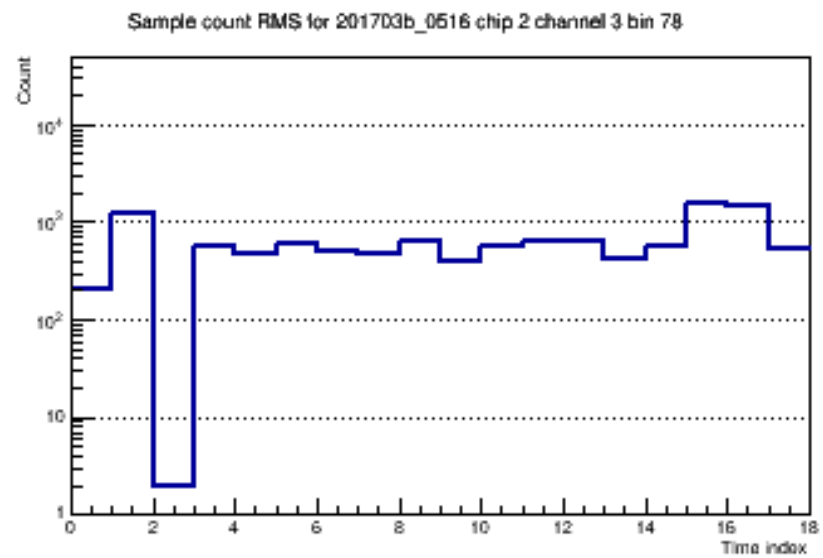


Time varying bins 38

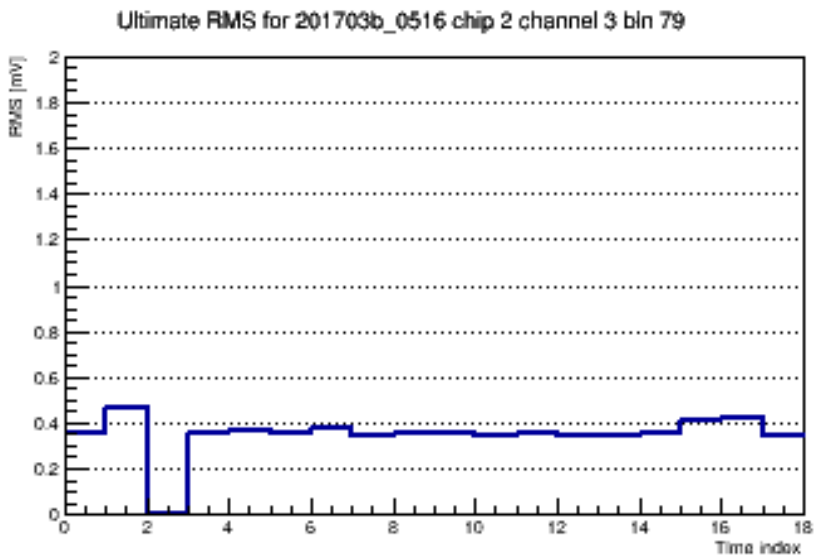


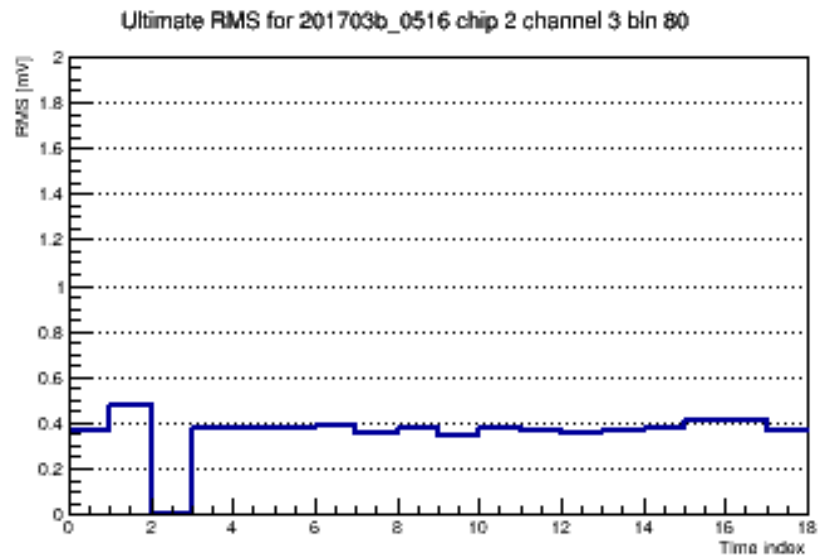


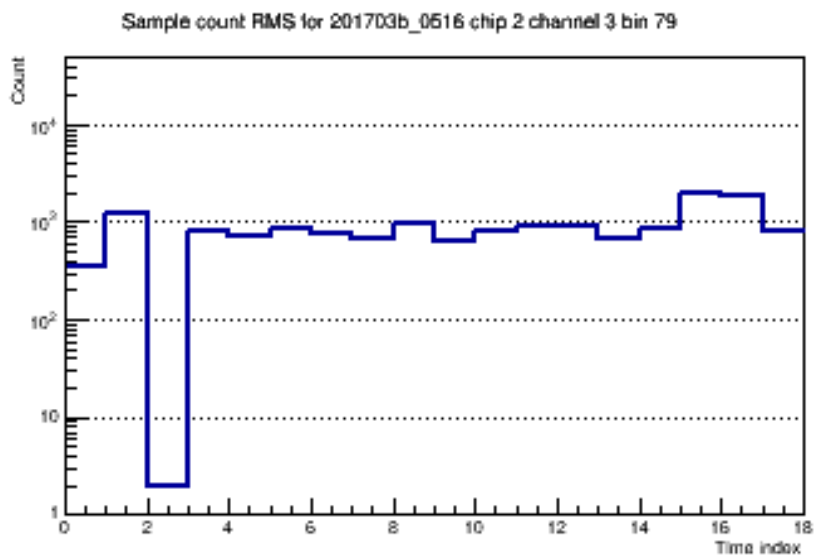


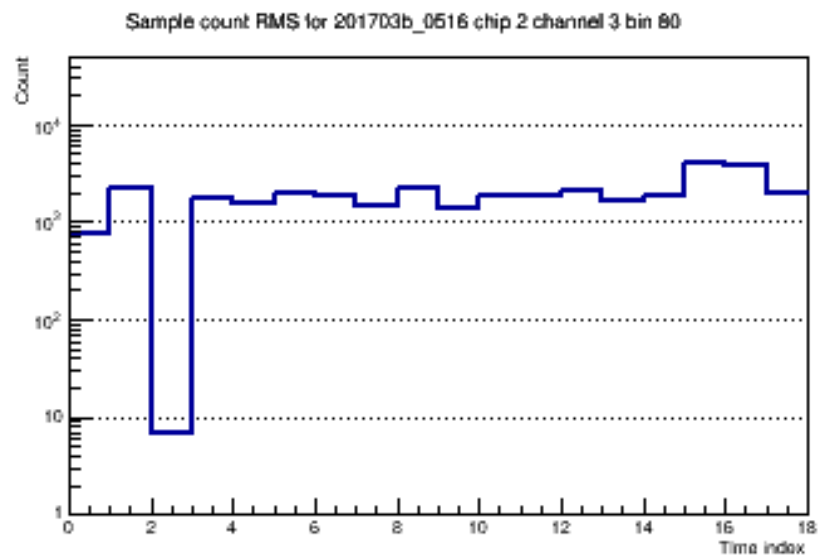


Time varying bins 39

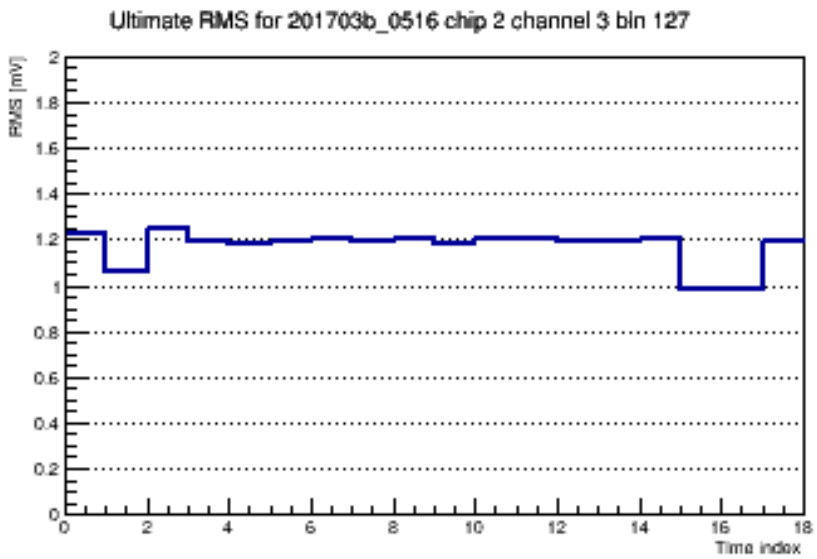


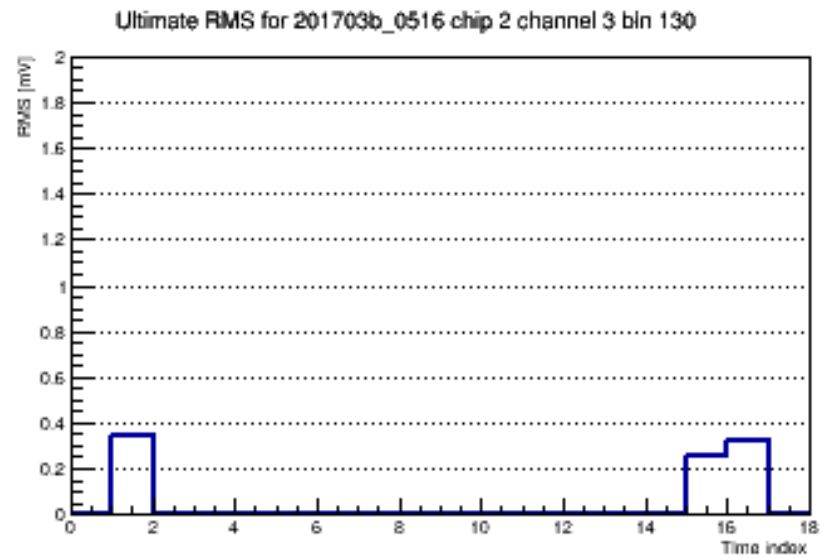


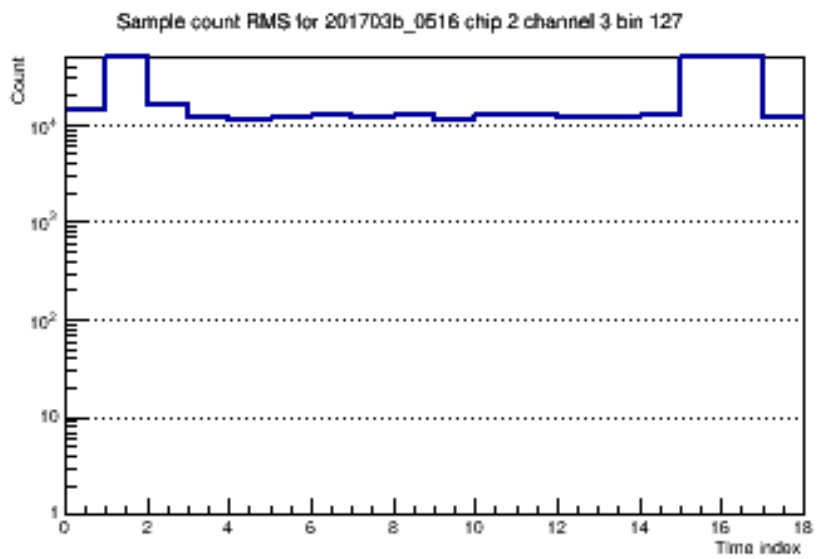


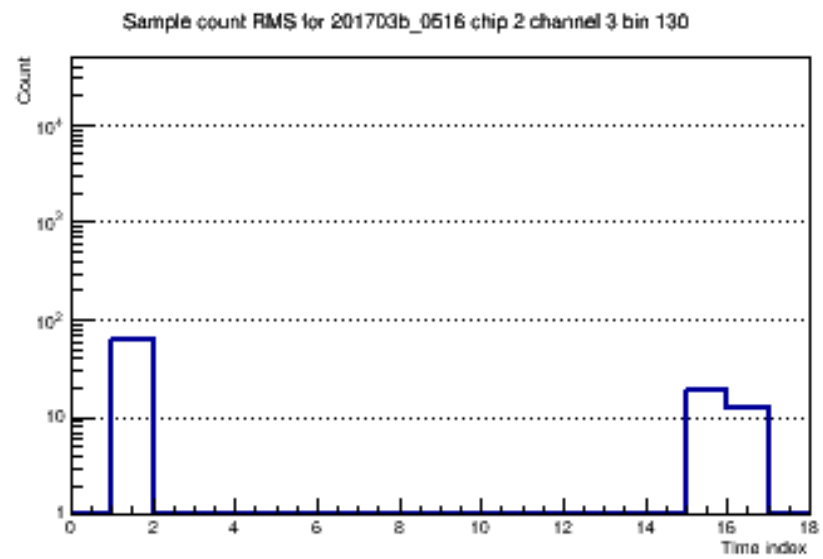


Time varying bins 40

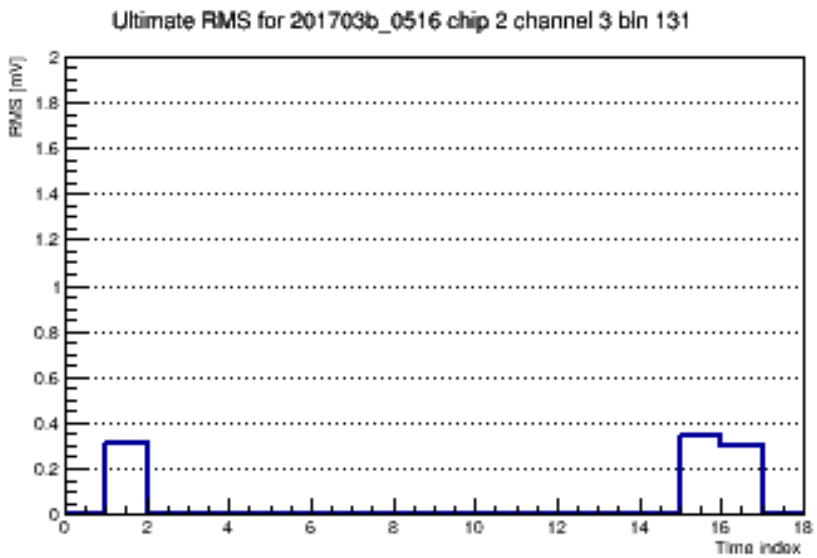


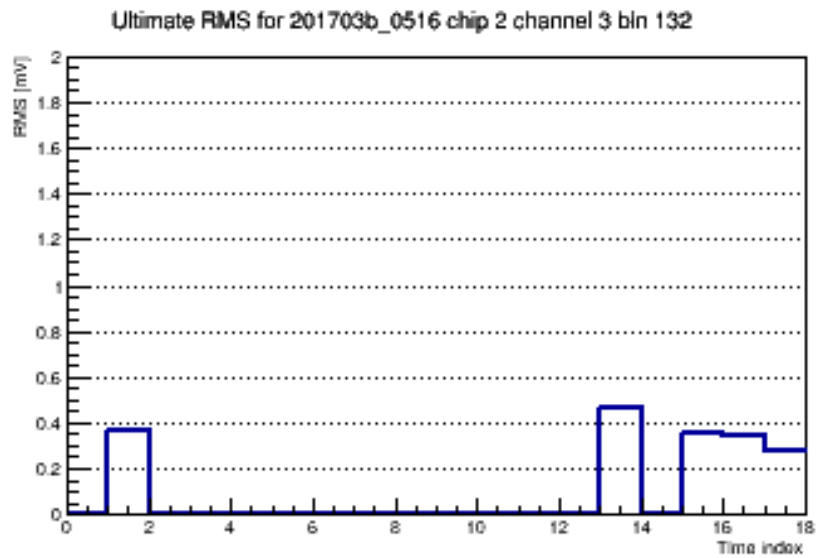


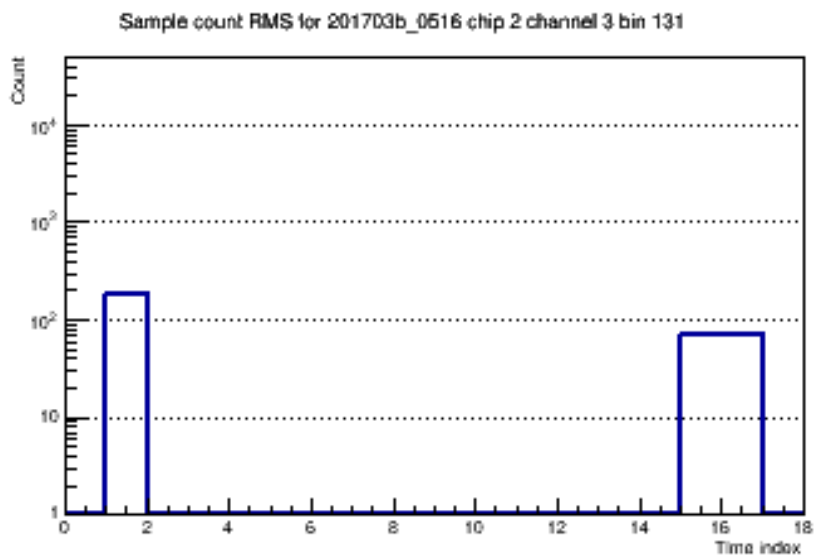


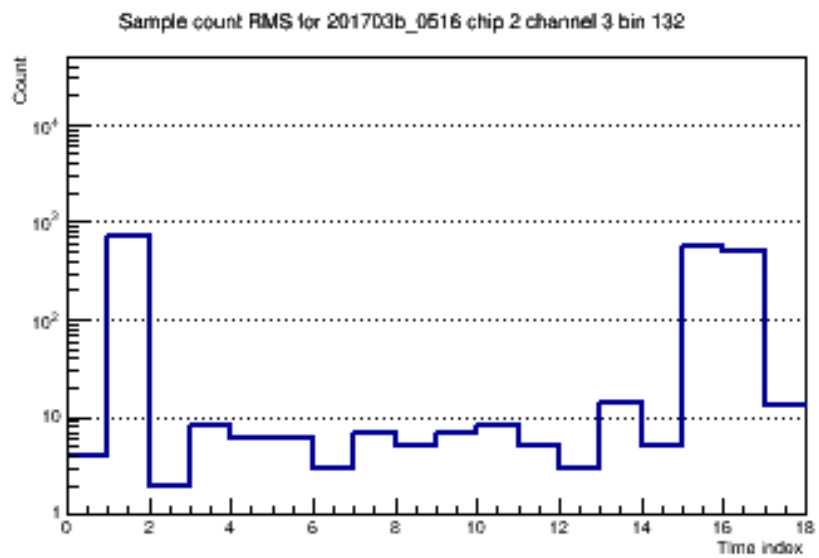


Time varying bins 41

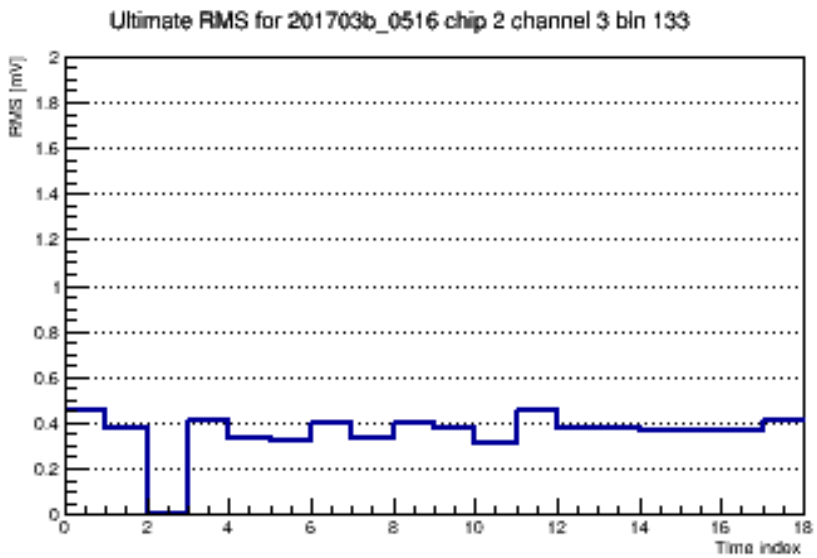


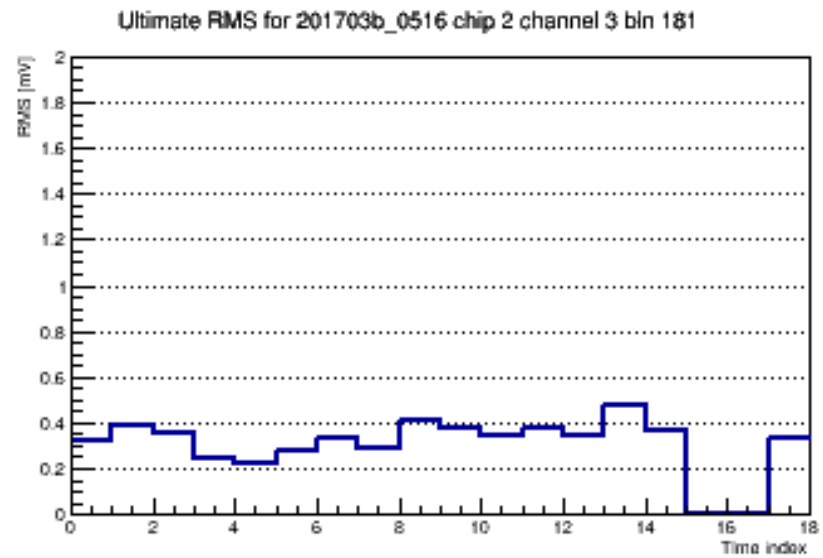


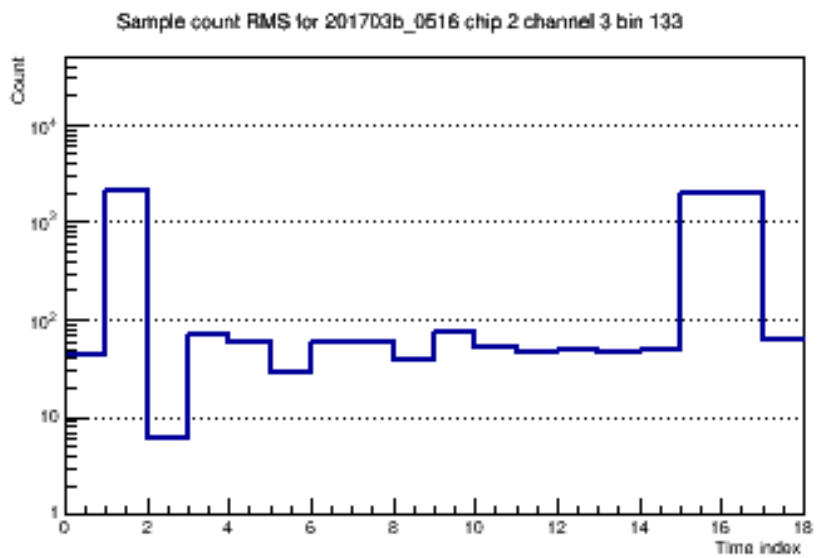


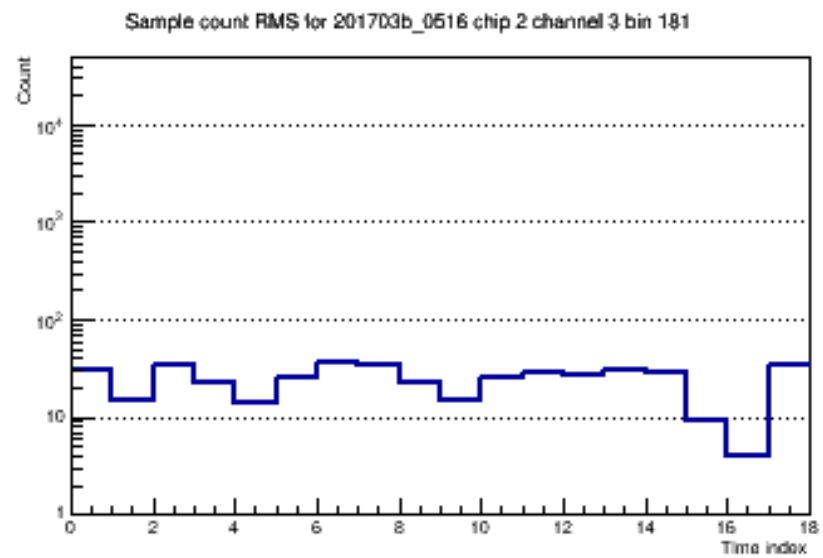


Time varying bins 42

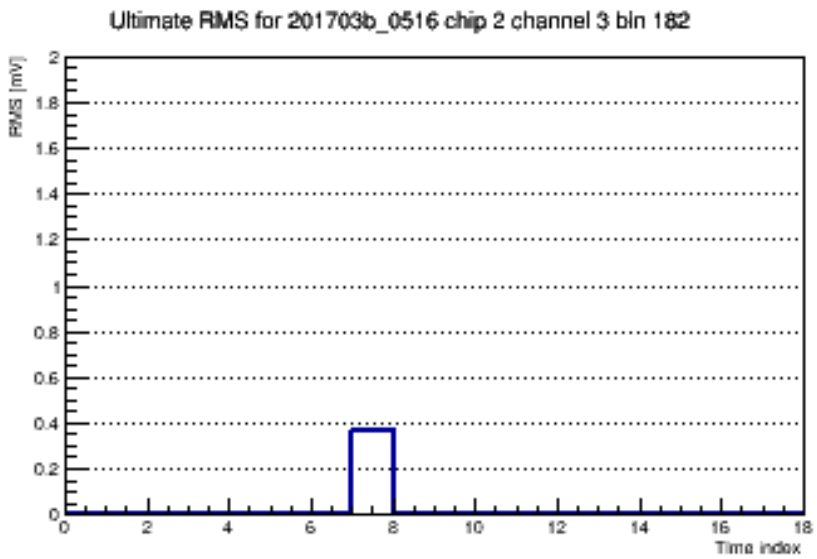


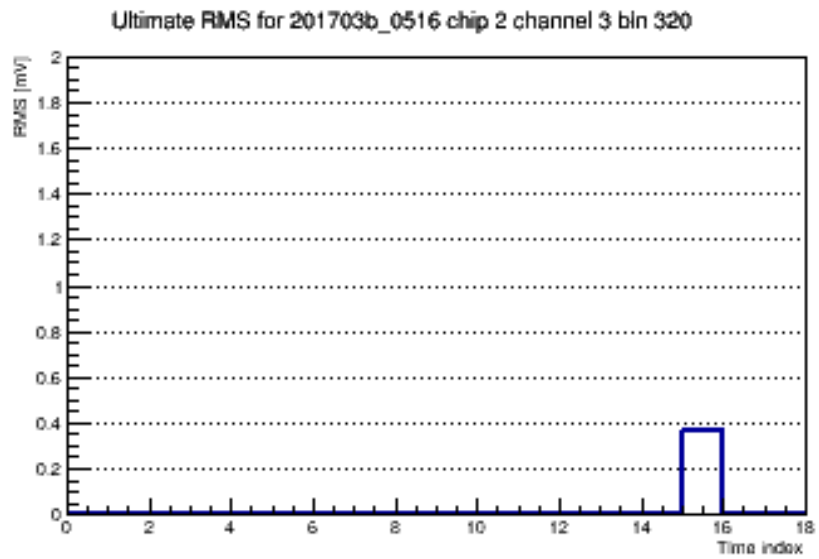


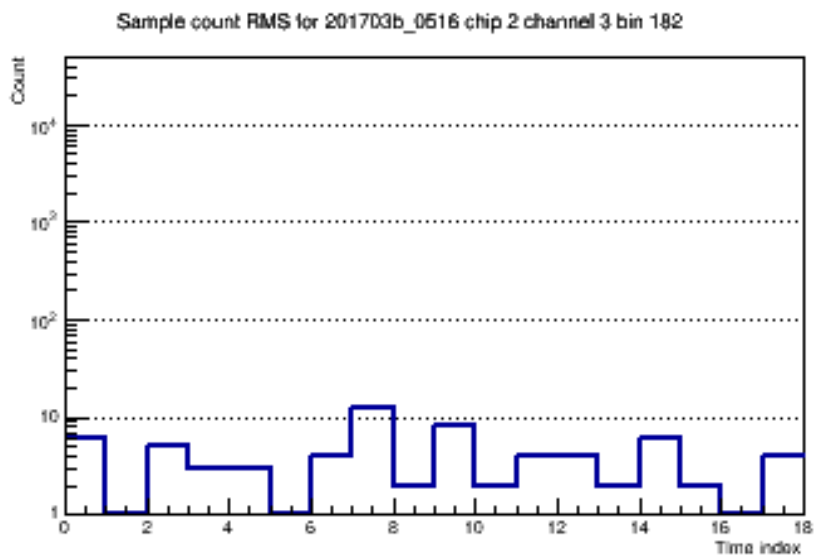


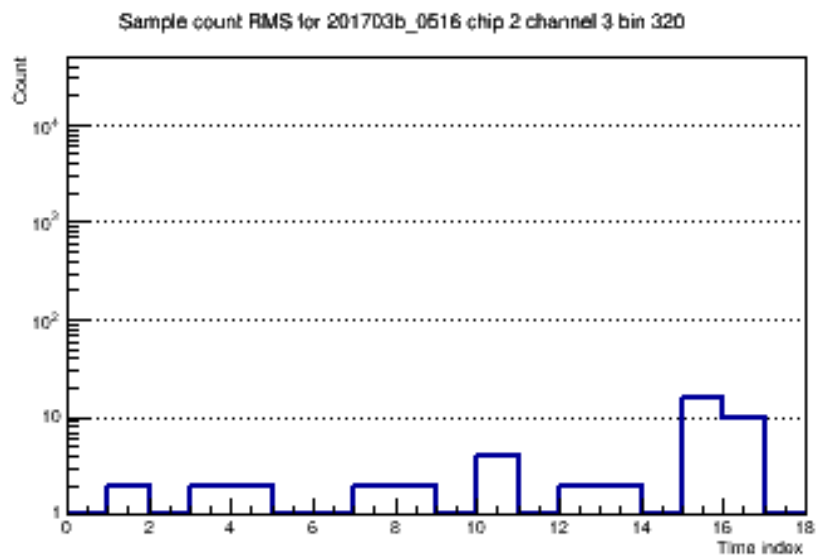


Time varying bins 43

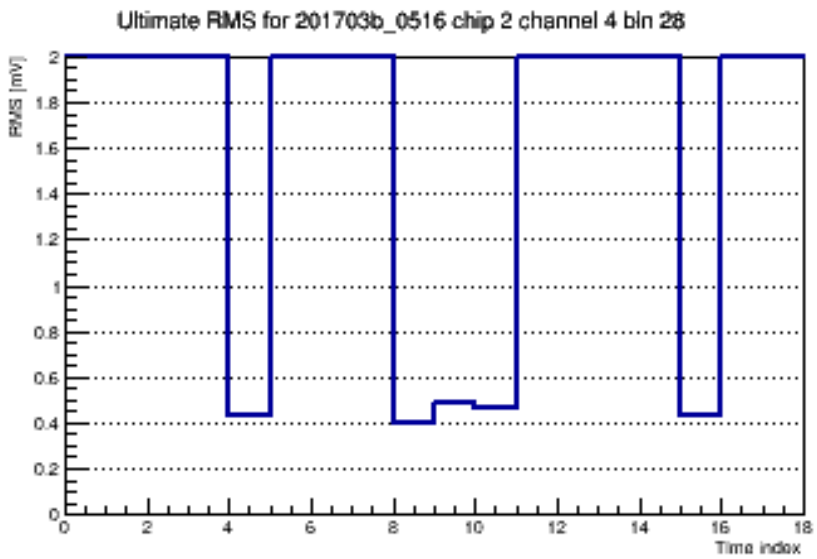


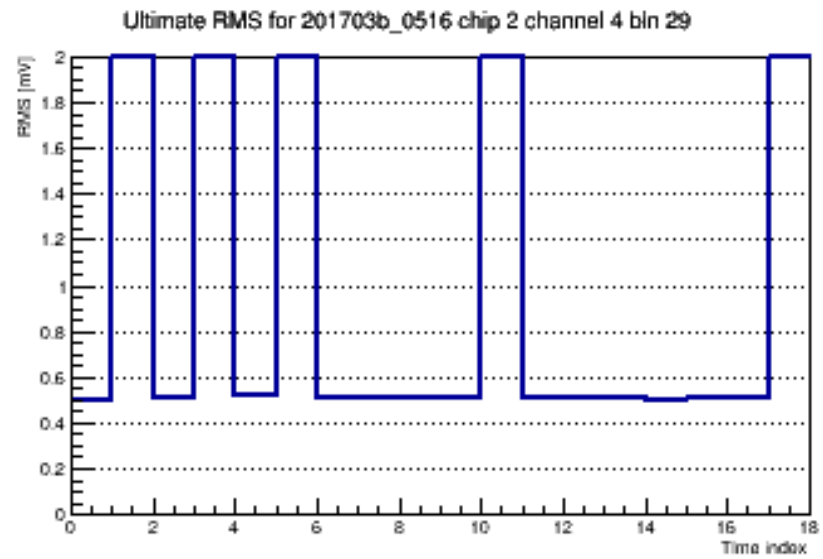


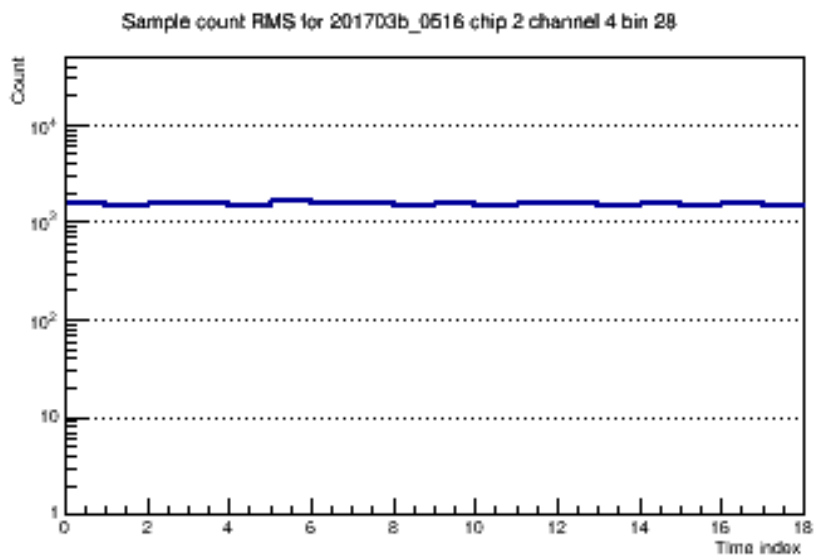


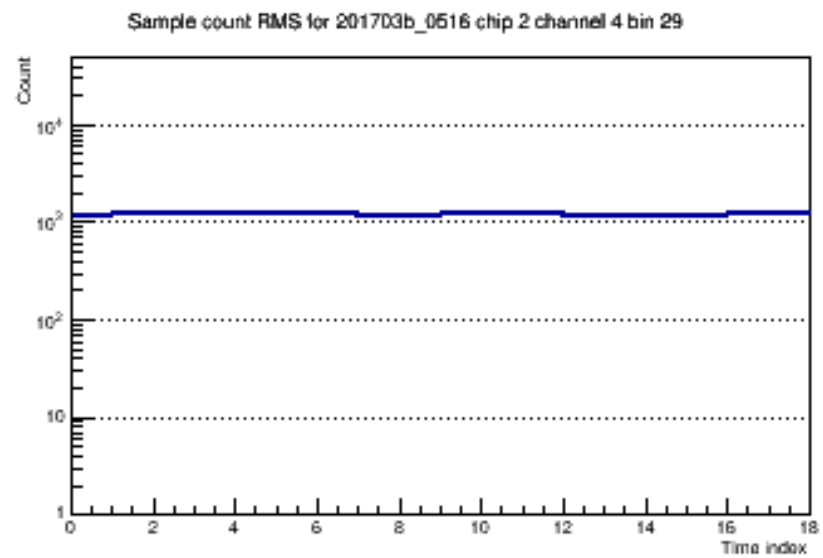


Time varying bins 44

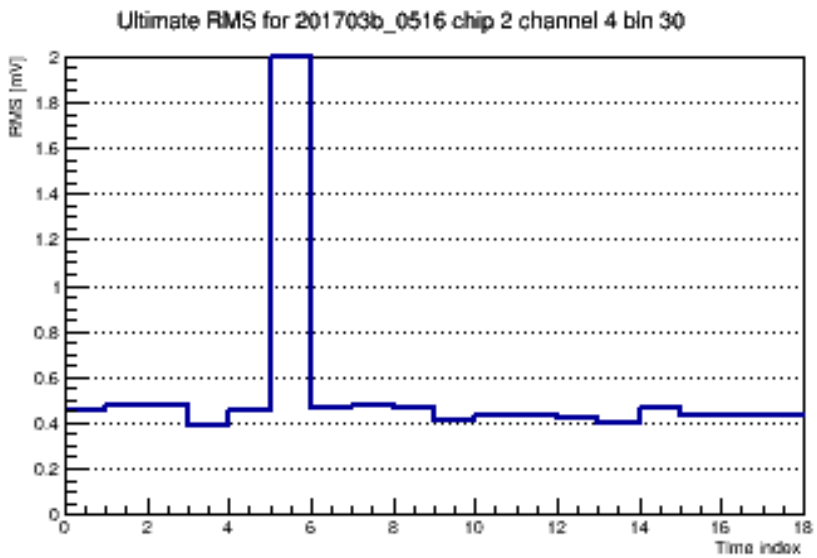


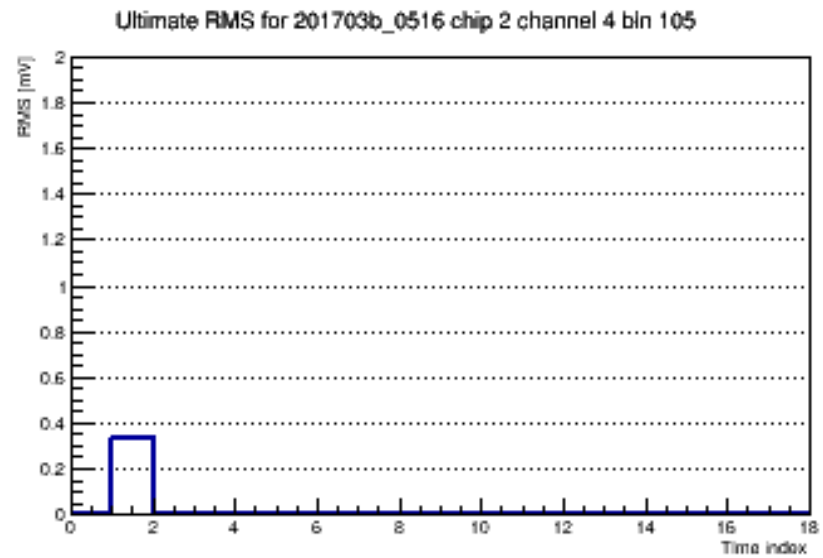


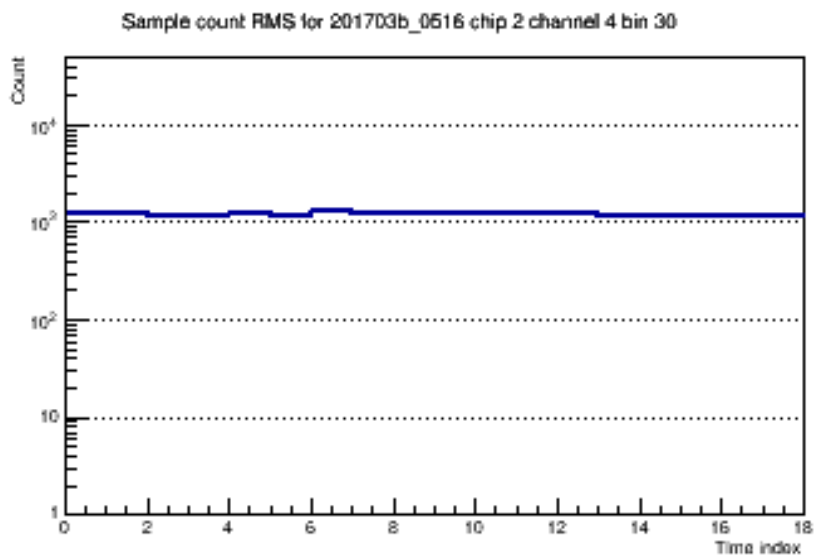


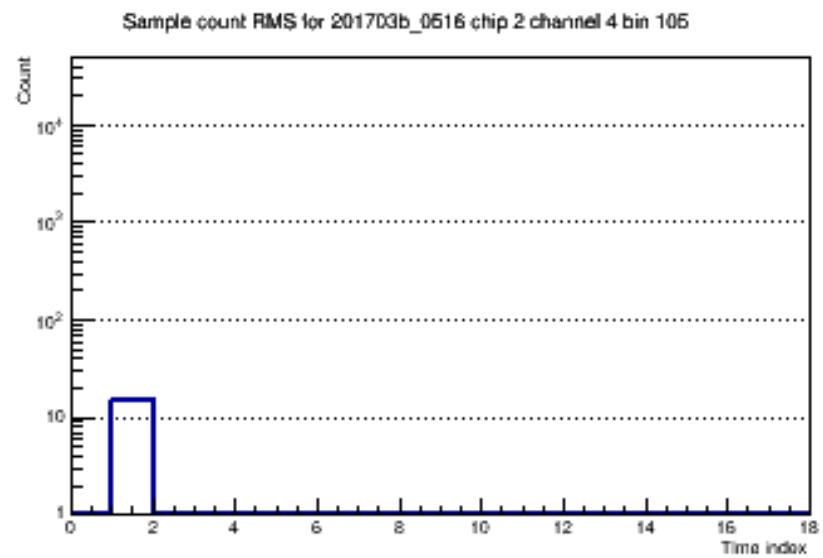


Time varying bins 45

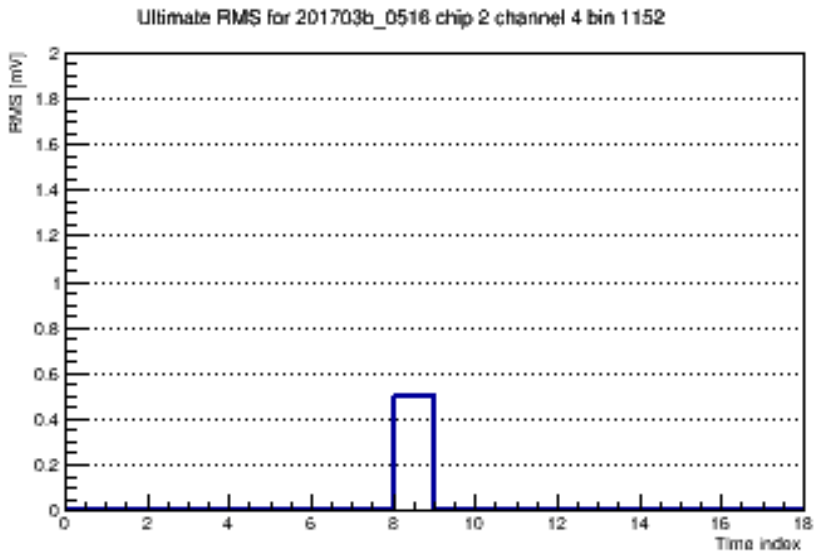


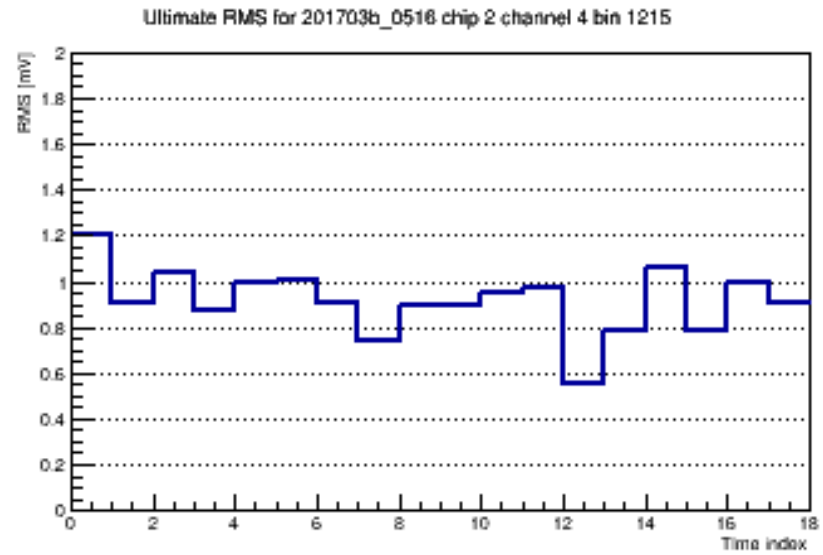


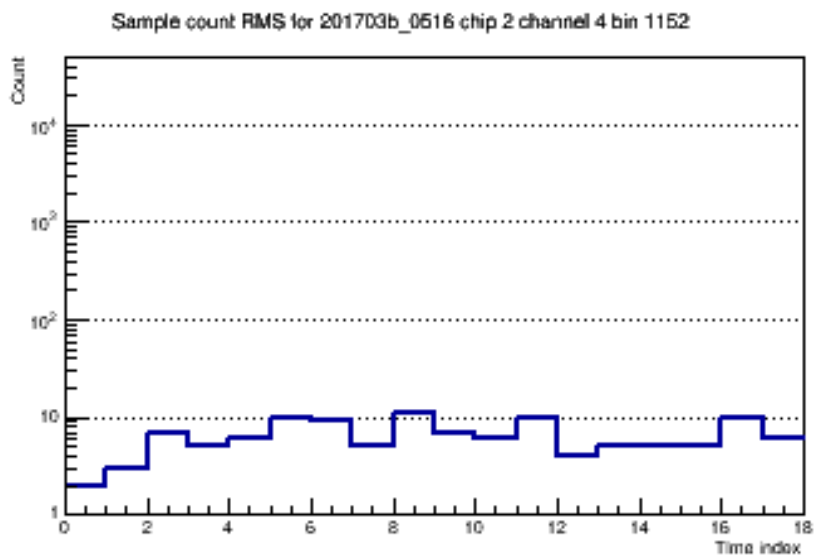


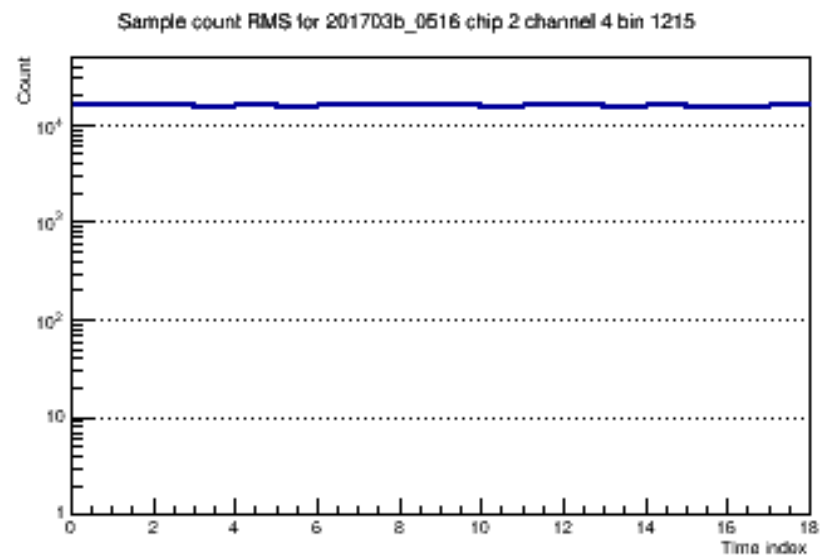


Time varying bins 46

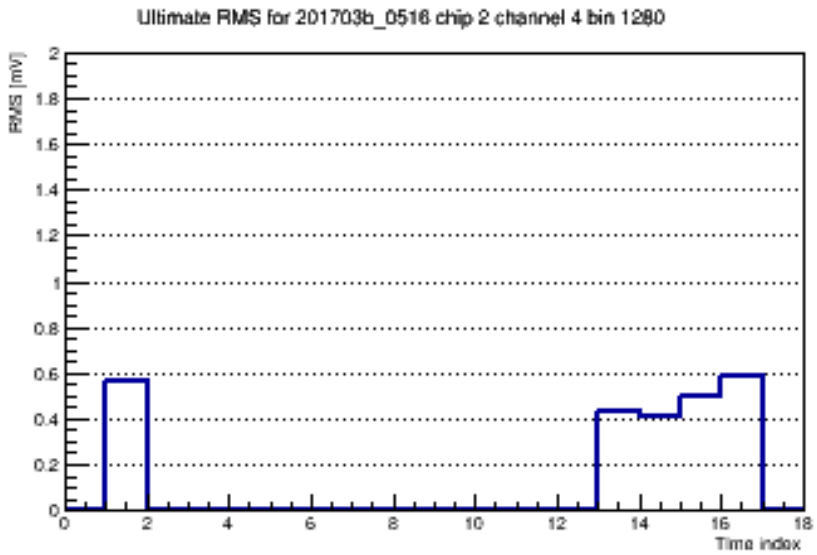


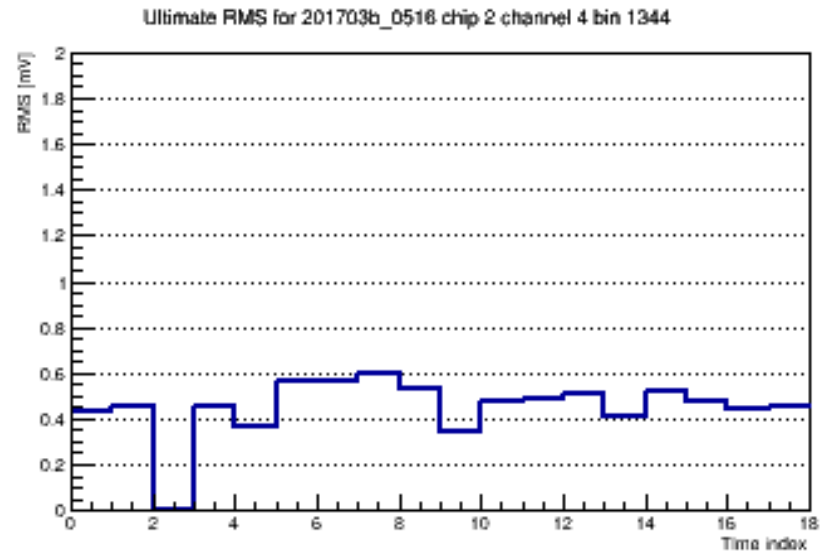


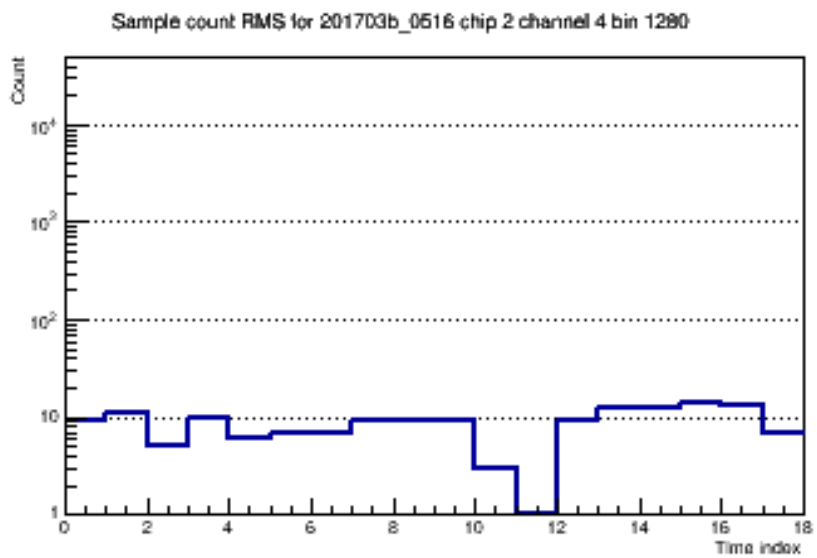


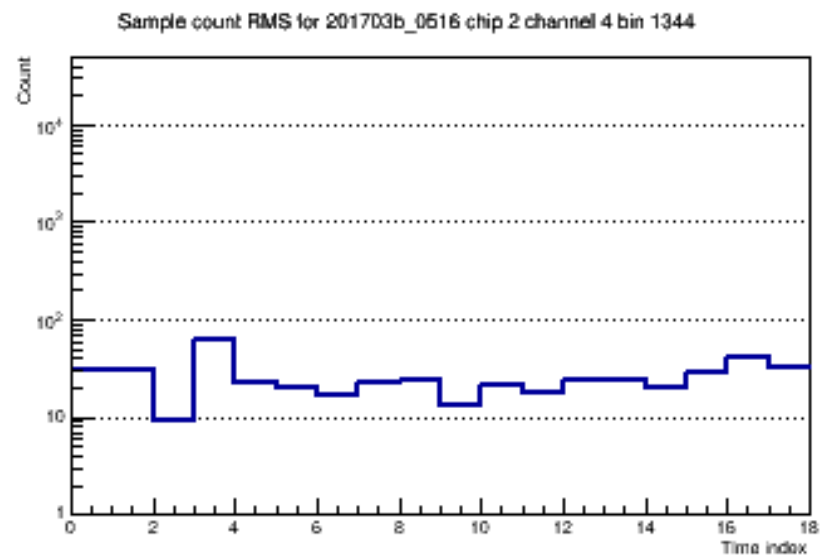


Time varying bins 47

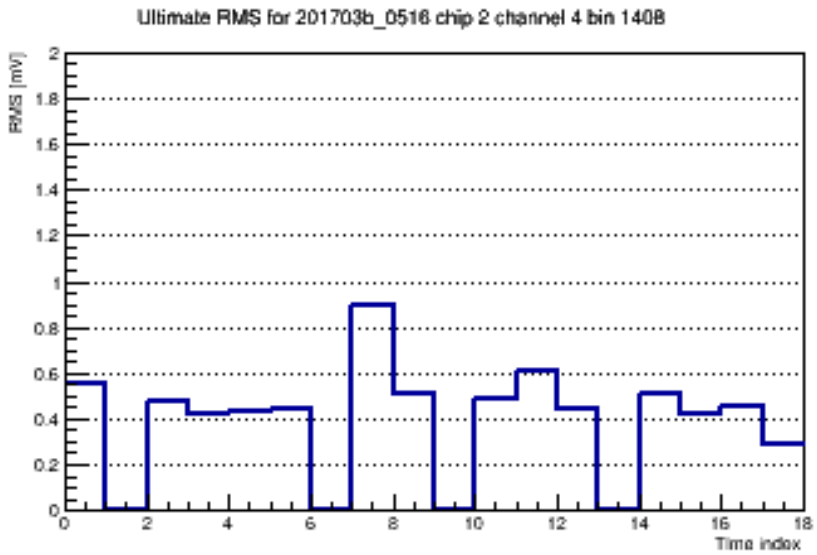


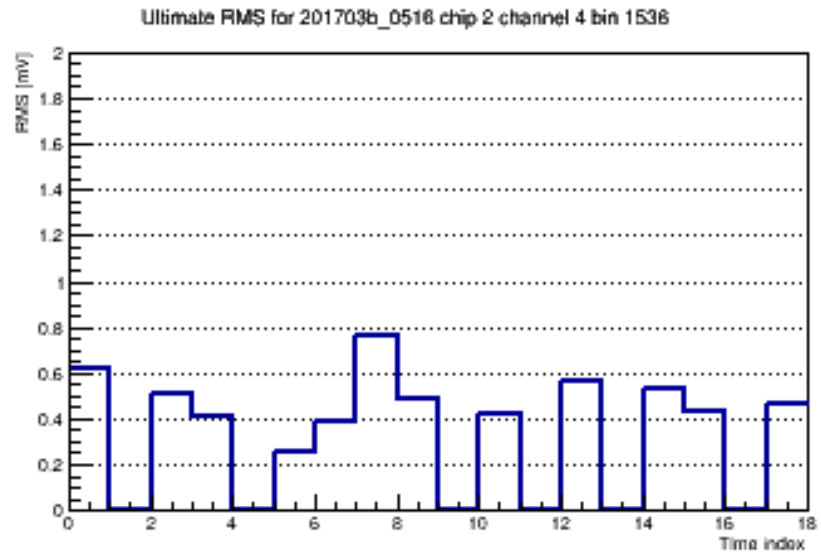


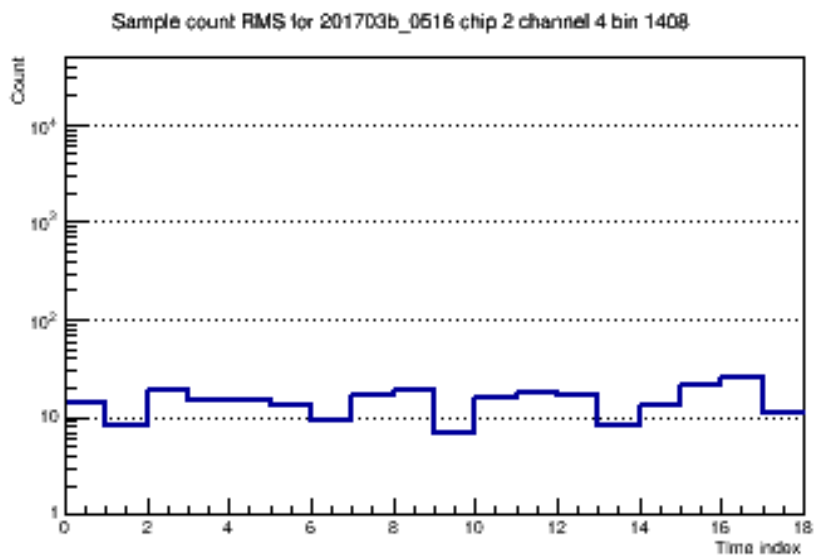


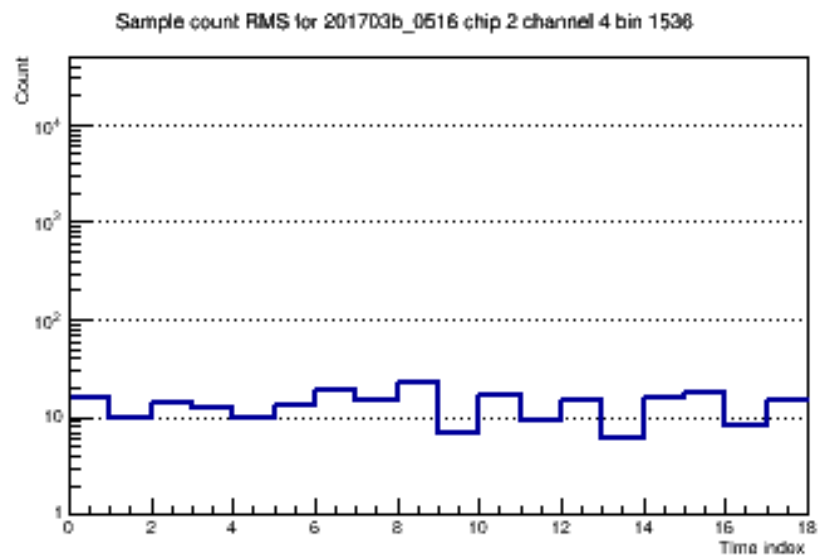


Time varying bins 48

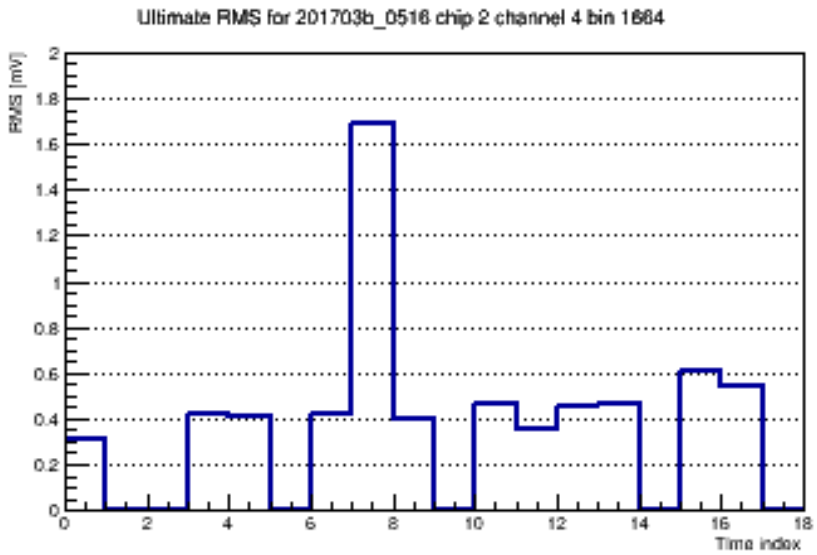


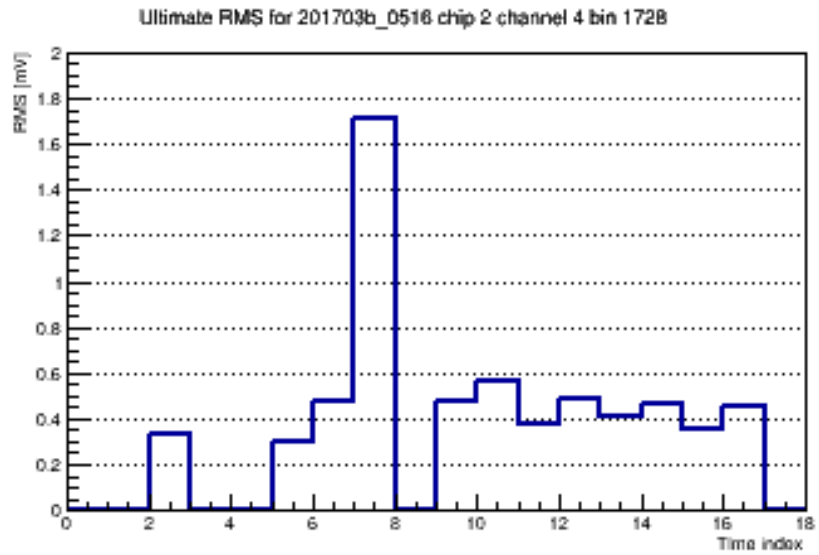


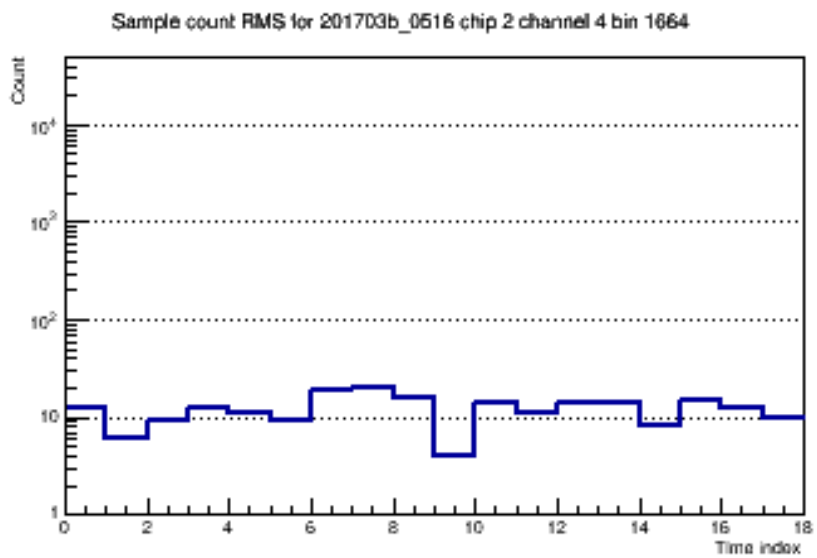


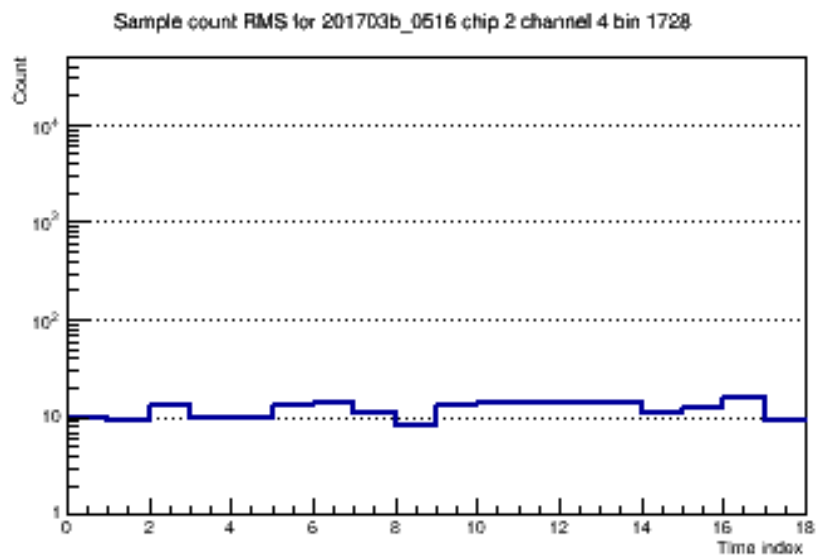


Time varying bins 49

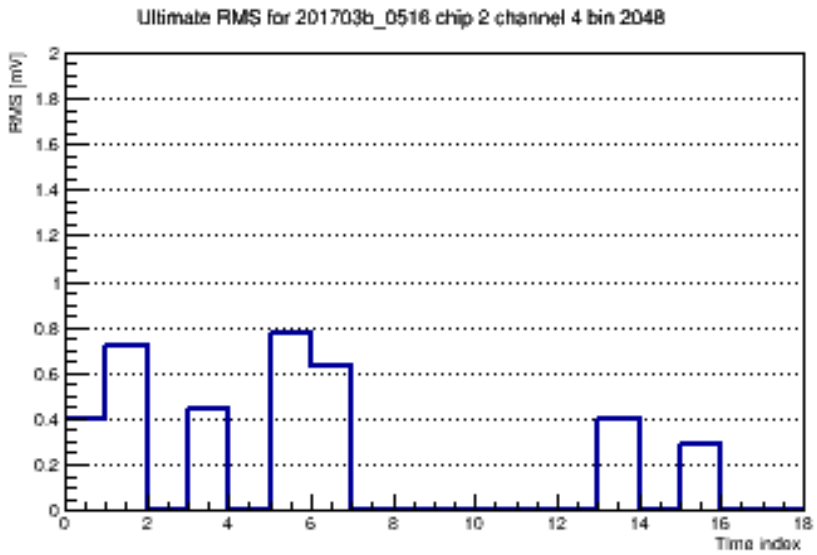


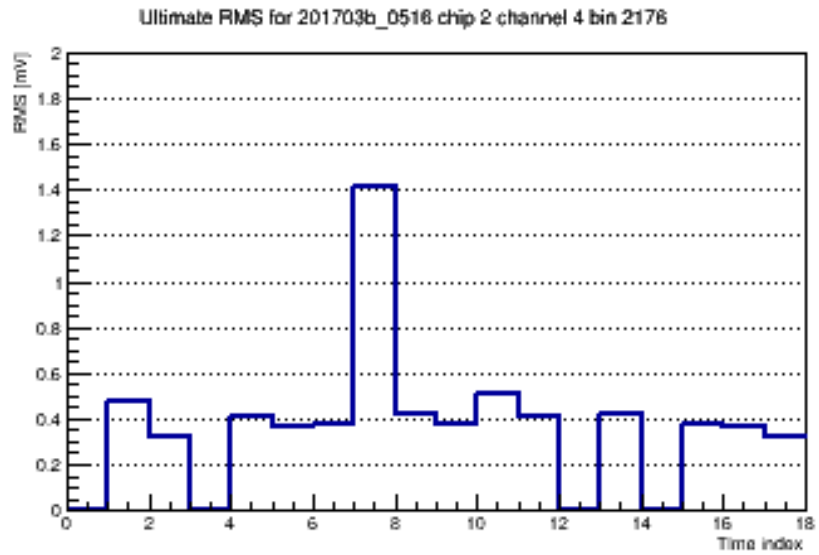


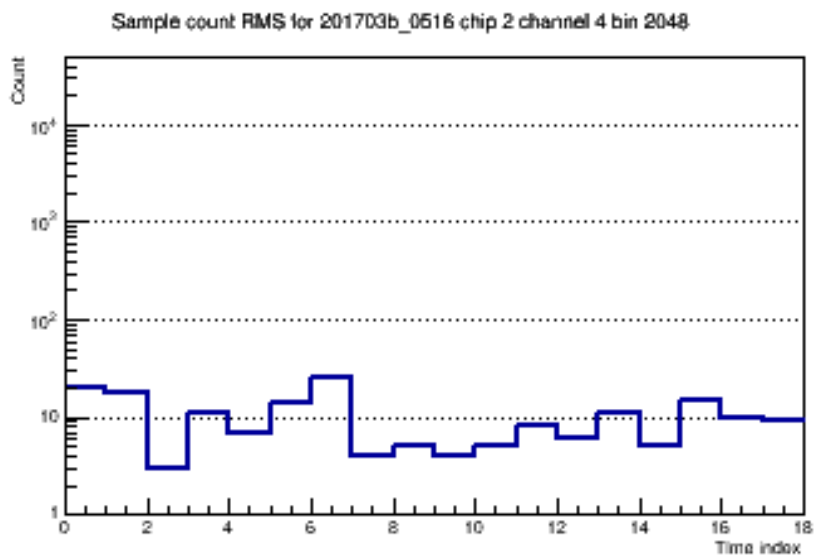


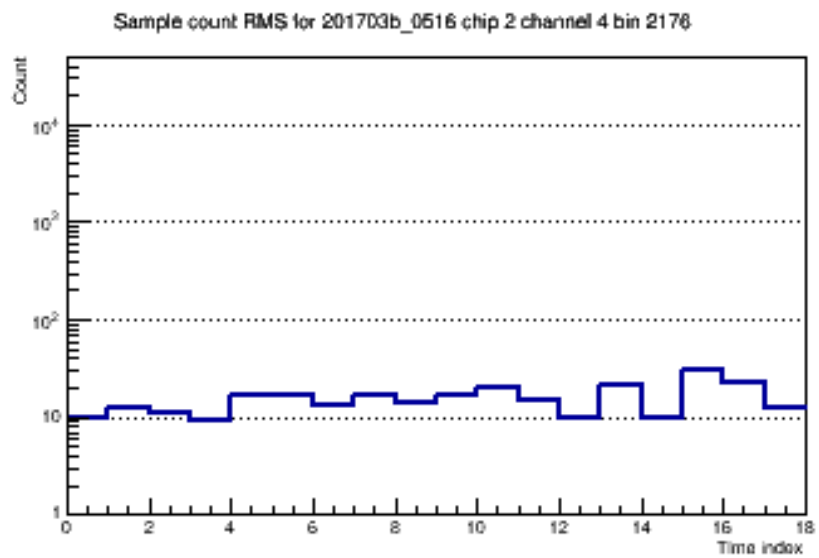


Time varying bins 50

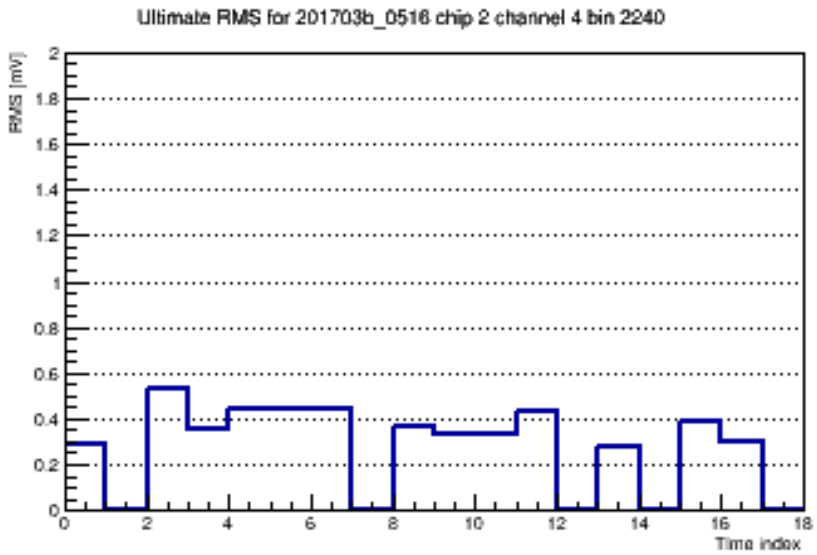


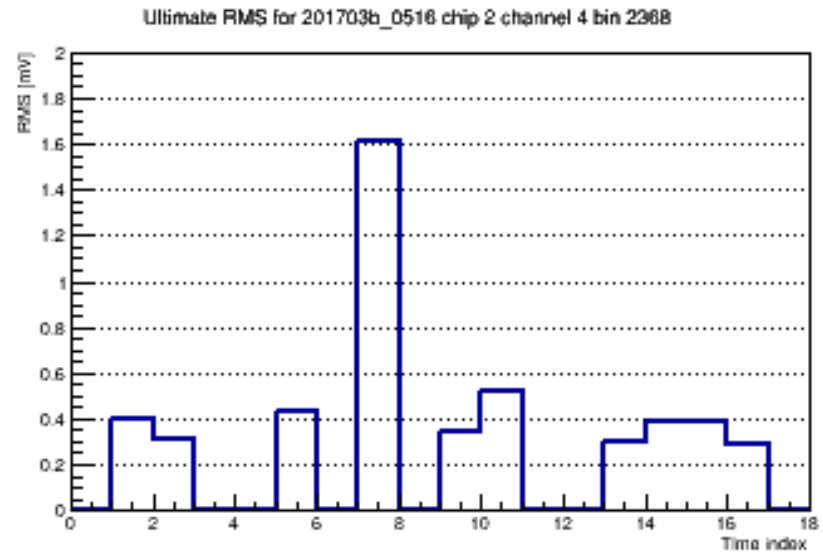


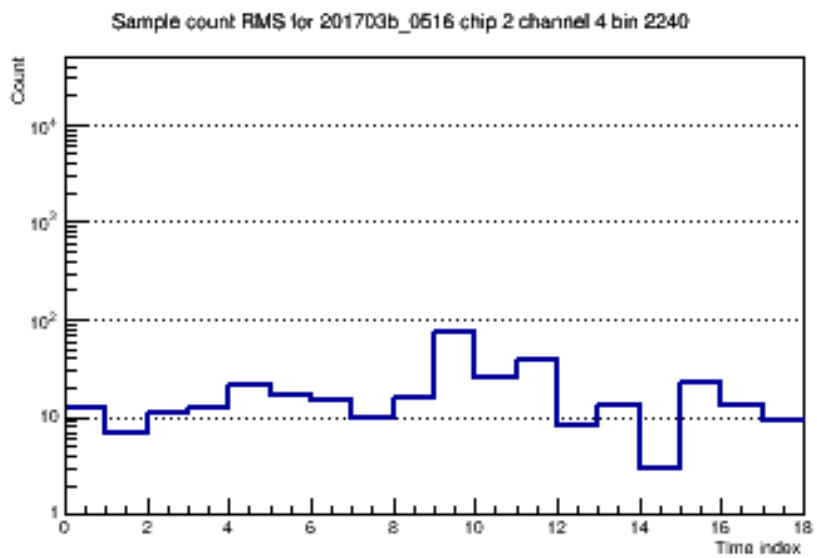


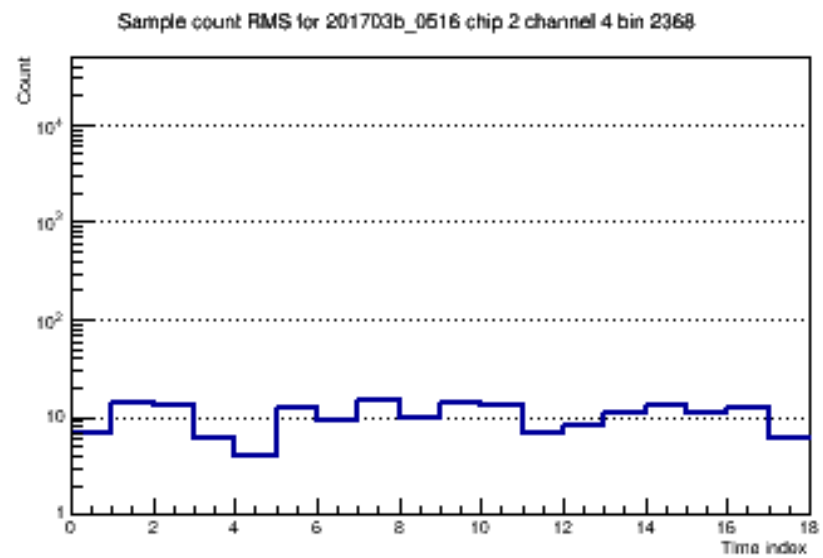


Time varying bins 51

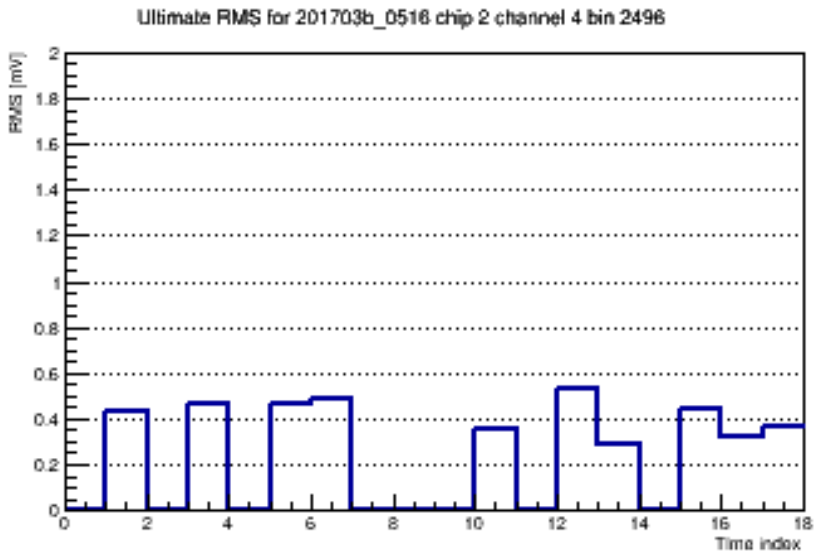


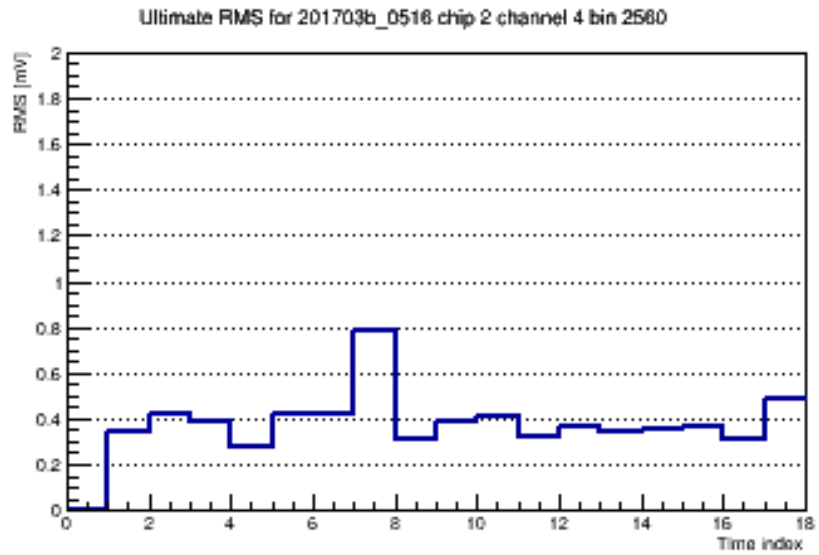


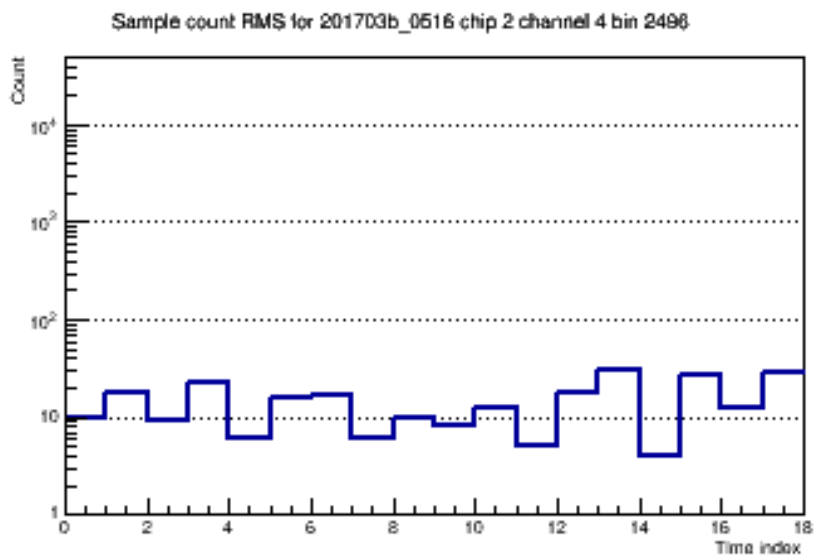


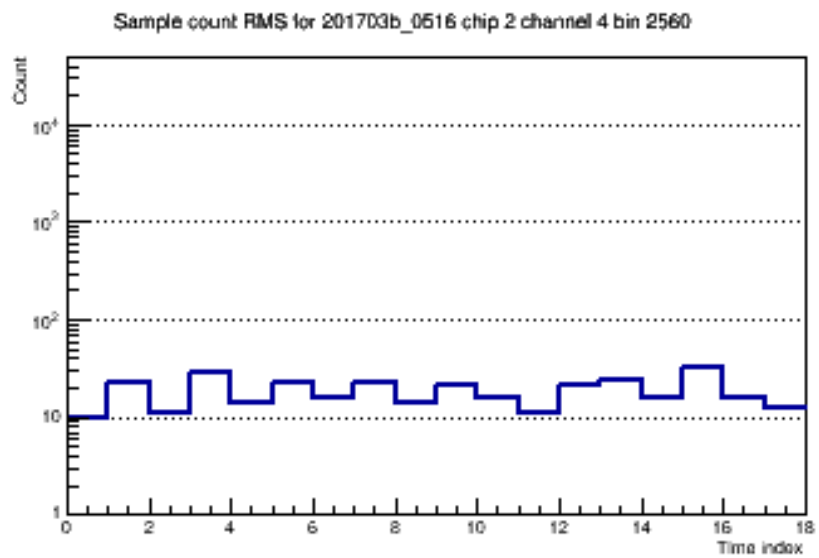


Time varying bins 52

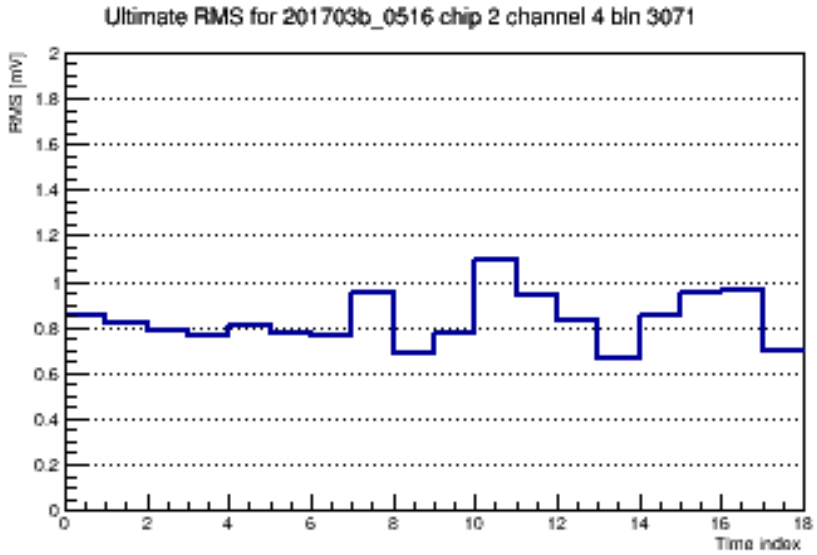


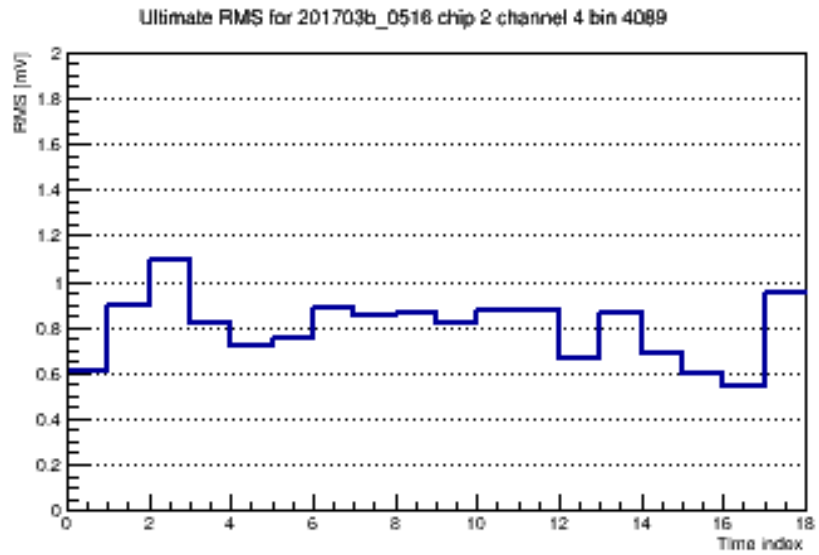


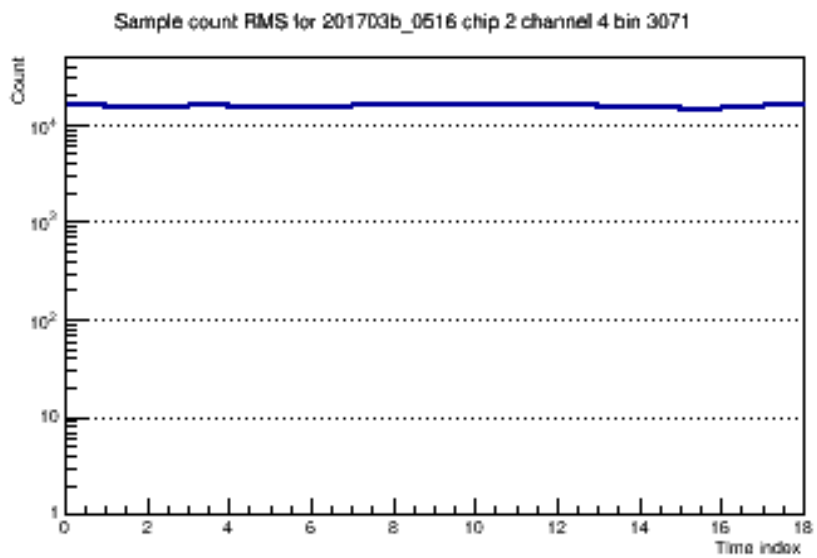


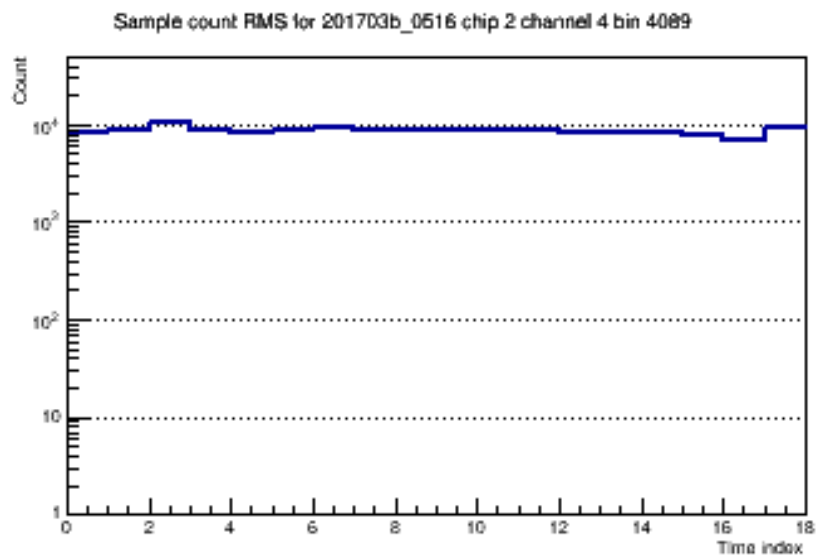


Time varying bins 53

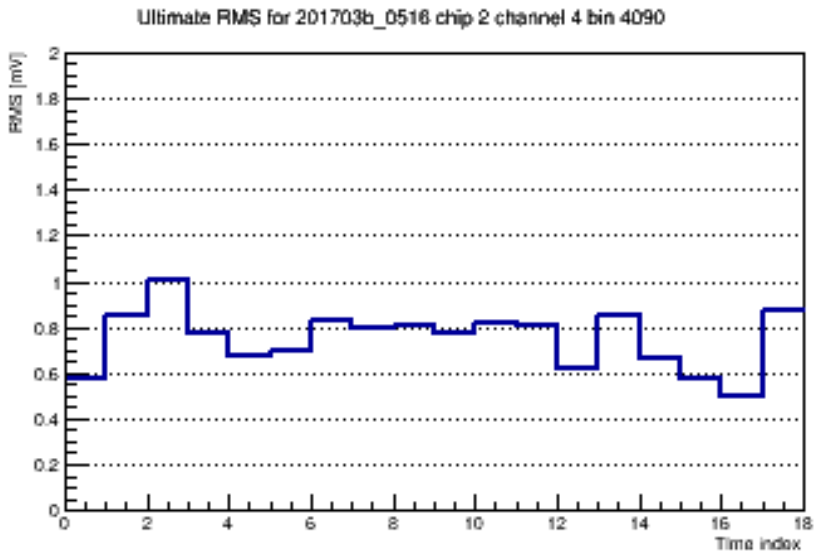


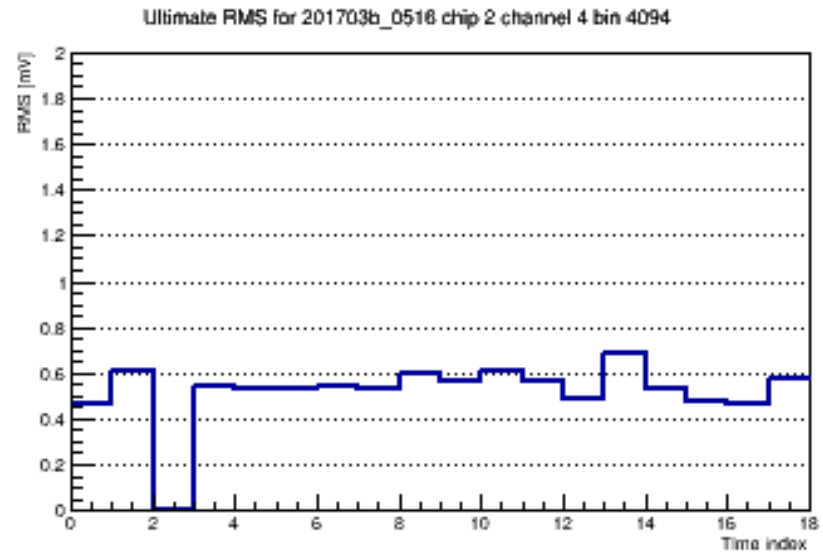


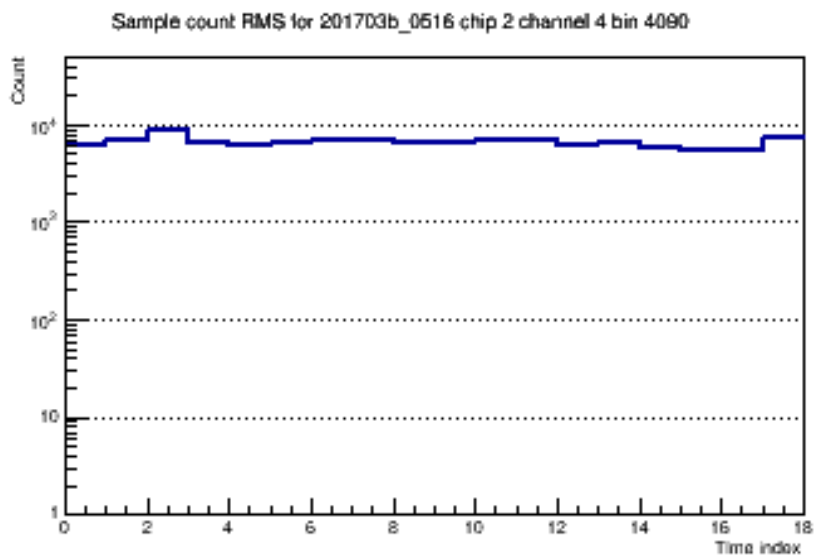


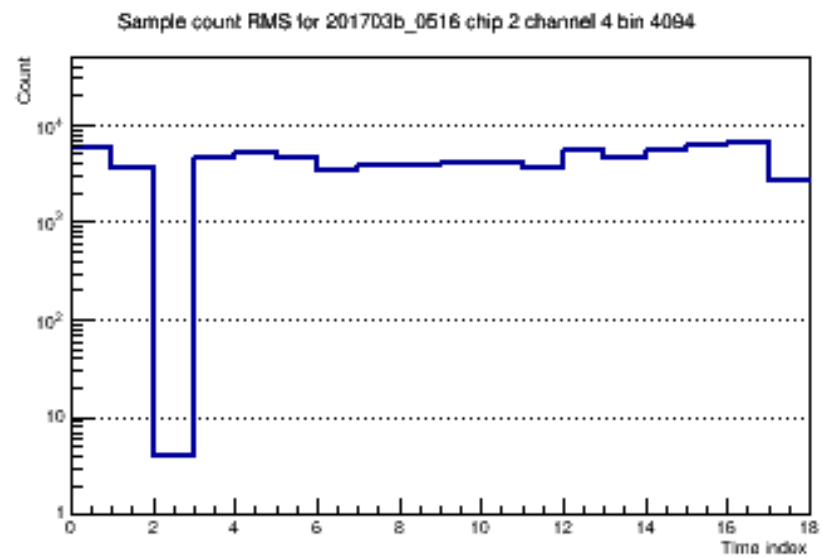


Time varying bins 54

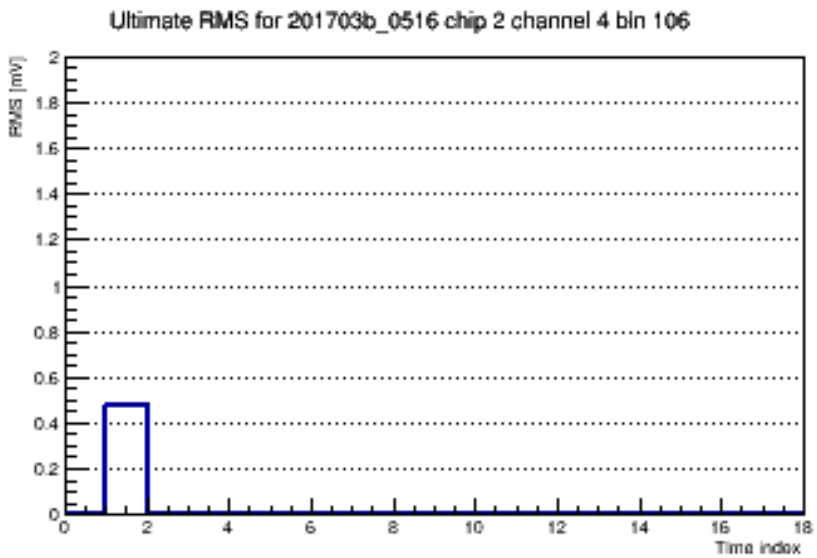


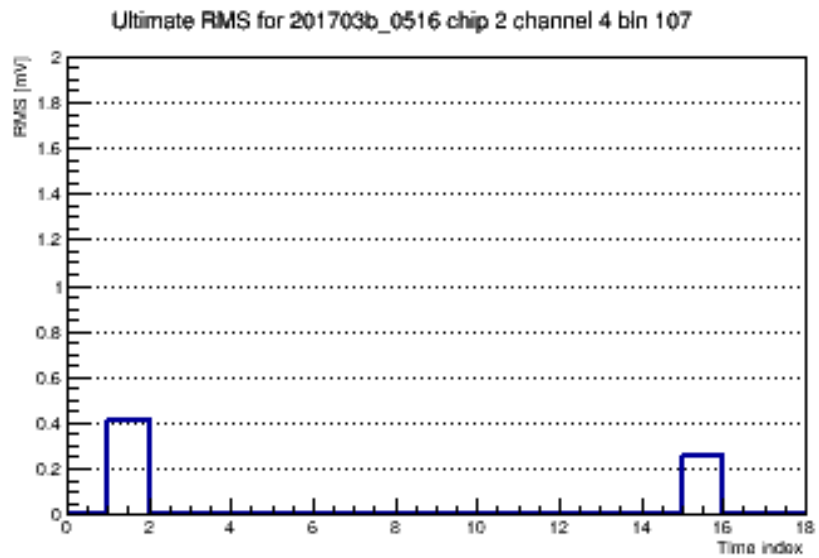


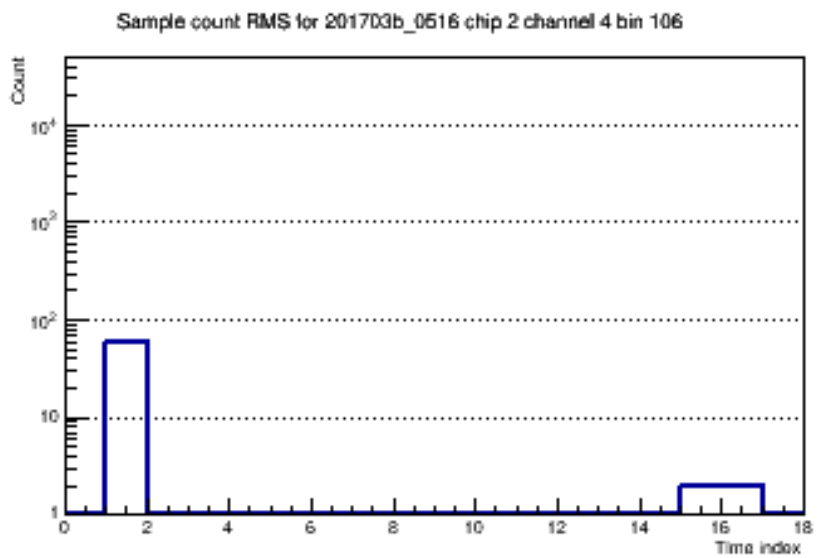


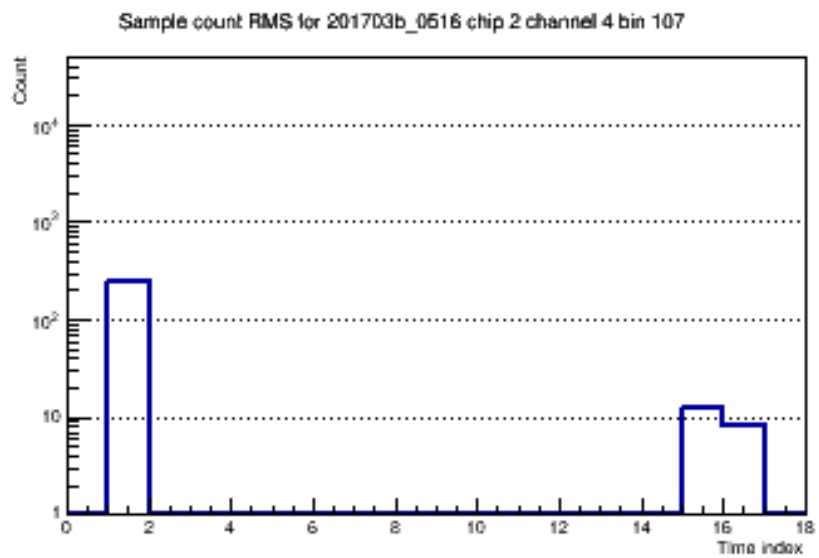


Time varying bins 55

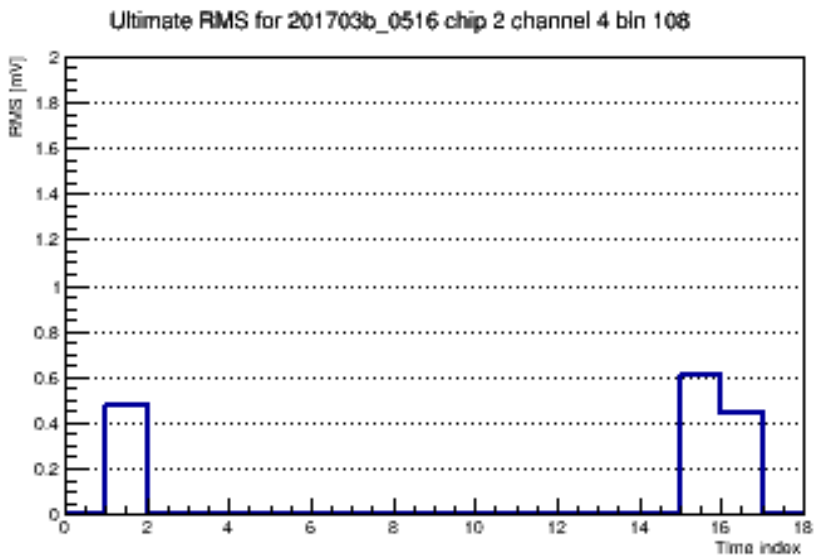


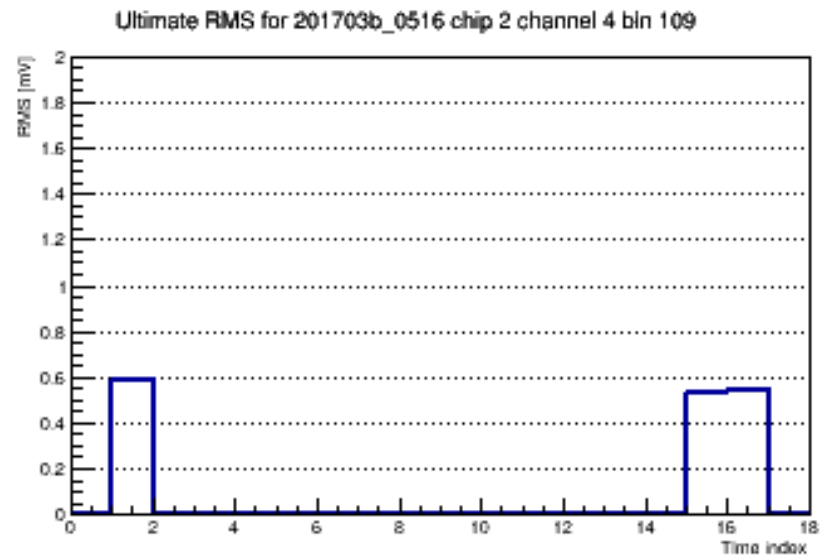


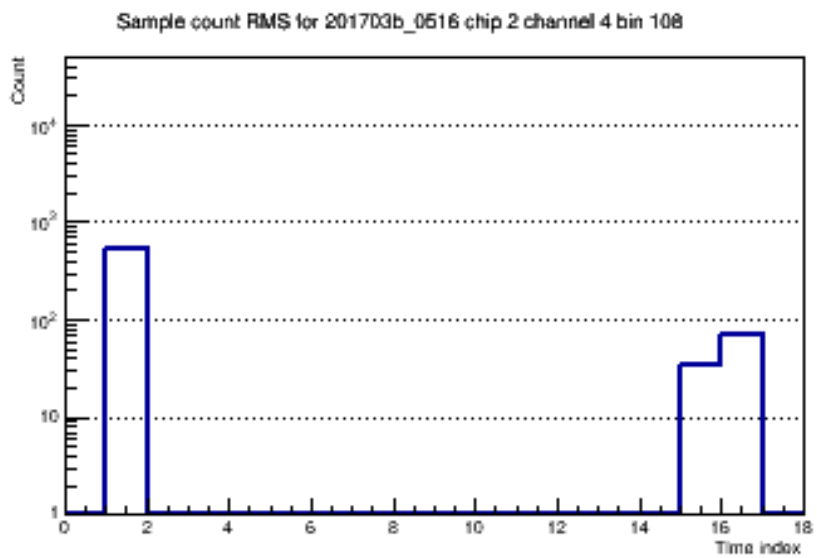


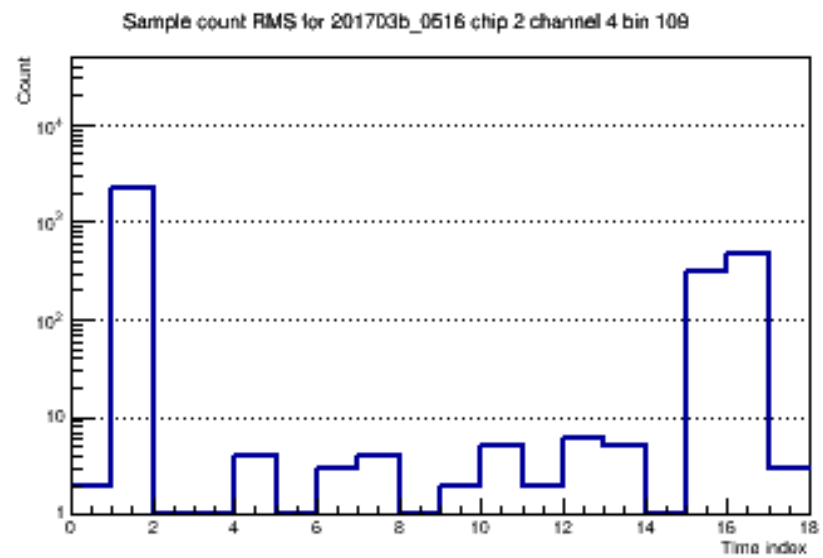


Time varying bins 56

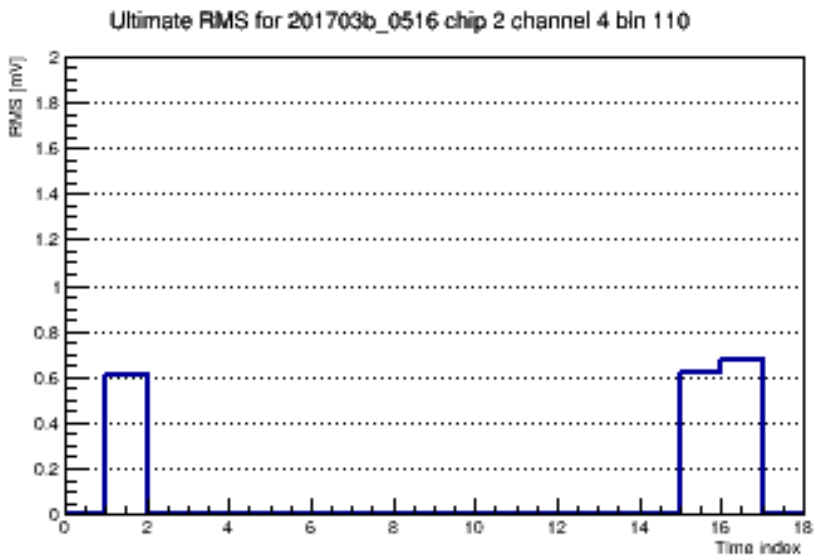


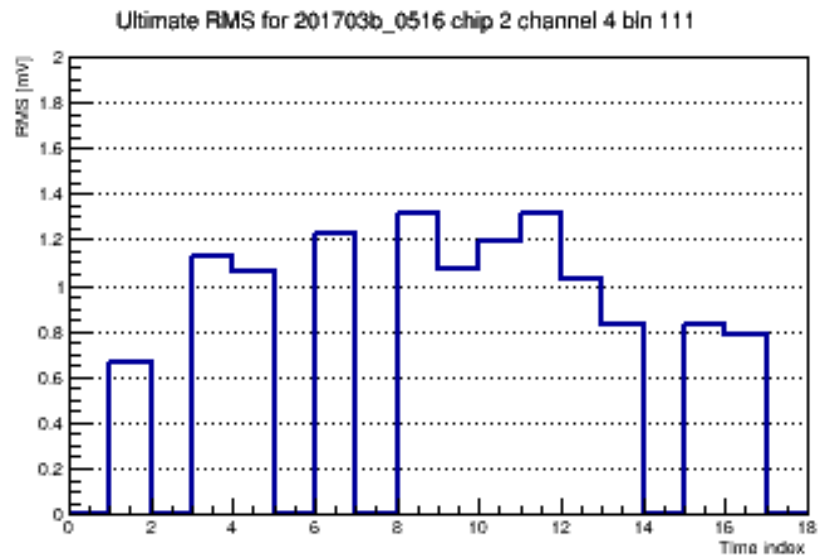


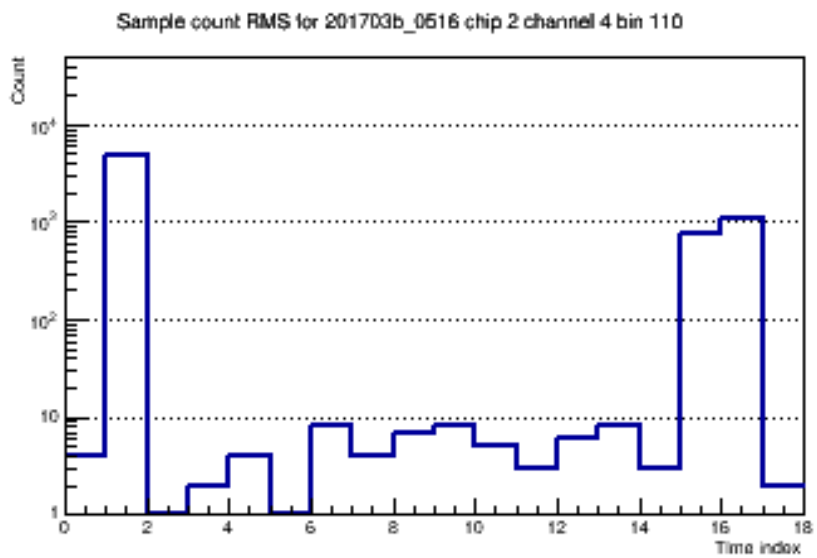


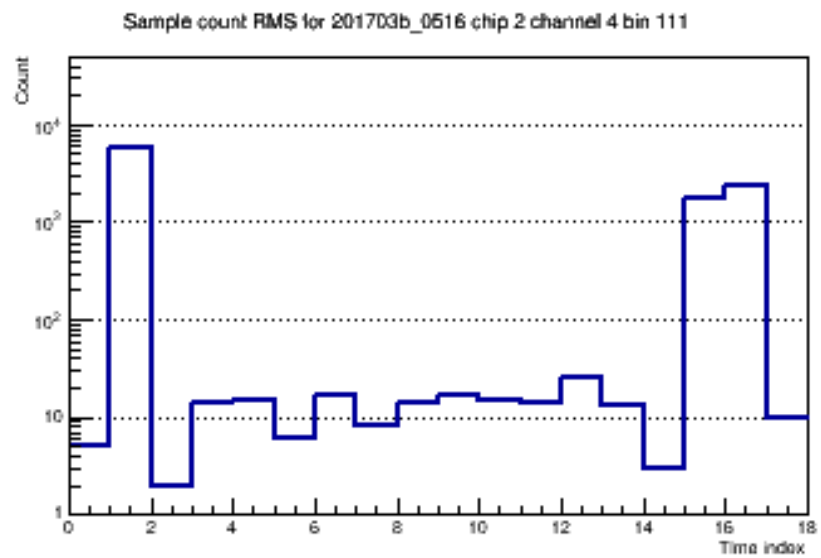


Time varying bins 57

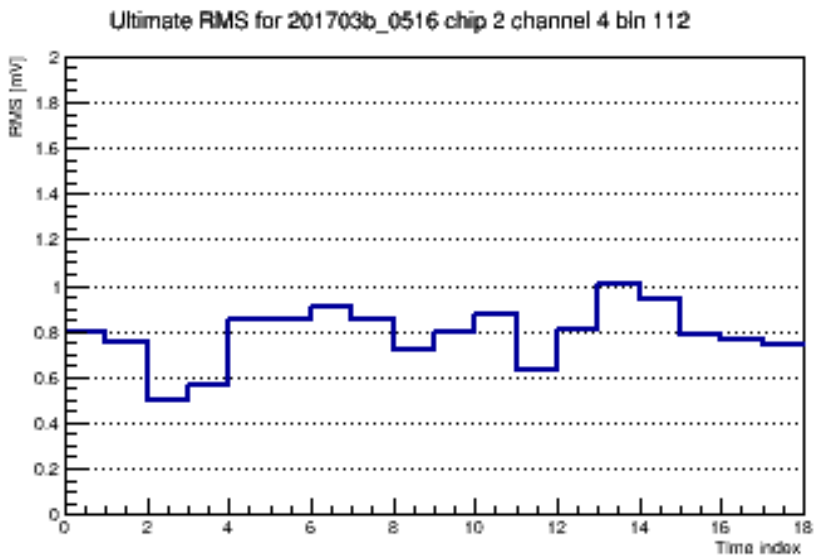


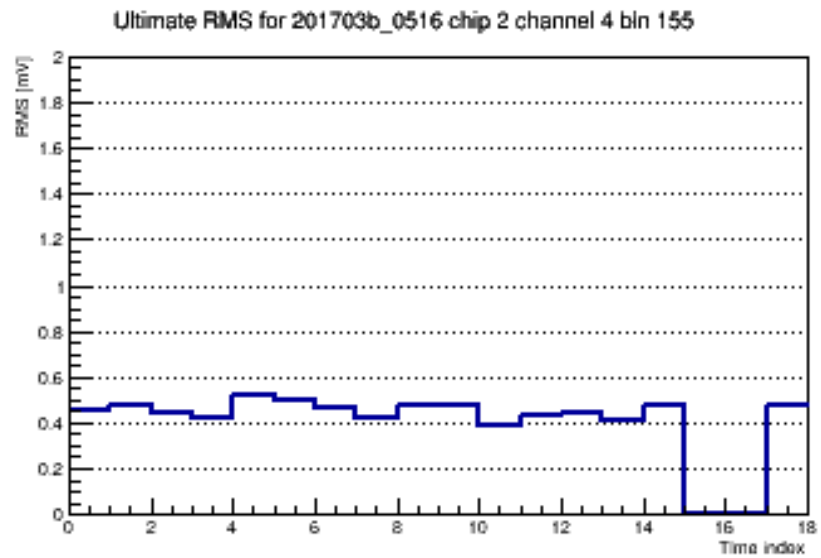


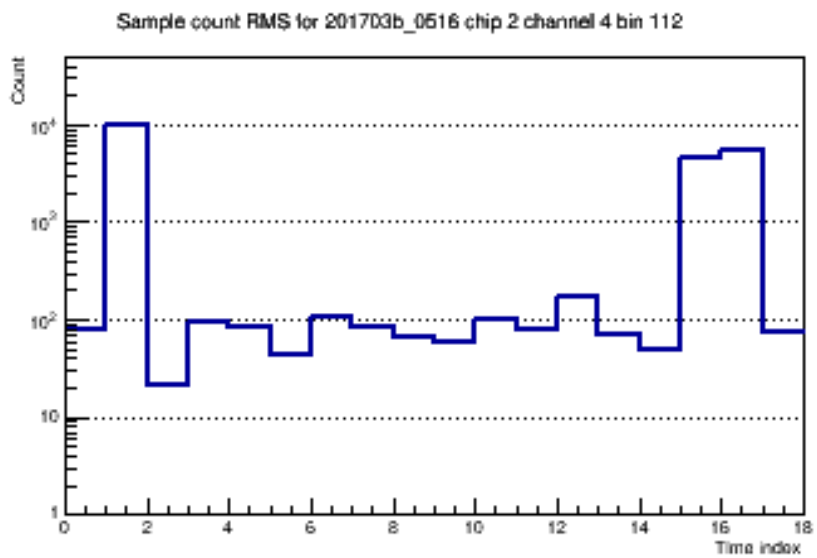


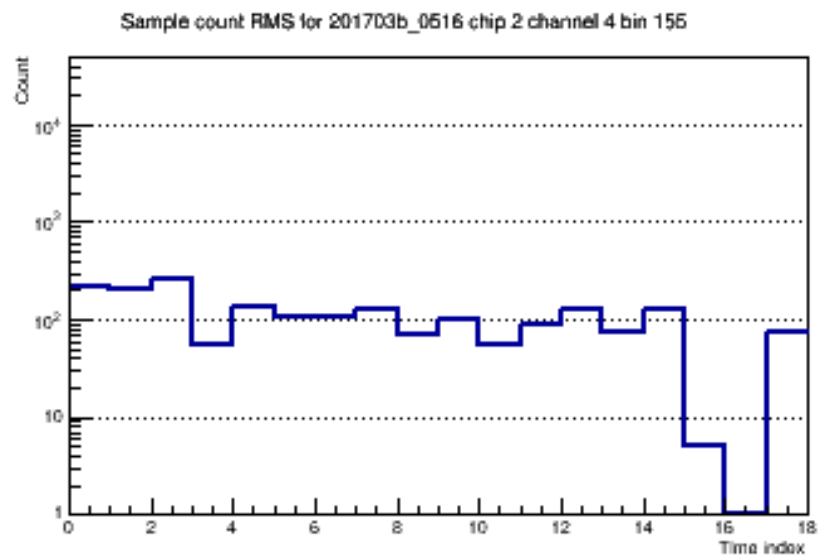


Time varying bins 58

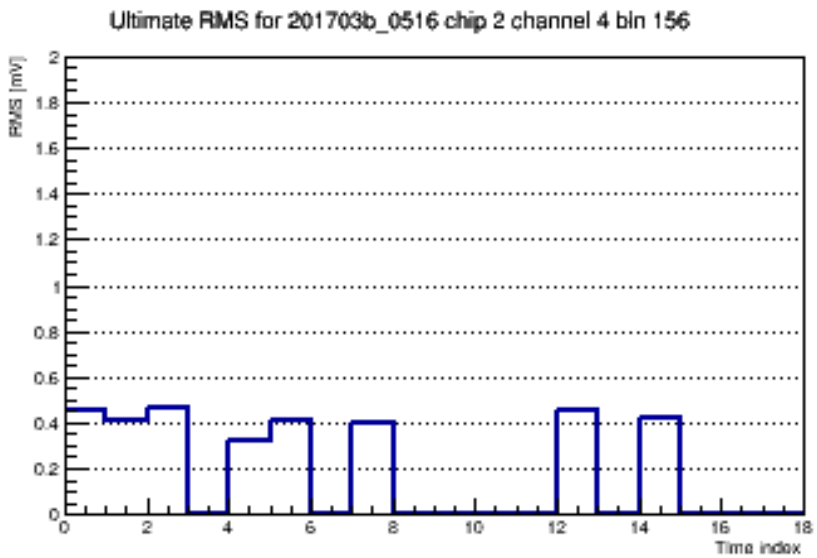


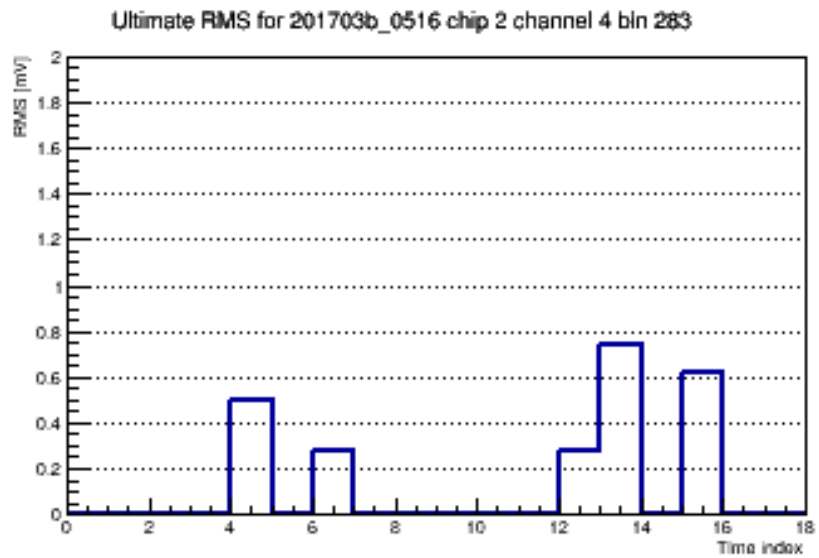


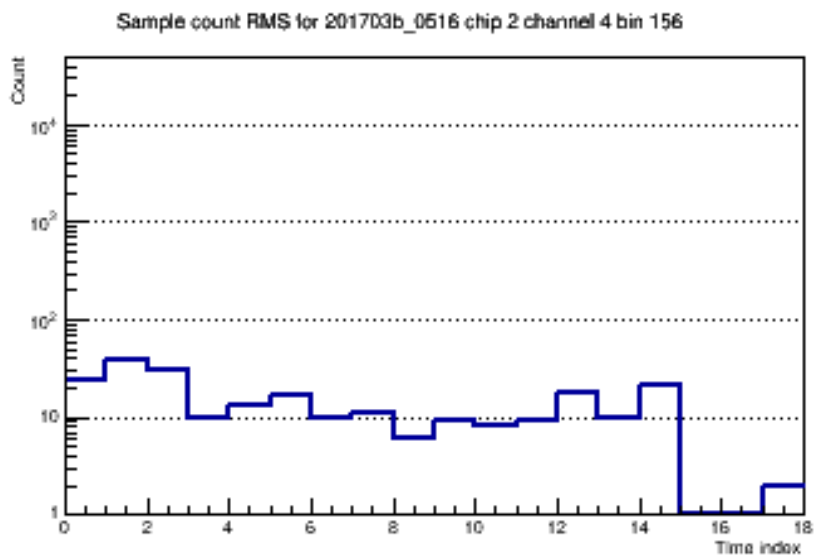


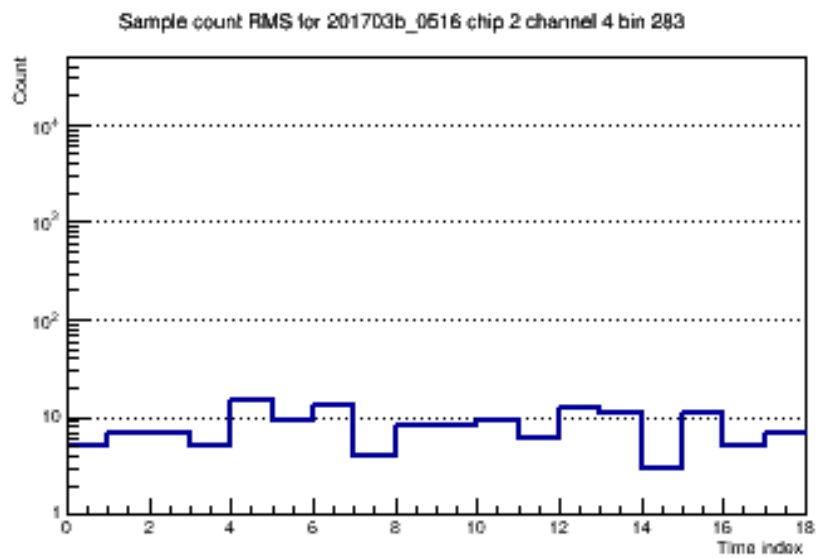


Time varying bins 59

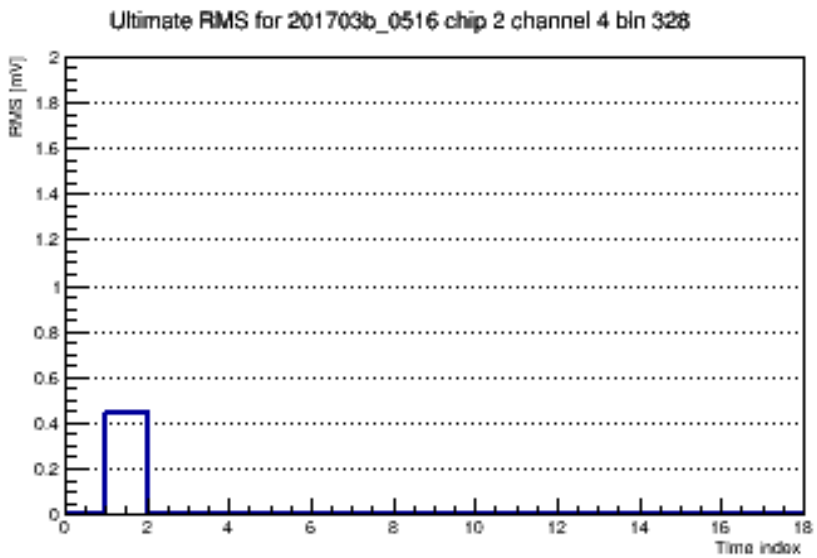


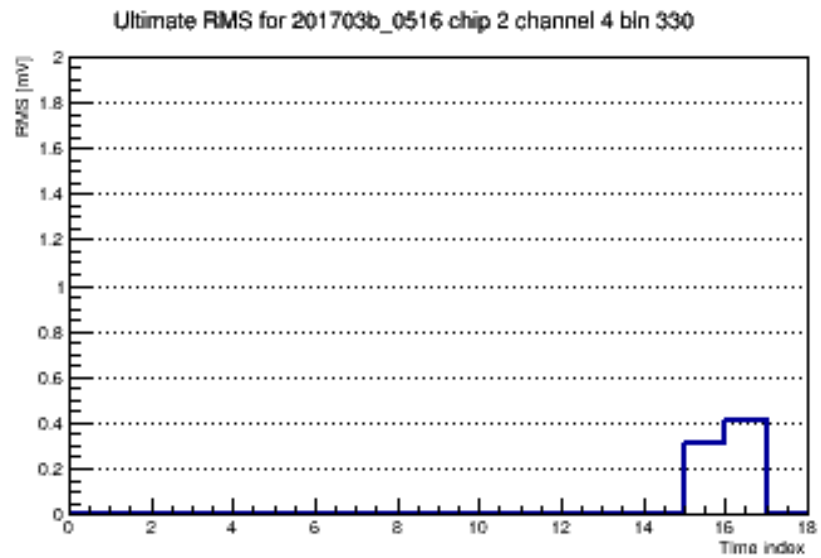


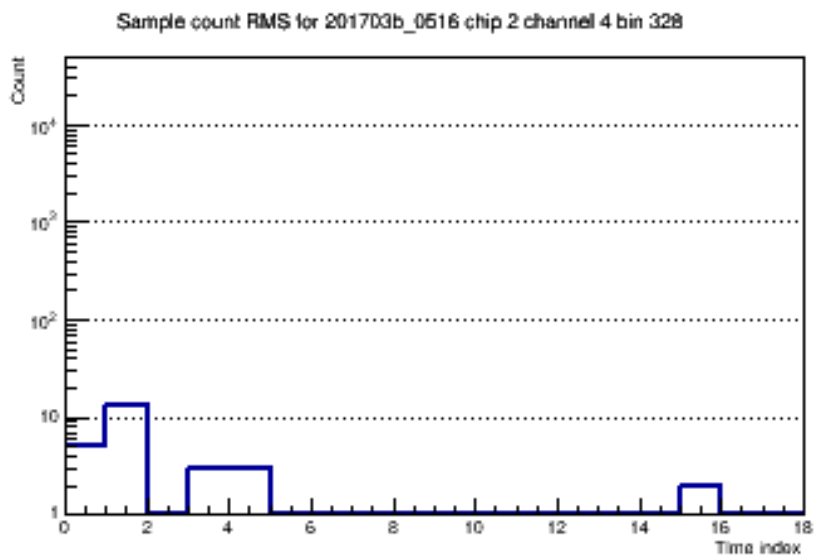


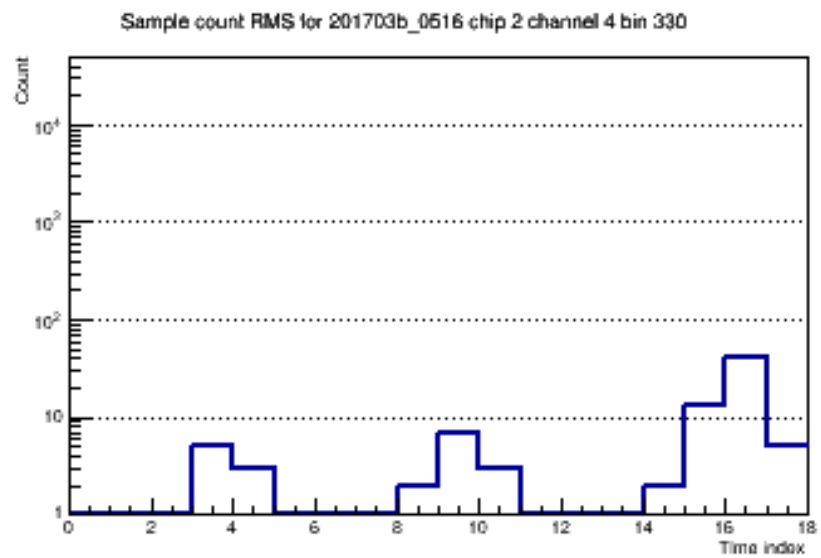


Time varying bins 60

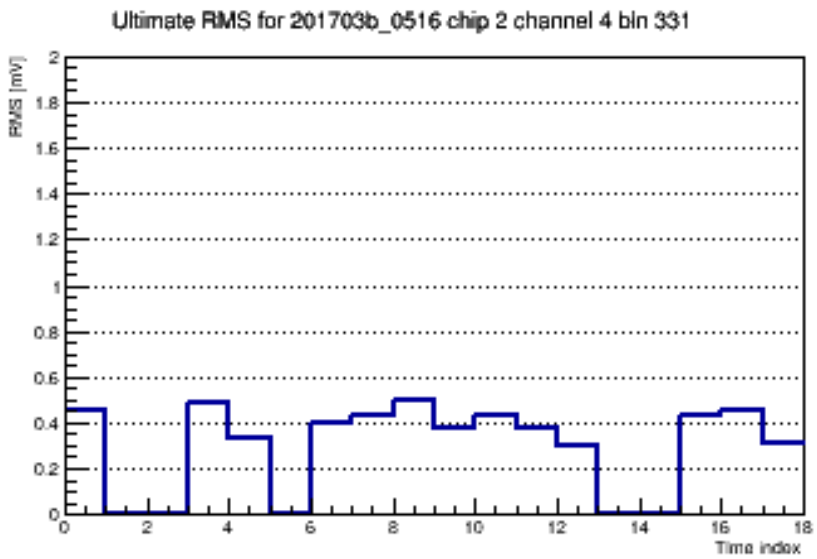


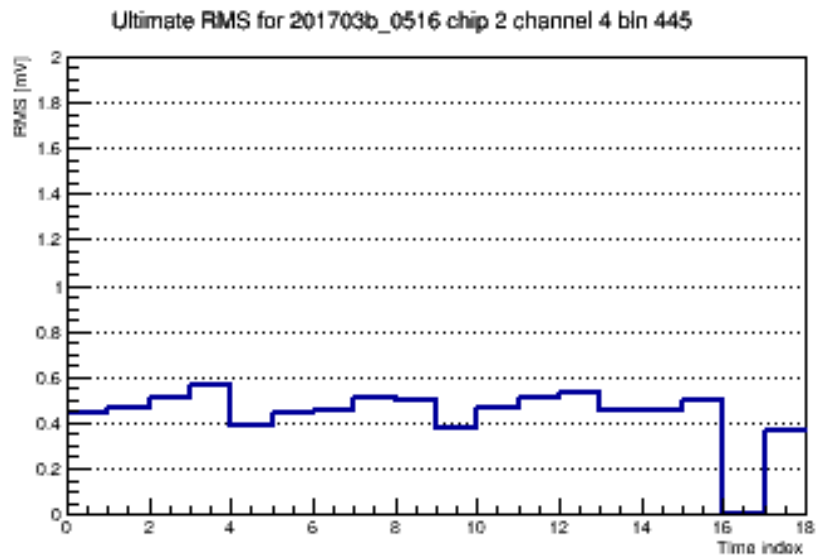


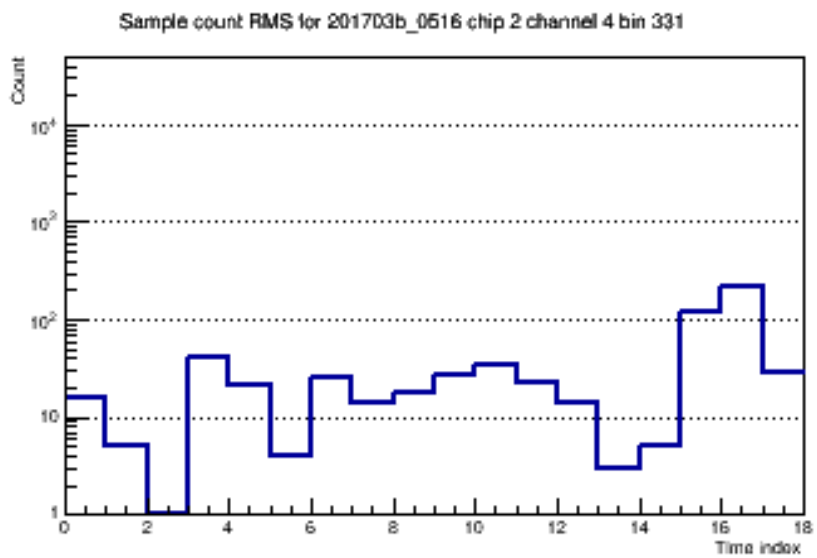


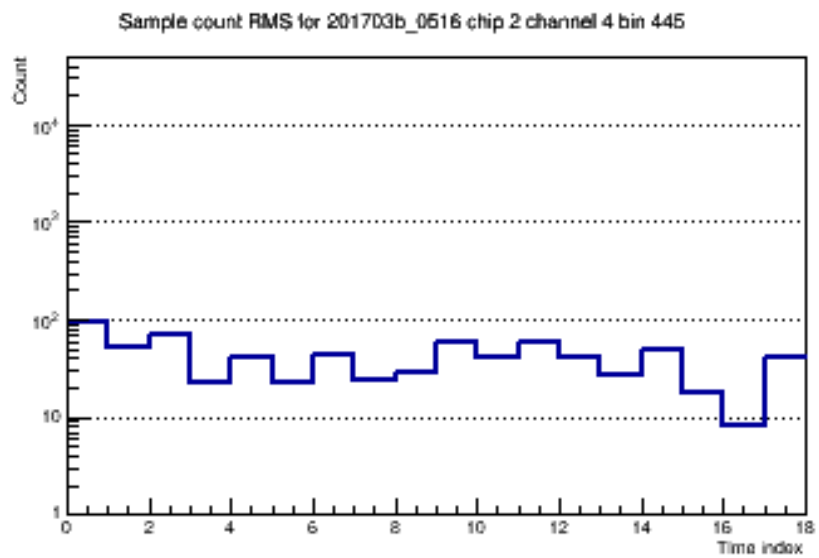
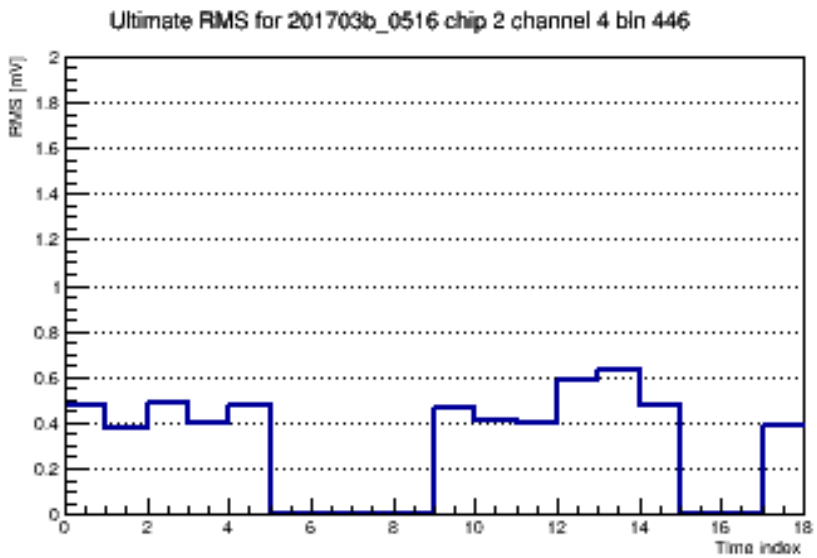
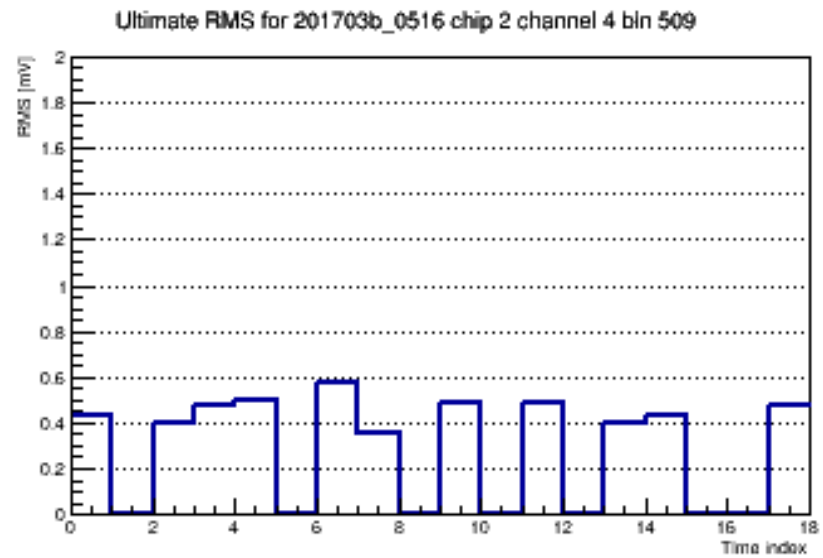
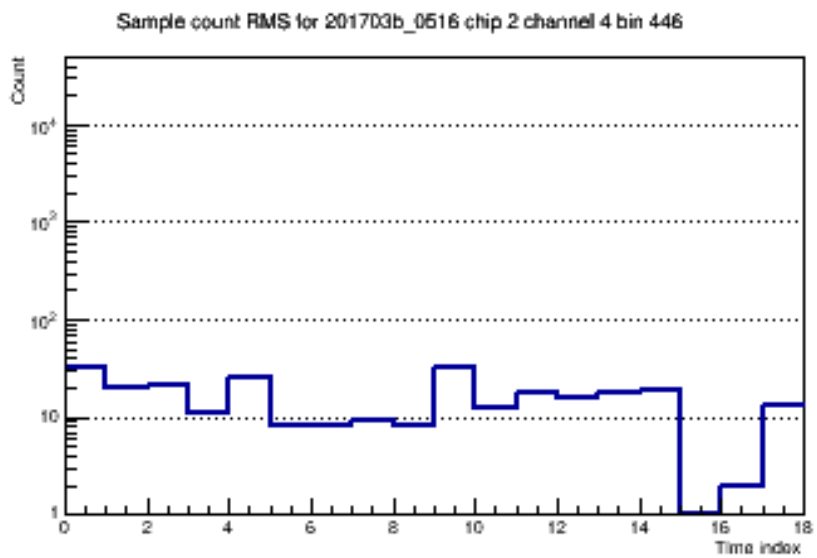
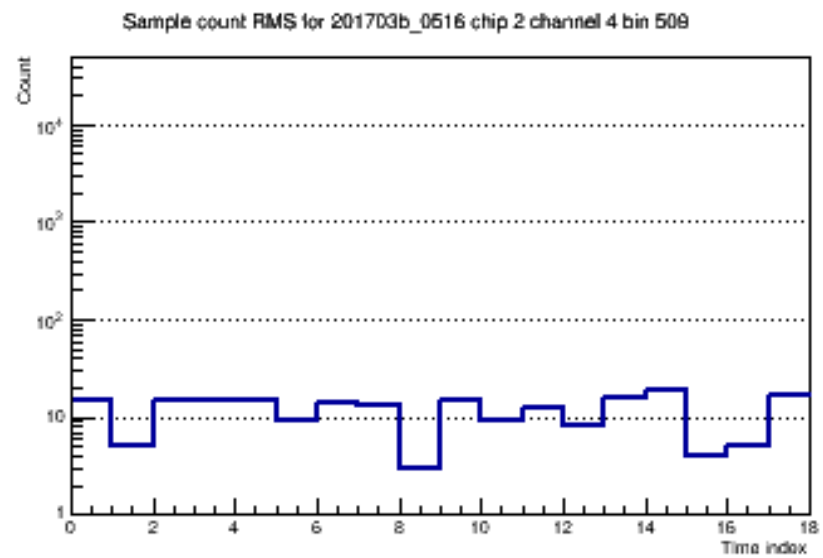


Time varying bins 61









Time varying bins 62