The VMM1 Front End IC for the ATLAS Muon System Upgrade

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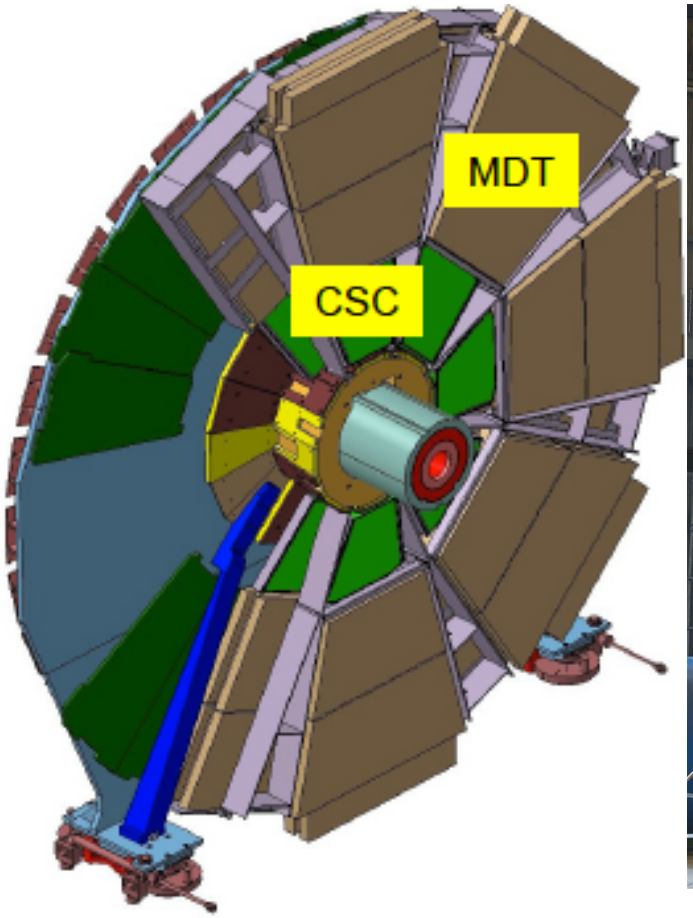
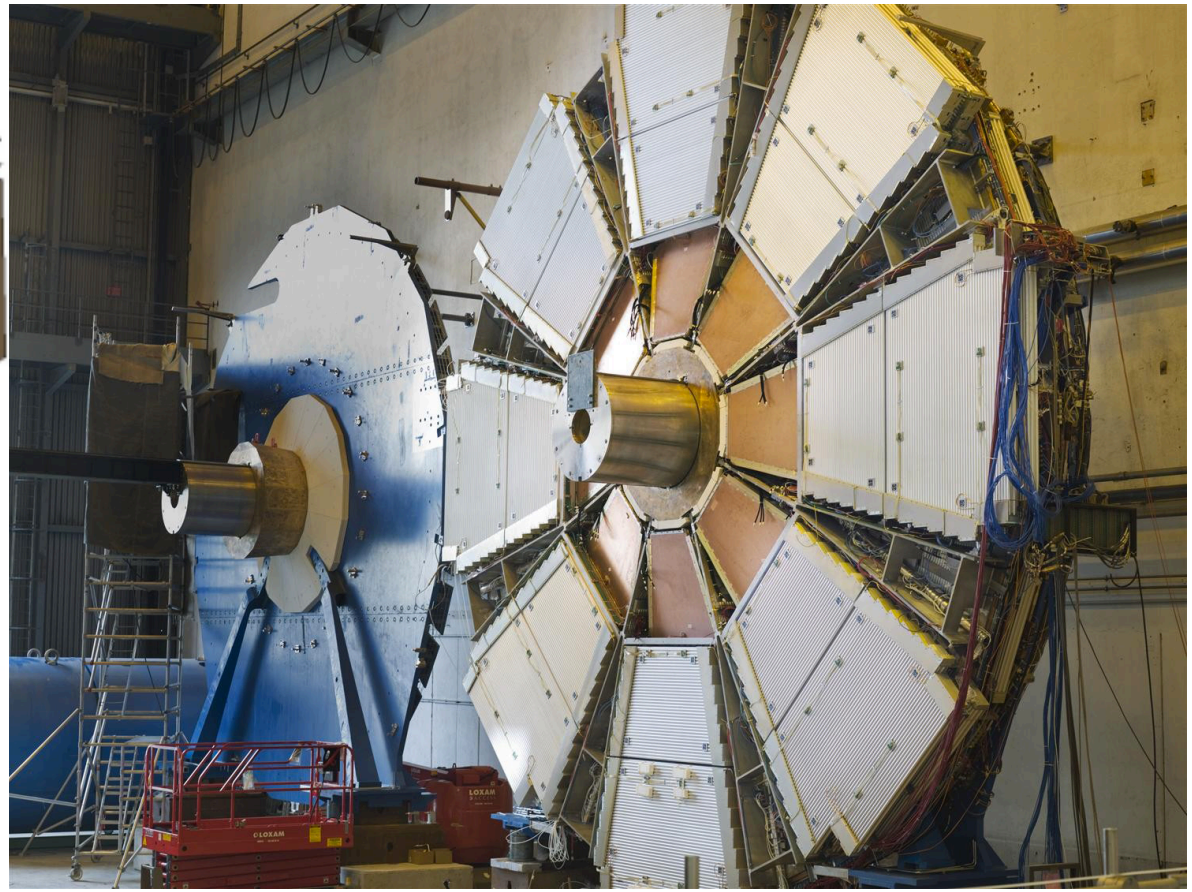
November 4, 2011

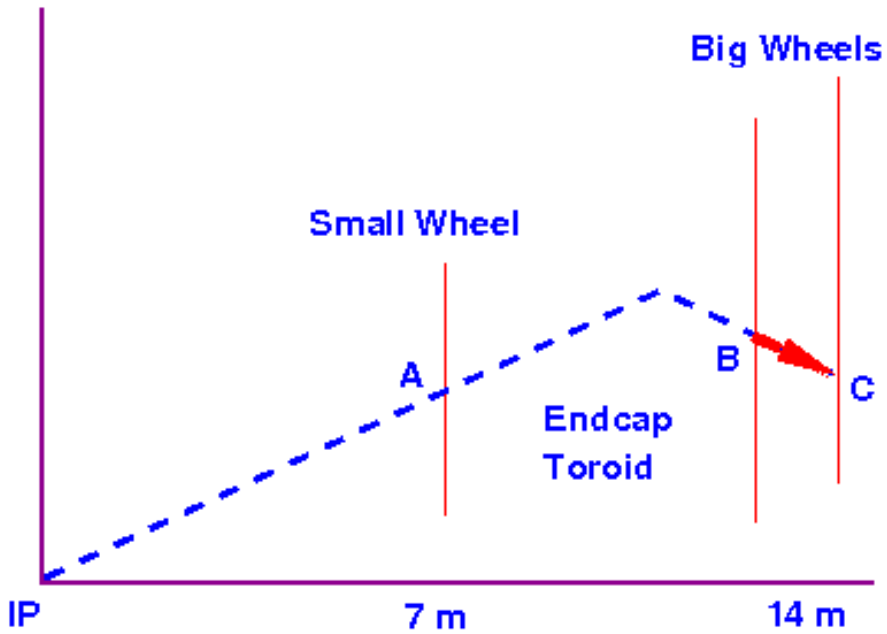
The Present "Small Wheels" (9m Diameter)

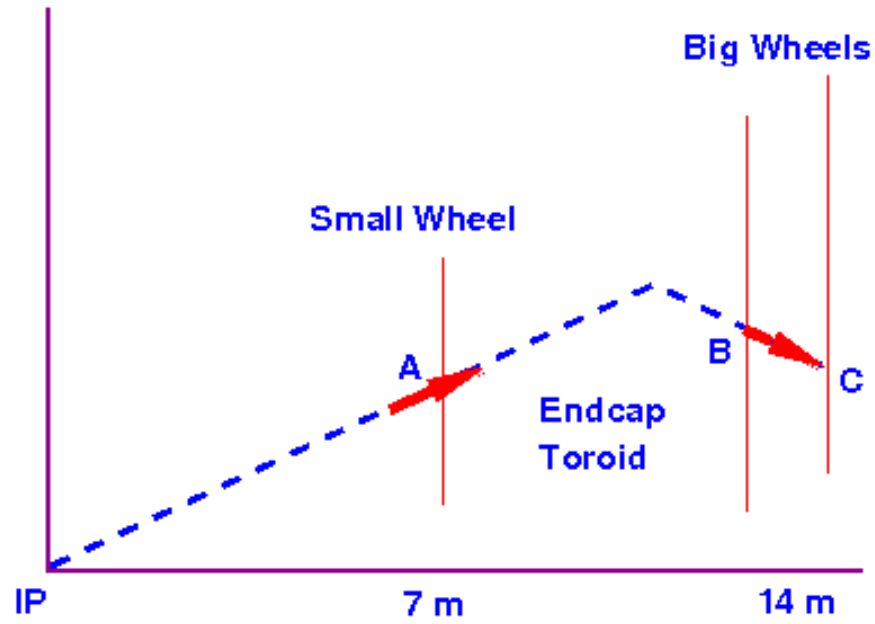




- Need New Detectors that participate in the Level1 Trigger by providing a vector with ~1 mrad resolution
- Need to handle considerably higher rates at L = 5x10e34

The Problem with High pT Triggers





Current Endcap Trigger

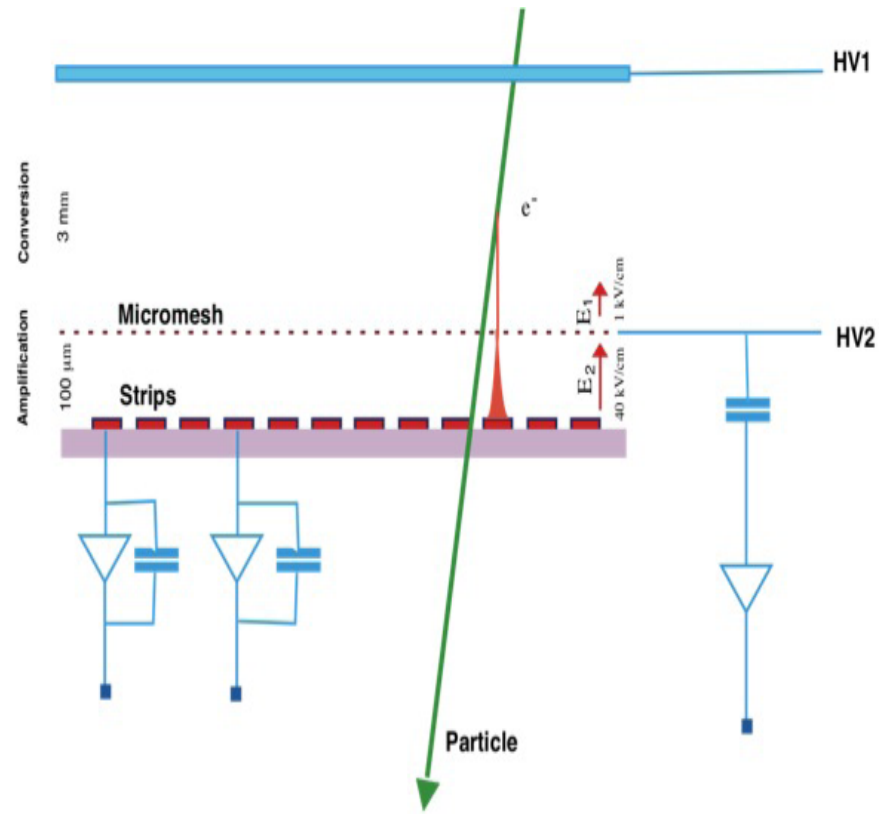
- Only a vector BC at the Big Wheels is measured
- Momentum defined by implicit assumption that track originated at IP
- Random background tracks can easily fake this

ProposedTrigger

- Provide vector A at Small Wheel
- Powerful constraint for real tracks
- With pointing resolution of 1 mrad it will also improve pT resolution
- Currently 96% of High pT triggers have no track associated with them

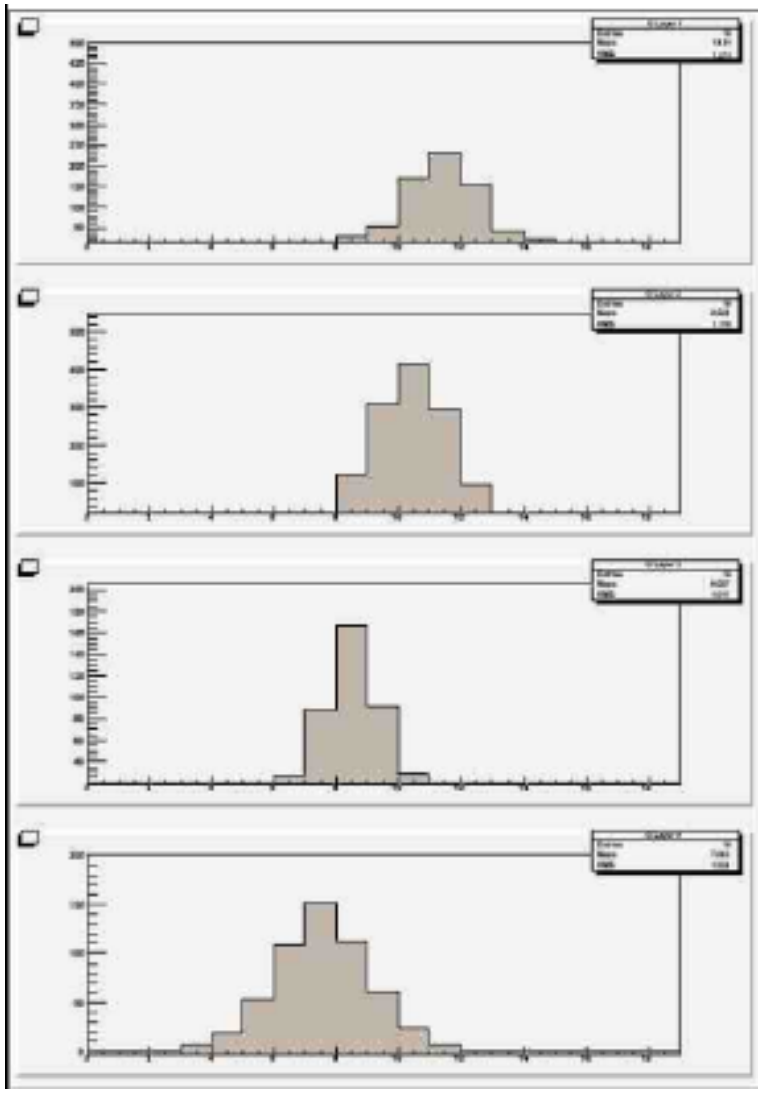
The Micromegas Option and what is required from the Front End

- Many good characteristics
  - Able to operate in high rate environment
  - Detector efficiency ~ 99%
  - Spatial resolution 80 μm
  - Time resolution 5 ns
  - Level-1 trigger capability
- Signal Processing requirements
  - Charge measurement for precision charge interpolation (a la CSC) for shallow incidence angles (resolution degrades as tanθ)
  - Time measurement with resolution of ~2 ns for the micro-TPC mode appropriate for large incidence angles



- Strip Capacitance ~200 pF
- Dynamic range ~400 fC
- Integration Time 50-100 ns

Front End Requirements for the TGC Option



- Determine Position by charge interpolation
- For Trigger, use Discriminator outputs and Time-over-threshold as a measure of charge

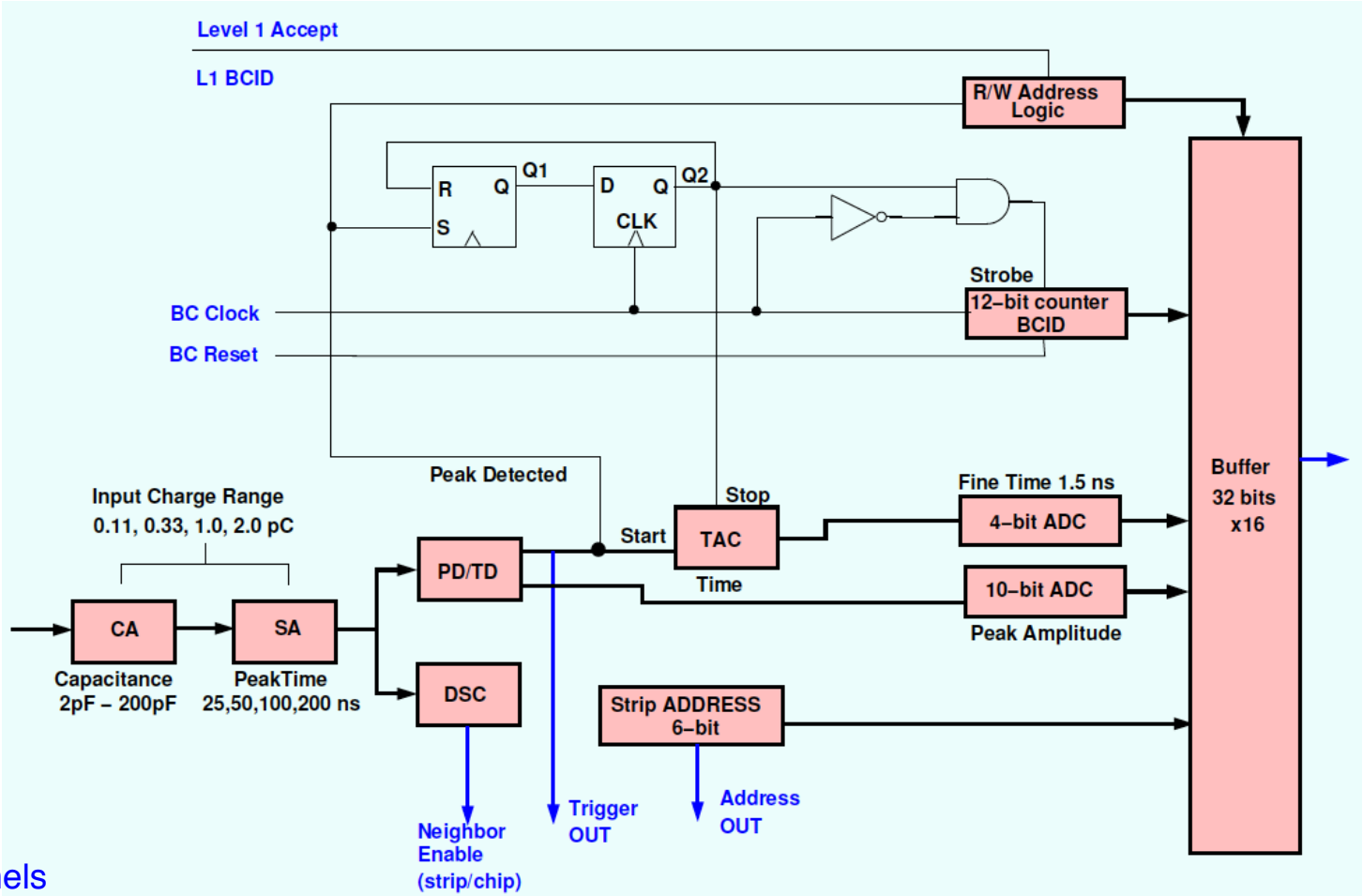
- Strip Capacitance ~200-300 pF
- Dynamic Range ~2 pC
- Integration time 25 ns
- LVDS outputs of ALL channels in parallel

The Challenge (micromegas case)

- The Small (~0.5 mm FWHM) charge footprint of the μMegas Detectors results in excellent position and double track resolution
- Results in a very large number of channels (order 10^6)
- Two Functions of the Readout:
  - Provide Precision measurement of charge and time at Trigger Level 1 accept
  - Provide in real time vector with ~1 mrad resolution to assist Trigger Level 1

- First task relatively easy to accomplish by highly multiplexed, data driven system
- Custom front end ASIC being under development

Block Diagram of the IC being designed

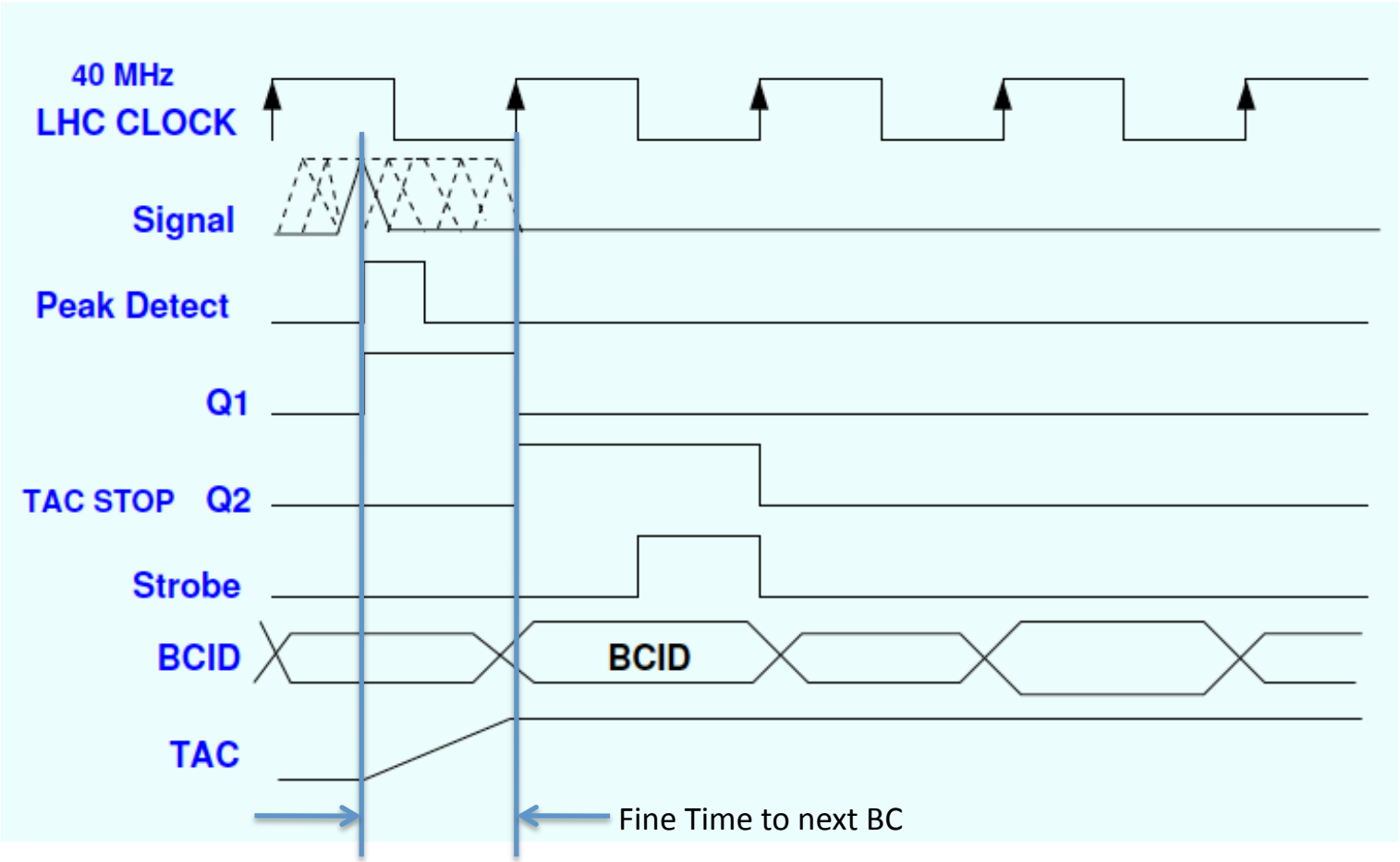


To SRS

- 64 channels
- adj. polarity, adj. gain (0.11 to 2 pC), adj. peaking time (25-200 ns)
- derandomizing peak detection (10-bit) and time detection (1.5 ns)
- real-time event peak trigger and address
- integrated threshold with trimming, sub-threshold neighbor acquisition
- integrated pulse generator and calibration circuits
- analog monitor, channel mask, temperature sensor
- continuous measurement and readout, derandomizing FIFO
- few mW per channel, chip-to-chip (neighbor) communication, LVDS interface

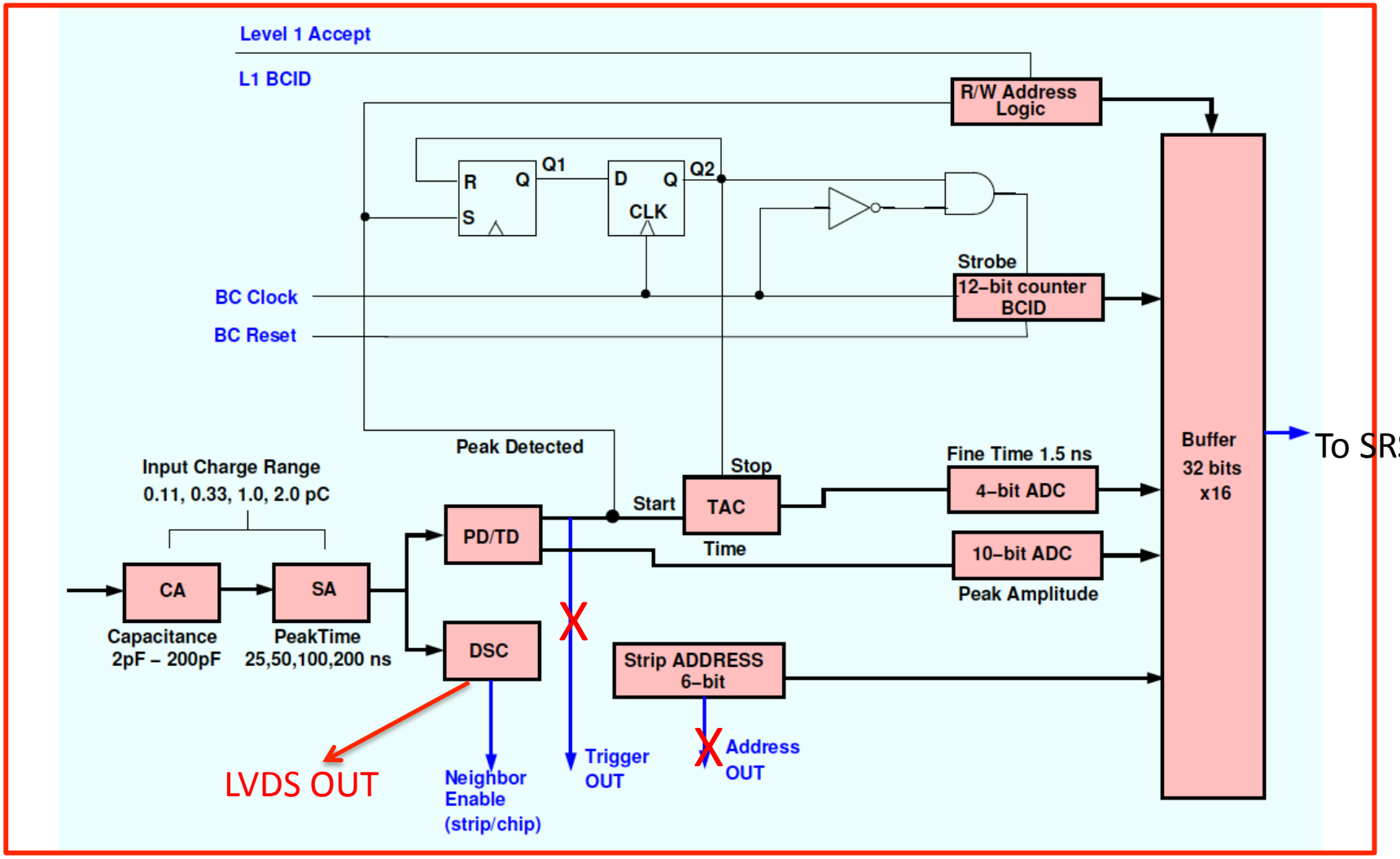
Readout at L1 Accept
No Problem
Zero-suppressed, already digitized, much of DAQ already on Front End IC

Timing Diagram



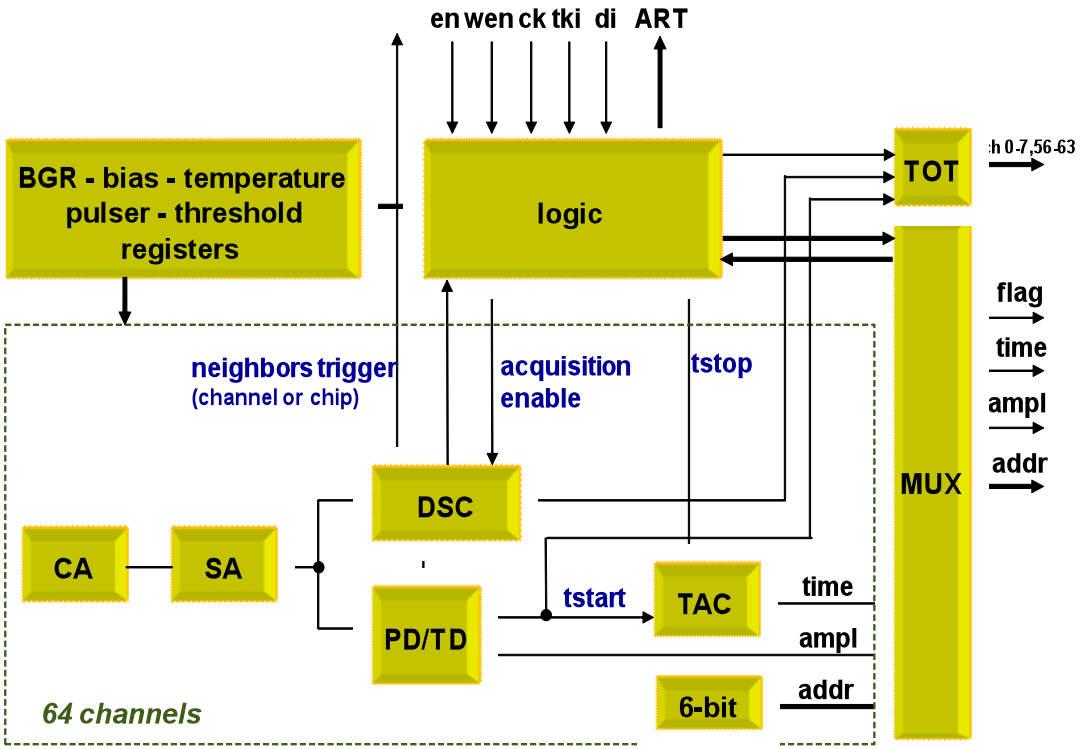
40 MHz BC clock convenient for LHC but any clock can be used to related hit with trigger accept

For a TGC-based Trigger/DAQSystem



For TGC there will be fewer (16 or 32) channels with LVDS outputs of individual discriminators
All other features remain the same

Operation and functions



Functions

- common
  - temperature monitor
  - pulse generator (10-bit adjustable amplitude)
  - coarse threshold (10-bit adjustable)
  - self-reset option
  - analog monitors
    - analog, trim thresholds, BGR, DACs, temp.
    - analog buffers
- analog section
  - charge amplifier (200pF), high-order DDF shaper
  - adjustable polarity (negative, positive)
  - gain: 0.5, 1, 3, 9 mV/fC (2, 1, 0.33, 0.11 pC)
  - peaktime: 25, 50, 100, 200 ns
  - test capacitor, channel mask
- discriminator
  - trimmer (4-bit adjustable, 1mV)
  - sub-hysteresis pulse processing option
  - neighbor logic on channels and chips (ch0, ch63)
- peak detector multiphase
- time detector
  - TAC ramp (selectable 100, 200, 500, 1000 ns)
  - start at peak-found
  - stop selectable (ena-low or stp-low)
- ART
  - address of the first event in real time
  - selectable at first threshold or at first peak
  - self-resets in 40ns
  - fflag indicates event
  - address available at fa0-fa5
- timing per channel
  - available for channels 0-7 and 56-63
  - selectable between ToT and TtP
- readout
  - flag at first peak indicates events to readout
  - sparse with smart token passing (skips empty chan.)
  - amplitude available at pdo
  - timing available at tdo
  - address available at a0-a5

Modes of operation

- acquisition: events are detected and processed (amplitude and timing)
  - charge amplification, discrimination, peak- and time-detection
  - address in real time (ART) of the first event
  - direct timing (ToT or TtP) per channel for channels 0-7 and 56-63
- readout: sparse mode with smart token passing (amplitude, timing, addr.)
- configuration: access to global and channel registers

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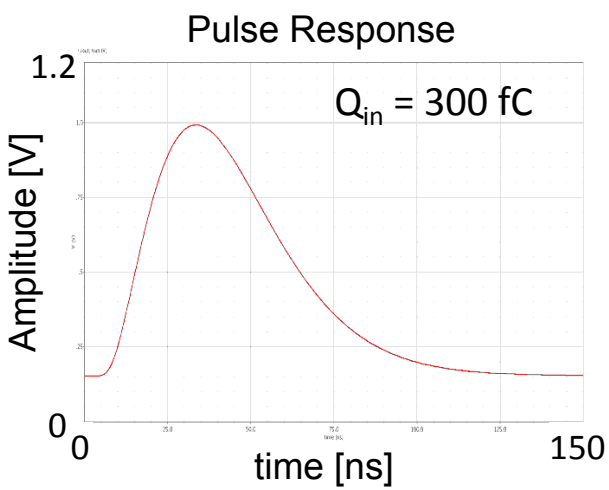
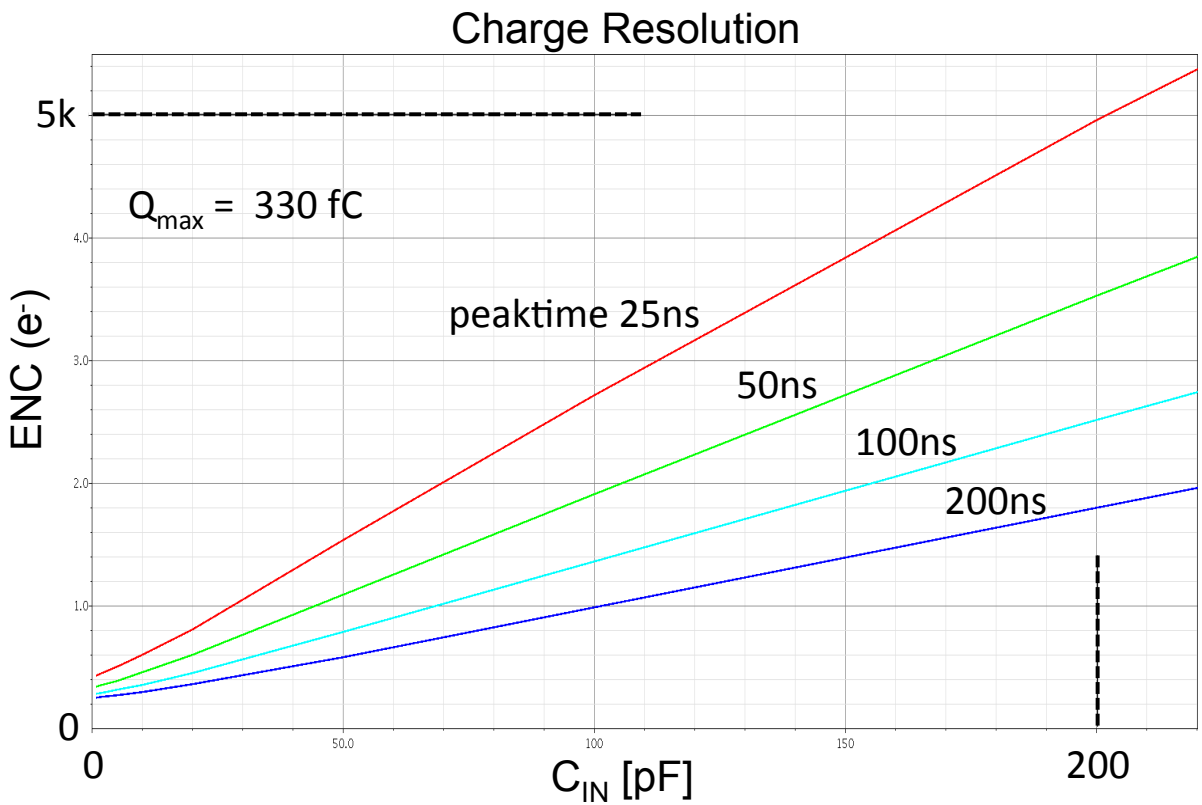
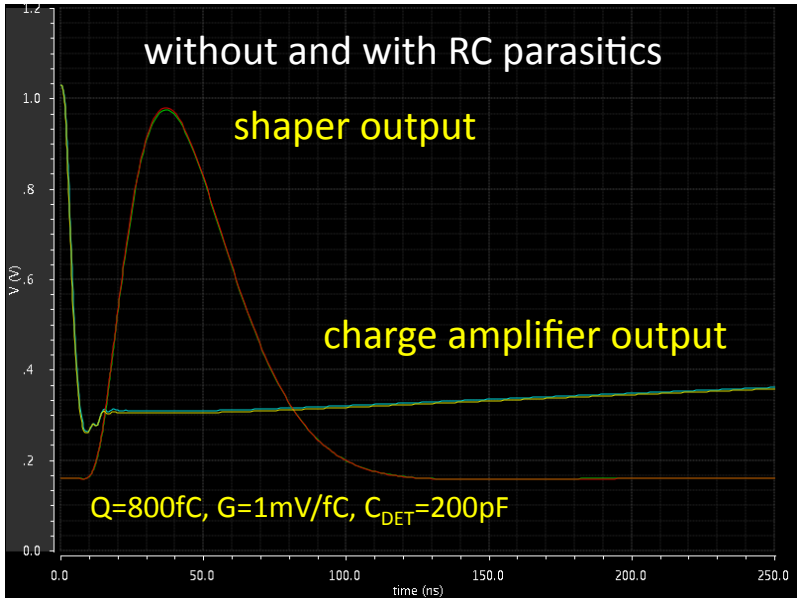
VMM1 IC SPICE Simulation performance

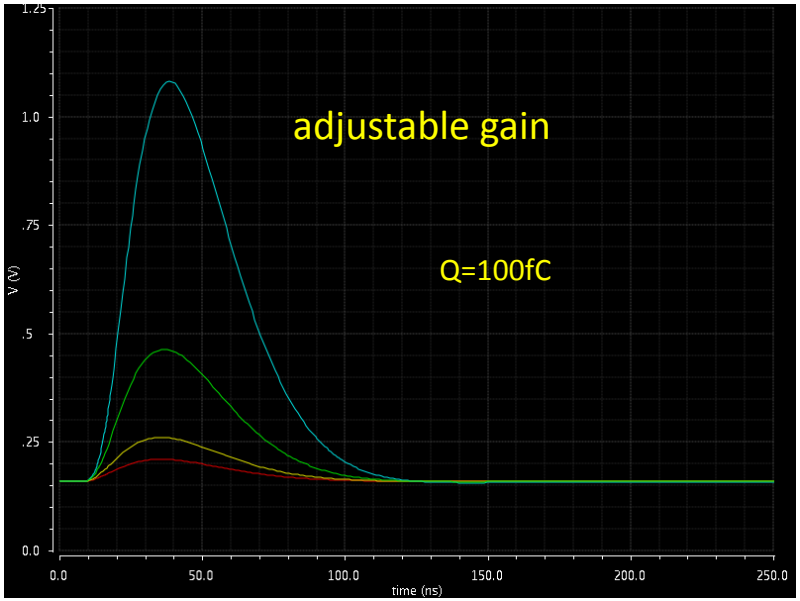
Analog section:
transistor-level simulations
power ≈ 4 mW

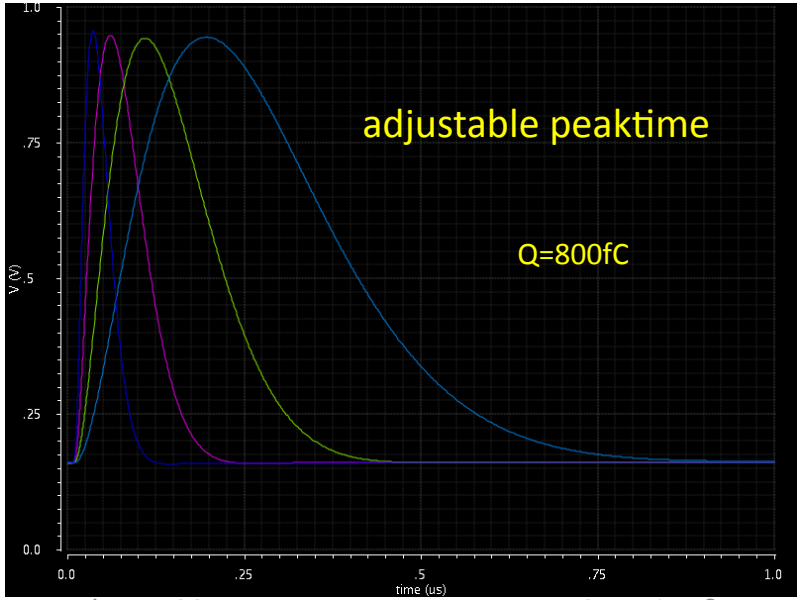


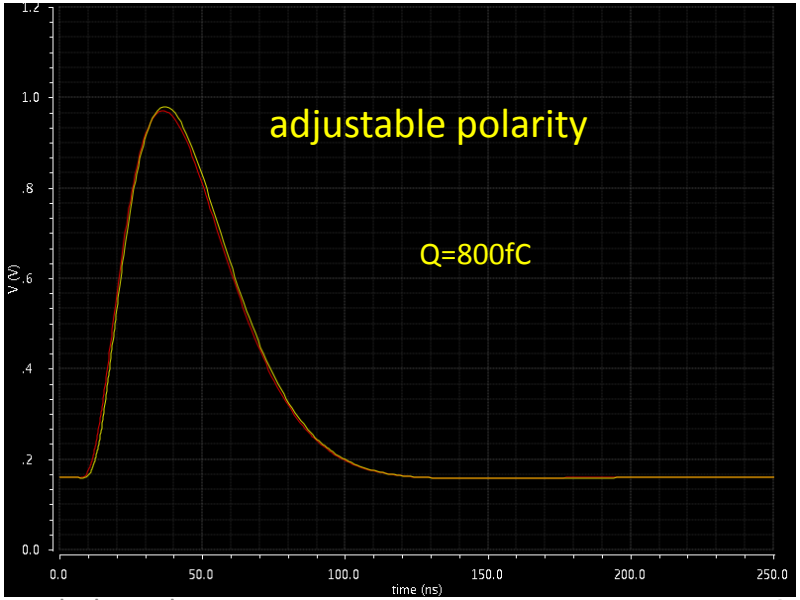


Analog section - simulations 2/2

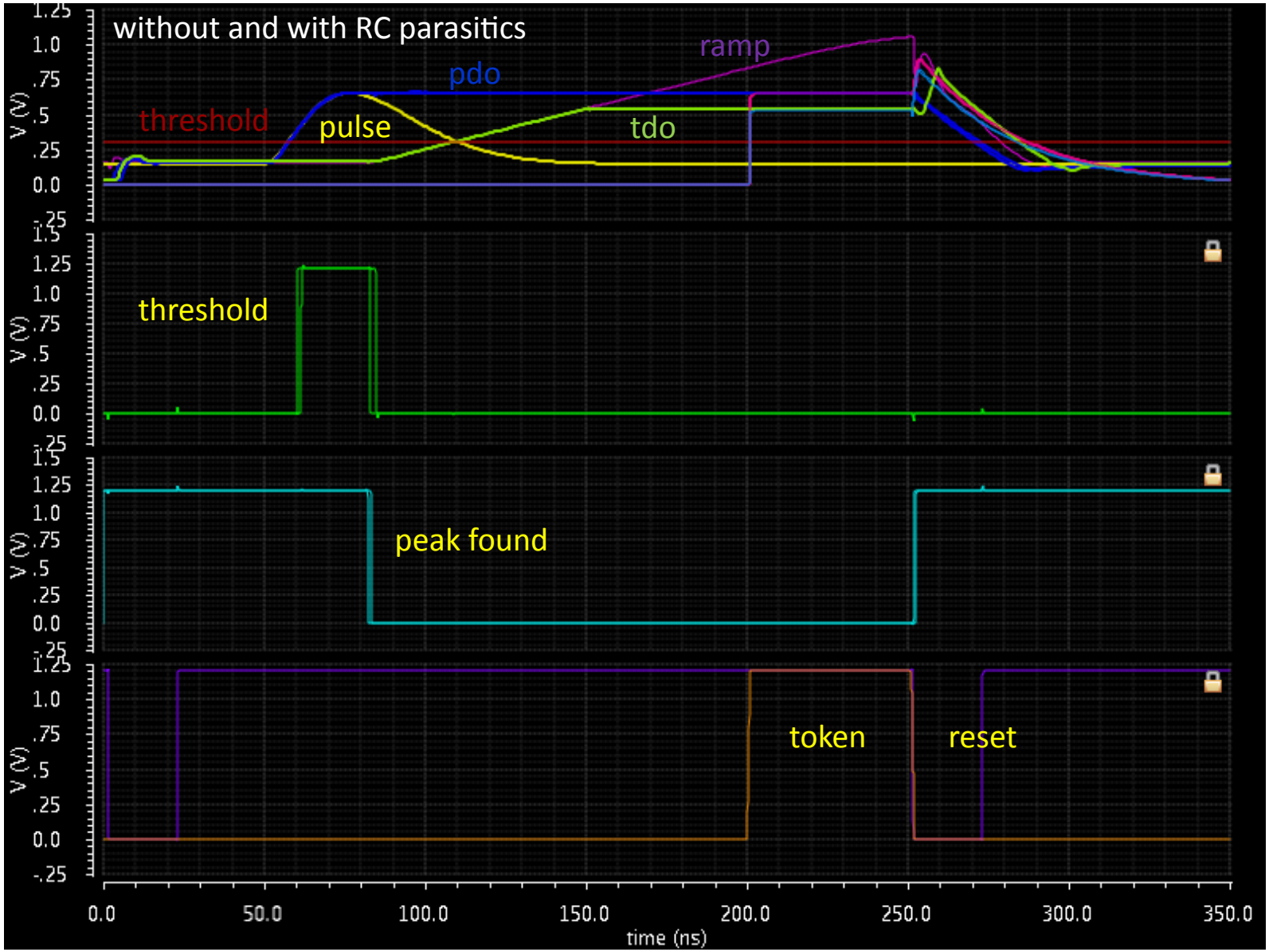






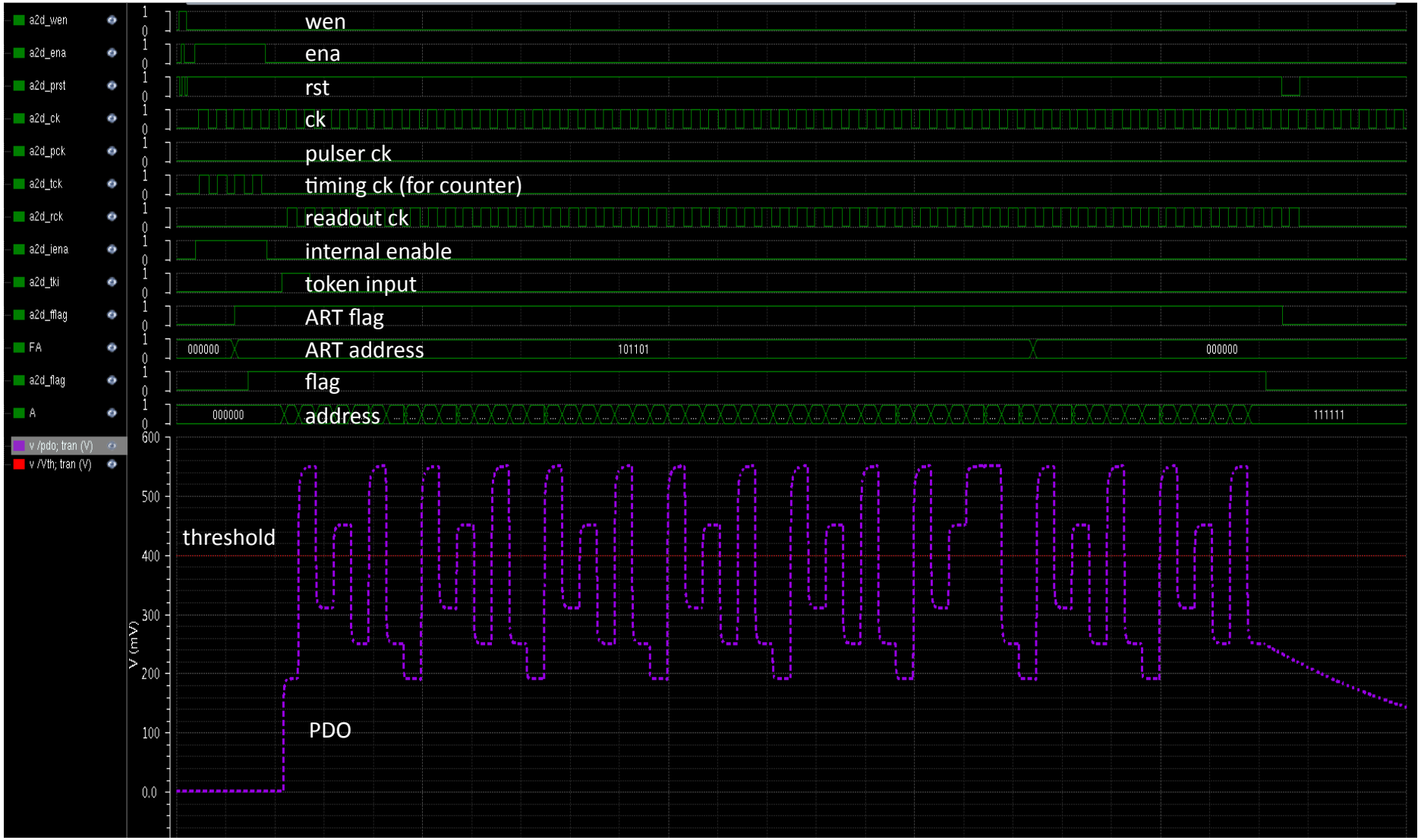


Peak and time detectors - simulations



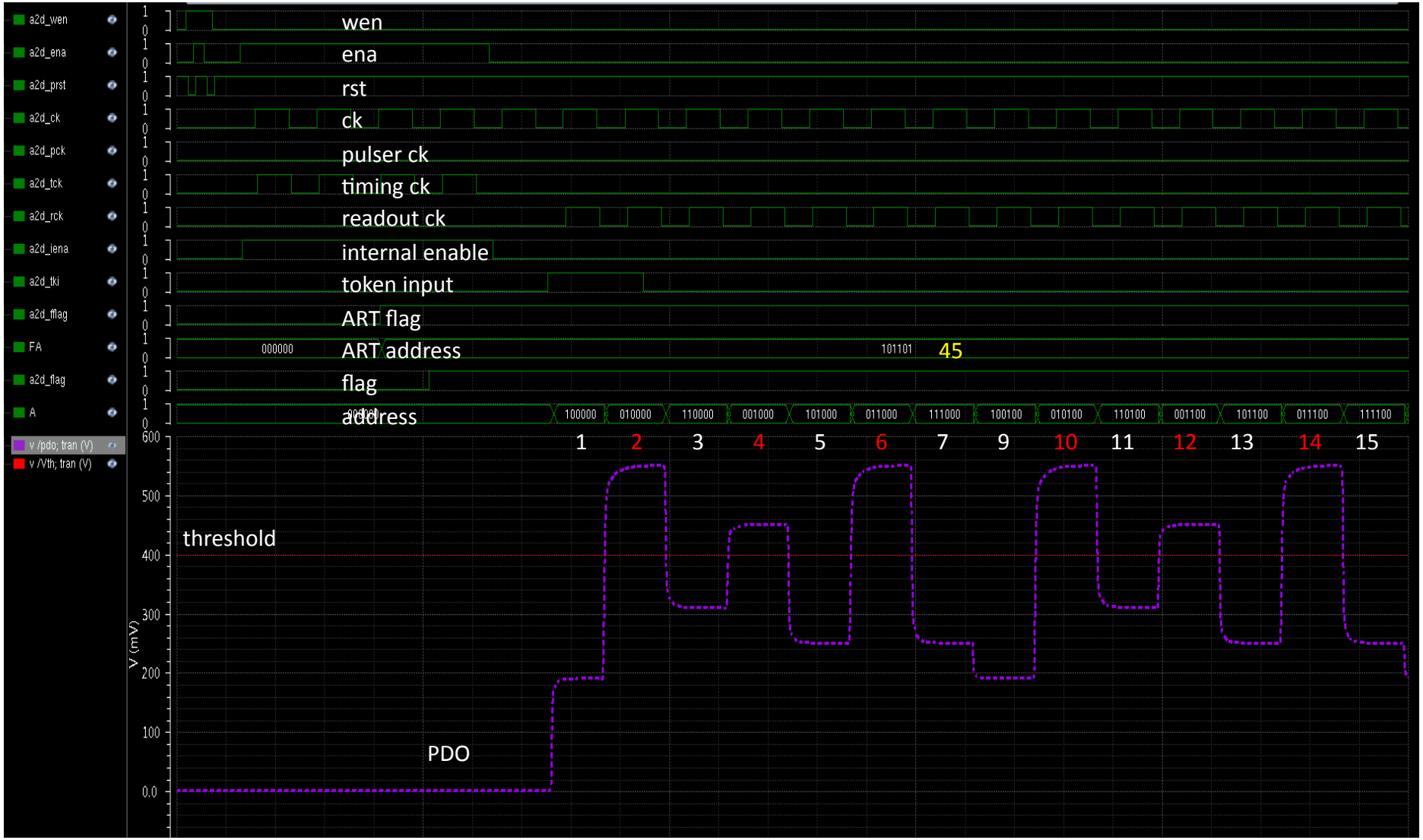
TAC stop signal at 150ns (not visible); timing at peak found (low time walk)

System-level simulations 1/2



ART at threshold (selectable), flag at peak

System-level simulations 2/2



channels 2, 4, 6, 10, 12, 14 exceed threshold; neighbors are collected
channel 45 hits 2 ns earlier than others (ART)

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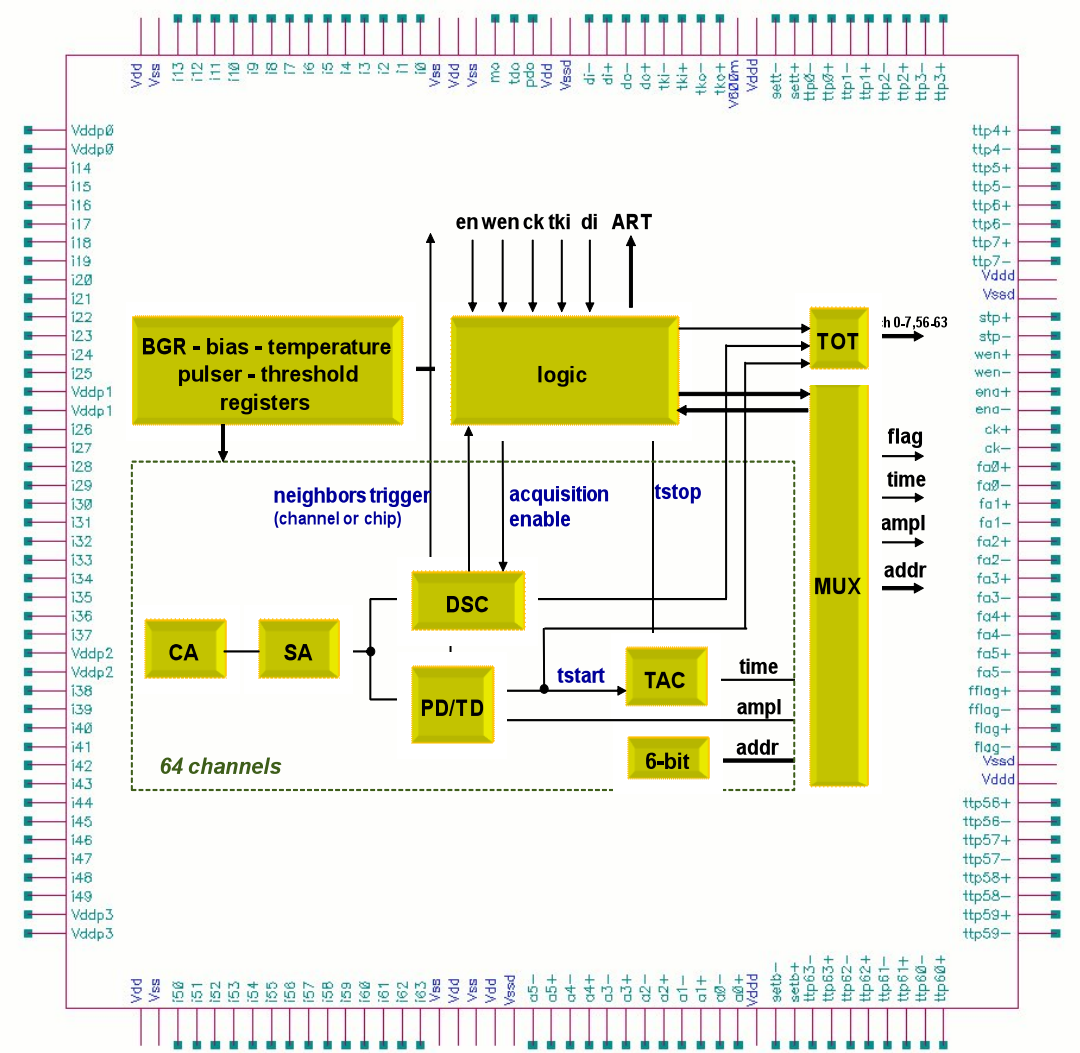
Pinout



Pinout

- 176 pins (44 each side)
- Vdd,Vss: analog supplies 1.2V and grounds 0V
- Vddd, Vssd: digital supplies 1.2V and grounds 0V
- Vddp0-Vddp3: charge amplifier supplies 1.2V
- V600m: reference for LVDS 600mV

- i0-i63: analog inputs, ESD protected
- mo: monitor multiplexed analog output
- pdo: peak detector multiplexed analog output
- tdo: time detector multiplexed analog output

- flag: event indicator
- a0-a5: multiplexed address, tristated (driven with token)
- ttp0-ttp7 and ttp56-ttp63: ToT or TtP

- fflag: ART event indicator
- fa0-fa5: ART address output

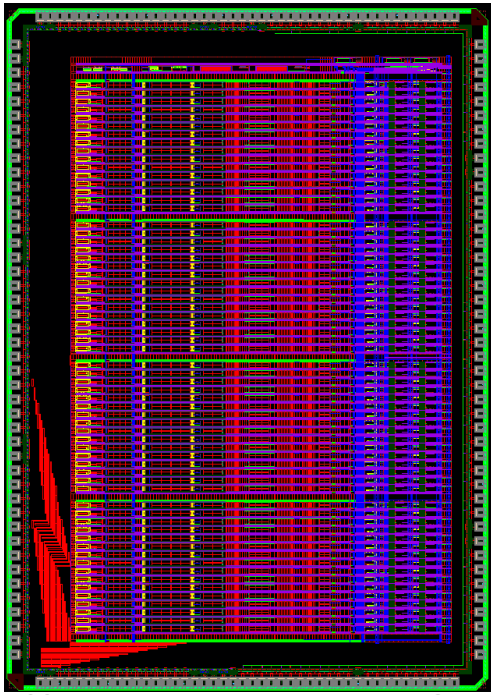
- stp: timing stop
- sett, setb: ch0, ch63 neighbor chip triggers (bi-directional)

- ena: acquisition enable
  - ena high, wen low: acquisition mode
  - ena low, wen low: readout mode
  - ena pulse, wen high: global reset
- wen: configuration enable
  - wen high: configuration mode
  - wen pulse: acquisition reset
- ck: clock
  - in acquisition mode ck is counter clock
  - in readout mode ck is readout clock
  - in configuration mode ck is writein clock

- tki, tko: token input and output (3/2 clock wider)
- di, do: data configuration input and output (1/2 clock shifted)
  - in acquisition mode di is pulser clock

Schedule and status

	scheduled	completed
Analog section	Jan 2011	February 2011
Peak/time section	March	April
Common circuitry	April	May
Digital sections	May	July
Physical layout	July	October
Fabrication	September	**Queued for November 7th**



- technology IBM 8RF CMOS 130 nm
- size 5.9 mm x 8.4 mm (~50mm²)
- pads count 176, package LQFP 176
- fabrication cost (MPW MOSIS) ~ $150k
- next available runs:
  - November 7th, 2011
  - February 6th, 2012

Summary

- Data driven, peak and amplitude detection, on-chip ADC and derandomizing buffers result in efficient DAQ with low data volume (essentially a "DAQ in a chip")
- Prototype has all Basic Functionality for both mMegas and TGC
- Has all 64 channels (16 for the TGC option) as required for the final version
- This is important for demonstrating the critical trigger functions

Extra Slides

BUT, How about Trigger?
Need to process in Parallel at 40 MHz

How can we take advantage of the 0.5 mm strip pitch?

Assume that we use ONLY one hit (the strip with the first arriving signal above a set threshold) from each 64-channel chip at each bunch crossing

This way:

- We have a trigger system with granularity of 3.2 cm (64 channels x 0.5 mm) BUT
- With spatial resolution ~ 0.5 mm
- We now have to deal with ~30,000 channels and not 2 million

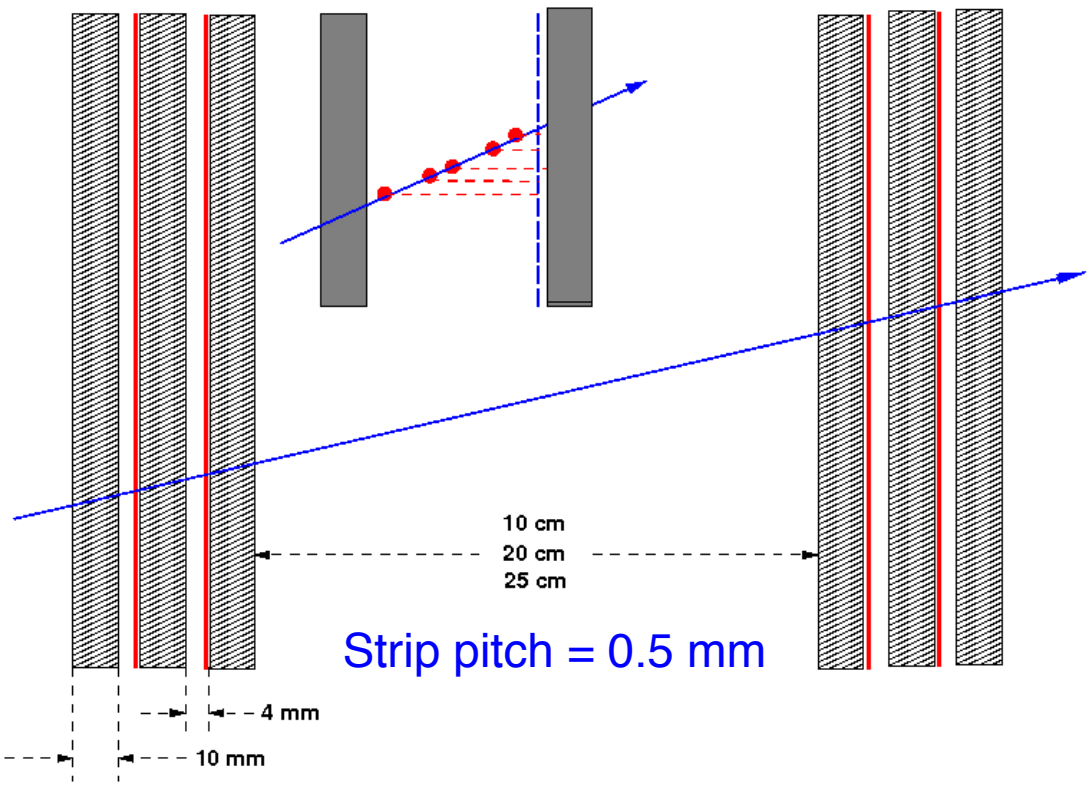
But are we paying a price for this? i.e. efficiency loss?

Consider worst case at η= 2.4:
Rate r = 10 kHz/cm^2, strip length l = 50 cm, strip width w = 0.5 mm

Occupancy/BC = rlwt = 6.25x10^{-4}

	Probability per Front End IC [%]		
# Hits	Probability per Chip per Bunch Crossing	Probability per Chip per 3 Bunch Crossings	Probability per Chip per 5 Bunch Crossings
0	96.1	88.7	81.9
1	3.8	10.6	16.5
>=2	0.1	0.6	1.6

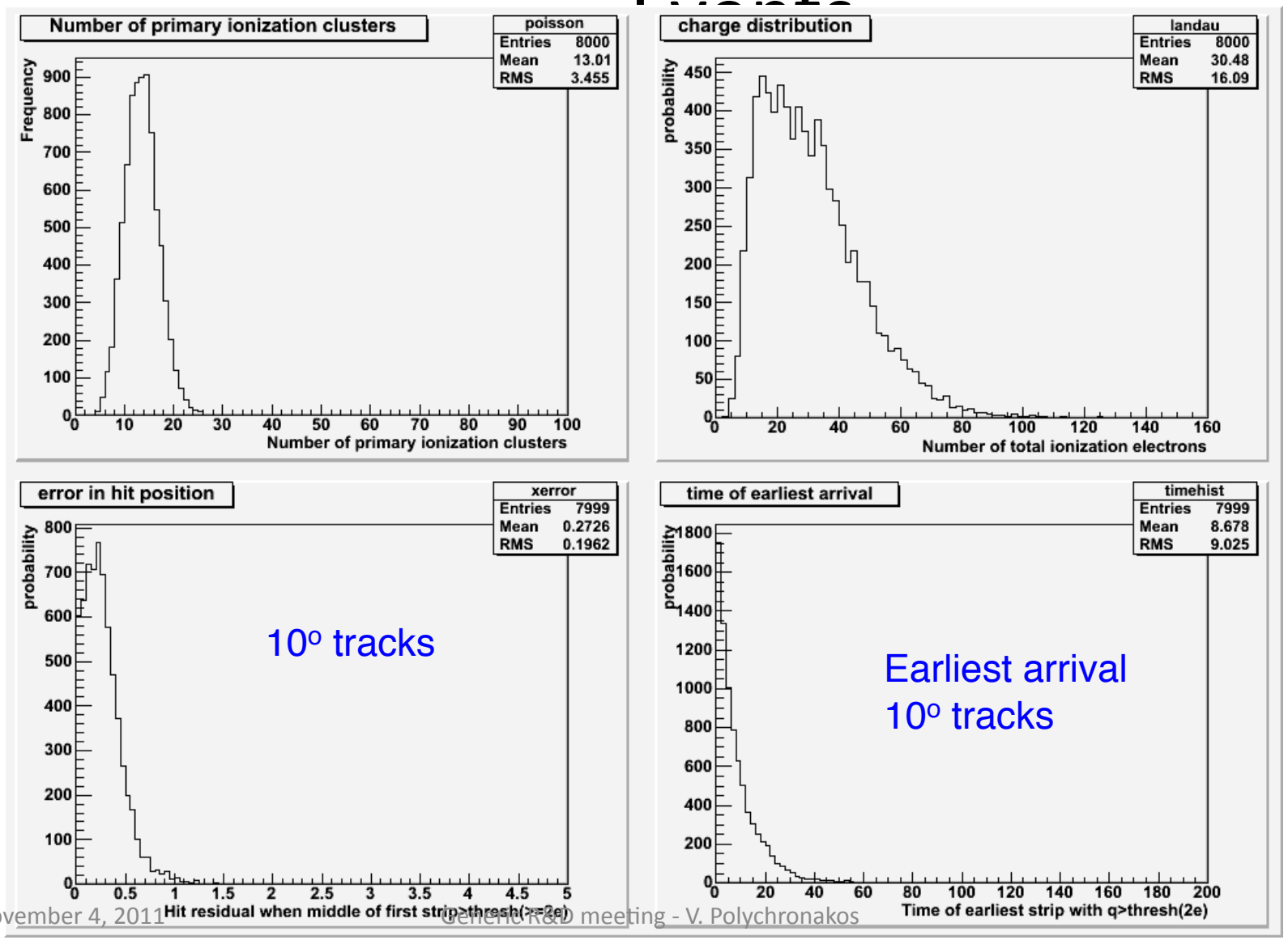
Toy Monte Carlo



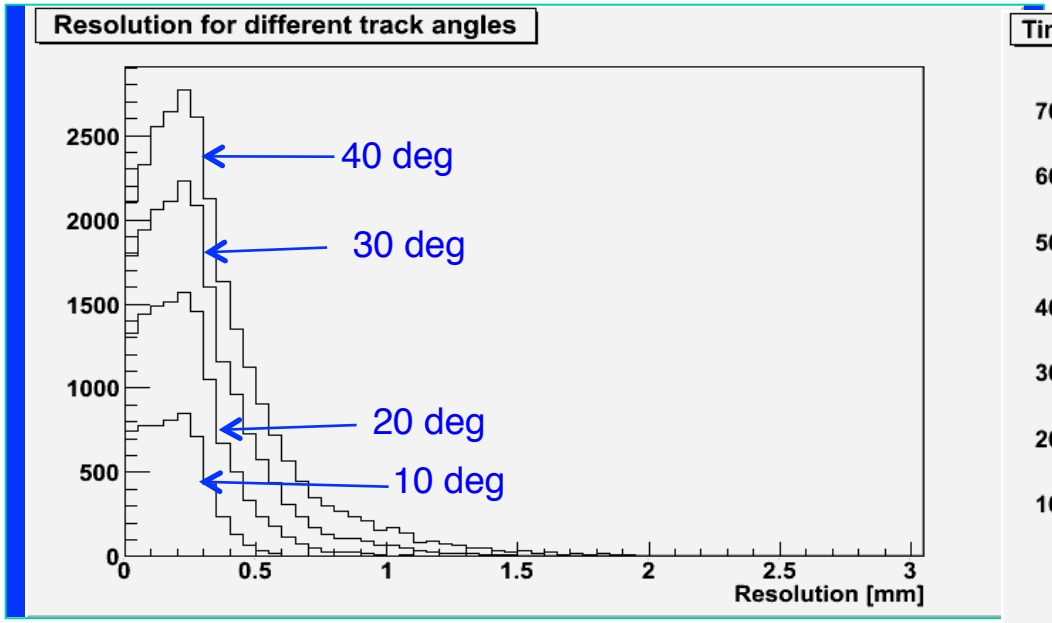
- Generate track at a given angle
- Track crosses a strip at a random position
- Generate primary ionization clusters Poisson distributed
- Generate number of electrons for each cluster
- Take strip with earliest time and charge over a certain threshold as the track's coordinate

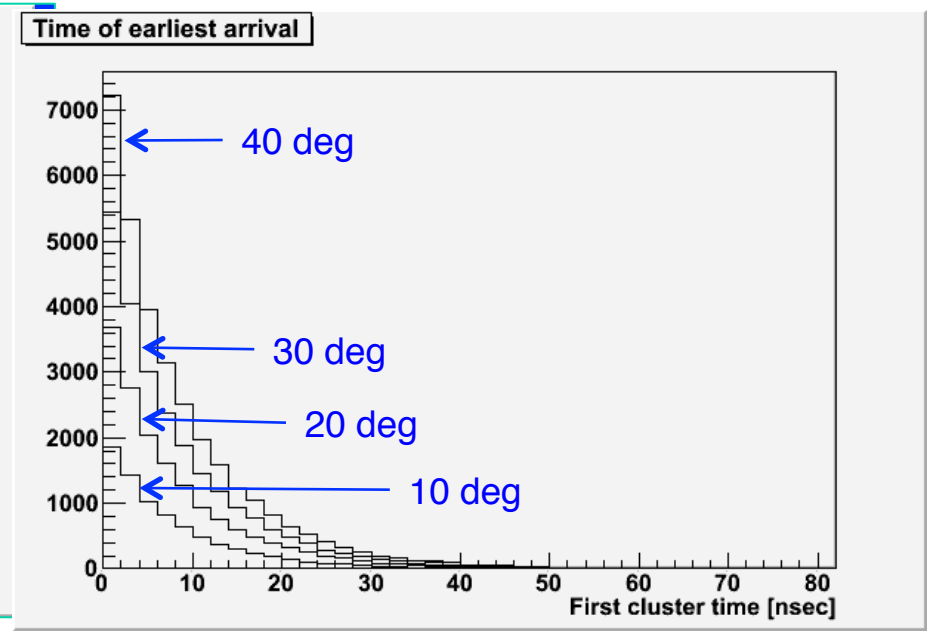
Reconstruct track and compare slope with the generated one
No transverse diffusion considered but effect is negligible for the first arriving cluster

Sanity Check
Distributions of MC generated Events



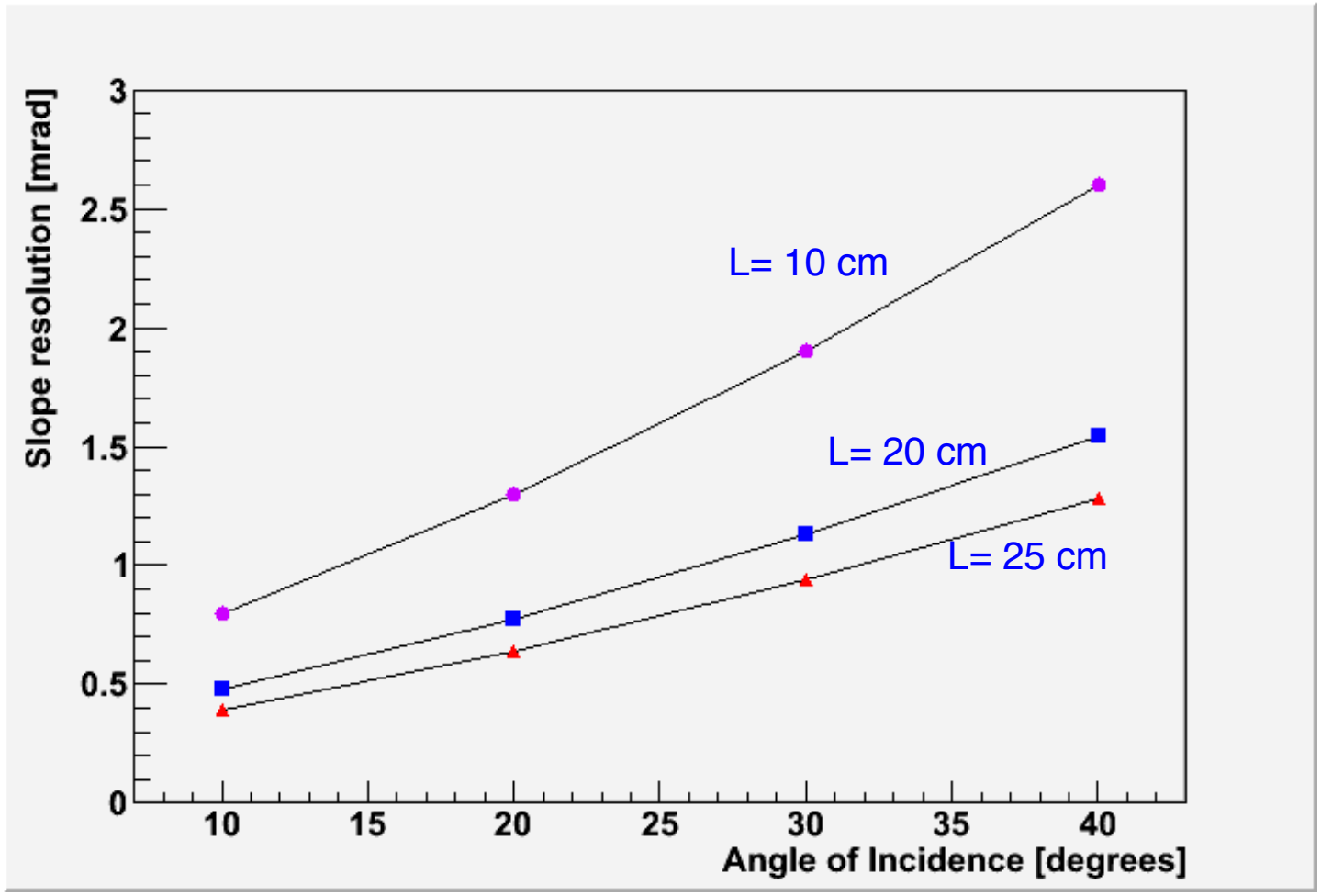
Position and Timing Resolution as a function of incidence angle



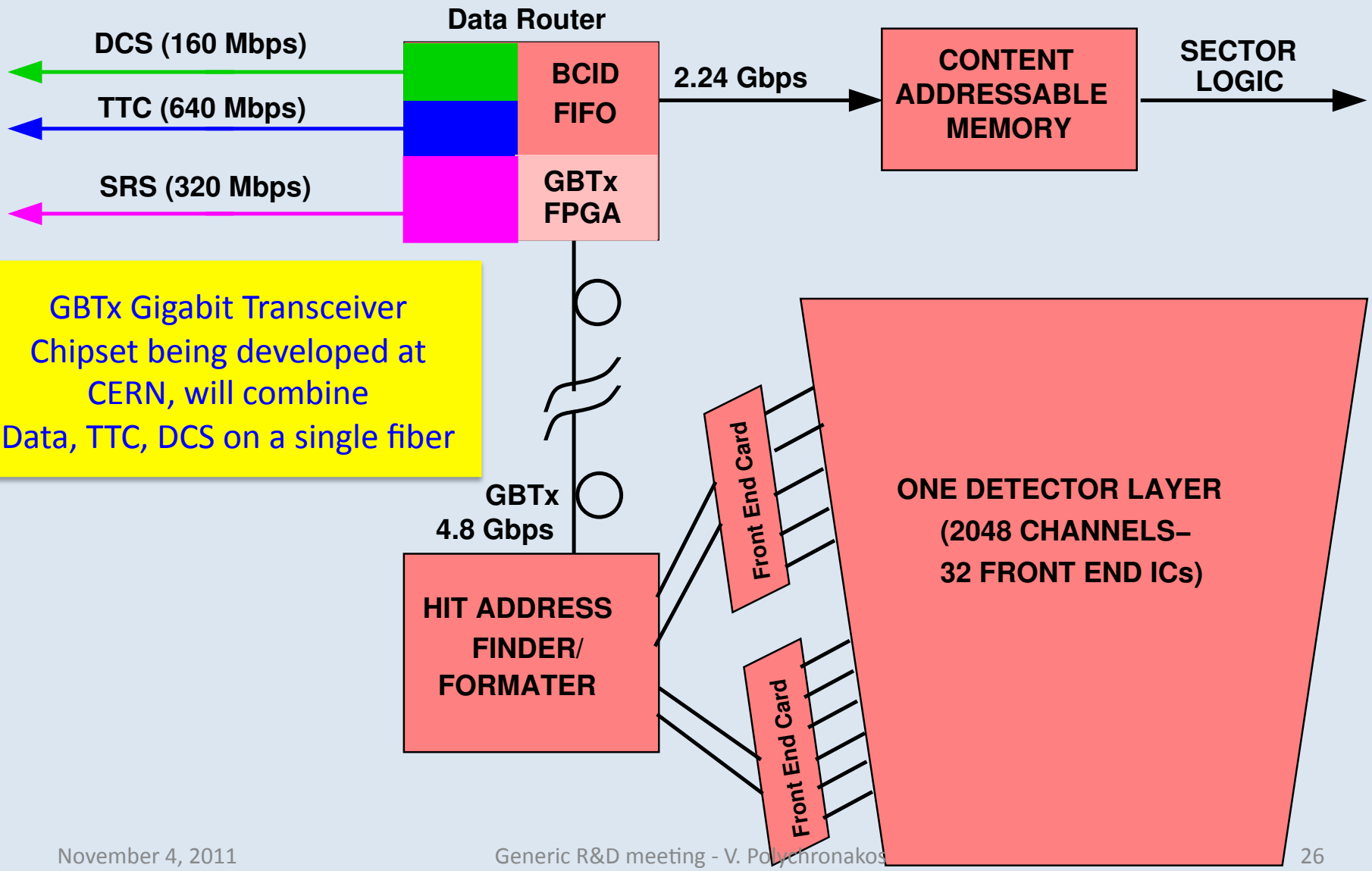


- Average spatial resolution below 0.5 mm for all angles in Small Wheel acceptance
- Time of first cluster above threshold mostly below 25 nsec
- Requiring, e.g, 3 out of 4 detectors to be within a BC should result in ~100% efficiency
- Address of strips can be directly used in a lookup table (e.g. Content addressable memories similar to FTK

Slope Resolution



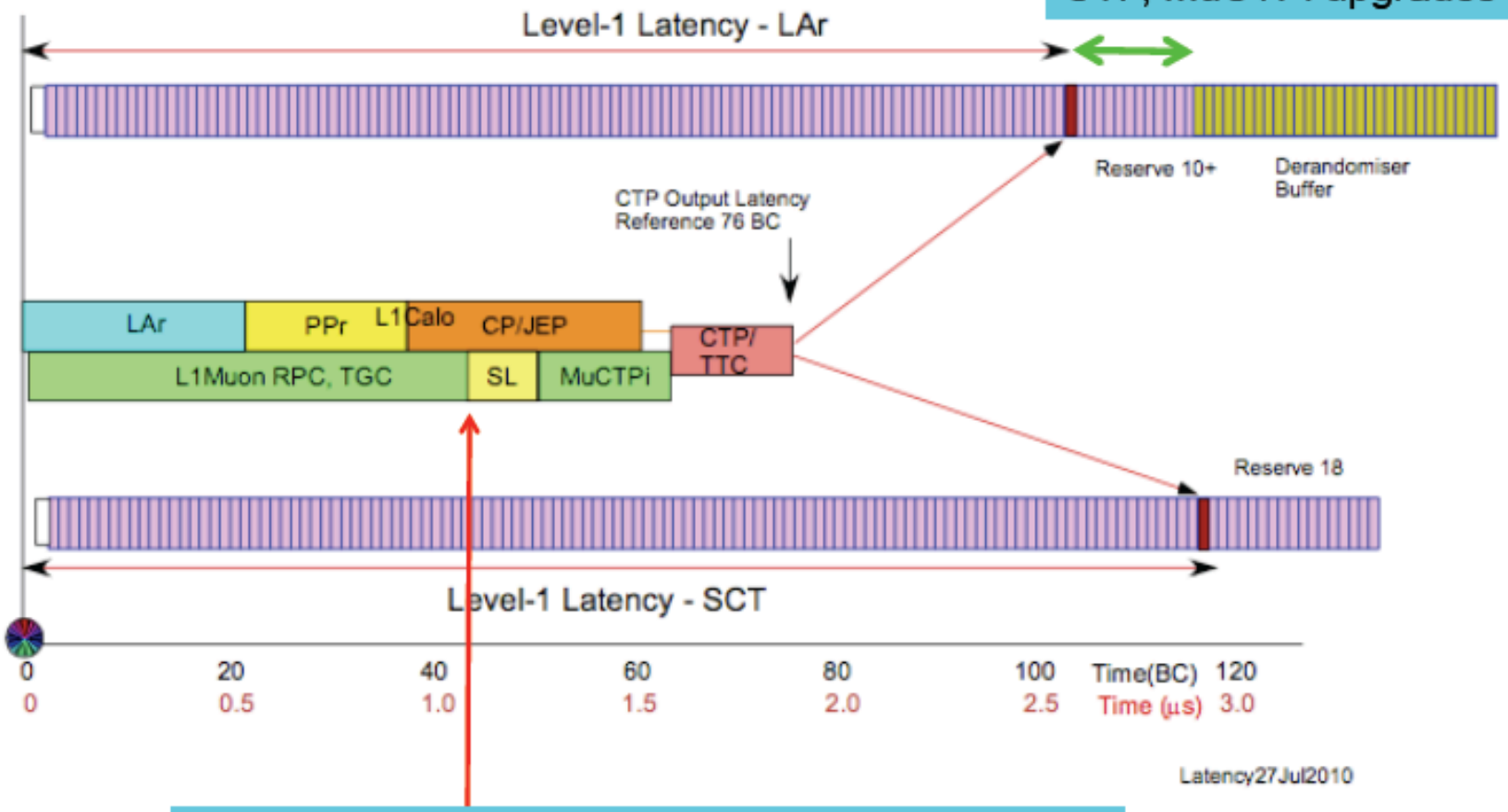
Trigger/DAQ Block Diagram



L1 latency

Current L1 Latency

This margin is shared by muon upgrade, topo trig, CTP, MuCTPi upgrades



BW TGC data arrives at SL 1088ns after collision.

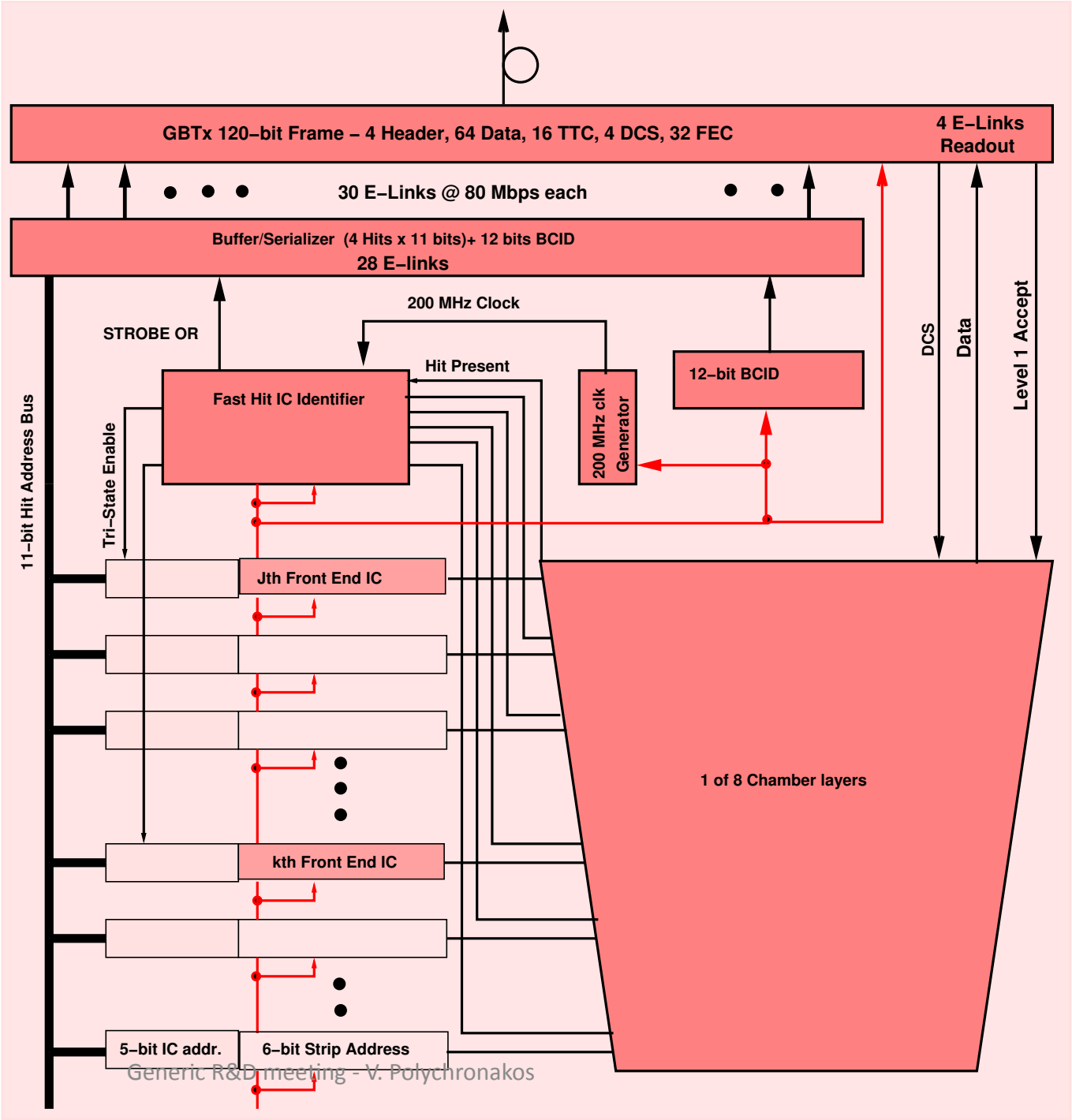
On-Detector Card

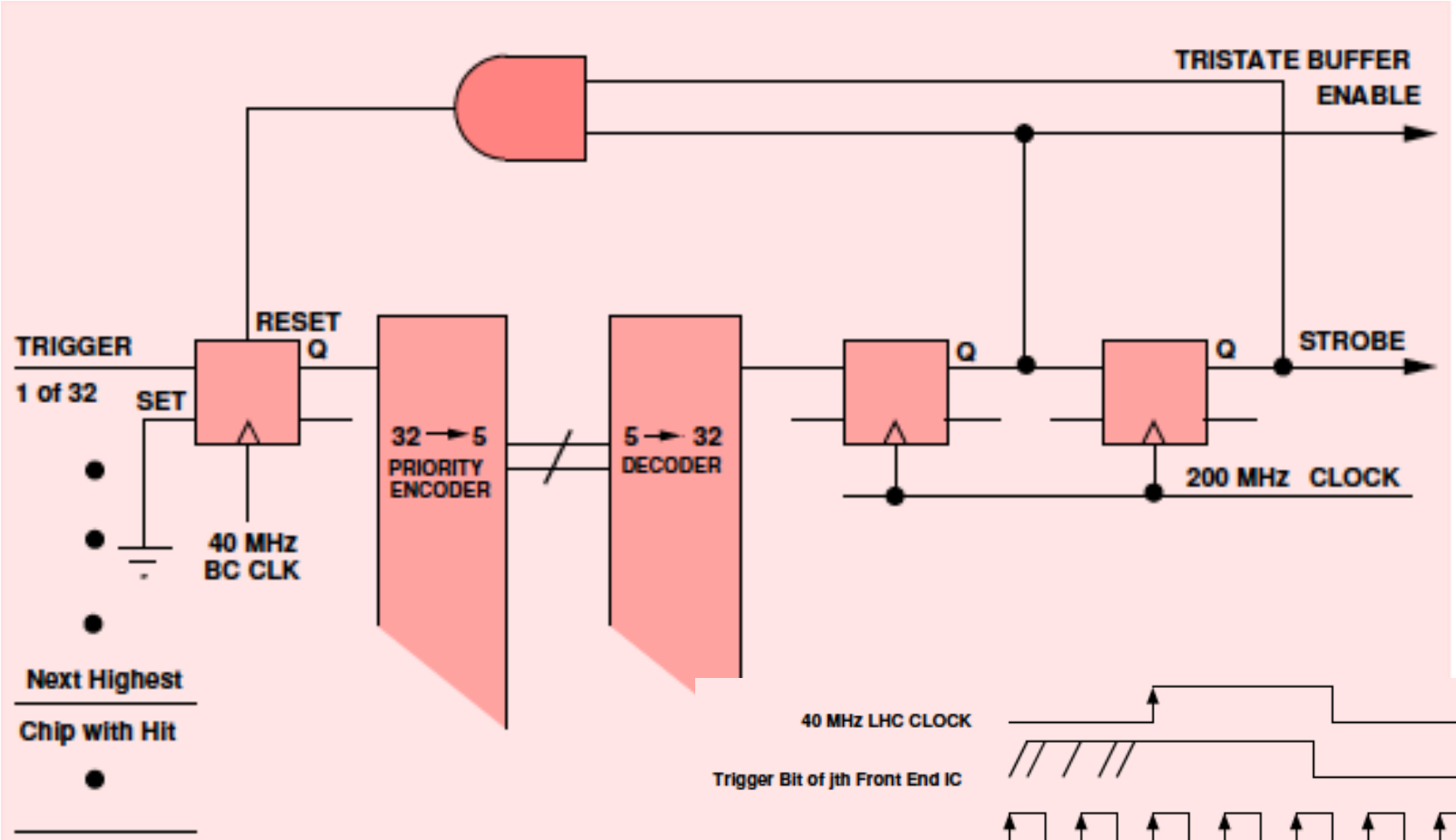
6 bit prompt strip address

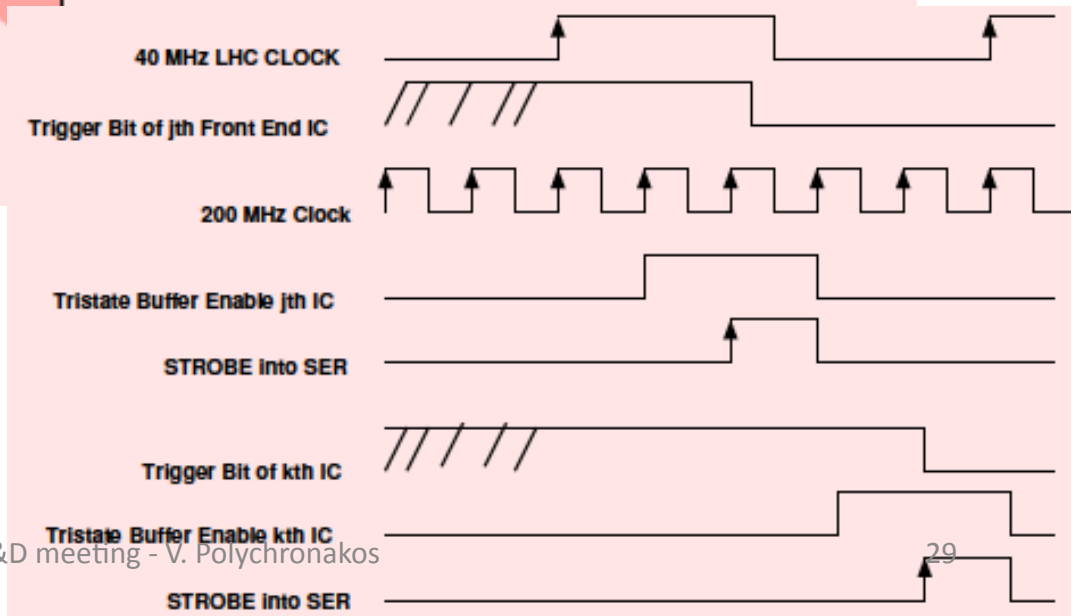
5 bit IC address per plane

Up to 4 hits per plane transferred in 2 BC

A Custom Digital IC the likely implementation







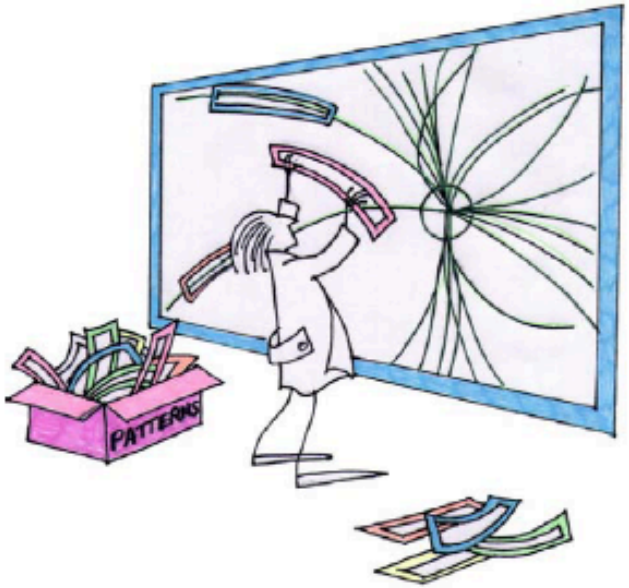
- Can transfer 2 addresses in 1 BC
- If 2 parallel paths each handling 16 chips then 4 hits can be moved in 1 BC
- Is 200 MHz clock too aggressive? (long ~0.5 m connections)
- Develop custom digital ASIC?

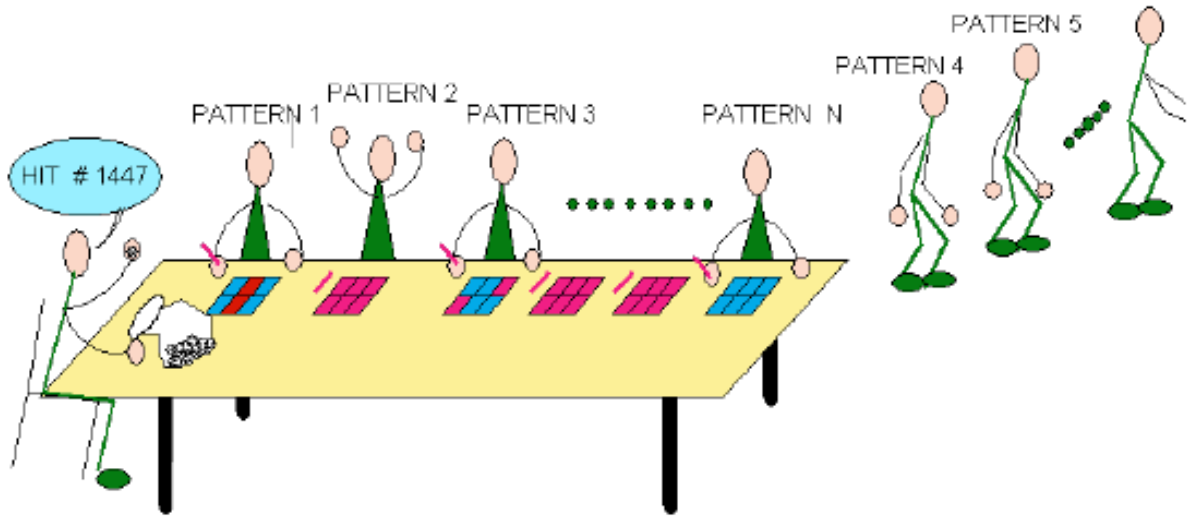
The Content Addresseable Memories

(From Mel Shochet FTK)

Two time-consuming stages in tracking

- **Pattern recognition – find track candidates with enough Si hits**

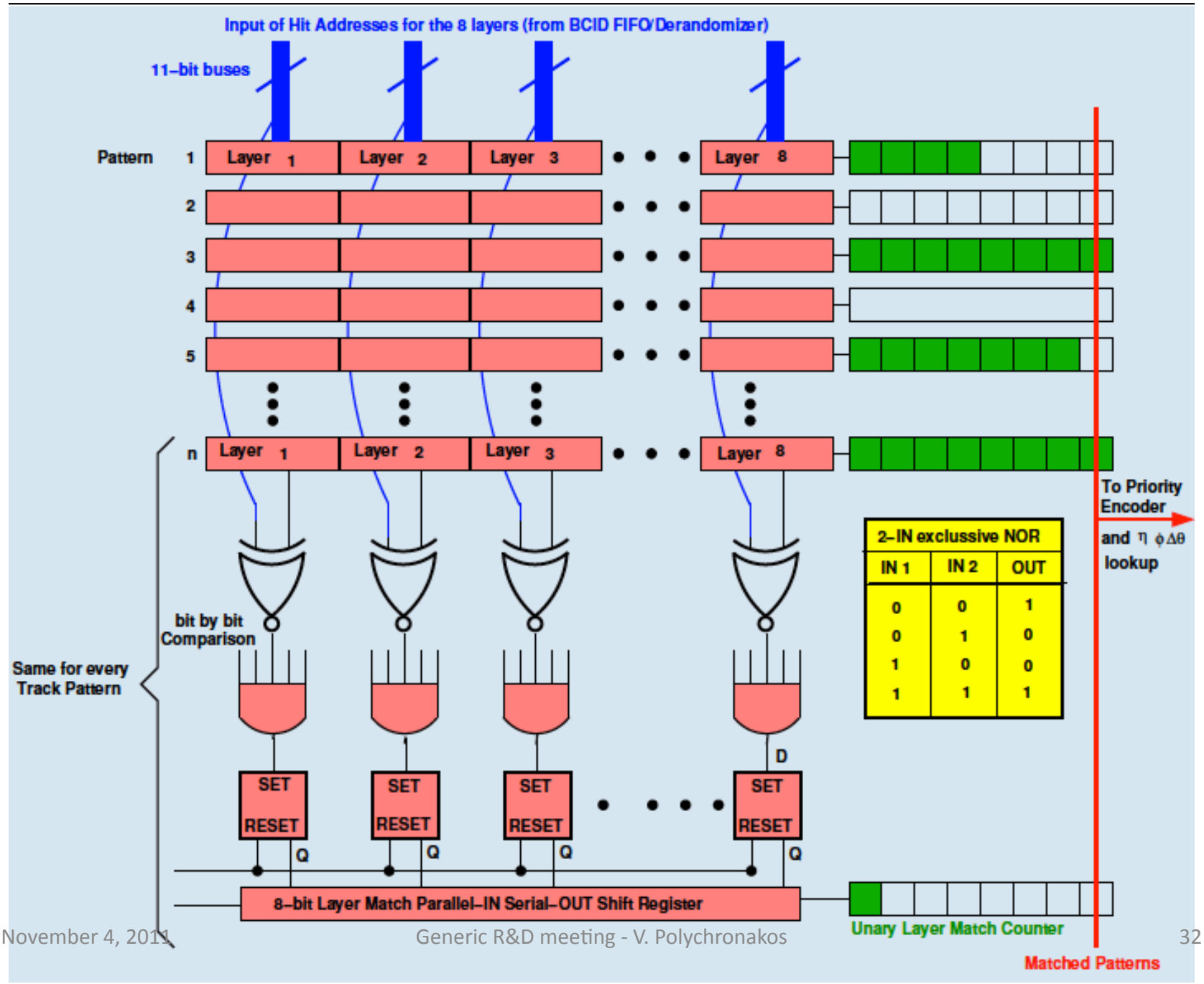




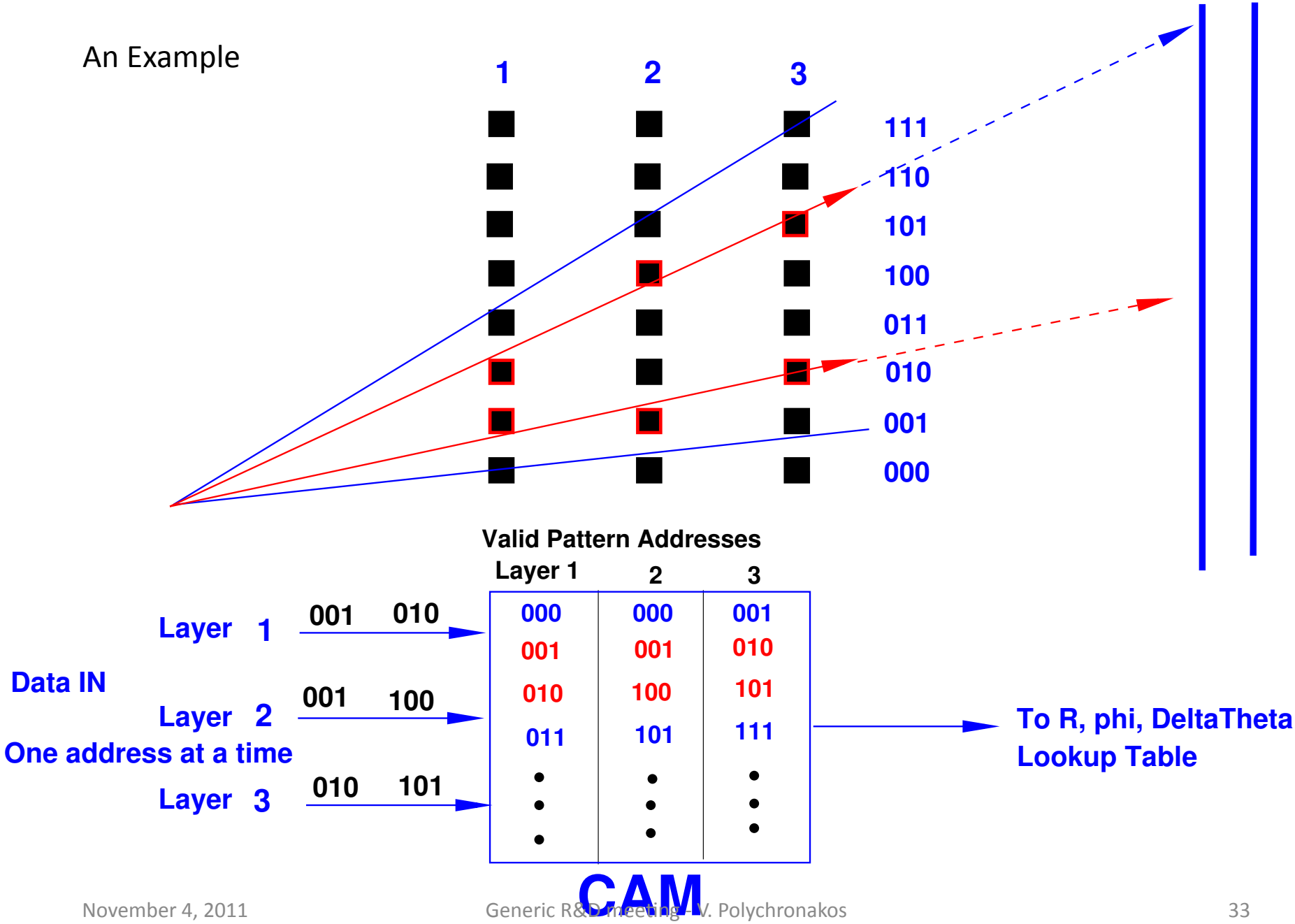
  - **10^9 prestored patterns simultaneously see each silicon hit leaving the detector at full speed.**
- **Track fitting – precise helix parameter & χ^2 determination**
  - **Equations linear in local hit coordinates give near offline resolution:**

$$p_i = \sum_{j=1}^{14} a_{ij} x_j + b_i$$

a & b are prestored constants; VERY fast in FPGA


Input of Hit Addresses for the 8 layers (from BCID FIFO/Derandomizer)
11–bit buses
Pattern
1
2
3
4
5
n
Layer 1
Layer 2
Layer 3
Layer 8
To Priority Encoder
and η φΔθ lookup
2–IN exclussive NOR
IN 1
IN 2
OUT
0 0 1
0 1 0
1 0 0
1 1 1
bit by bit Comparison
Same for every Track Pattern
D
SET
RESET
Q
8–bit Layer Match Parallel–IN Serial–OUT Shift Register
Unary Layer Match Counter
Matched Patterns

An Example


1
2
3
111
110
101
100
011
010
001
000
Valid Pattern Addresses
Layer 1
2
3
000
001
010
011
000
001
100
101
001
010
101
111
Layer 1
001
010
Layer 2
001
100
Layer 3
010
101
Data IN
One address at a time
To R, phi, DeltaTheta
Lookup Table
CAM