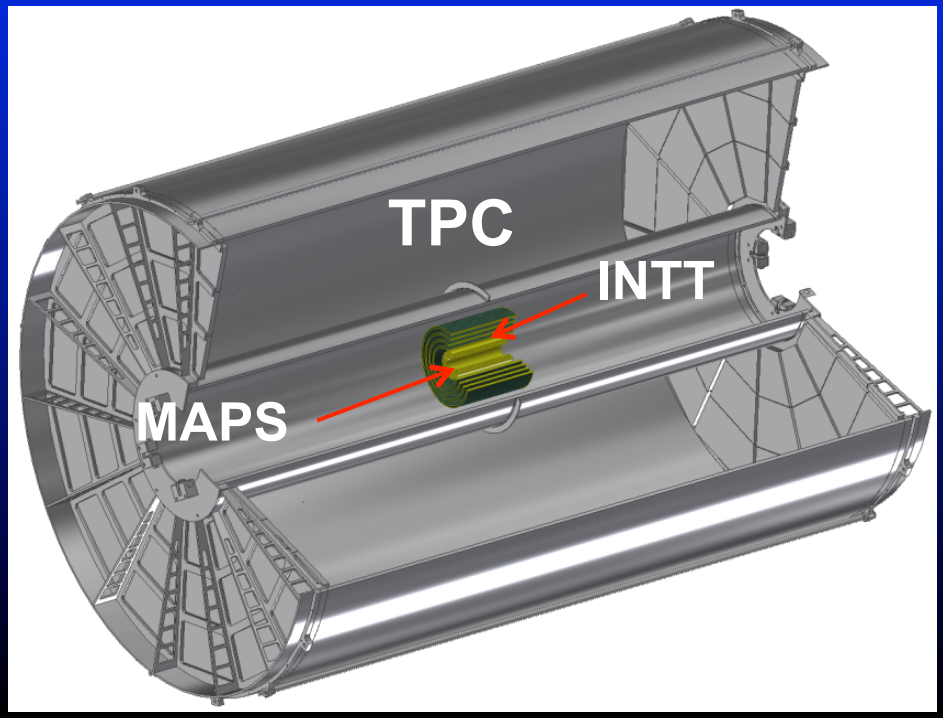
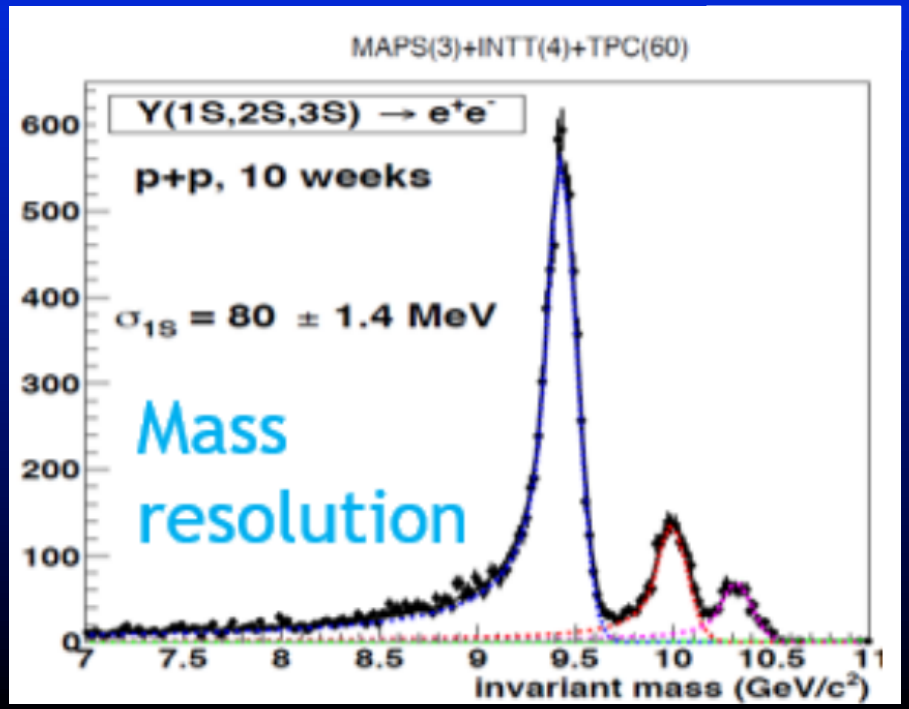
INTT Status Report

RIKEN/RBRC
Itaru Nakagawa
on behalf of
the INTT Group

Importance of Tracking

Physics Goal	Detector Requirement
Fragmentation Functions	Excellent Momentum Resolution: dp/p ~ 0.2%p to > 40 GeV/c
Jet Substructure	Excellent track pattern recognition
Distinguish Upsilon States	Mass resolution: $\sigma_M < 100$ MeV/c^2
HF jet tagging	Precise DCA resolution $\sigma_{DCA} < 100\ \mu$m
High Statistics Au+Au 200 GeV	Handle multiplicity and full RHIC luminosity

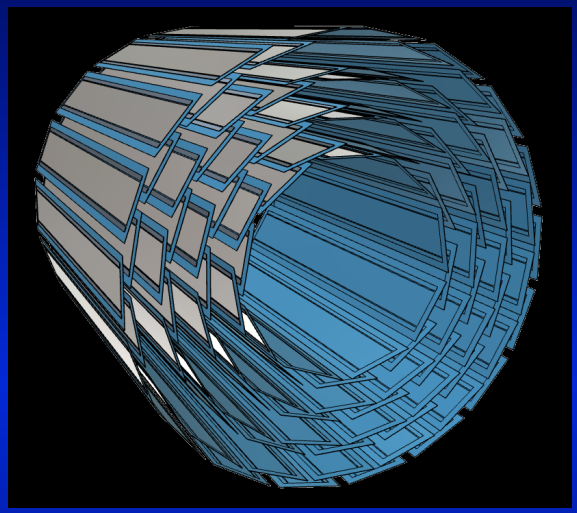




INTmediate Tracker: INTT

Design of the INTT

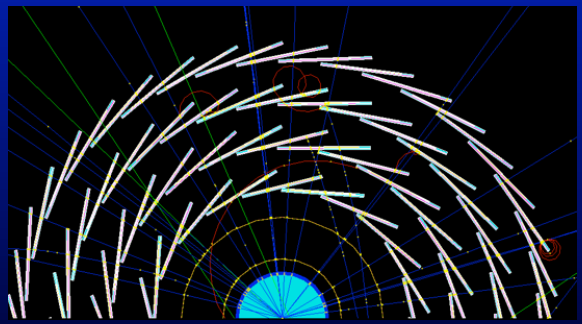
INTT



Intermediate silicon tracking (INTT) adds to the robustness of pattern recognition, momentum reconstruction, and capability of high multiplicity trigger in a challenging environment of high luminosity and high multiplicity.

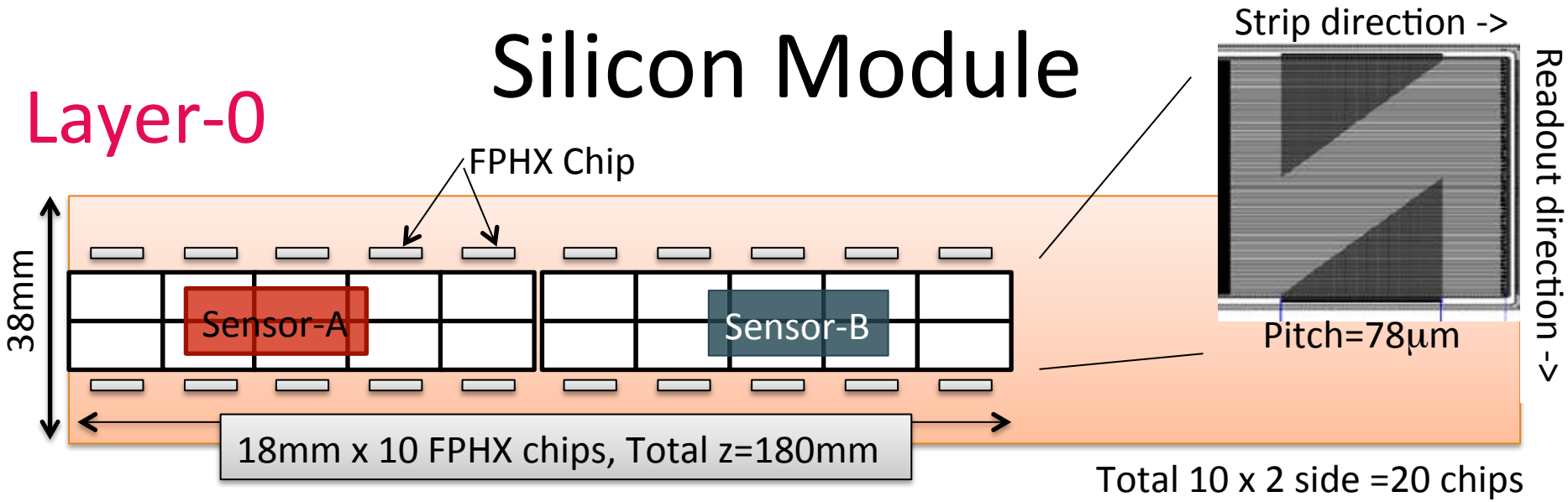
Key concepts of INTT:

i) contribute unique association between inner and outer trackers
ii) ensure both high track reconstruction efficiency and purity
iii) azimuthal 2π and $|\eta| < 1.1$ coverages at $|z_{vtx}| < 10$ cm
iv) four planes of strip detectors from Layer 0 to Layer 3
- same readout chip and electronics as used in the PHENIX forward silicon vertex detector
- cooling by air or high-thermal-conductivity-plate
- maintain low material budget

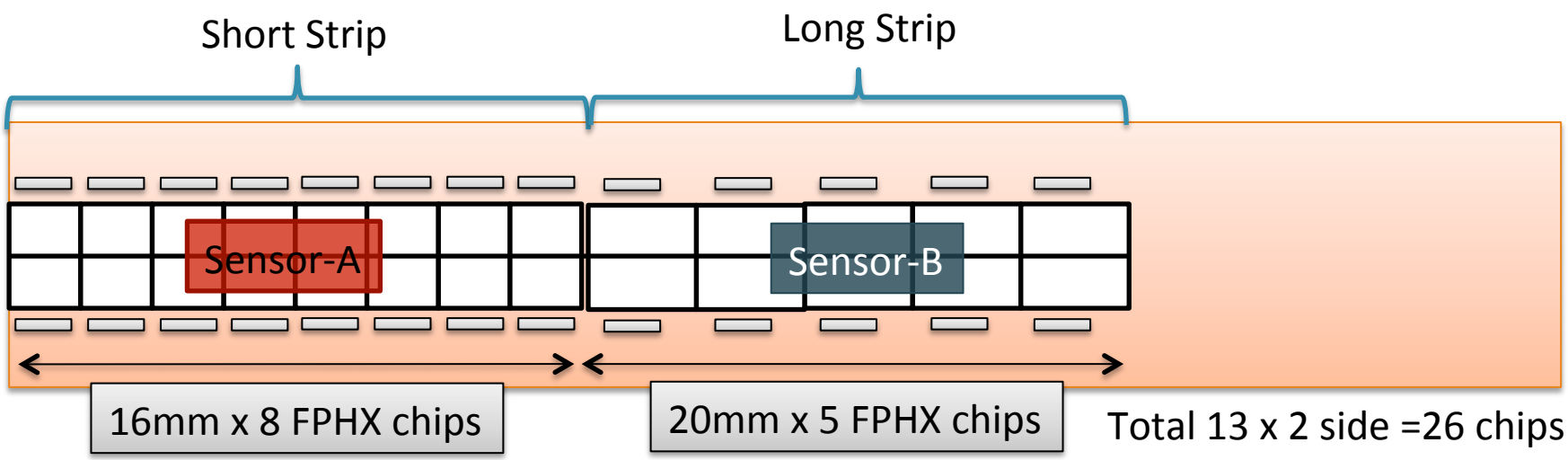


Silicon Module

Layer-0

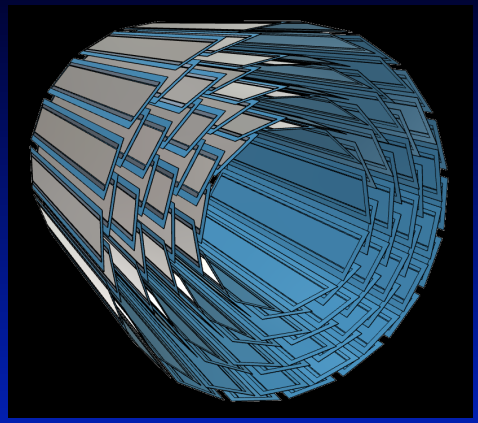


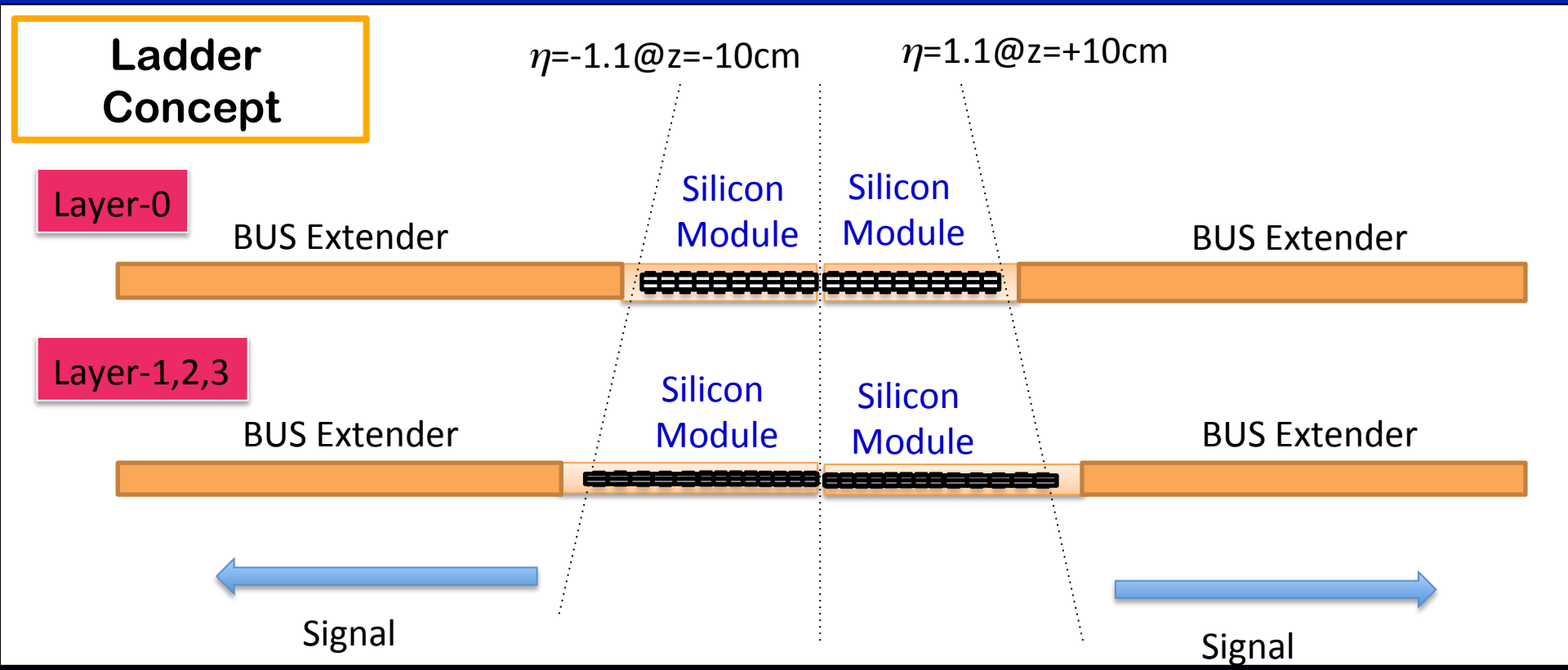
Layer-1,2,3



INTT: Ladder Concept

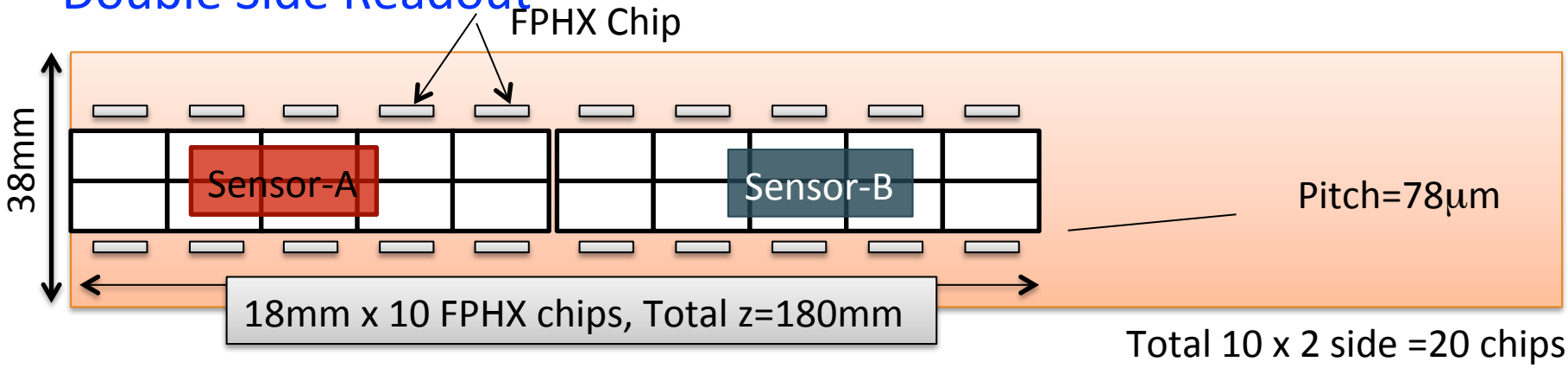
Layer	Radius (cm)	The number of ladders	Strip size (φ x z, mm)
0	6	20	0.078 x 18 (18)
1	8	26	0.086 x 12 (20)
2	10	32	0.086 x 12 (20)
3	12	38	0.086 x 12 (20)





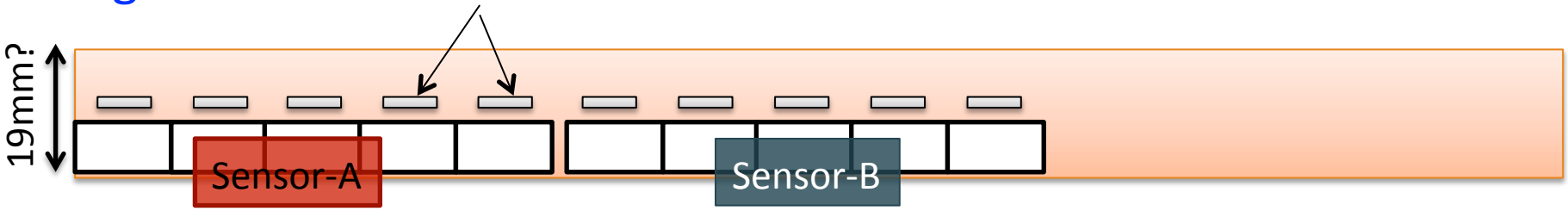
Layer-0 Optimization

- Double Side Readout

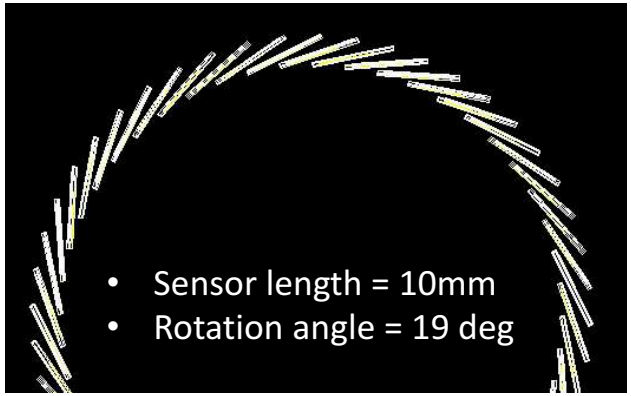


Total 10 x 2 side =20 chips

- Single Side Readout



Total 10 x 1 side =10 chips



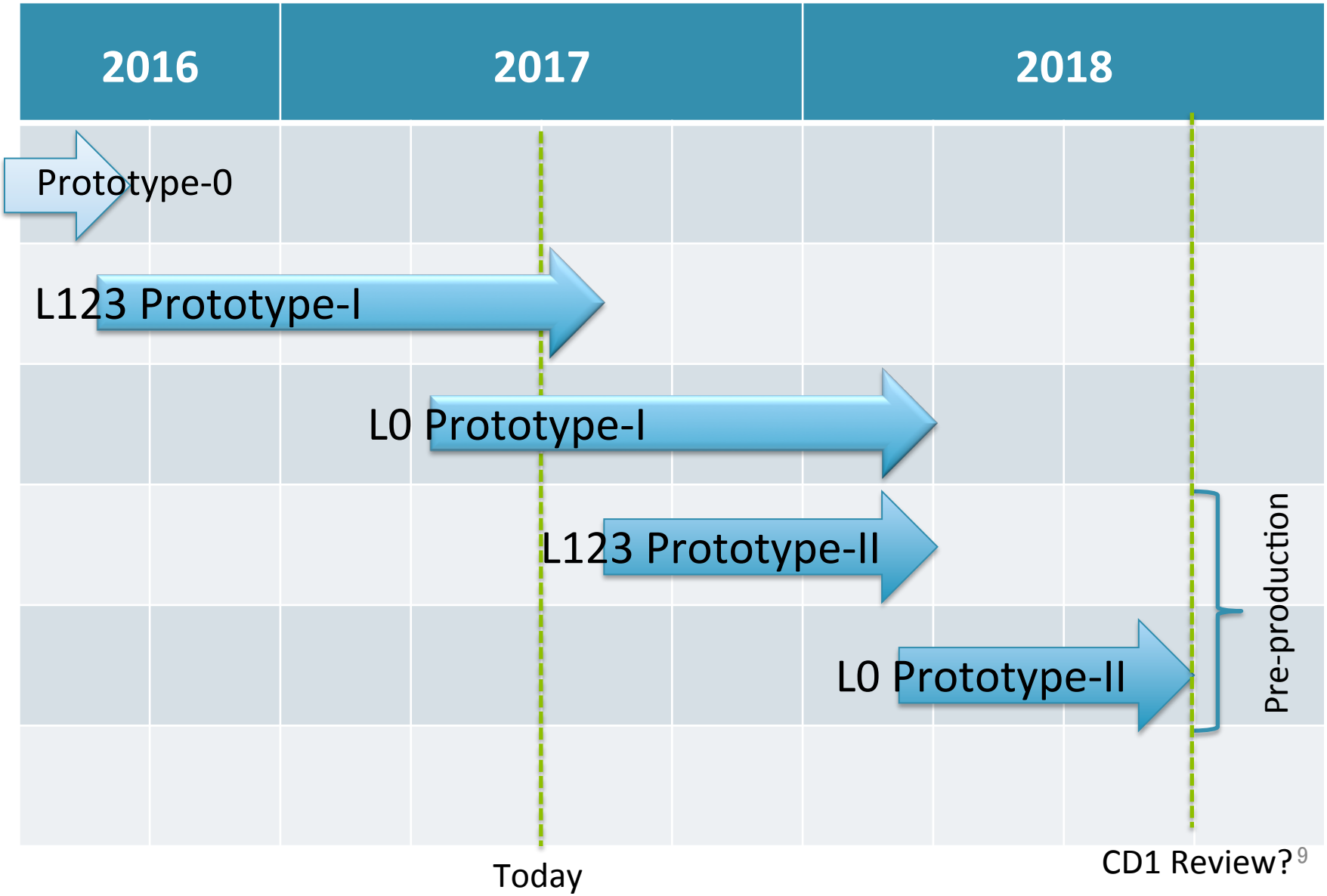
Layer-0 optimization is ongoing by Yorito Yamaguchi

Technological Challenge

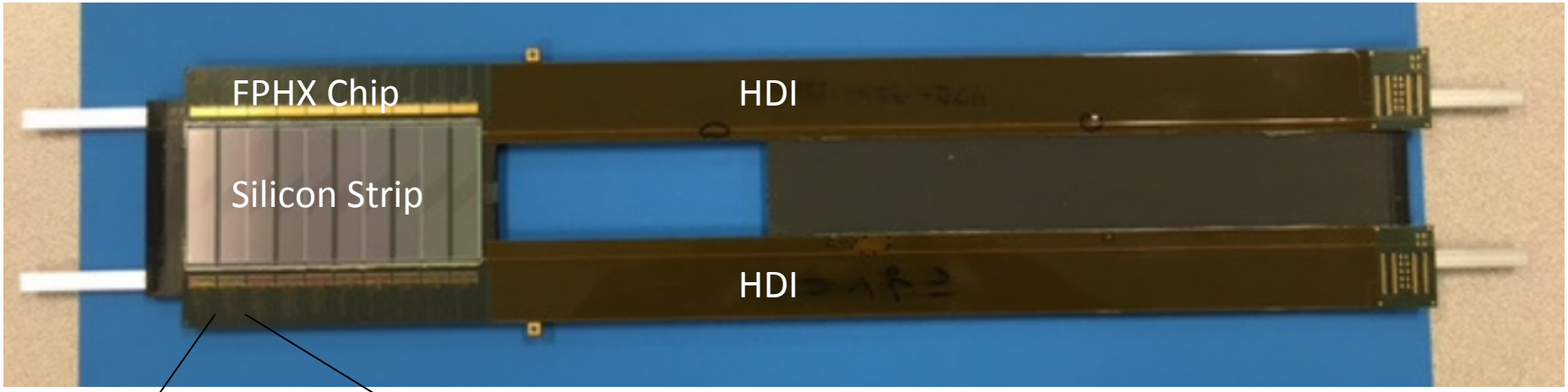
1. Thinner Silicon sensor than standard 320μm.
2. Mesh pattern ground layer rather than solid copper ground layer.
3. Long bus extender 1.2 m
4. Cooling design of longer silicon module (longer than FVTX)

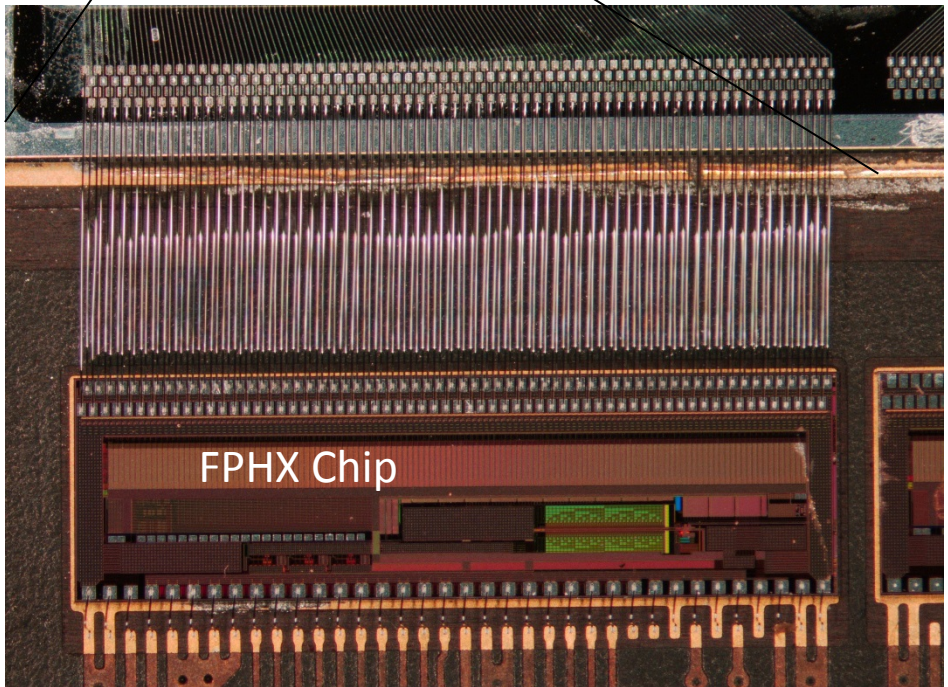
R&D STATUS AND SCHEDULE

Ladder R&D Schedule



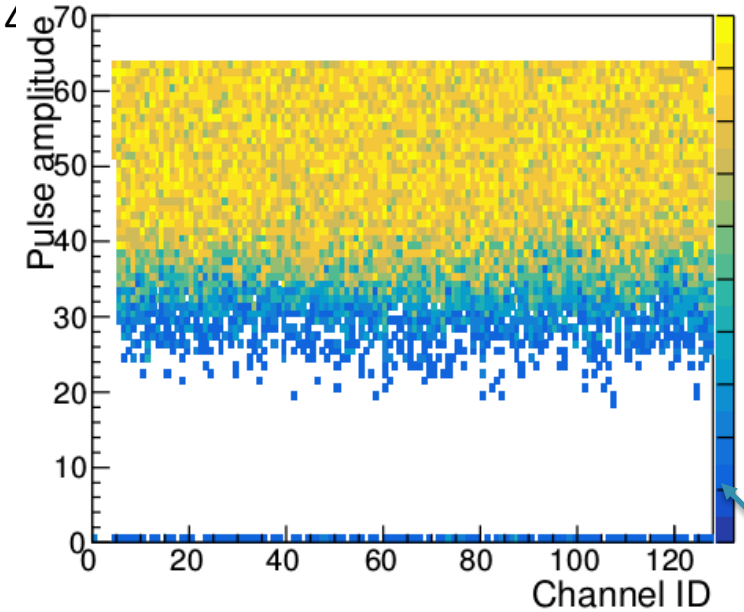
Ladder Prototype−0 Assembly



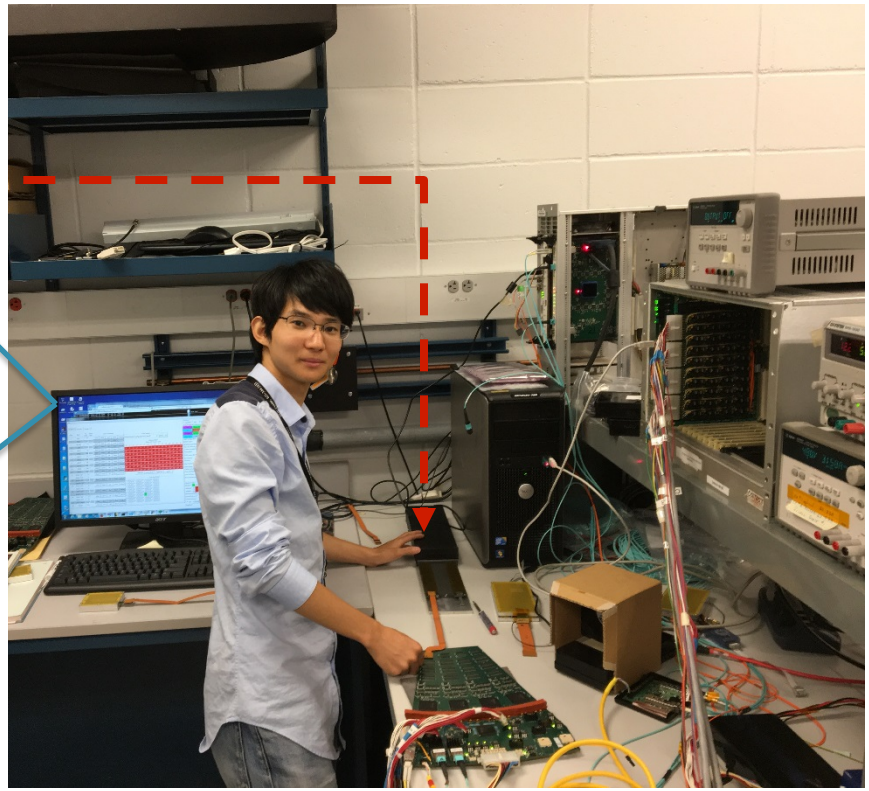


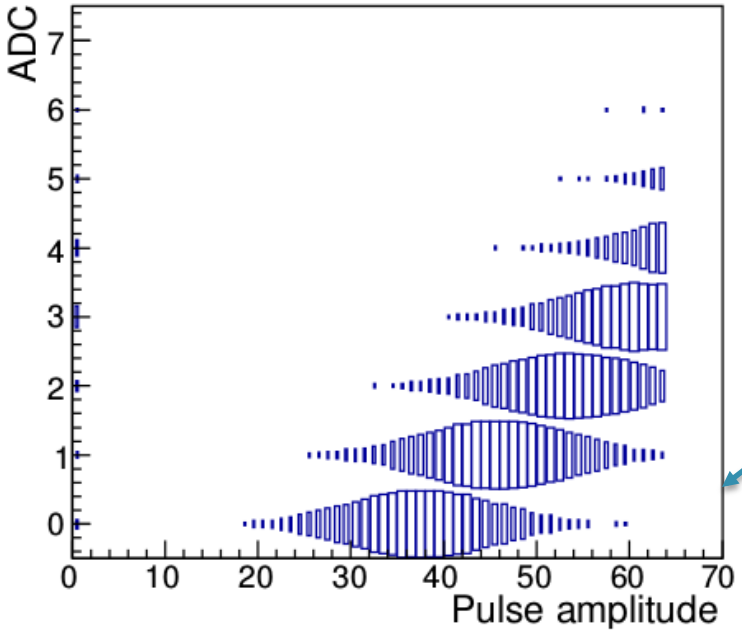
Wire-bondig of the FPHX chip was done at Inst. Div. BNL

Ladder Prototype-0 Test

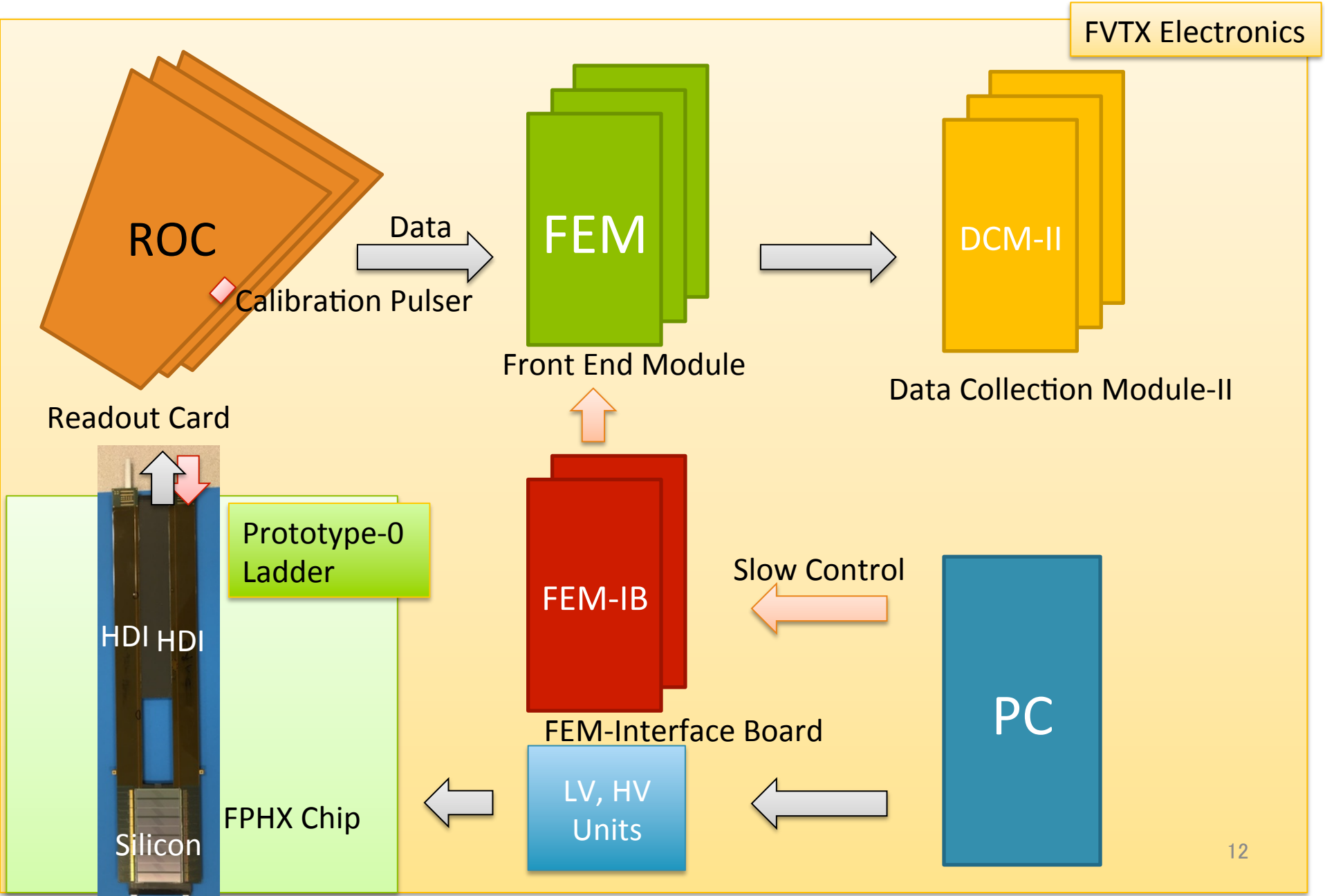


Testing bench at BNL
Student: Masuda Hidekazu





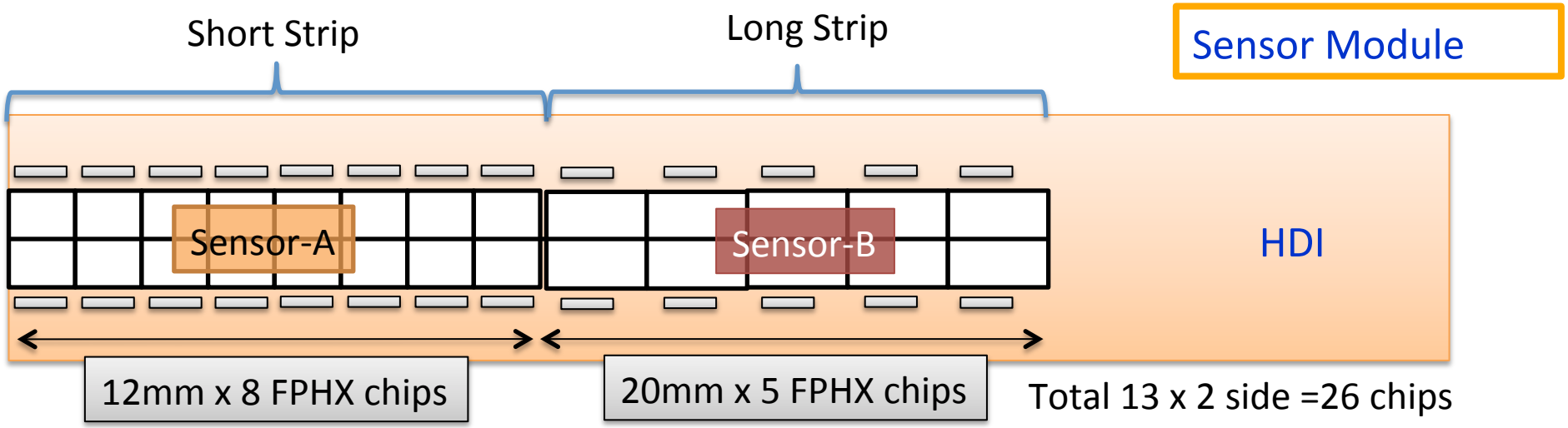
INTT Readout Chain



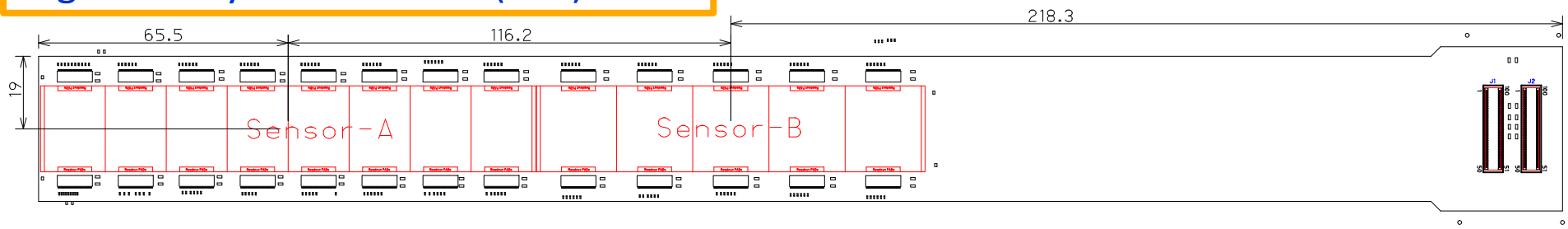
Achievement by Prototype-0

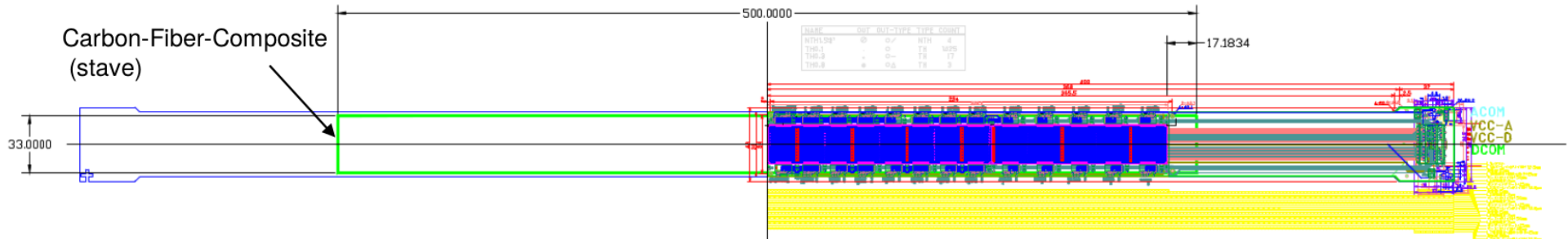
- Achieved Communication Line up to FPHX Chip.
- Signal from the silicon sensor has not been observed yet.

INTT: Sensor Module Concept and HDI



High Density Interconnect (HDI)





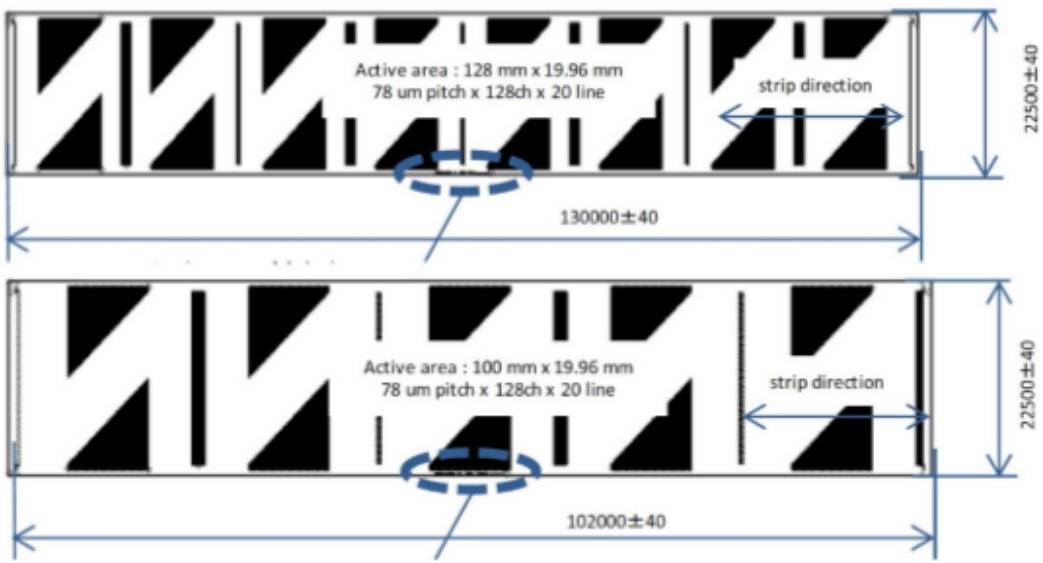
LAYER123 PROTOTYPE-1

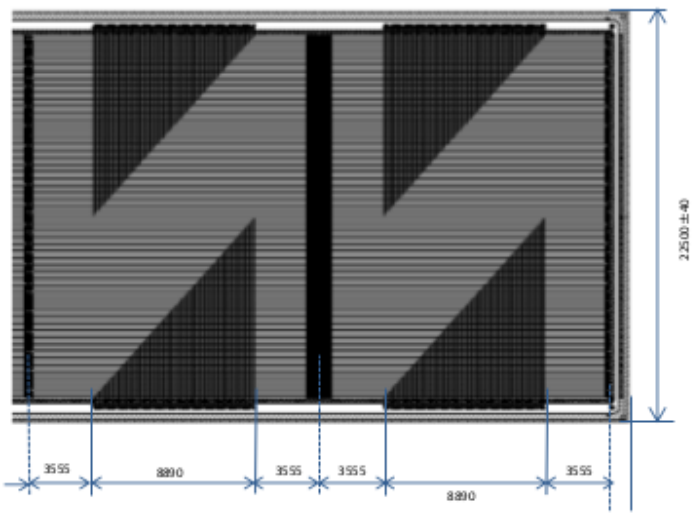
Layer 1,2,3 Silicon Sensors

Delivered end of March, 2017. No ganging. 320 and 200 μm thick.

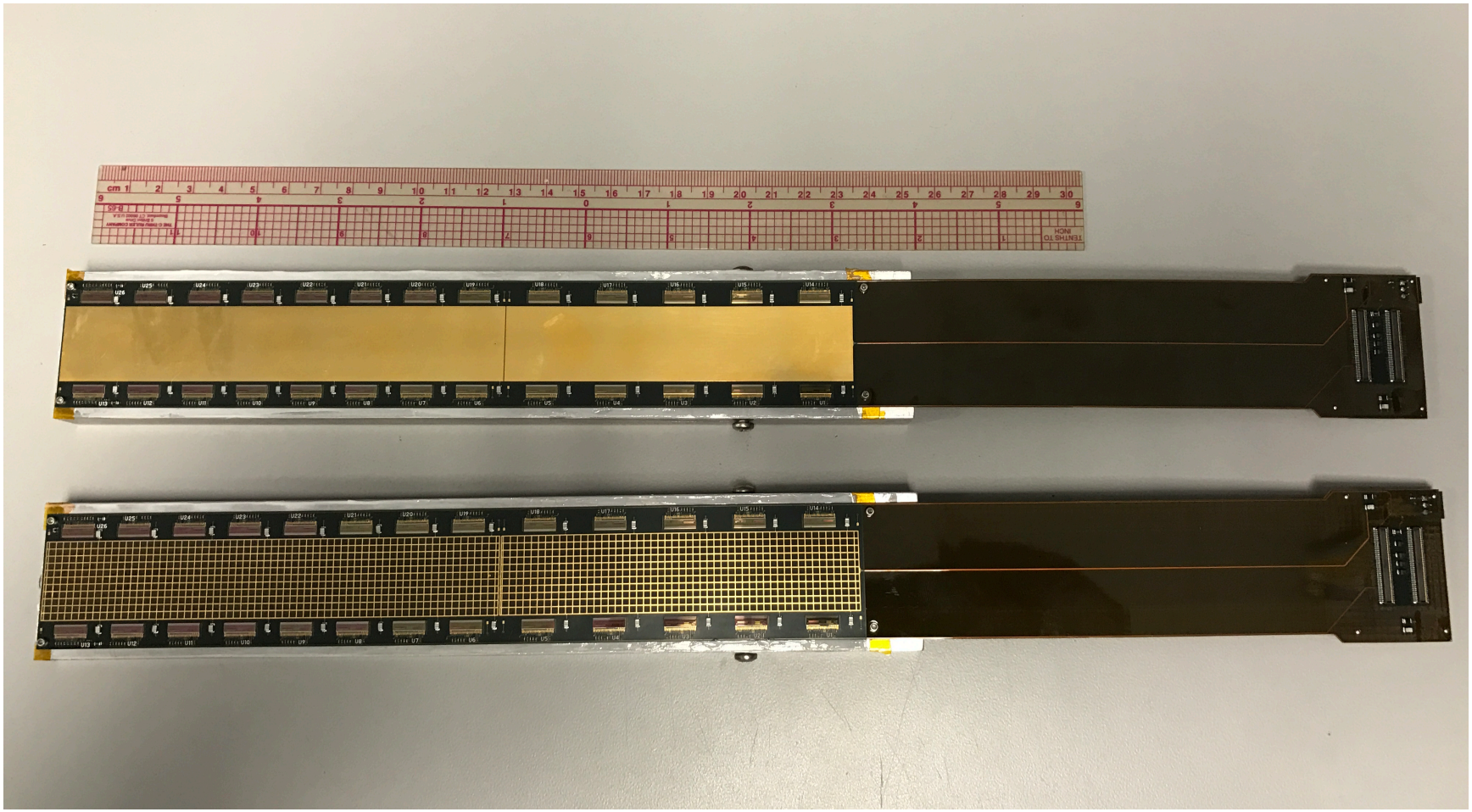
INTT: Silicon Sensor

Type	number of blocks	active area dimension	strip pitch
A	8	128 mm × 19.96 mm	78 μm
B	5	100 mm × 19.96 mm	78 μm

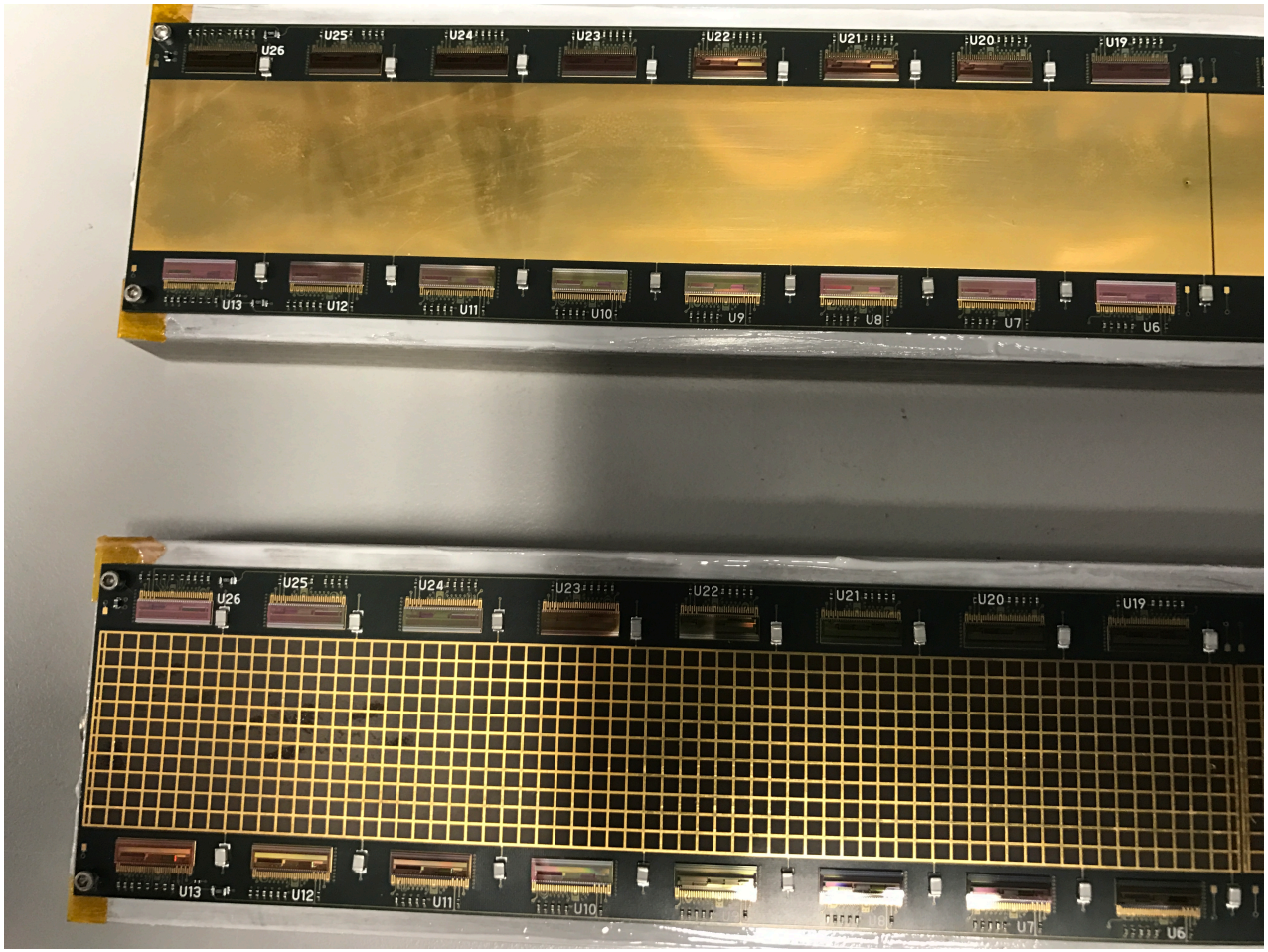




Layer 1,2,3 HDI

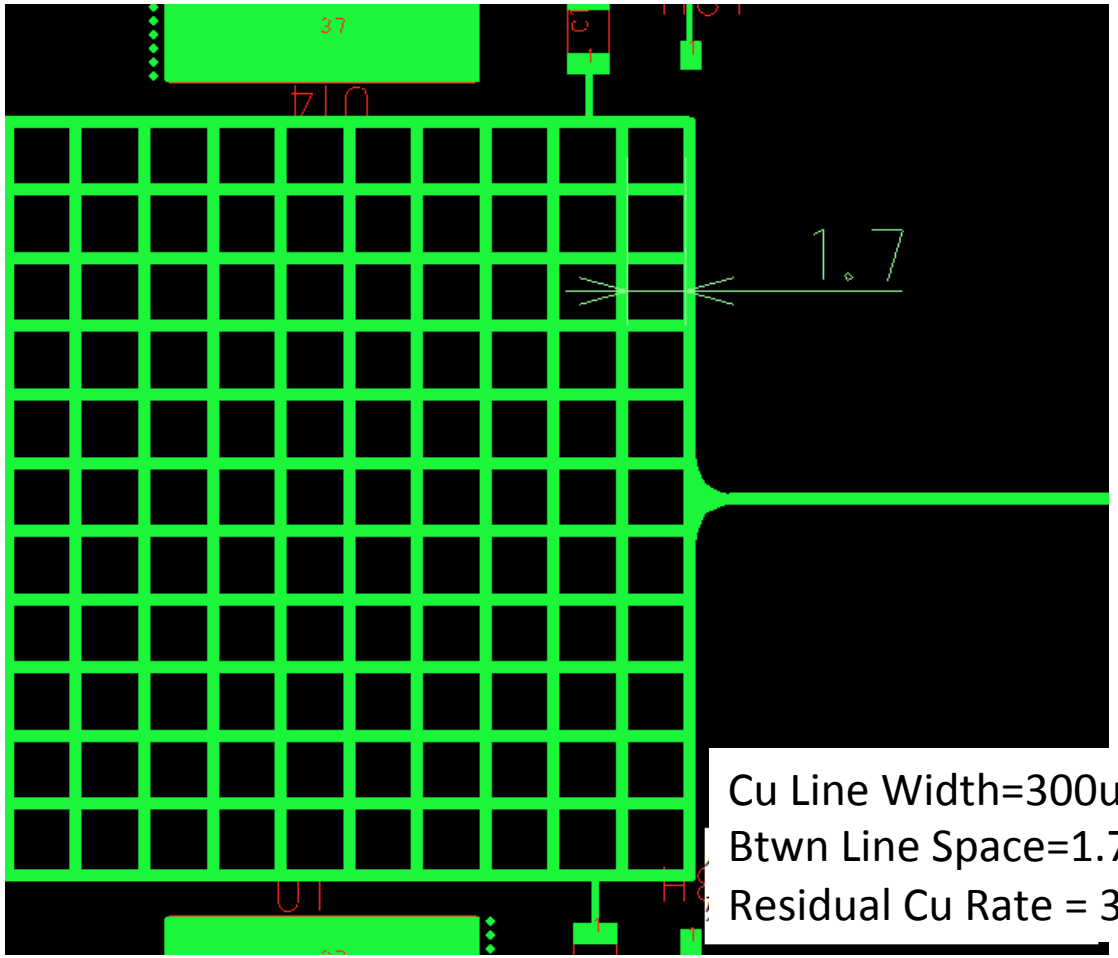


Delivered beginning of June.



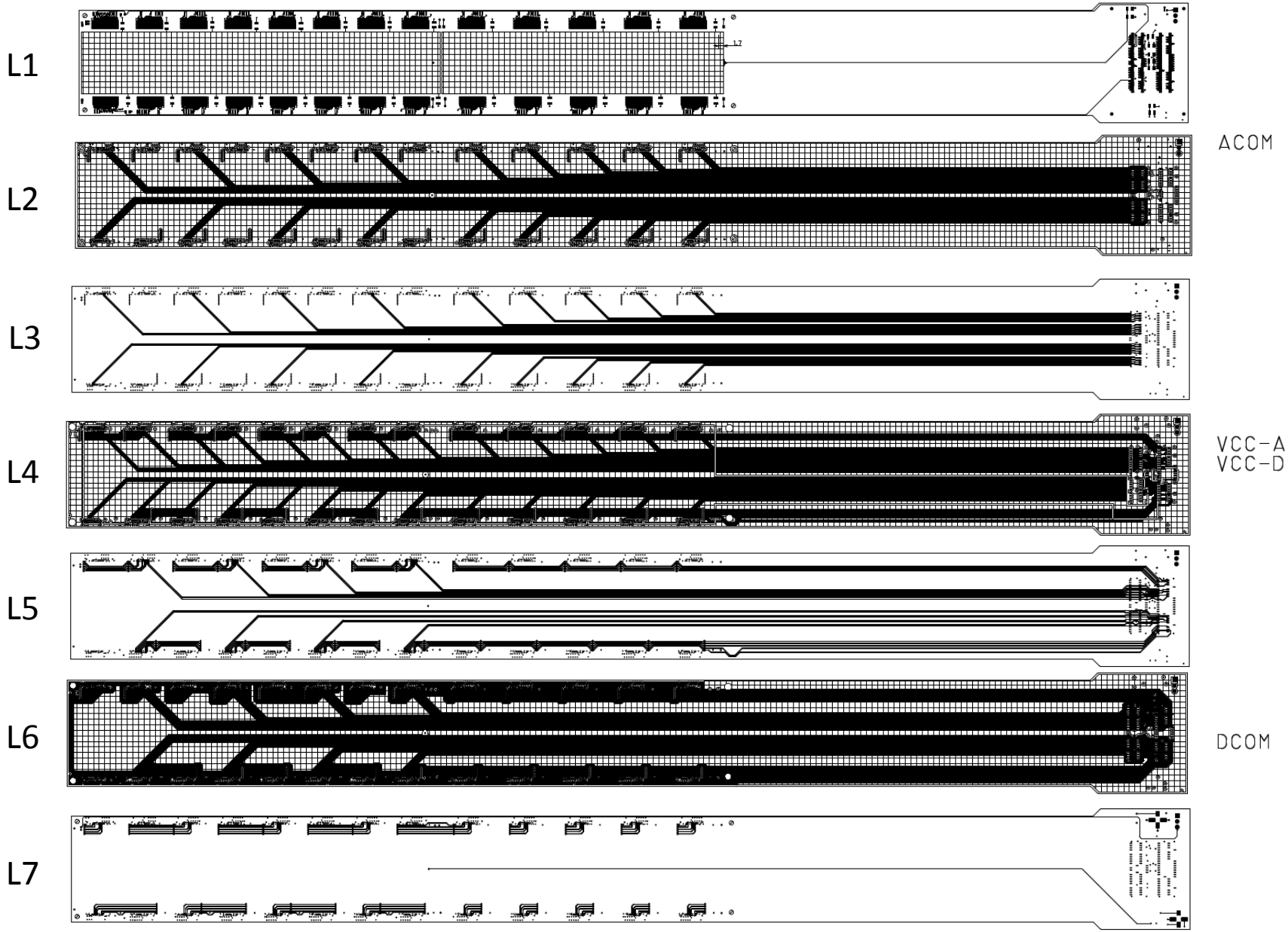
FPHX Chips a mounted June 12th. To be tested this week.

2. Mesh Ground Design



Cu Line Width=300um
Btwn Line Space=1.7mm
Residual Cu Rate = 30%

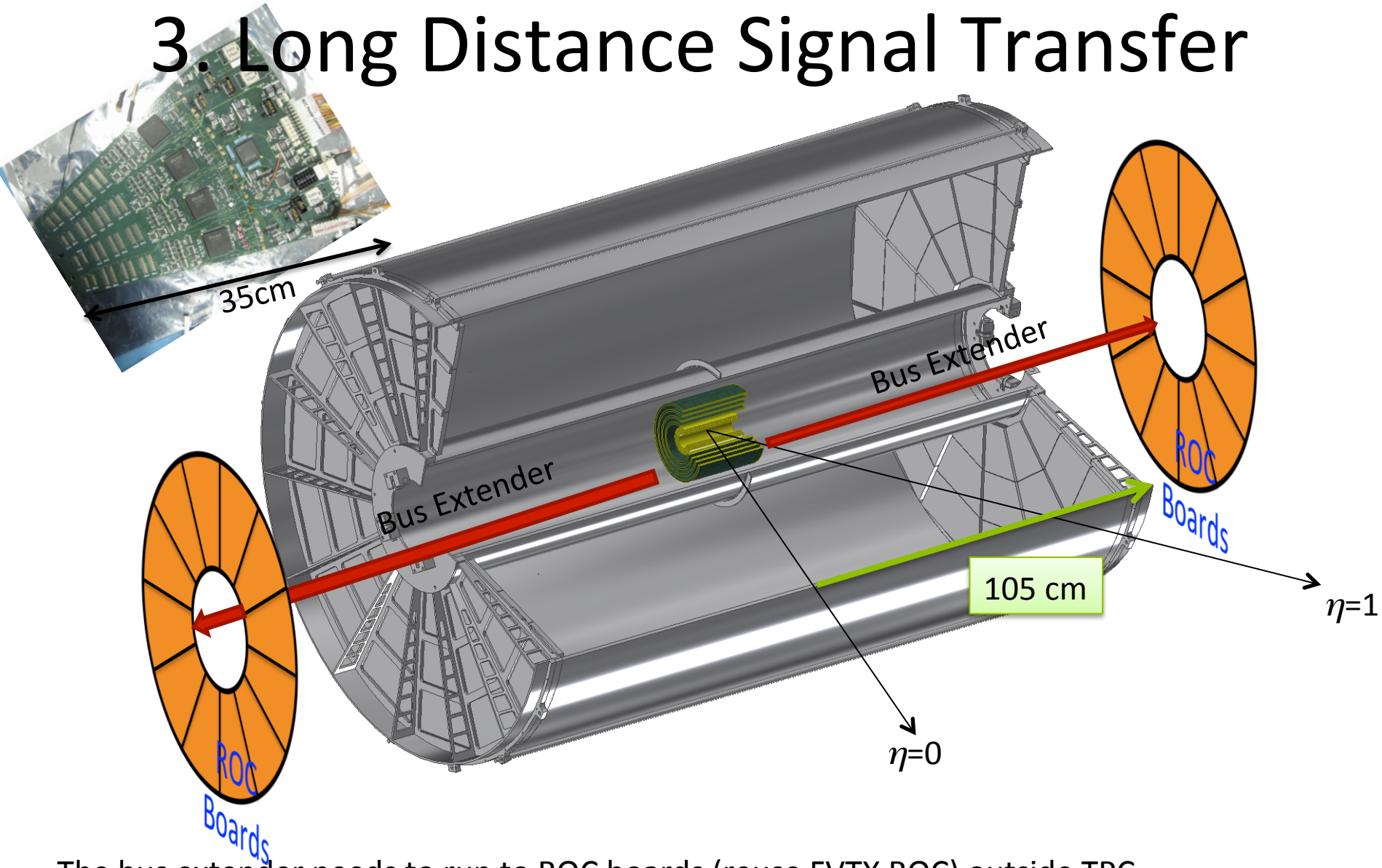
Residual Cu	10%	30%
HDI Radiation Length	0.76%	0.86%



INTT HDI Layers

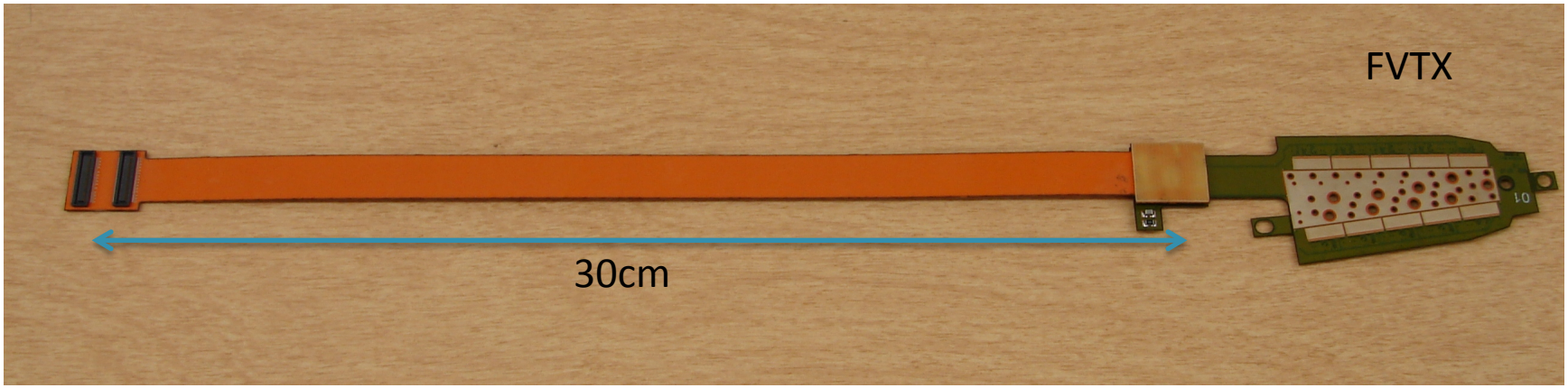
BUS EXTENDER

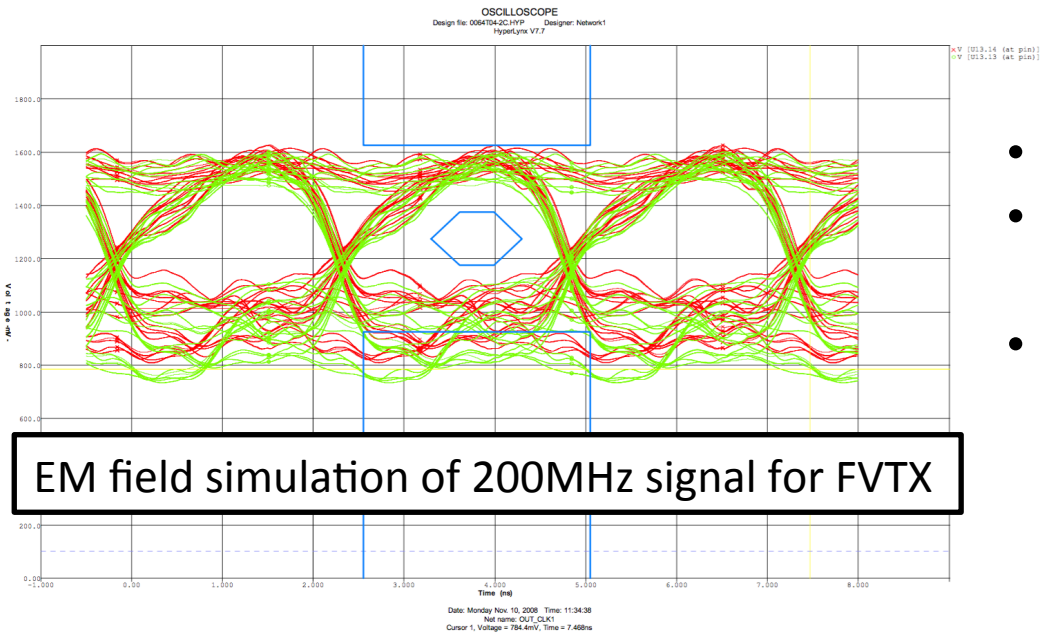
3. Long Distance Signal Transfer



The bus extender needs to run to ROC boards (reuse FVTX ROC) outside TPC.
The bus extender will be 1.2 meter long which is challenging.

Bus Extender

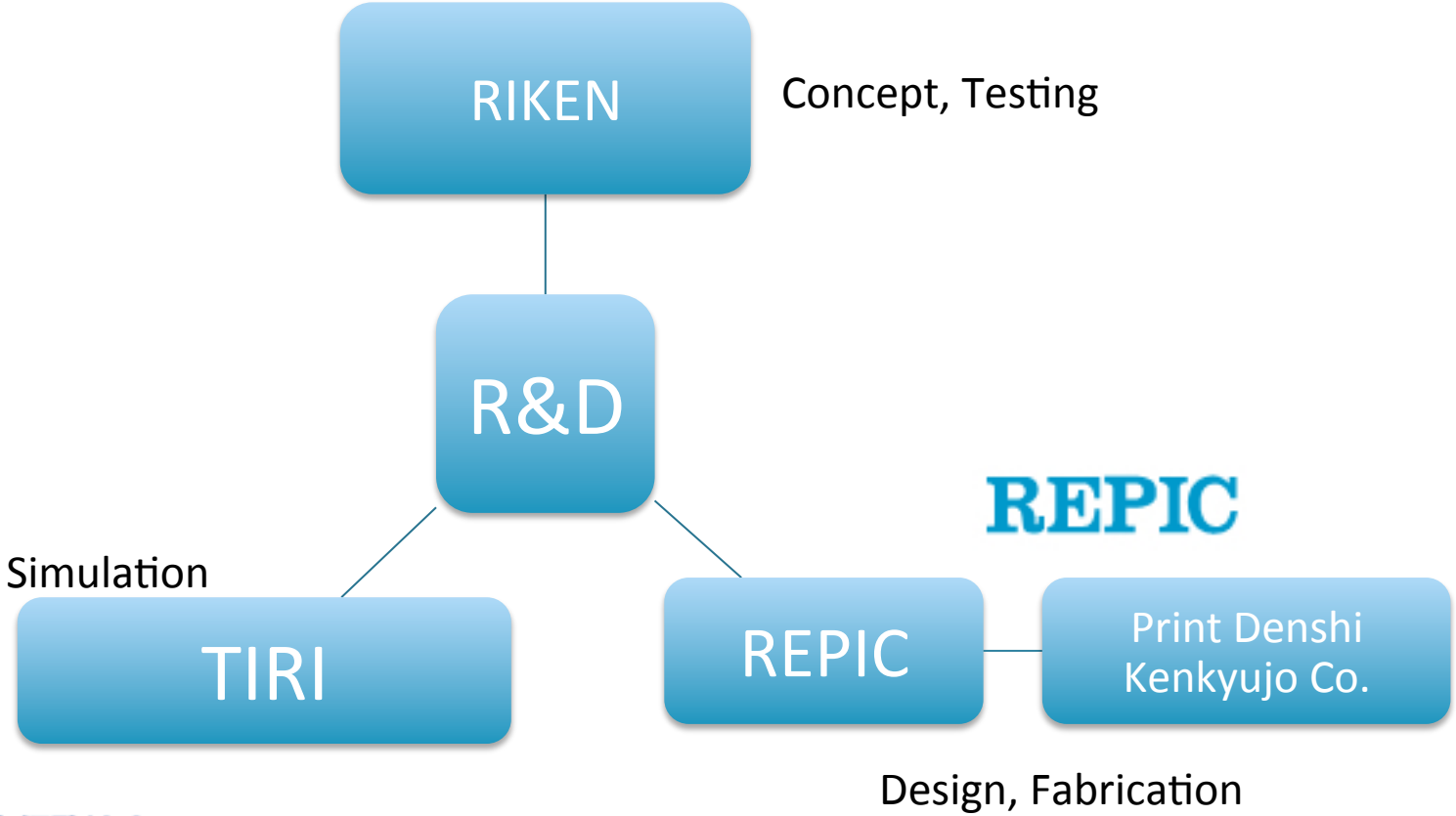




EM field simulation of 200MHz signal for FVTX

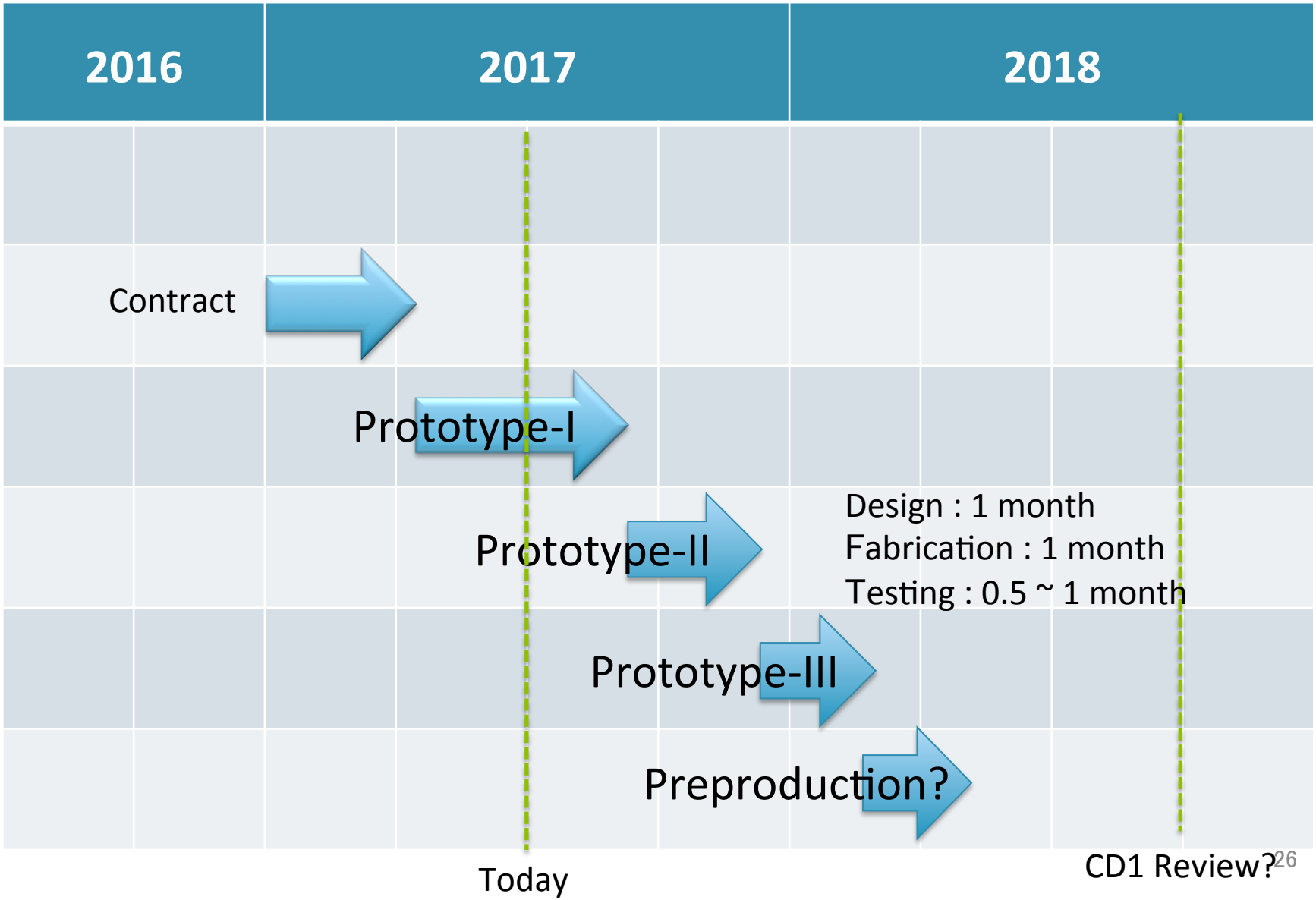
- Multilayer flexible cable.
- There is no 1.2 meter multilayer flexible cable in the market.
- R&D has just started in Japan.

Bus Extender R&D

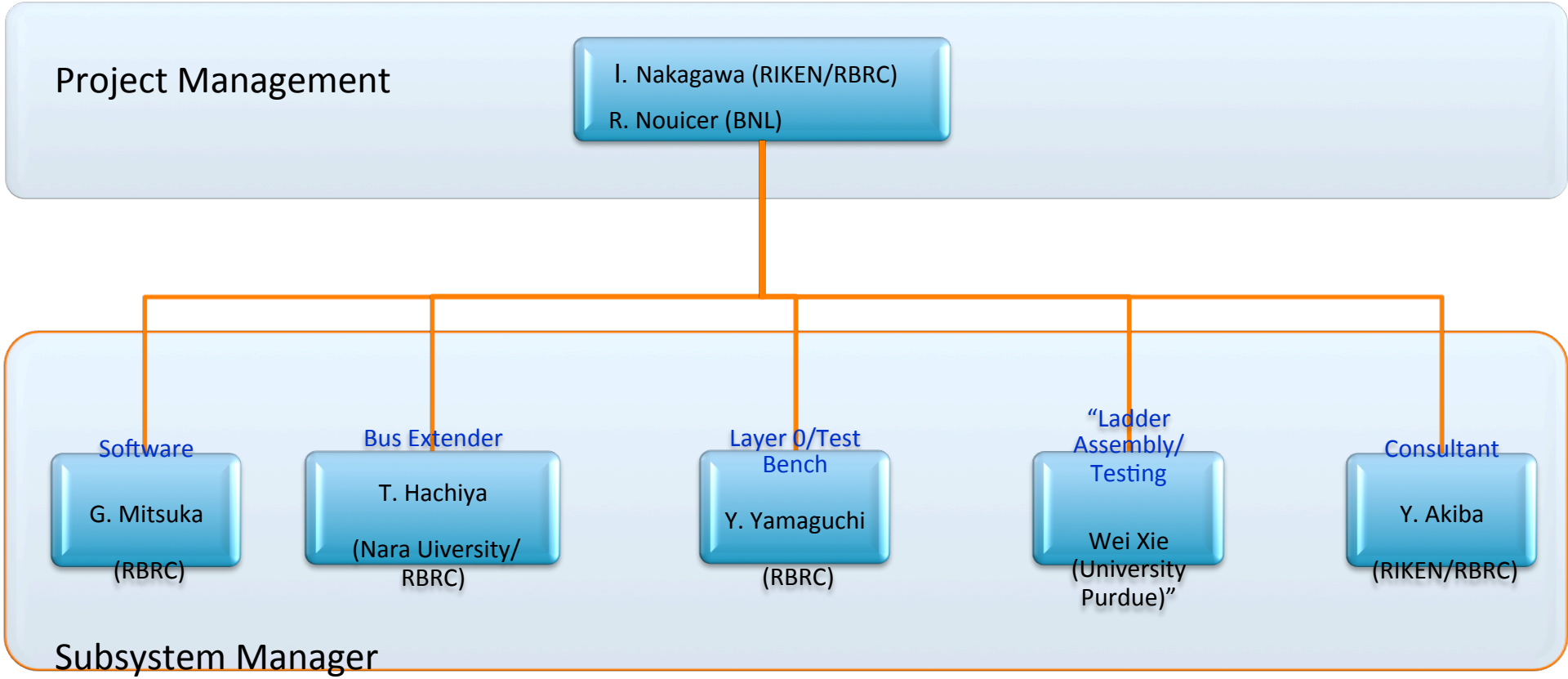


地方独立行政法人
東京都立産業技術研究センター
TOKYO METROPOLITAN INDUSTRIAL TECHNOLOGY RESEARCH INSTITUTE

Bus Extender R&D Schedule

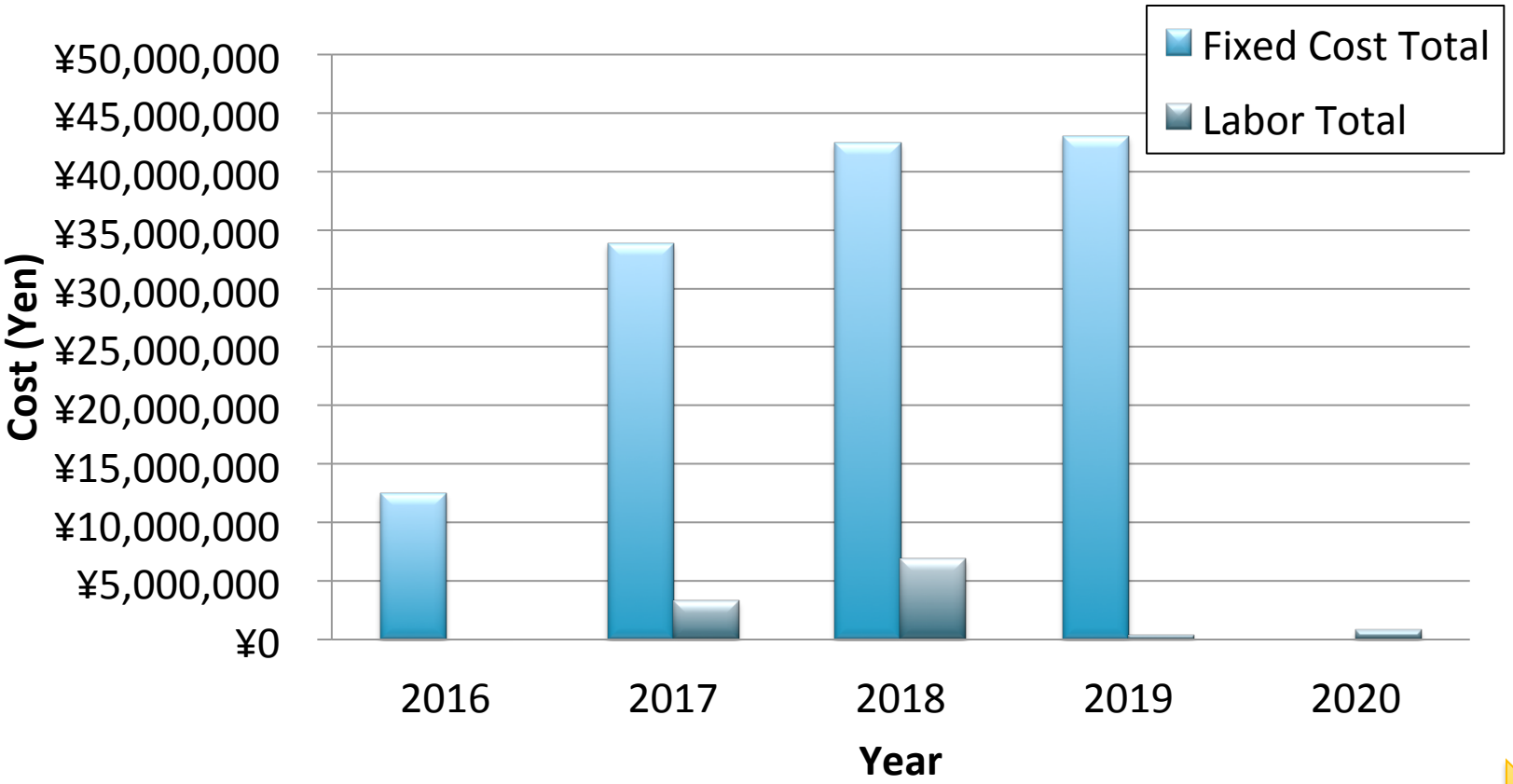


Summary: Organization Chart

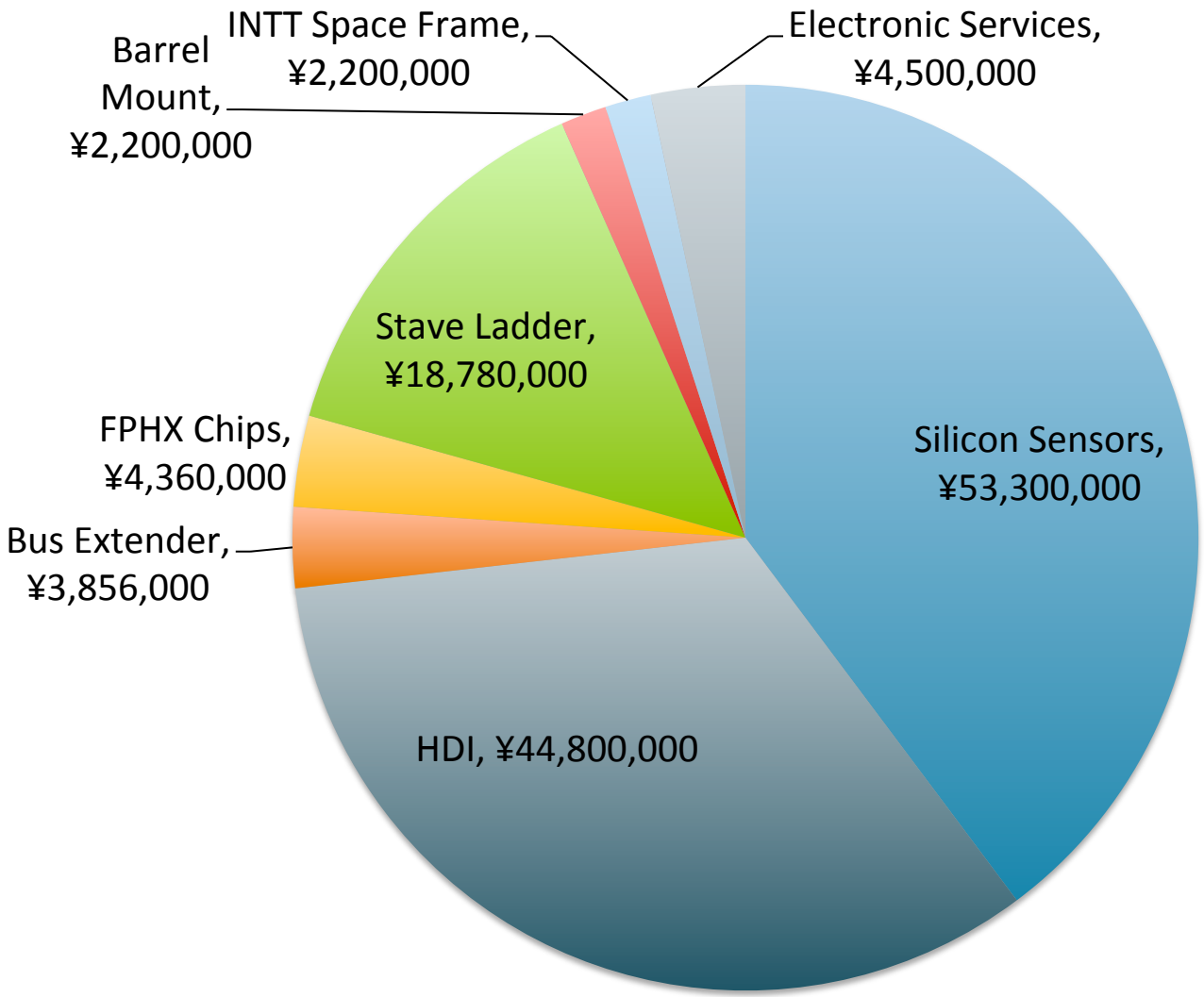


BACKUP

Cost Profile



CD0 CD1/CD-3a? CD2/CD-3b

R&D Fabrication Install

Fixed Cost Breakdowns