WBS: 6.8.y.2
Level-0 MDT Trigger

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U.S. ATLAS HL-LHC NSF Conceptual Design Review
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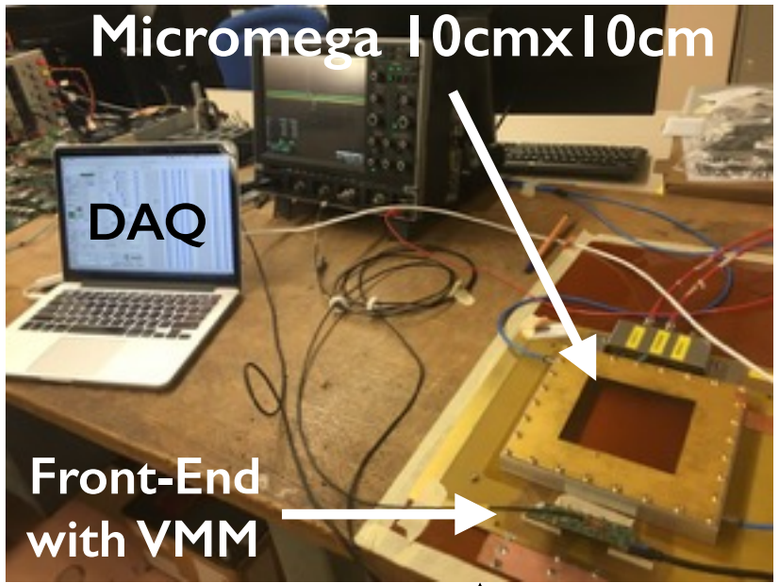
About the Expert

- ✓ Expert: Anyes Taffard, Associate Professor of Physics
- ✓ Institute: University of California Irvine
  - ATLAS member since 2007
  - Previously, CDF member (Tevatron)
- ✓ Experiences:
  - CDF:
    - ❖ Level-1 track trigger extrapolator
    - ❖ CDF Top Properties Convener
  - ATLAS Phase-I New Small Wheel muon upgrade
    - ❖ NSW TDR: Feasibility simulation studies for sTGC muon trigger
    - ❖ sTGC muon trigger simulation with ATLAS full simulation
    - ❖ NSW Readout and trigger electronics
    - ❖ Supervision of 1 postdoc and 1 graduate student contributing to NSW
  - ATLAS Data Quality convener [Jan-2015-Sept 2016]
  - US-ATLAS Muon R&D L2 R&D manager for HL-LHC [March 2015-present]



About the Institution

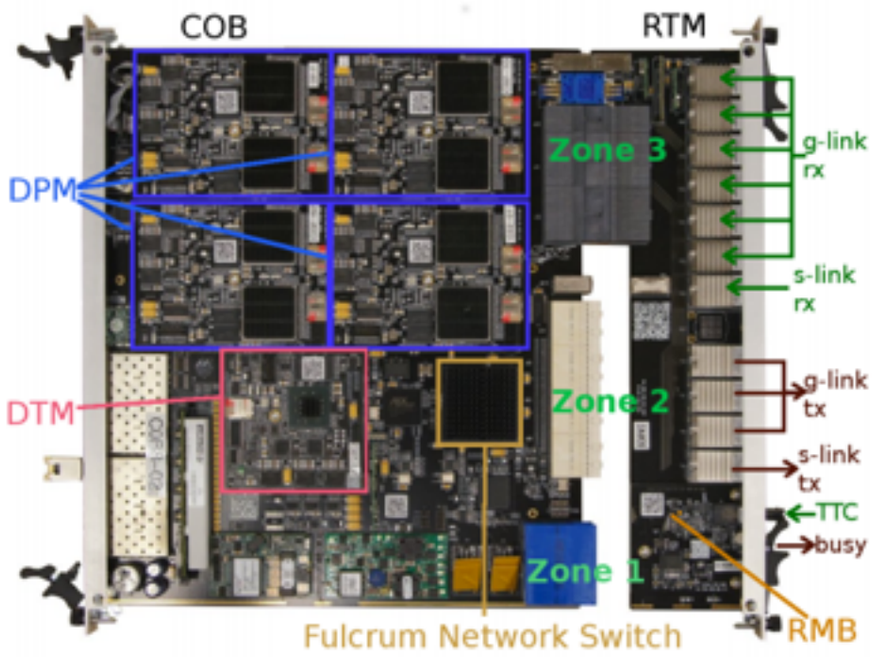
✓ Group involved in ATLAS since 1996

✓ Muon Cathode Strip Chambers: CSC (Muon Small wheel)

- CSC Readout system (ROD) and upgraded design installed in 2014 during Long-Shutdown-1
- CSC chambers installation and commissioning
- CSC maintenance, operation, performances and data quality monitoring (online & offline)

✓ Typical personnel available (off project):

- One Project Scientist
  - ❖ New hire underway
- One Software Engineer
- Two postdocs
- Two grad students
- Some undergraduate students



CSC Run-2 ROD

Outline

- ✓ Challenges & Motivations
- ✓ The solution: Level-0 MDT muon trigger
  - Overview
  - Functionalities
  - Conceptual design
- ✓ R&D needed
- ✓ Summary

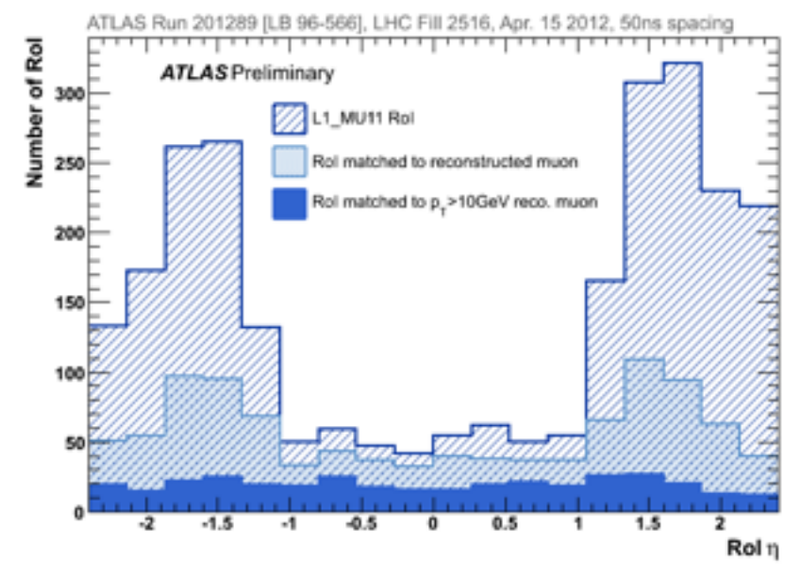
Current Muon Trigger System

- ✓ Muon trigger provided by RPC (barrel) and TGC (endcap)
- ✓ Phase-I New Small wheel endcap 1.3<|η|<2.7
  - Will provide 2-3 reduction in single-μ trigger rate

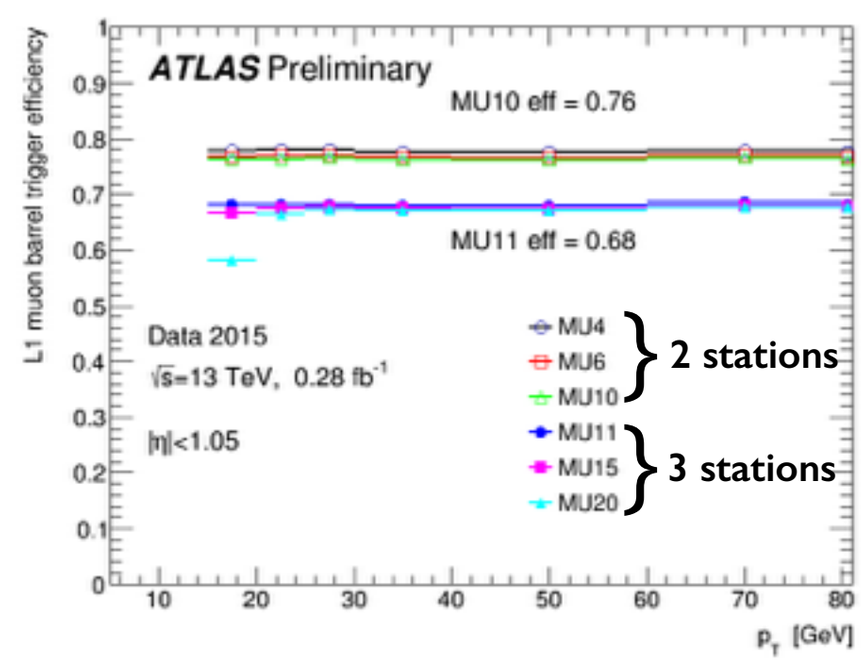
Limitations of current system

- Moderate spacial resolution of RPC/TGC
  - ❖ 10-20 GeV trigger rate dominated by mis-measured muon p_T or "fake" muon ($K/\pi \rightarrow \mu$)
- Low trigger efficiency (~65% in barrel)
  - ❖ Down by 10% for HL-LHC since RPCs need to be operated at a reduced voltage to mitigate aging
- Reduced acceptance in barrel RPC
  - ❖ Address in HL-LHC by adding RPC chambers

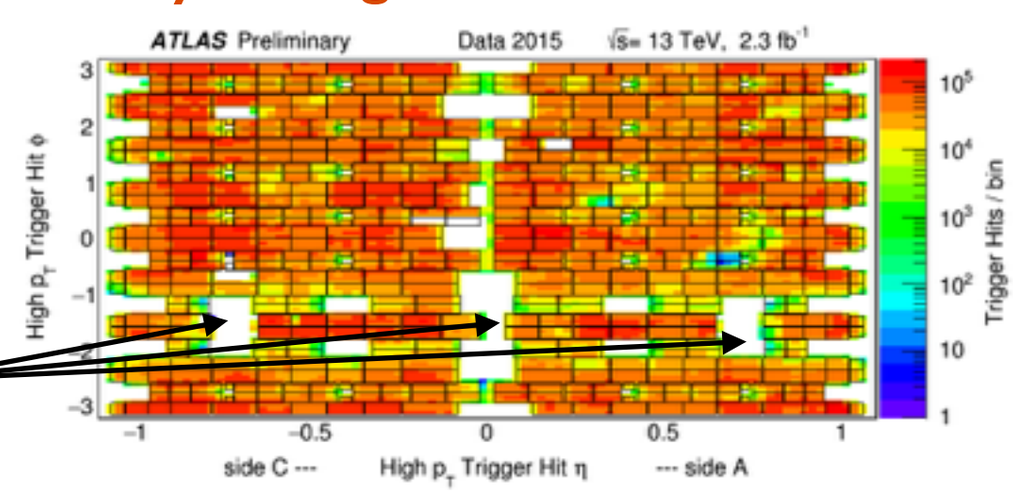
Level-1 Muon Trigger Composition



RPC trigger efficiency for reconstructed muon p_T>15GeV

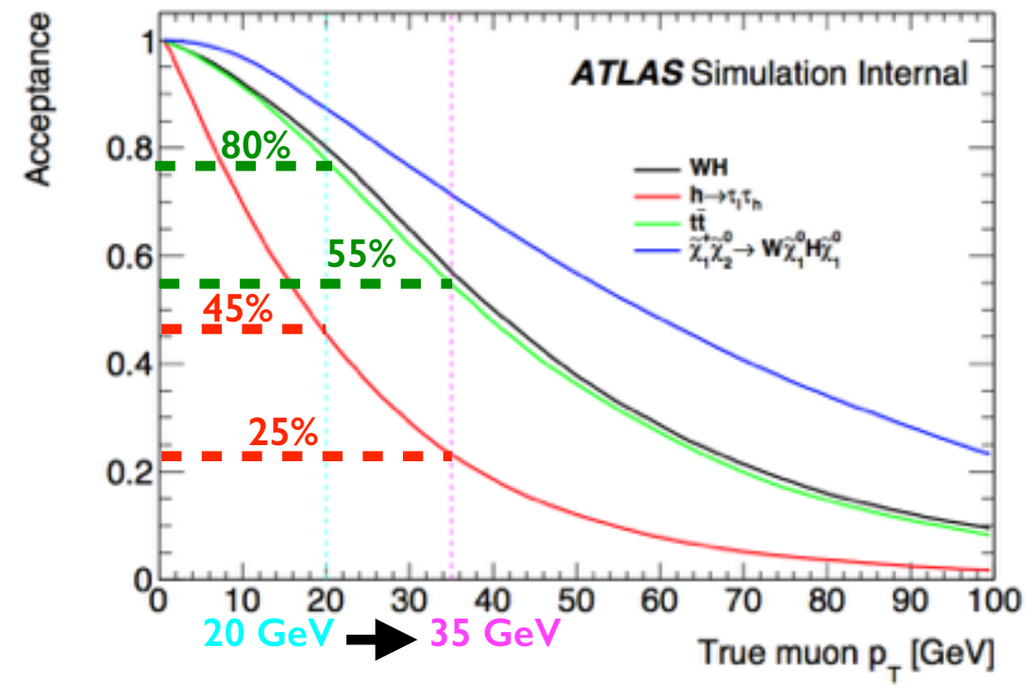


RPC trigger coverage

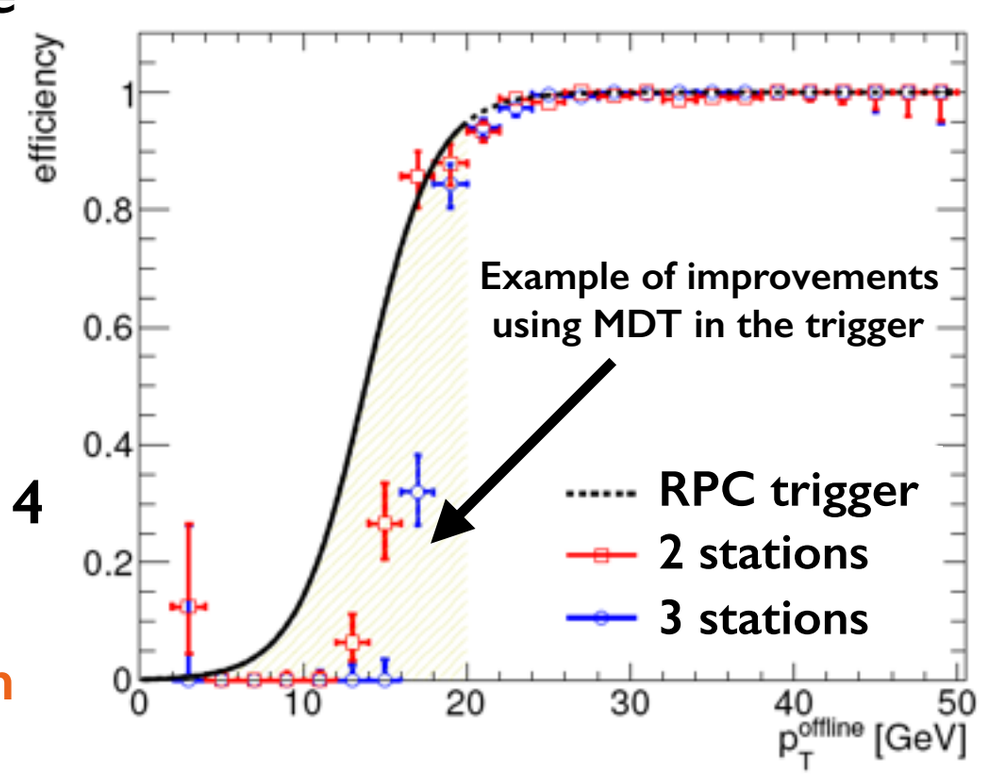


Motivations to Muon Trigger Upgrade

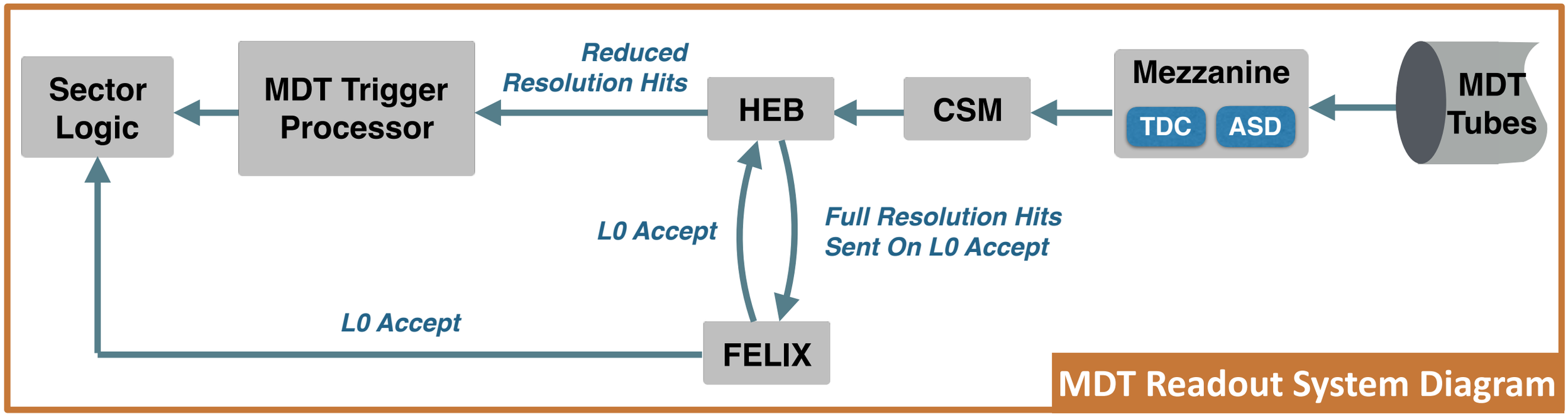
- ✓ HL-LHC physics program necessitates maintaining single μ trigger p_T threshold of ~20 GeV
- ✓ With current system and with HL-LHC conditions, the single μ trigger rate for p_T>20GeV would increase by a factor 2
  - To maintain the current trigger rate, the p_T threshold would need to be increased to 35 GeV
  - Such p_T threshold would significantly degrade the physics performance.



- ✓ Solution: Sharpen muon p_T threshold
  - By using MDT precision hits, muon p_T can be measured more accurately at level-0
  - Reduces fake muon trigger rate by up to a factor 4
  - Add redundancy to triggers based on RPC/TGC
    - ❖ Less stringent requirements imply improvement in trigger efficiency



Overview of Muon Trigger Upgrade



- ✓ To handle increase in rates and fakes associated with HL-LHC conditions, MDT readout electronics needs to be upgraded
- ✓ Offers the opportunity to implement an MDT based Level-0 muon trigger

- ✓ Level-0 MDT trigger is one of the critical component necessary to maintain the muon trigger performances necessary for the HL-LHC physics program
- ✓ This project is synergetic with NSF US-ATLAS plans in the muon upgrade for HL-LHC
  - UCI well position based on past/current experience in muon readout and trigger system

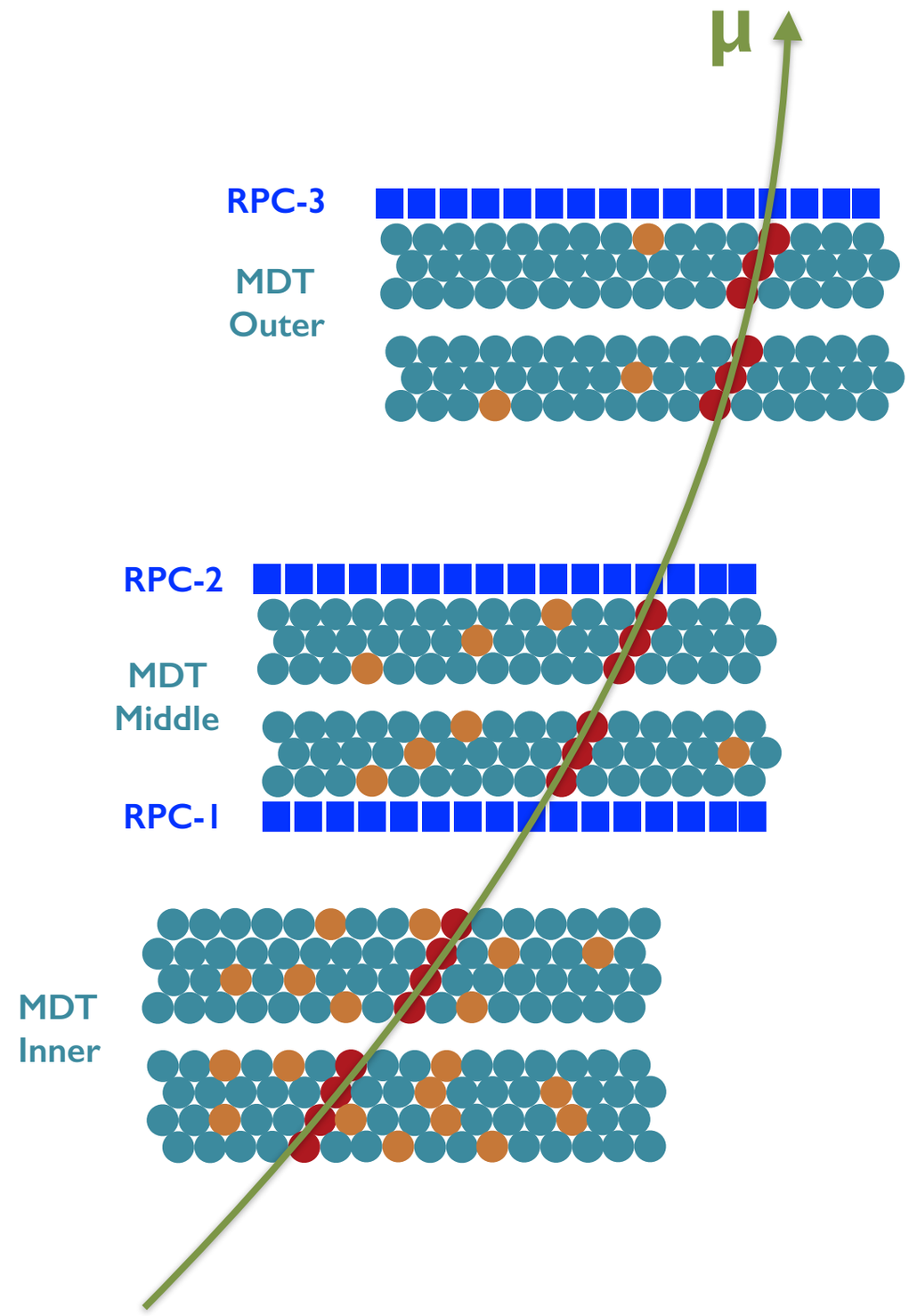
System Requirements

✓ Goals:

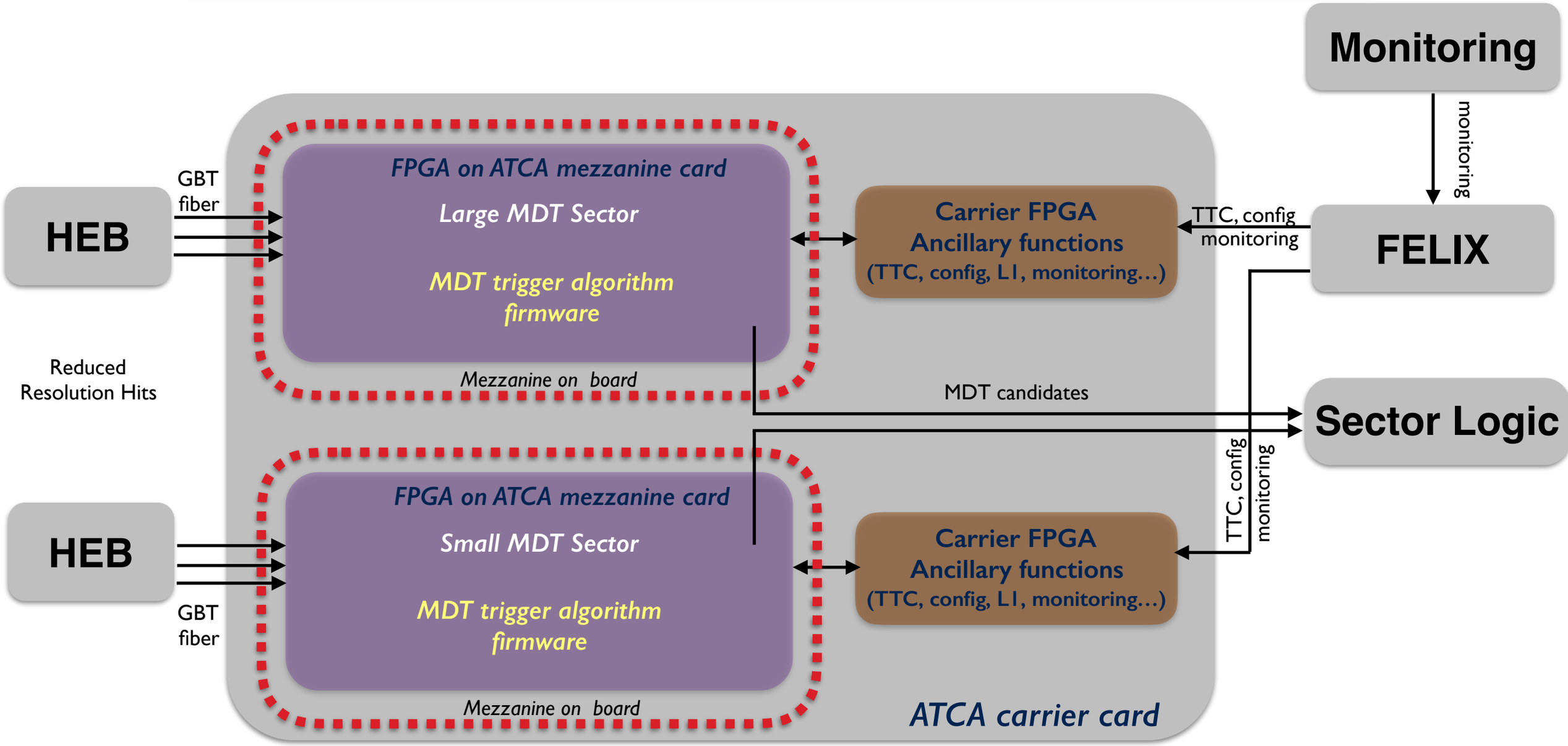
- Use MDT and sMDT precision hits to preform a Level-0 muon trigger decision within 6μs latency

✓ Functionalities

- Calibrate MDT hits drift time
- Segment finding on each MDT layer
- Segments linking
- Track fitting



Conceptual Design



✓ **Deliverables: Design, production and testing of**

- **Mezzanine board**
- **Firmware for MDT trigger algorithm**

R&D Effort Toward TDR

TDAQ TDR: End-2017
Muon TDR: Mid-2017

✓ What are the major challenges remaining?

- **Latency budget**
  - ❖ Preliminary studies show that an MDT trigger algorithm can be performed within 4.5µs (with 1.6µs used to received hits from CSM to MDT trigger)
  - ❖ Latency depends on algorithm implementation choices

✓ What R&D needs to be done to address these challenges

- **Develop an MDT based trigger algorithm that can meet the stringent latency budget.**
  - ❖ Define specifications, functionalities and performance goals
  - ❖ Implement preliminary algorithm on a demonstrator board to estimate its latency.
  - ❖ Estimate the full data chain latency

R&D effort (cont.)

Planned activities and milestones beyond TDR:

✓ **FY18:**

- **Refine trigger algorithm and estimate performance**
- **Define hardware choice**
  - ❖ **Start design and simulation of firmware**

✓ **FY19:**

- **Finalize firmware design, simulation and implementation on evaluation board to test performances**
- **Start design and simulation of mezzanine board**

✓ **FY20:**

- **Begin full prototype design of mezzanine board and firmware**

Summary

- ✓ Level-0 MDT trigger is one of the critical component to maintain the muon trigger performances necessary for the HL-LHC physics program
- ✓ Project is synergetic with the rest of NSF US-ATLAS muon upgrade
- ✓ Effort built on group expertise and experience
- ✓ Clear R&D path toward TDR and beyond to insure readiness for construction phase

BACKUP

Cost Estimate

✓ Cost was estimated based on the experience from the New Small Wheel (NSW) trigger processor, which is a comparable system with AMC fitted with FPGA within an ATCA carrier card (see p5 of BoE)

- Cost driven by FPGA
  - ❖ For the estimate used Xilink Virtex-7 FPGA (same as for NSW)

Element TDAQ	Quantities	Unit Cost	Cost [$ 2015]
ATCA board base for MDT trigger processor			**12,717**
FPGA segment finding, linking & track fitting	2	4,674	9,348
PCB	2	1,087	2,174
PCB assembly	2	326	652
PCB misc parts	2	272	543

Table 2: Cost estimate for the MDT trigger AMC

- 32 production boards
- 4 additional boards for testing and verifications
- 2 prototypes
  (see p2 of BoE)

6.8.y.2 MDT Trigger						
WBS	Description	Labor FTE	Labor Ayk$	M&S Ayk$	Travel Ayk$	TOTAL Ayk$
6.8.y.2	MDT Trigger	11.81	1,610	597	49	2,256
	Engineers	5.06				
	Techs	2.50				
	Students	4.25				

Table 1: The deliverables from UC Irvine

Risk Estimate

✓ **Schedule Risk**

- R&D does not yield sufficient information to define completely specifications for mezzanine board and/or firmware
- Mitigate risk by ensuring that relevant informations are available to define them. Ensure that there is viable path for communication between boards and all is accounted for in latency calculation.

✓ **Cost Risk**

- Final FPGA cost may be higher than anticipated.
- Mitigate risk by performing studies leading to the best hardware solution both in term of performance and cost.

✓ **Scope Risk**

- ATCA carrier cards fairly new system to ATLAS
- Mitigate risk by working with collaborators experience with such systems

✓ **External Risk**

- ATCA carrier card developed by external collaborators. Delay in delivery will reduce testing time of final integrated design
- Mitigate risk by developing standalone testing stands. Modest delay can be accommodated within current schedule

See BoE p4-5