sPHENIX TPC DAM Protocol DRAFT

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1 FEE to DAM Protocol

Two ideas: custom protocol 8b10b encoding or standard 5/10 Gigabit Ethernet (UDP) between FEE to DAM. Using UDP offers cheaper debugging/development hardware (COTS). If using 8b10b encoding, we would use `K28.5` and `D16.2` idle codes. FEE would derive its system clock off of link's recovered clock. Trigger information would also be sent over this link, requiring the links to be deterministic and synchronous to the level 1 trigger system (I think).

1.1 8b10b Protocol

Name	Bits	Description
Op Code	8	SAMPA Read = `0x1`
		SAMPA Write = `0x02`
		FPGA Control Write = `0x03`
		FPGA Control Read = `0x04`
		Write ACK = `0x11`
		Read ACK = `0x12`
		ADC Data = `0xFF`
FEE Addr	10	Board address
Hw Addr	4	Hardware address of SAMPA ASIC
Chan Addr	5	Channel Address of SAMPA
Reg Addr	5	SAMPA Register Address
Data	20	Register data to write to SAMPA

1.1.1 8b10b Register Write

0 1 2 3 4 5 6 7	8 9 10 11 12 13 14 15 16 17	18 19 20 21	22 23 24 25 26	27 28 29 30 31
Op Code	FEE Addr	Hw Addr	Chan Addr	Reg Addr
Data (SAMPA is 20 bits)				

1.1.2 8b10b Register Read

1.1.3 Request Frame

0 1 2 3 4 5 6 7	8 9 10 11 12 13 14 15 16 17	18 19 20 21	22 23 24 25 26	27 28 29 30 31
Op Code	FEE Addr	Hw Addr	Chan Addr	Reg Addr

1.1.4 Reply Frame

0 1 2 3 4 5 6 7	8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27	28 29 30 31
Op Code	Reply Data	$\cdots$

1.1.5 8b10b ADC Data

0 1 2 3 4 5 6 7	8 9 10 11 12 13 14 15 16 17	18 19 20 21	22 23 24 25 26	27	28	29	30	31
Op Code	FEE Addr	Hw Addr	Chan Addr	E	T	0	0	0
N Words	BX Count						0	0
10-bit ADC Data (Byte aligned) ...								

1.2 UDP Application Protocol

FEE's geographical address (FEE Addr from above) would set the IPv4 address. The UDP port changes for each operation (register read, register write, ADC stream data) rather than the op-code from above.

1.2.1 UDP Register Read

0 7	8 15	16 23	24 31	
IPv4 Source Address				UDP Header
IPv4 Destination Address				
Zeros	0x11 (UDP)	UDP Length		
Source Port		Destination Port		
Length		Checksum		
Preamble (0xbeef)		Register Address		Payload

1.3 UDP Register Write

0 7	8 15	16 23	24 31	
IPv4 Source Address				UDP Header
IPv4 Destination Address				
Zeros	0x11 (UDP)	UDP Length		
Source Port		Destination Port		
Length		Checksum		
Preamble (0xbeef)		Register Address		Payload
Register Data				

1.4 UDP ADC Data

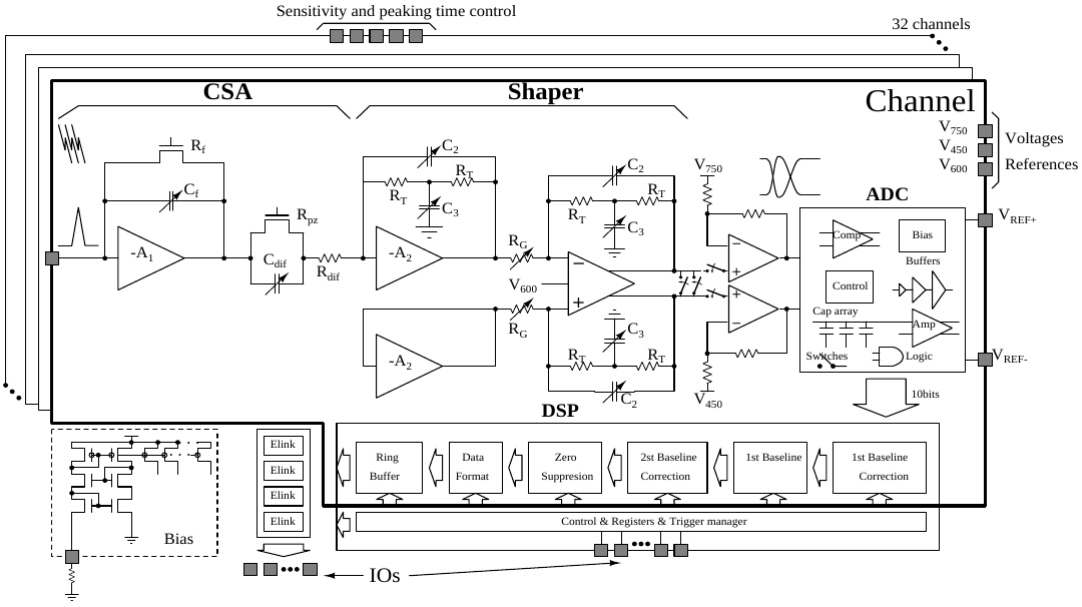
0 7	8 15	16 23	24 31	
IPv4 Source Address				UDP Header
IPv4 Destination Address				
Zeros	0x11 (UDP)	UDP Length		
Source Port		Destination Port		
Length		Checksum		
Preamble (0xbeef)		N Words		Payload
E T Hw Addr	Ch Addr	CX Counter	0	
10-bit ADC Data (Byte aligned) ...				

2 From DAM to Linux Host

Two PCIe endpoints, total reported throughput is about 101.7 Gb/s. FELIX card has 2x DDR4 SODIMM supporting up to 16GB, could we memory map the whole TPC and perform clustering in memory before DMA transfer to the Linux host? Here we'll also add the missing bits (MSBs?) to the CX counter (timestamp).

3 SAMPA Data Format

The following information [1] is assumed to be current. Is there a more up-to-date document?



- Clocks
  - ADC Clk (10-20 MHz)
  - Bunch Crossing Clk (40 MHz max)
  - Serial Link (320 MHz max)
- Serial Link
  - 4 LVCMOS 1.5V
  - 125 MHz @ 20pF (or 348 MHz @ 0.05pF)
- Slow Control
  - Rx and Tx @ LVCMOS 1.5 V
  - Data latched in relation to the ADC clk.

3.1 Slow Control

0	1	2	3	4 … 7	8 … 12	13 … 17	18 … 37
S	P	B	W	Hw Addr	Chan Addr	Reg Addr	Data

Name	Bits	Description
S	1	Start bit, always 1
P	1	Parity (odd) of packet, excluding the start bit
B	1	Broadcast bit
W	1	0=Read, 1=Write to address
Hw Addr	4	Hardware address of chip
Chan Addr	5	Channel Address
Reg Addr	5	Register Address
Data	20	Register data to write

3.2 Slow Control Reply

0	1 … 21
S	Data

Name	Bits	Description
S	1	Start bit, always 1
Data	20	Command Msg: 0x55555 (ACK) If write: data written If read: data returned for read

3.3 Serial Stream Data

0 … 7	8	9	10	11 … 14	15 … 19	20 … 29	30 … 49
Preamble	P	E	T	Hw Addr	Ch Addr	N Words	BX Count
ADC Stream (Payload) …							

Name	Bits	Description
Preamble	8	0x33 (0b00110011)
P	1	Parity (odd) of header
E	1	Early Trigger, trigger recieved before end of timewindow
T	1	Data truncated due to overflow (0 data following)
Hw Addr	4	Hardware address of chip
Chan Addr	5	Channel address
N Words	10	Number of 10-bit words in payload
BX Count	20	Bunch-crossing counter (40 MHz)

References

[1] Arild Velure, SAMPA Specification MPW1
`http://folk.uib.no/ave082/SAMPA/SAMPA_MPW1_specs.pdf`