R&D for ATLAS LAr Calorimeter Readout and Trigger Upgrade

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BROOKHAVEN NATIONAL LABORATORY

a passion for discovery

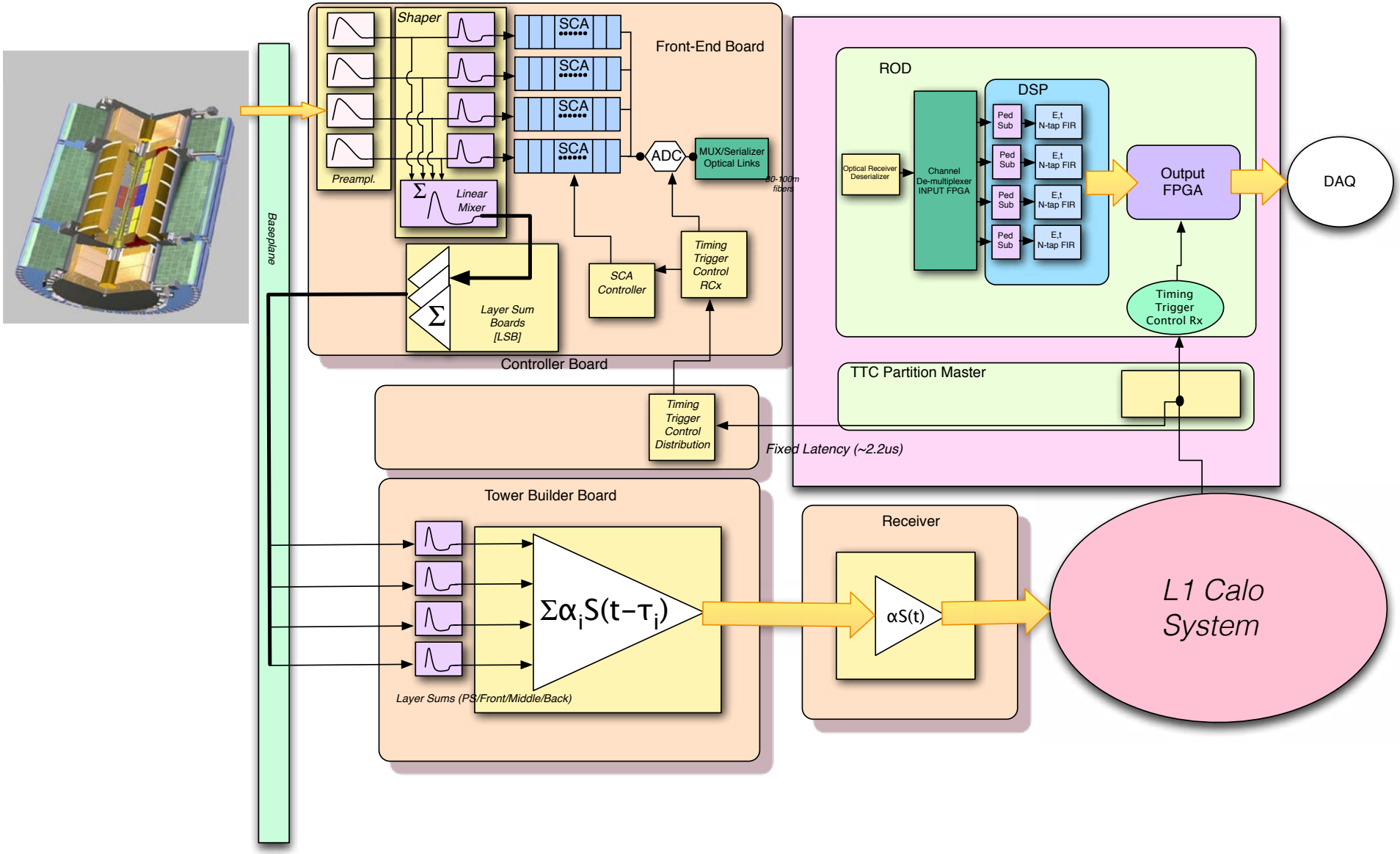
U.S. DEPARTMENT OF ENERGY | Office of Science

Detector R&D Program Manager (P. Kim) Visit to BNL, Oct 16th, 2012

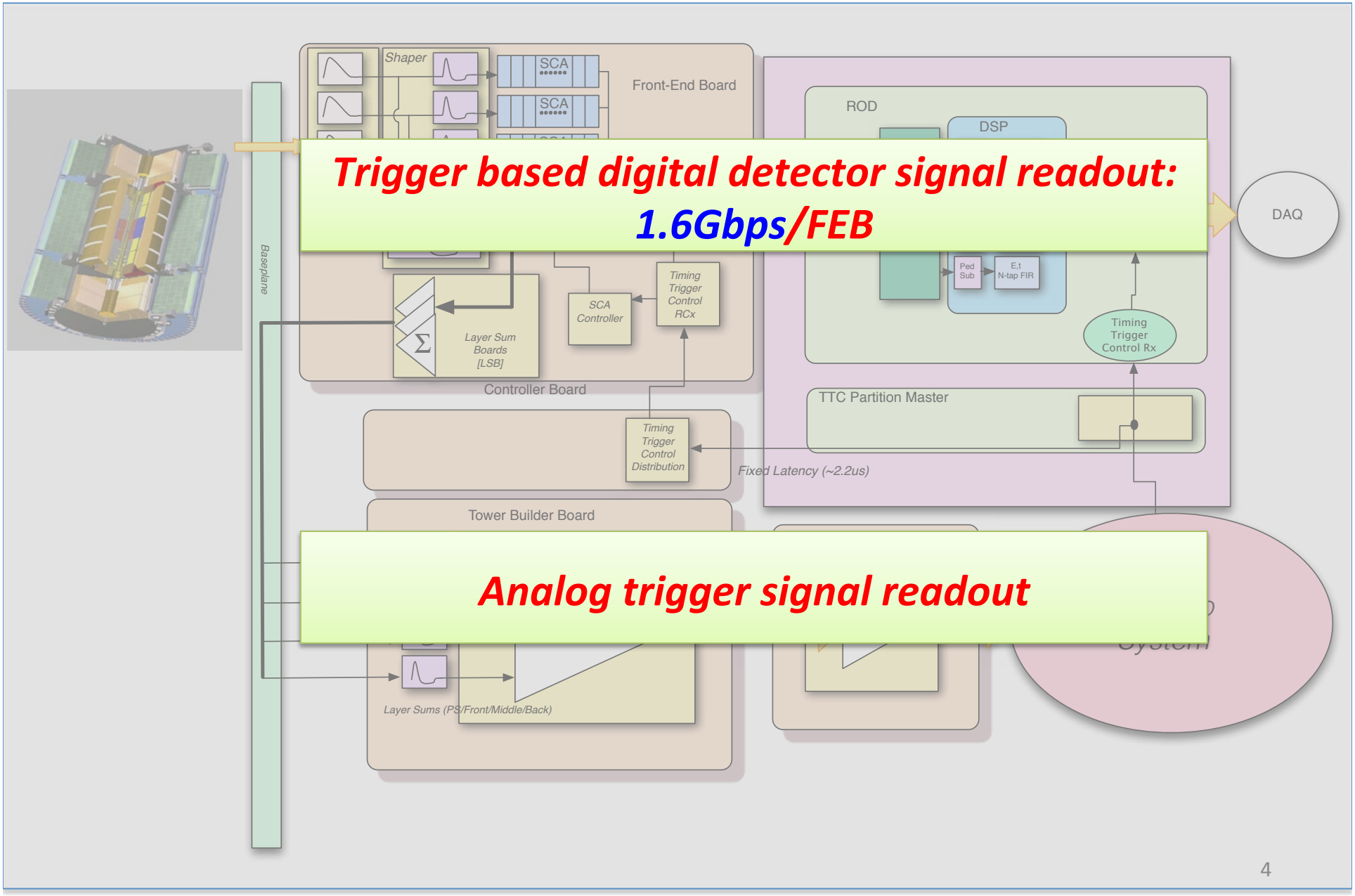
Outline

- Introduction
  - Phase-I and Phase-II Upgrade
- R&D for LAr Calorimeter Readout & Trigger Upgrade
  - Front-end development
  - Back-end development

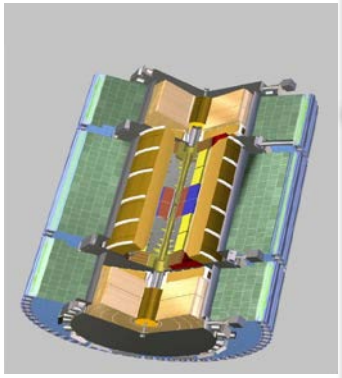
Current LAr Readout Architecture

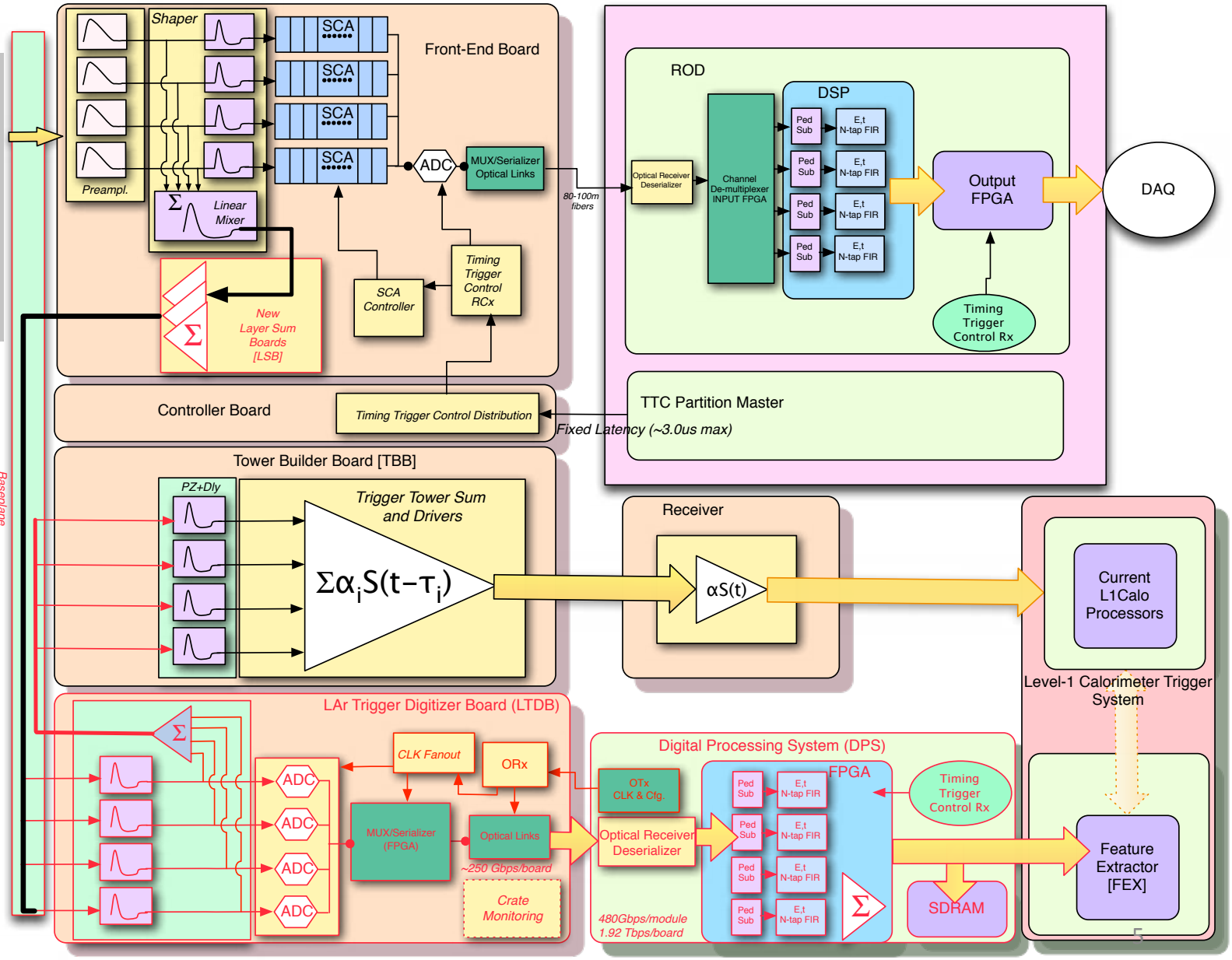


Current LAr Readout Architecture



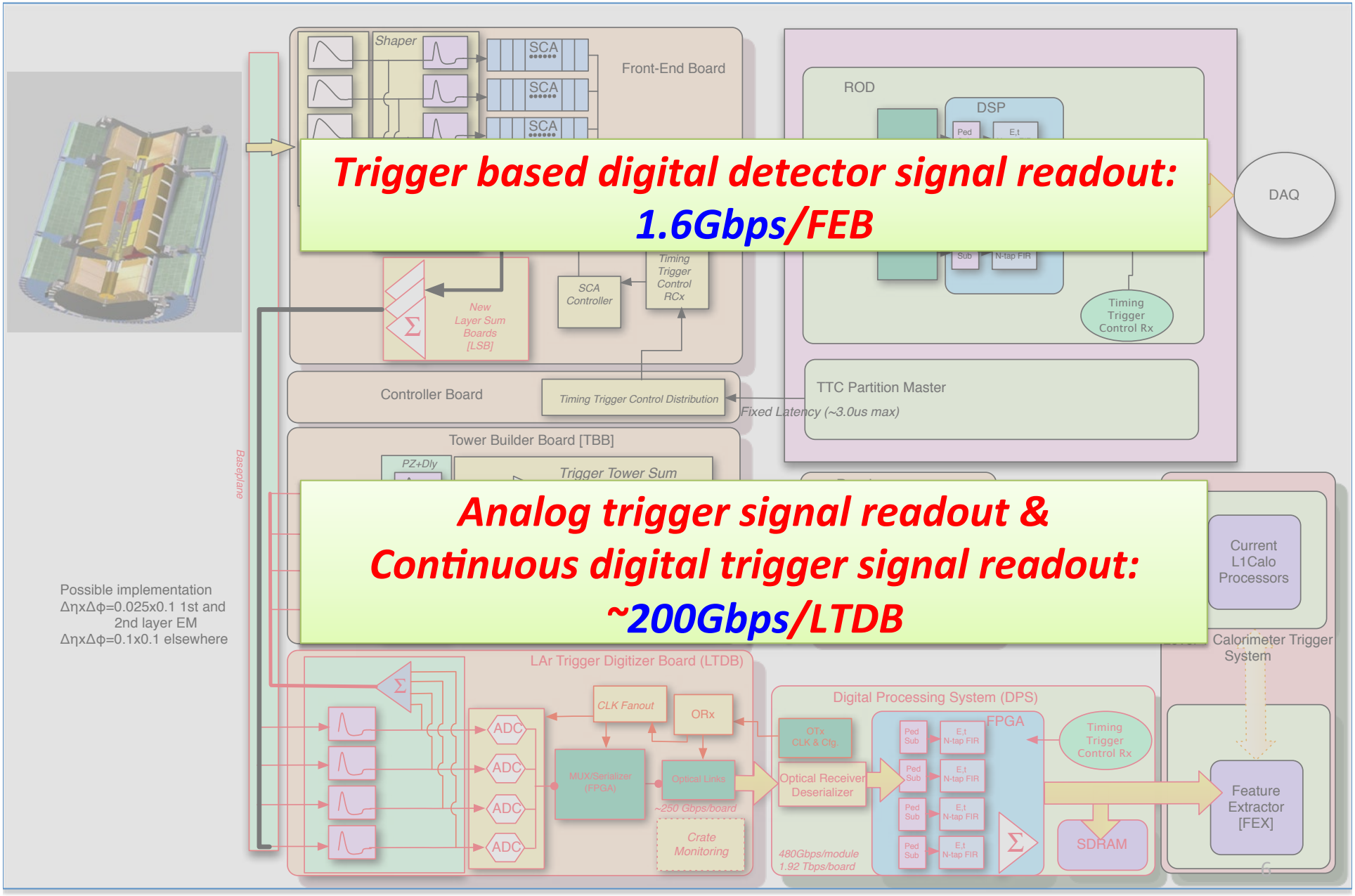
Readout Architecture in Phase-I Upgrade



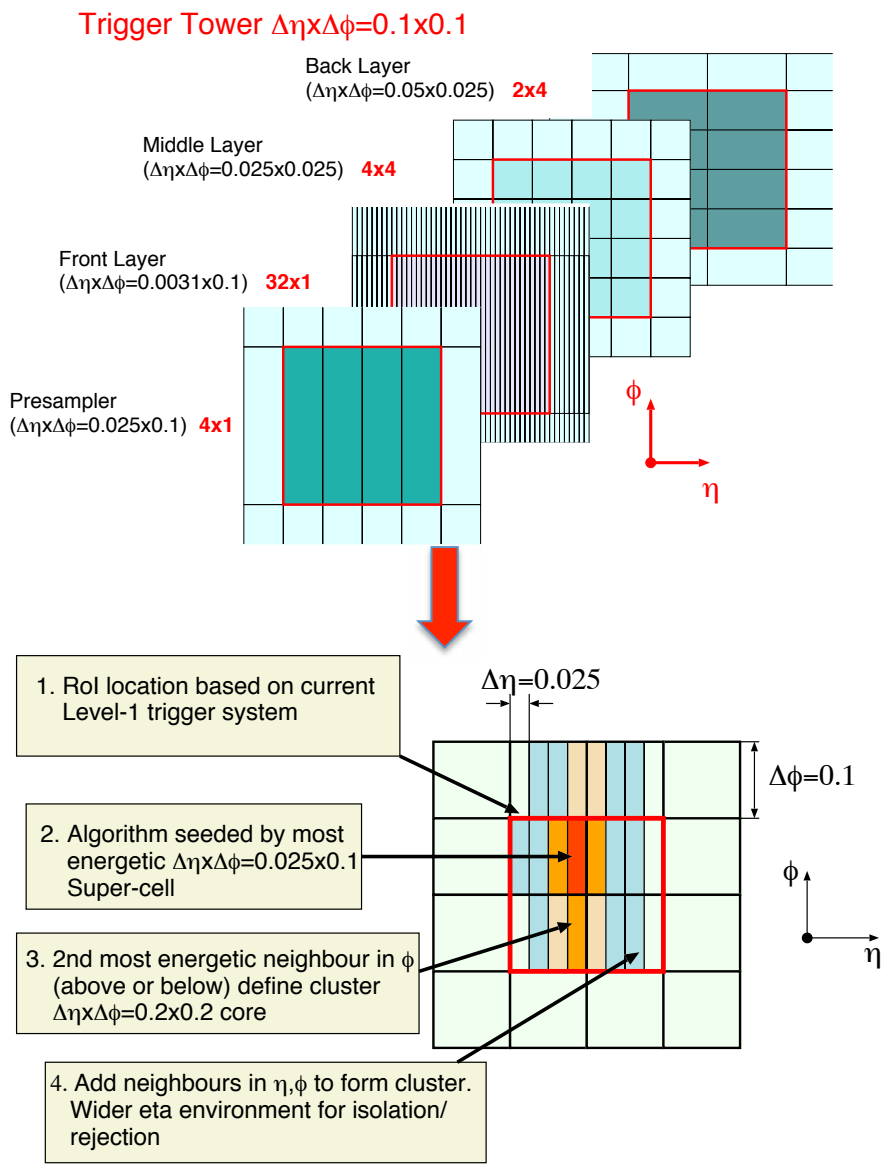


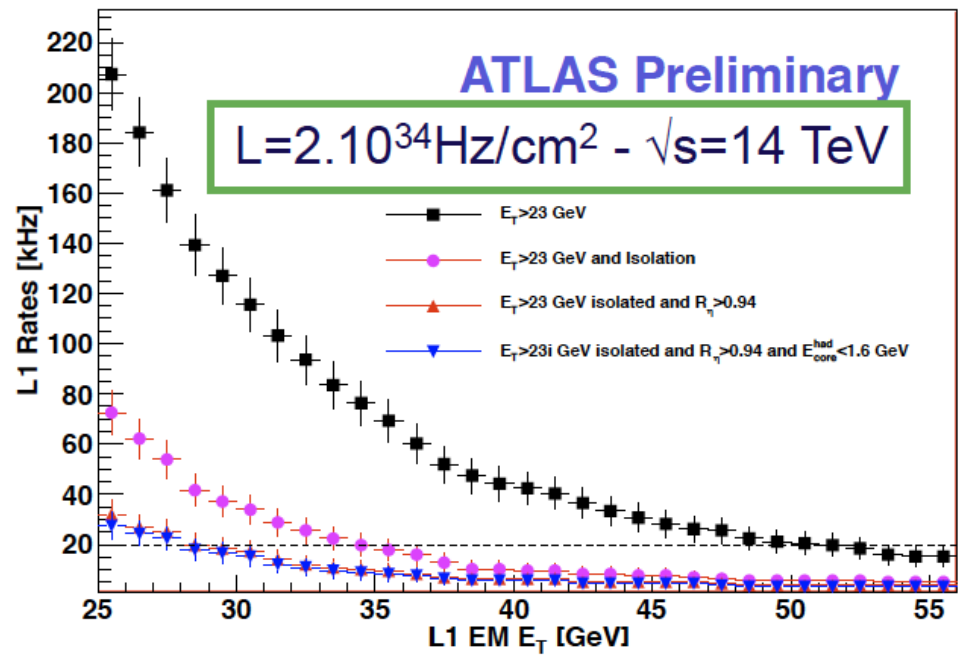
Possible implementation
$\Delta\eta\times\Delta\phi$=0.025x0.1 1st and 2nd layer EM
$\Delta\eta\times\Delta\phi$=0.1x0.1 elsewhere

Readout Architecture in Phase-I Upgrade



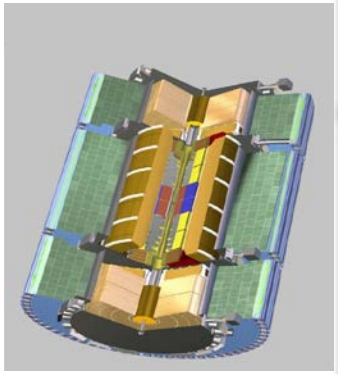
Improvement of L1 Trigger

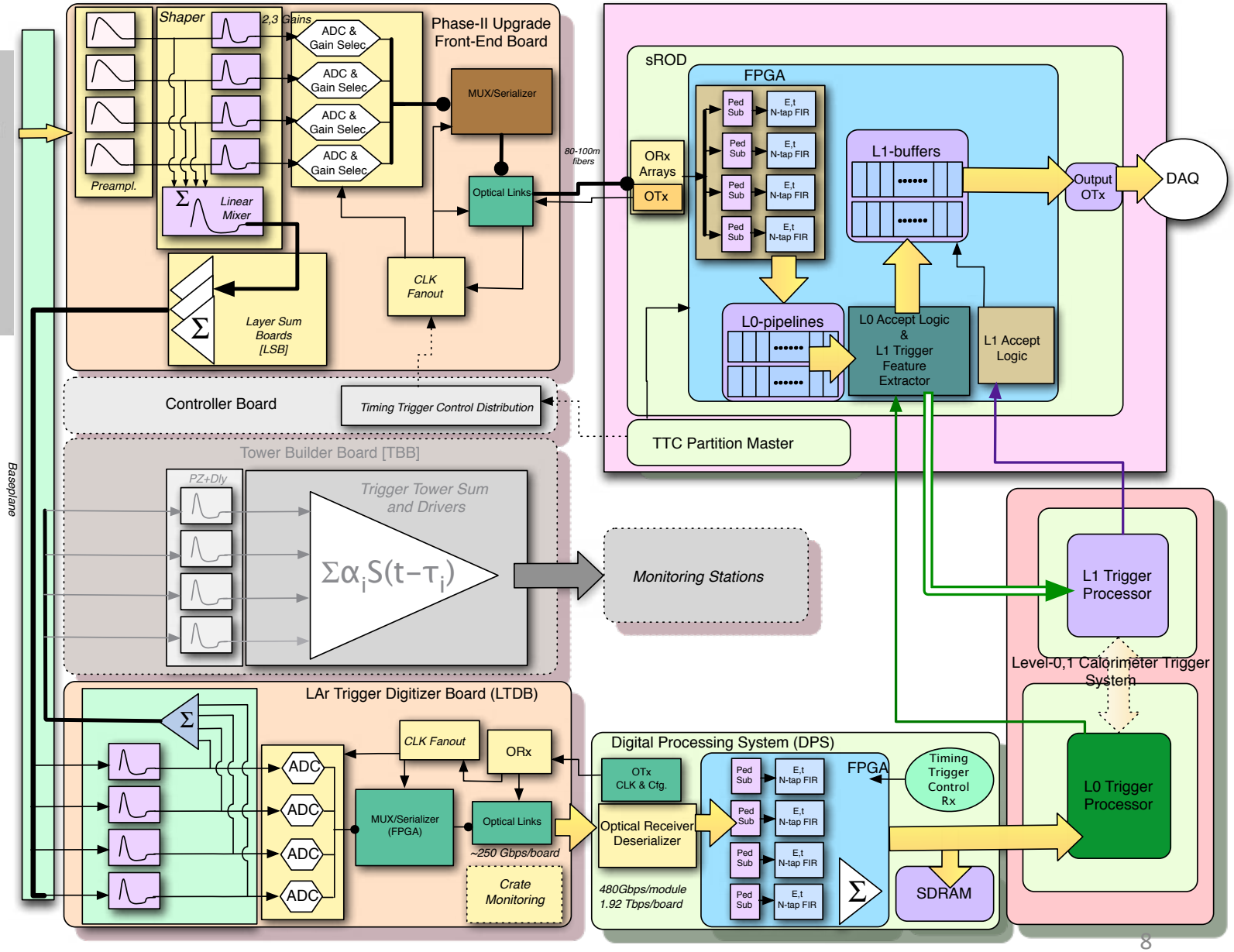




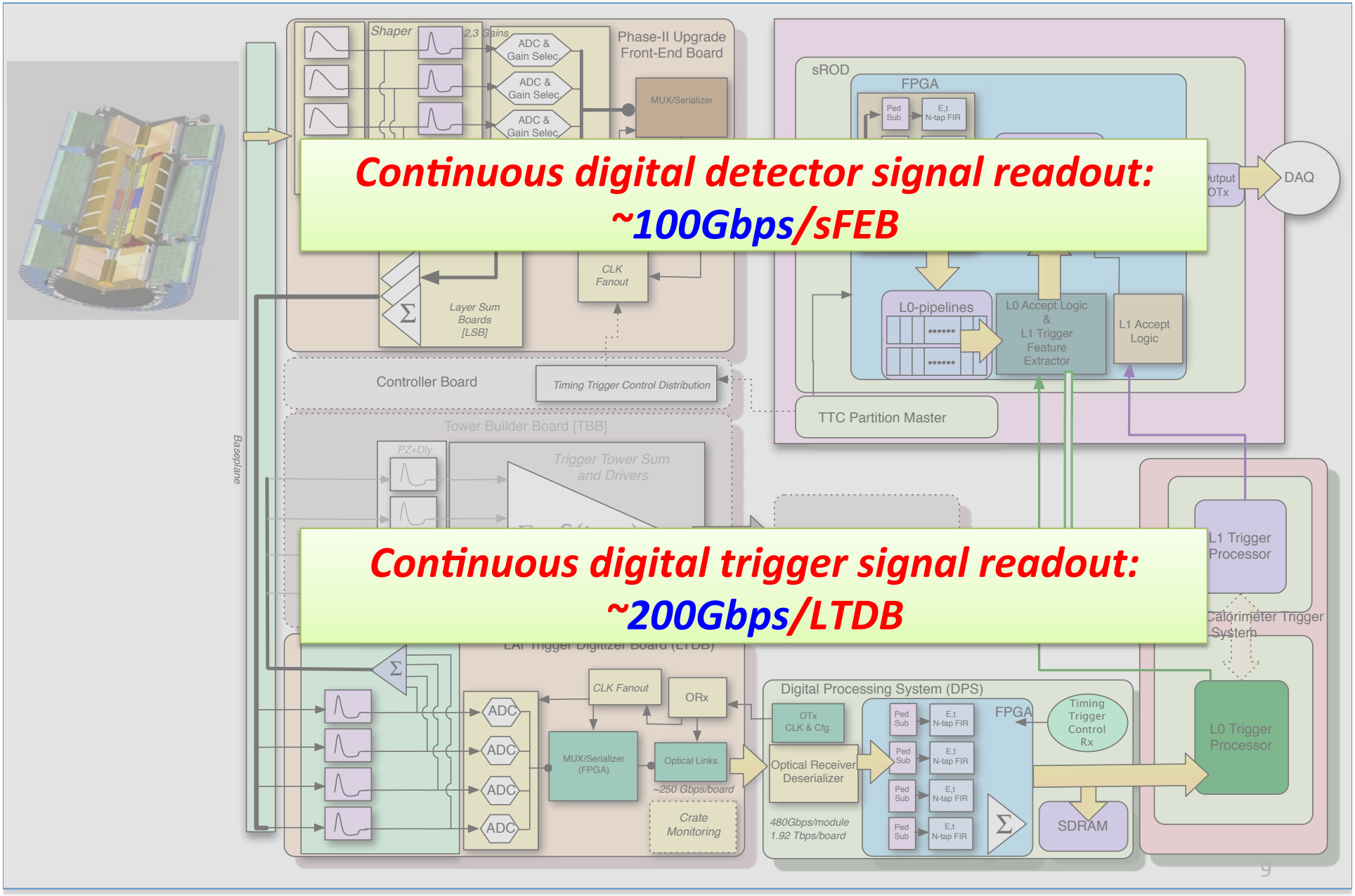
Critical to maintain low threshold for single lepton Level-1 trigger

Readout Architecture in Phase-II Upgrade

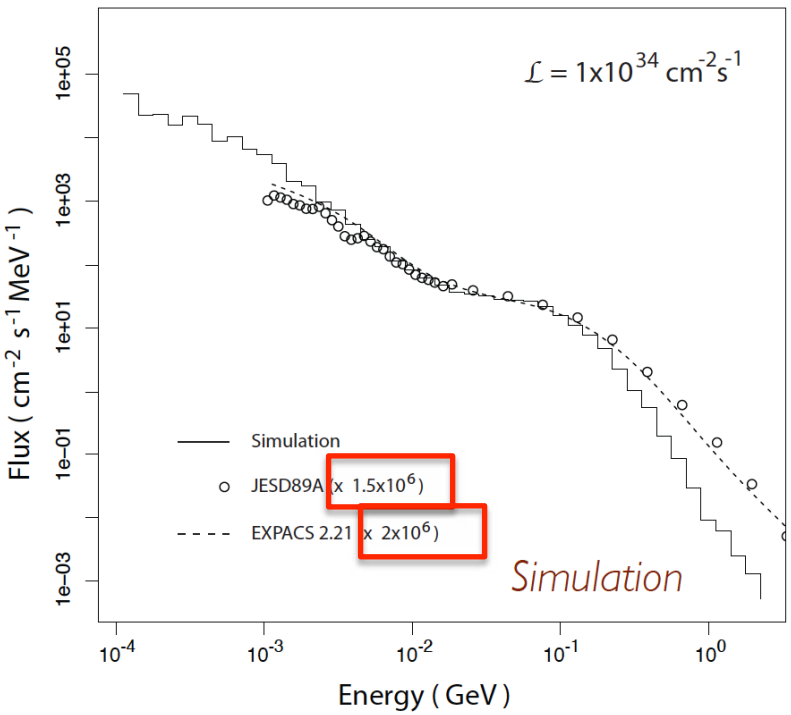




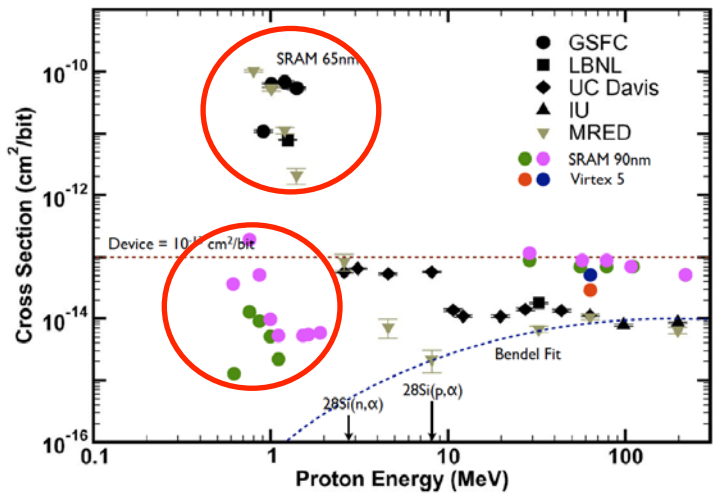
Readout Architecture in Phase-II Upgrade



Evaluation of Rad-hard Electronics and Mitigation of Radiation Related Problems



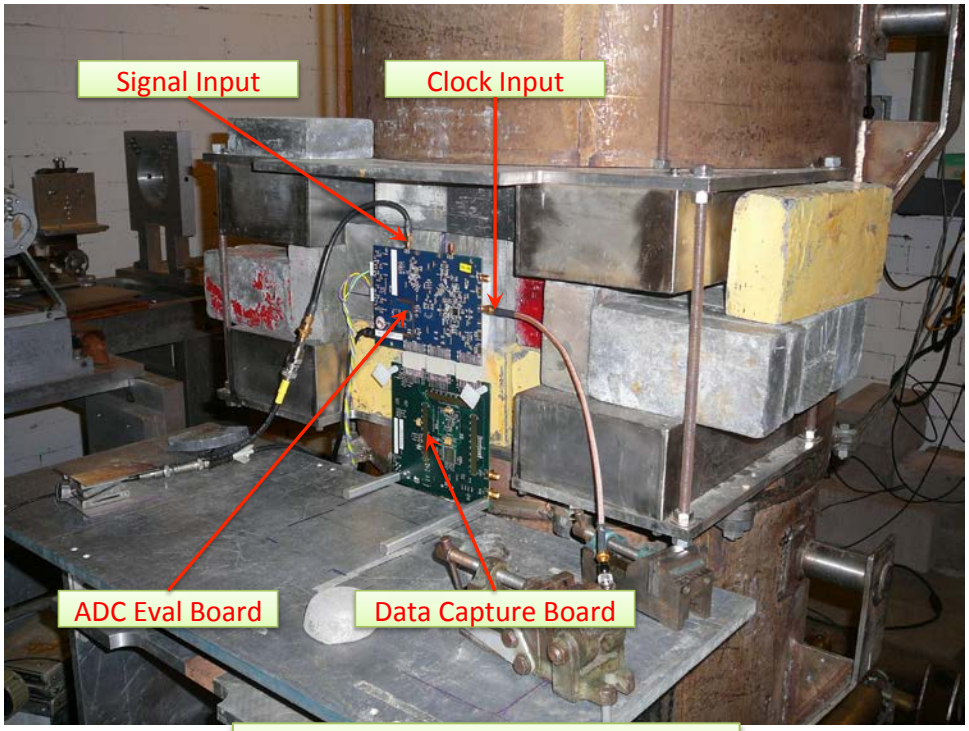
Neutron Spectrum compared to JEDEC and EXPACS



65 vs 90 nm SRAM

- Present and ***Future accelerator environment*** will require the use of radiation tolerant or hard components
- Small feature size devices are more tolerant to total dose, but more sensitive to single event effect
- Initiated a program to qualify components off-the-shelf for total dose at the BNL gamma radiation facility
- Those that pass total dose requirements will be tested for single event effects and mitigation techniques developed

Irradiation Test of COTS ADC



Gamma irradiation test setup

- ADC is the most technologically challenging component in the new architectures of LAr Calorimeter Upgrade
  - 15(6) bit dynamic range – 12 bit resolution – 40MSPS
  - Radiation tolerant and SEE immune
- ***Strategies*** being followed
  - Find the magic bullet with commercial parts
    - Verify radiation tolerance of commercial ADC
    - Gamma irradiation test at BNL for prescreening
    - SEE test with proton beam or neutron beam will be followed
  - Developing a custom ADC

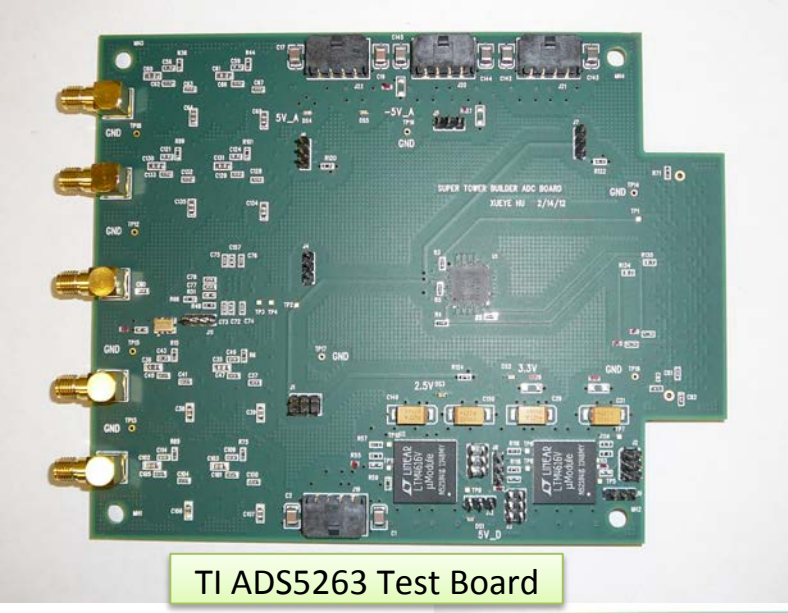
Summary of COTS ADC TID Irradiation Test

Table 3. TID test results of COTS ADCs by June 2012

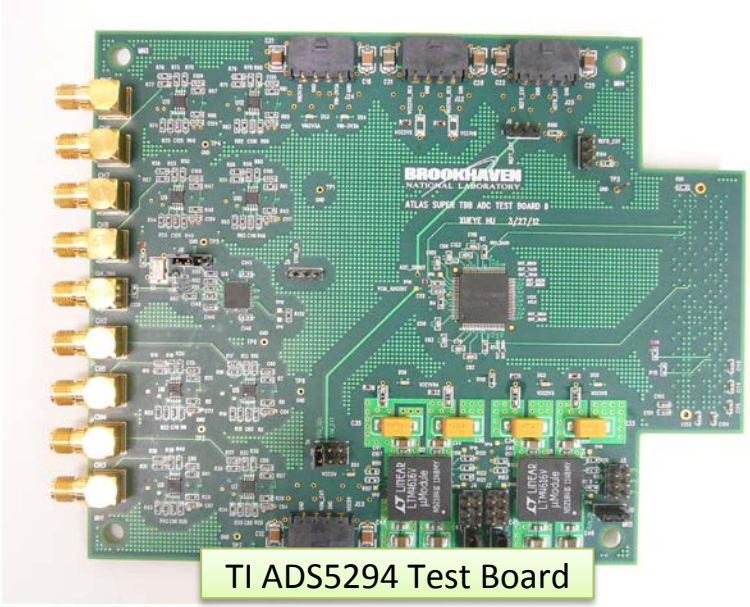
COTS ADC	Dynamic Range [bit]	Max Sampling Frequency [$MSPS$]	Analog Input Span [V_{p-p}]	Number of Channels per Chip	P_{total} per Channel [mW]	Technology	Vendor	TID [$kRad(Si)$]
AD9265-80	16	80	2	1	210	0.18 µm CMOS	ADI	~220
AD9268-80	16	80	2	2	190	0.18 µm CMOS	ADI	~160
AD9269-40	16	40	2	2	61	0.18 µm CMOS	ADI	~120
AD9650-65	16	65	2.7	2	175	0.18 µm CMOS	ADI	~170
AD9253-125	14	125	2	4	110	0.18 µm CMOS	ADI	~105
LTC2204	16	40	2.25	1	480	0.35 µm CMOS	Linear	~180
LTC2173-14	14	80	2	4	94	0.18 µm CMOS	Linear	~105
LTC2193	16	80	2	2	125	0.18 µm CMOS	Linear	~100
ADS4245	14	125	2	2	140	0.18 µm CMOS	TI	~235
ADS6445	14	125	2	4	320	0.18 µm CMOS	TI	~210
ADS5282	12	65	2	8	77	0.18 µm CMOS	TI	~460
ADS5263	16	100	4	4	280	0.18 µm CMOS	TI	~2100
ADS5294	14	80	2	8	77	0.18 µm CMOS	TI	~1070
ADS5292	12	80	2	8	66	0.18 µm CMOS	TI	~1060
ADS5272	12	65	2.03	8	125	0.18 µm CMOS	TI	~8800
HMCAD1520	14	105	2	4	133	0.18 µm CMOS	Hittite	~2300
HMCAD1102	12	80	2	8	59	0.18 µm CMOS	Hittite	~1730

- SEE test will be performed on three COTS ADC candidates
  - TI ADS5263, TI ADS5294, TI ADS5272

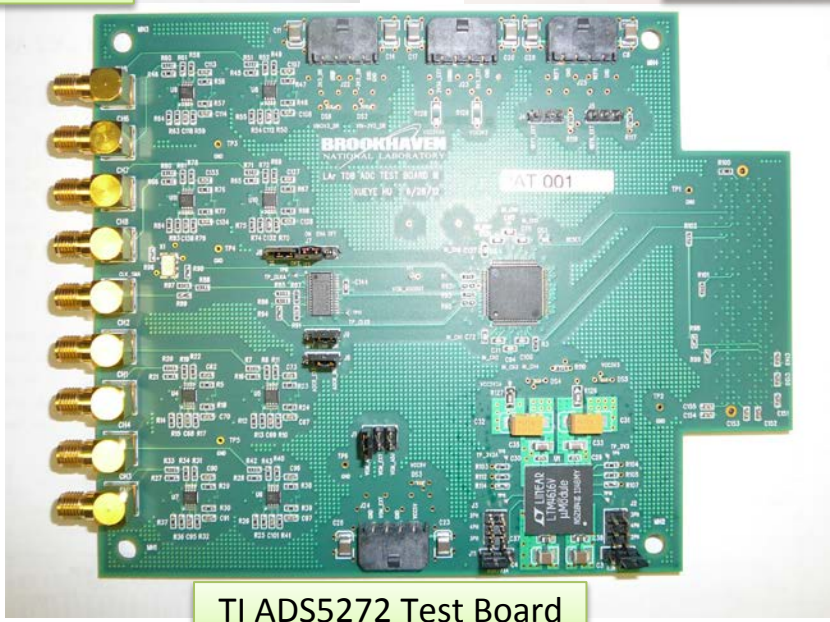
ADC Test Boards for SEE Studies



TI ADS5263 Test Board

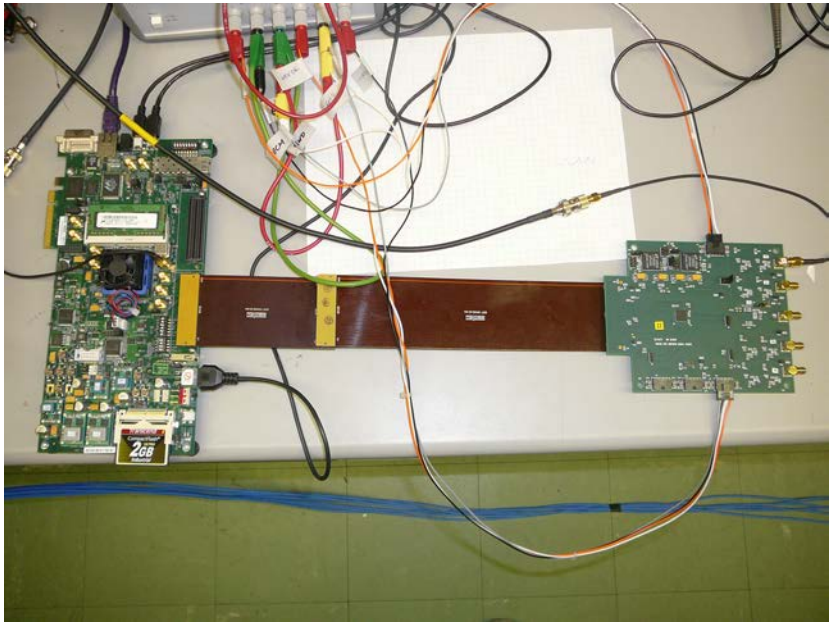


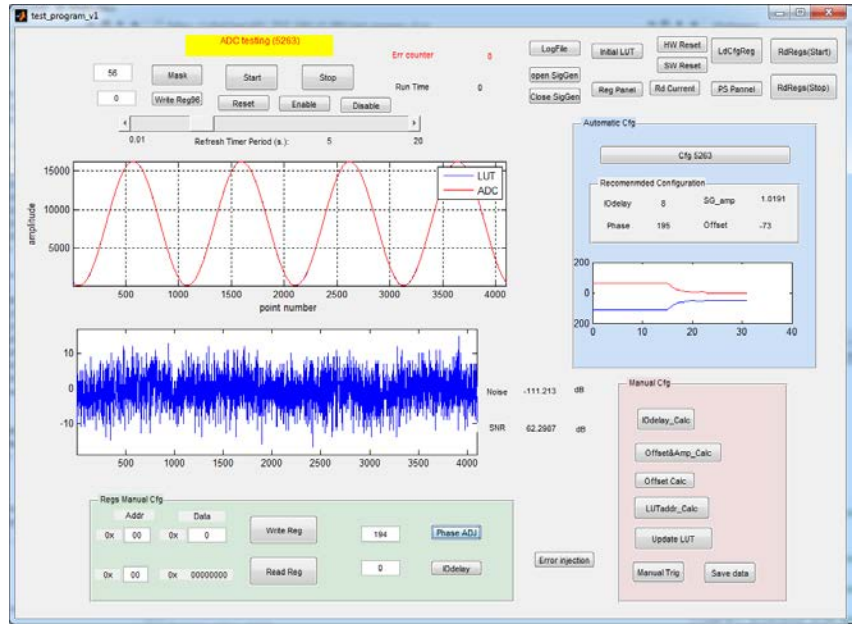
TI ADS5294 Test Board

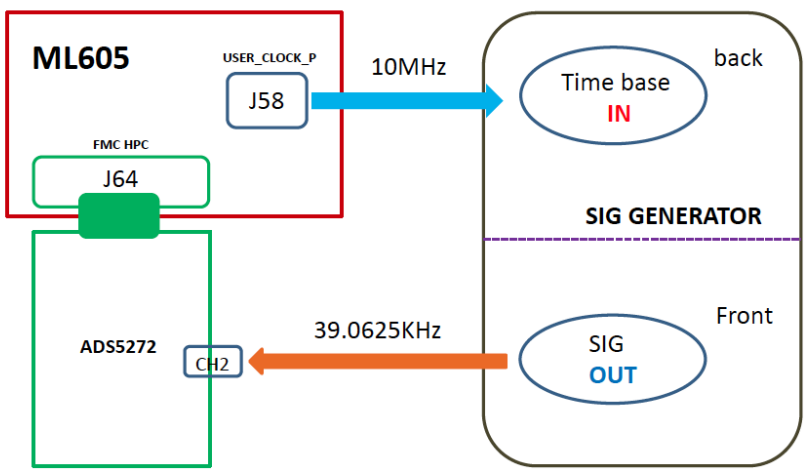


TI ADS5272 Test Board

ADC SEE Test Setup

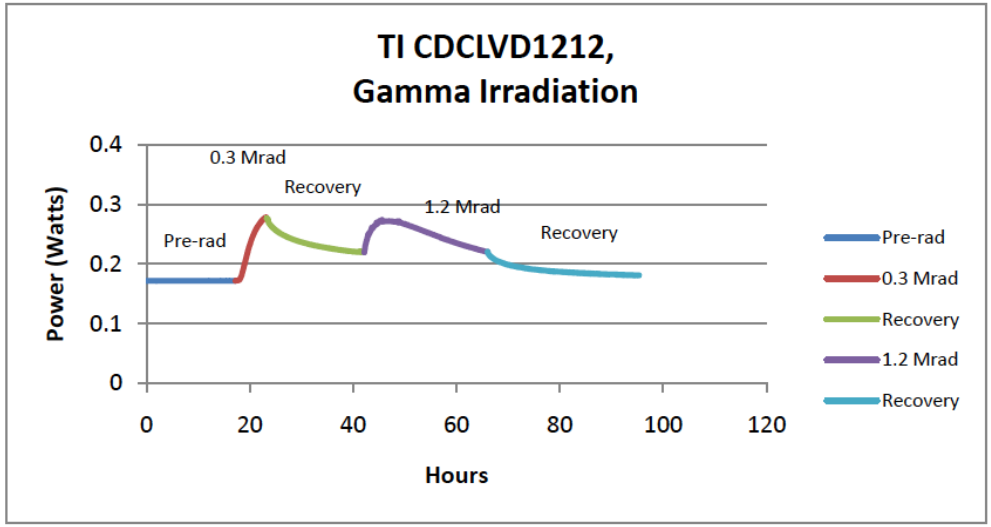


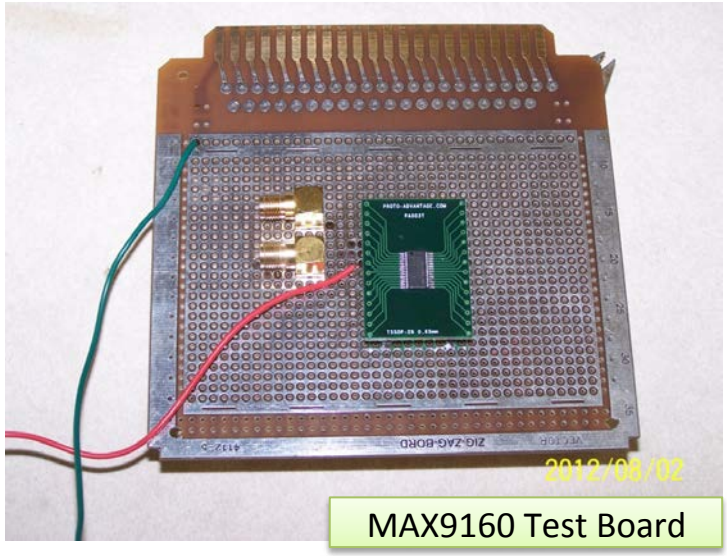


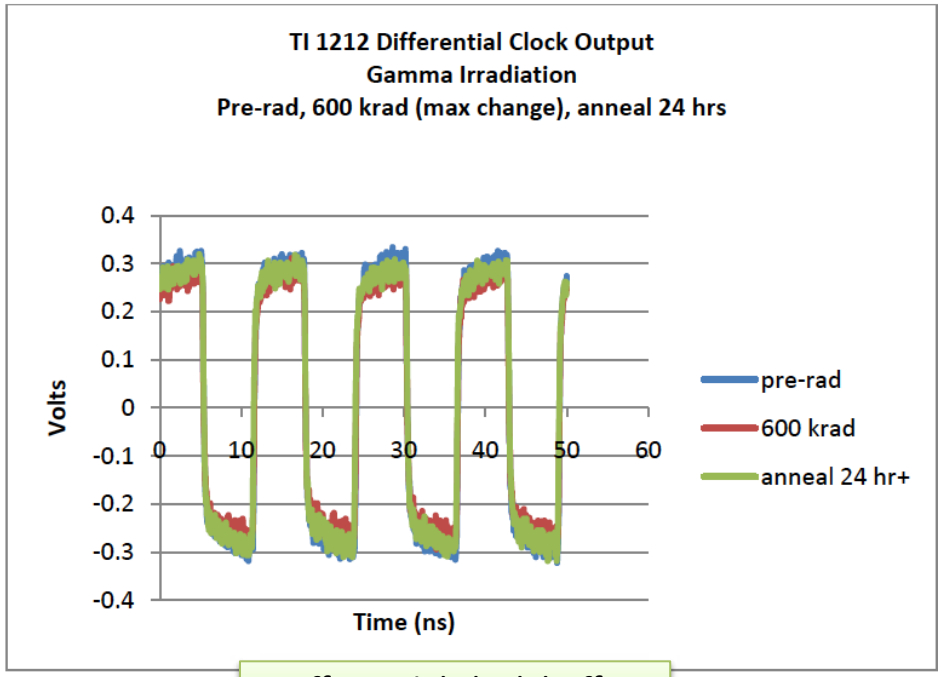


- System Setup
  - MicroBlaze based embedded processor is running on Xilinx ML605 board to handle the communication to PC over TCP/IP
  - 10MHz timebase is generated on ML605 and fed into signal generator for system synchronization
  - Sine wave from signal generator is injected into ADC test board, ADC data is checked against programmable LUT in real time
- ***Beam test plan***
  - Neutron beam test: 10/10 to 10/16 at LANSCE, Los Alamos
  - H4IRRAD beam test: 11/15 to 12/03 at North Area, CERN

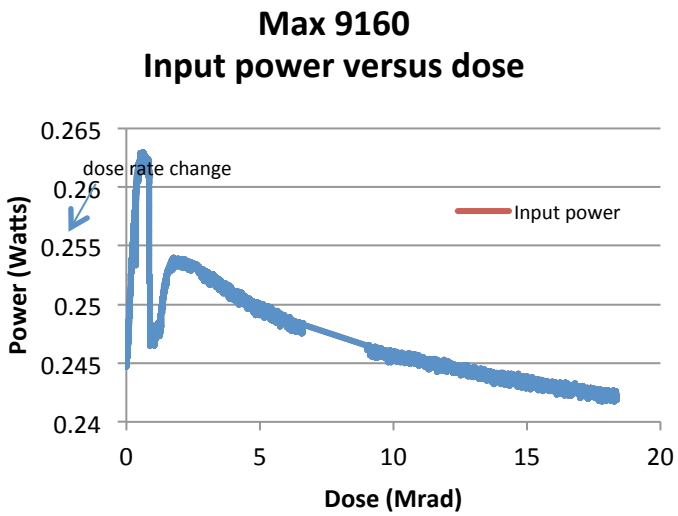
Irradiation Test of Other COTS Components





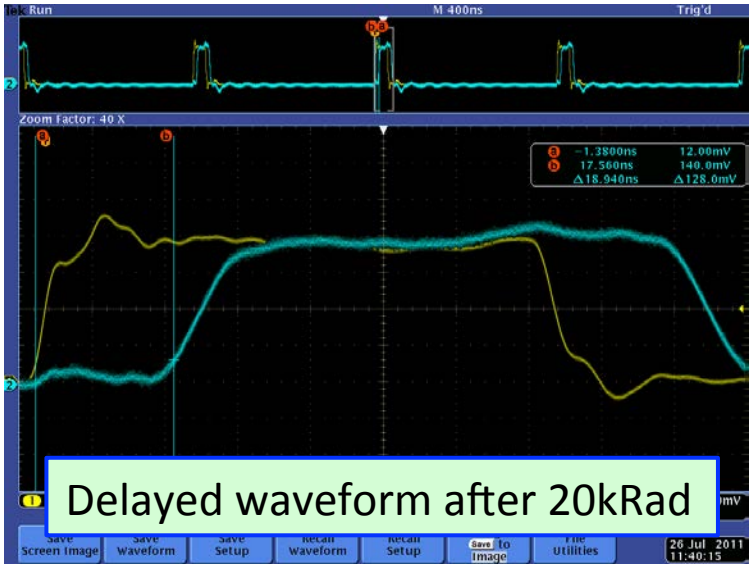


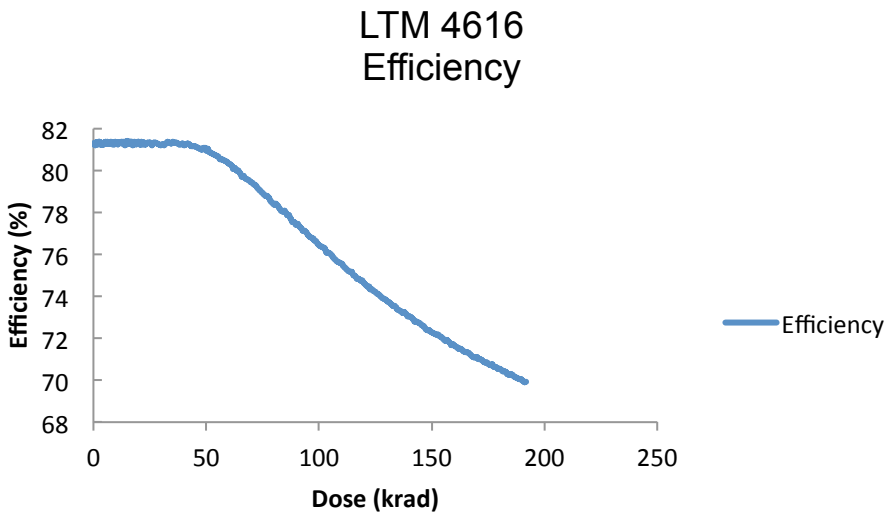
Differential clock buffer

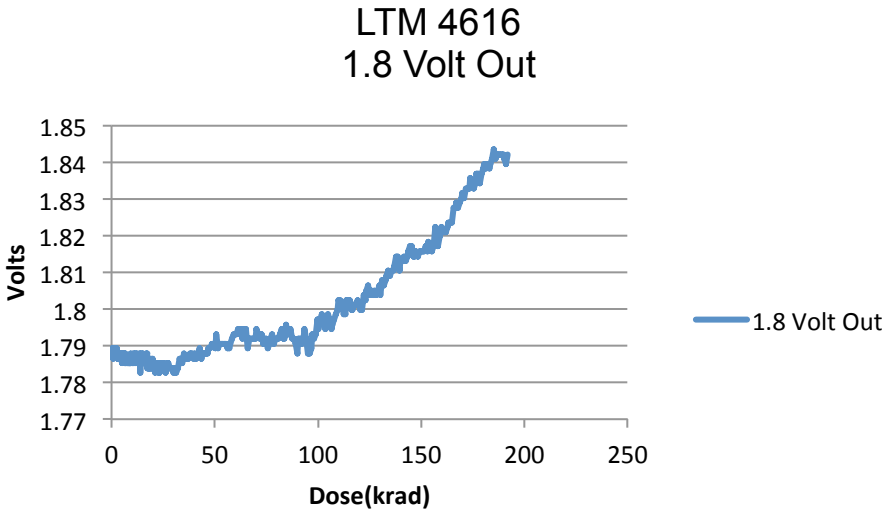


Single ended clock buffer

Irradiation Test of Other COTS Components







Programmable analog delay chip

Point-of-Load power converter

SEU Mitigation of Modern FPGA

Table 1-15: **ESD and Latch-up Data for 7 Series FPGAs**

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO and Special Functions	Transceiver	SelectIO and Special Functions	Transceiver
XC7K325T	Pass	±2,000V	±1,500V	±350V	±300V

Table 1-17: **Real Time Soft Error Rates**

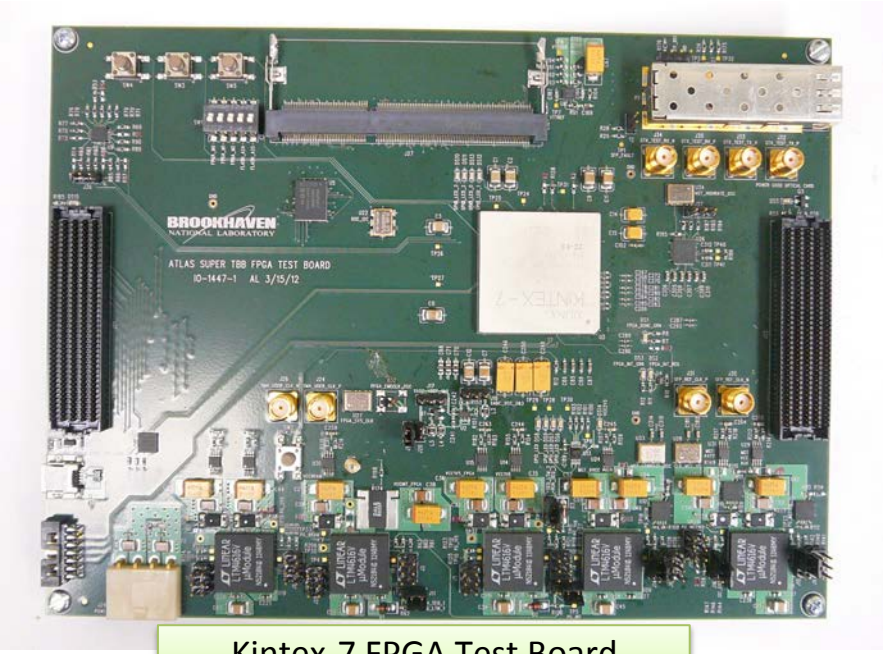
Technology Node	Product Family	Neutron Cross-section per Bit[1]			FIT/Mb (Alpha Particle)[2]			FIT/Mb (Real Time Soft Error Rate)[3]		
		Configuration Memory	Block Ram	Error	Configuration Memory	Block RAM	Error[4]	Configuration Memory	Block RAM	Error[4]
250 nm	Virtex	9.90×10^{-15}	9.90×10^{-15}	±10%				160	160	±20%
180 nm	Virtex-E	1.12×10^{-14}	1.12×10^{-14}	±10%				181	181	±20%
150 nm	Virtex-II	2.56×10^{-14}	2.64×10^{-14}	±10%				405	478	±8%
130 nm	Virtex-II Pro	2.74×10^{-14}	3.91×10^{-14}	±10%				437	770	±8%
90 nm	Virtex-4	1.55×10^{-14}	2.74×10^{-14}	±10%				263	484	±11%
65 nm	Virtex-5	6.70×10^{-15}	3.96×10^{-14}	±10%				165	692	–13% +15%
40 nm	Virtex-6	1.26×10^{-14}	1.14×10^{-14}	±10%	40	100	–50% +100%	101	239	–18% +22%
90 nm	Spartan-3	2.40×10^{-14}	3.48×10^{-14}	±10%				190	373	–50% +80%
90 nm	Spartan-3E Spartan-3A	1.31×10^{-14}	2.73×10^{-14}	±10%				104	293	–80% +90%
45 nm	Spartan-6	1.00×10^{-14}	2.20×10^{-14}	±10%	135	180	–50% +100%	185	389	–14% +18%
28 nm	7 Series FPGAs	6.99×10^{-15}	6.32×10^{-15}	±10%	34	53	–50% +100%	79	31	–27% +40%

28nm Stratix V SER FIT Rate Summary

- SER FIT rates observed at 28nm lower than at 40nm

28nm Stratix V Neutron and Alpha SER FIT Rates (FIT/Mb)		
	Neutron	Alpha
CRAM	69	13
M20K	455	350
MLAB	286	286
Core Register	1 FIT/1000 Reg	1 FIT/1000 Reg
I/O Register	1.2 FIT/10K Reg	1.2 FIT/10K Reg

- No SEL (Single-Event-Latchup) is observed even at 100C (case temperature) @ Vccmax

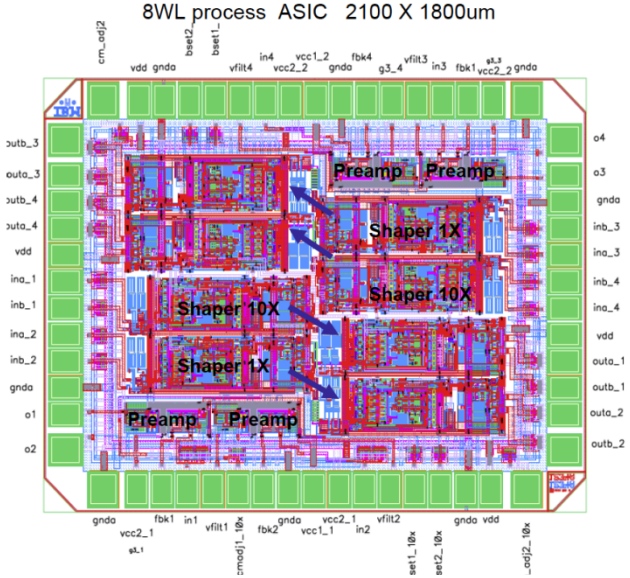


Kintex-7 FPGA Test Board

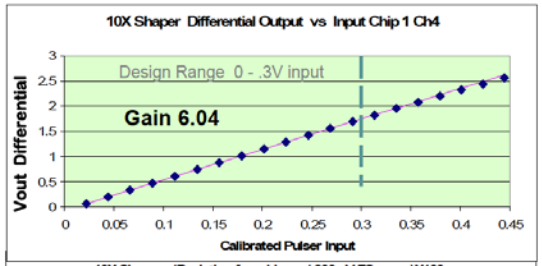
- Modern FPGAs are using smaller feature size
  - Both Xilinx 7-series and Altera Stratix V are 28nm
- FPGAs are more tolerant to total dose, but more sensitive to single event effect
  - Many FPGAs have been tested to be ***SE Latch-Up free***
- SEU can be mitigated by vendor provided features
  - Hardwired on-chip mitigation logics
  - Scrubbing, fault-injection, error tagging and classification features
- FPGAs have great potential to be used in ***accelerator based experiments in radiation environment***
  - Xilinx Kintex-7 FPGA test board is being used to study SEU mitigation techniques

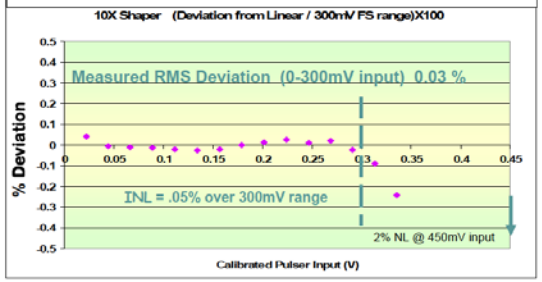
Analog Front-End Development

LAPAS: Liquid Argon PreAmplifier Shaper
8WL process ASIC 2100 X 1800um

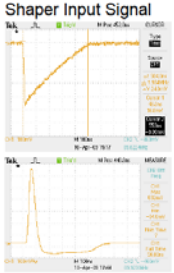


LAPAS ASIC Automated Linearity Measurement
Using AFG3252 & MSO4401

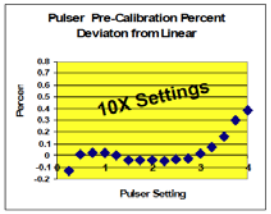




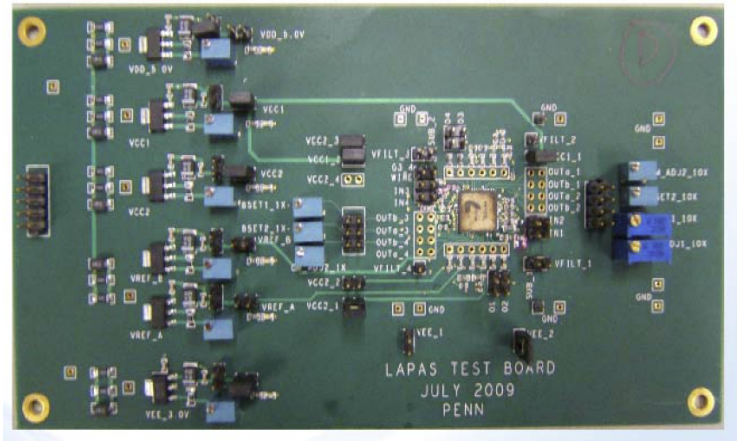
Shaper Input Signal



LAPAS Shaper Output

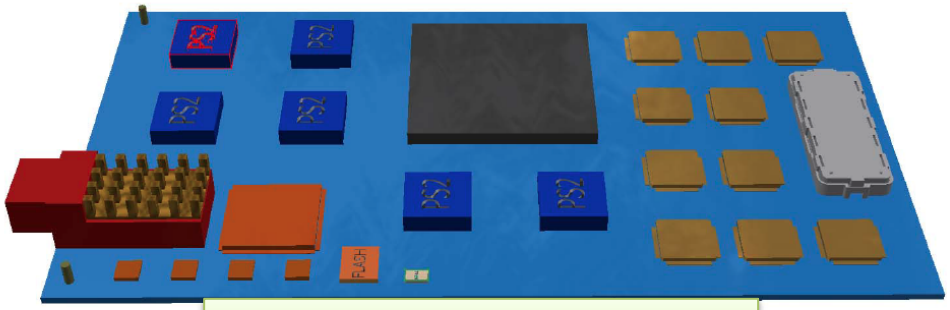


Test Printed-Circuit Board

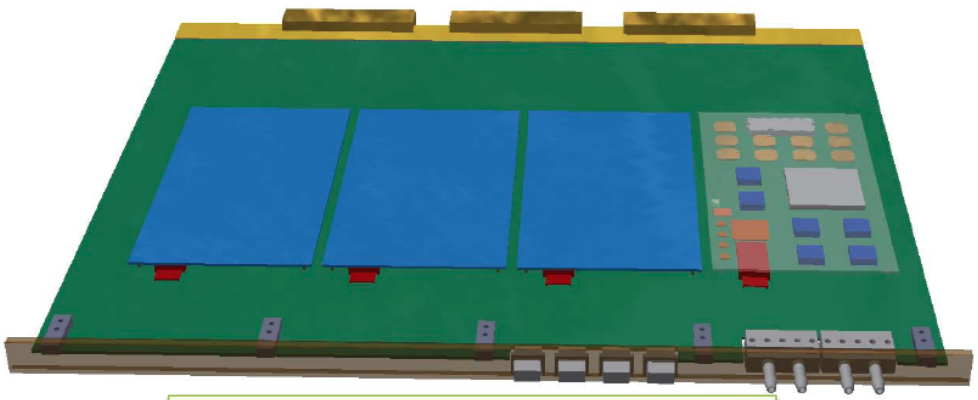


- LAPAS ASIC
  - Quad preamplifier & shaper ASIC in 0.13um SiGe 8WL
  - Joint development of BNL and Upenn for Phase-II Upgrade
- Preamplifier
  - Based on low noise line-terminating preamplifier circuit topology used presently
  - High breakdown devices allow for higher swing to accommodate full ***16-bit dynamic range***
  - e_n ~ 0.26nV/√Hz
  - ENI ~ 73nA RMS (included 2nd stage and for C_d = 1nF)
  - P_{tot} ~ 42mW
- Shaper
  - ***16-bit dynamic range*** with two gain settings
  - e_n ~ 2.4nV/√Hz
  - ENI ~ 34nA RMS
  - P_{tot} ~ 130mW (combined 1X, 10X channels)
  - Uniformity: better than 5% across 17 tested ASICs
  - INL: < 0.1% over full scale of 1X and 10X channels

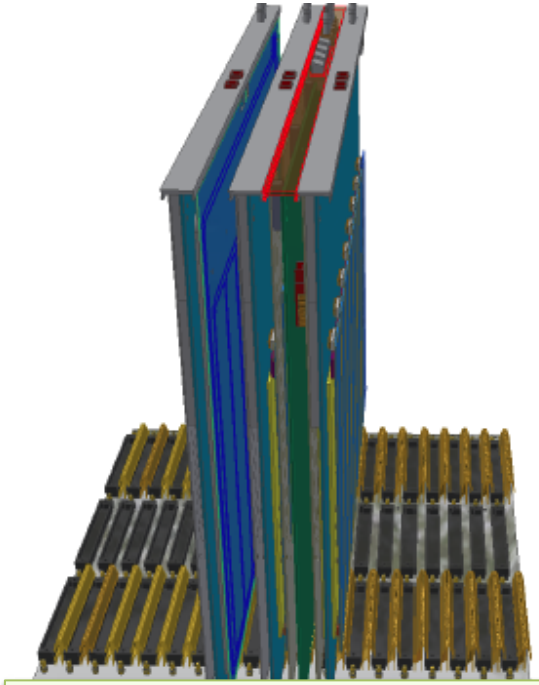
Development of LTDB



¼ Slice Digital Mezzanine Card



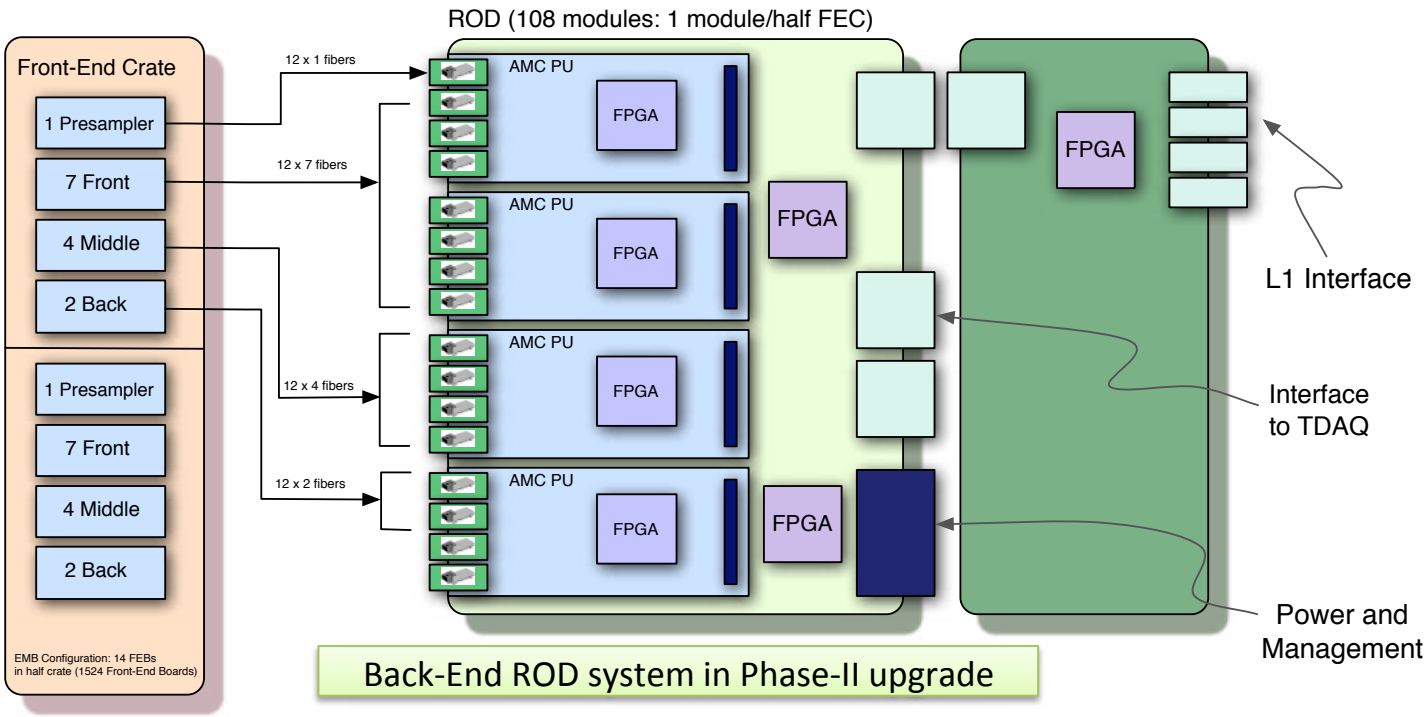
LTDB with four ¼ slice mezzanines



LTDB plugged on baseplane

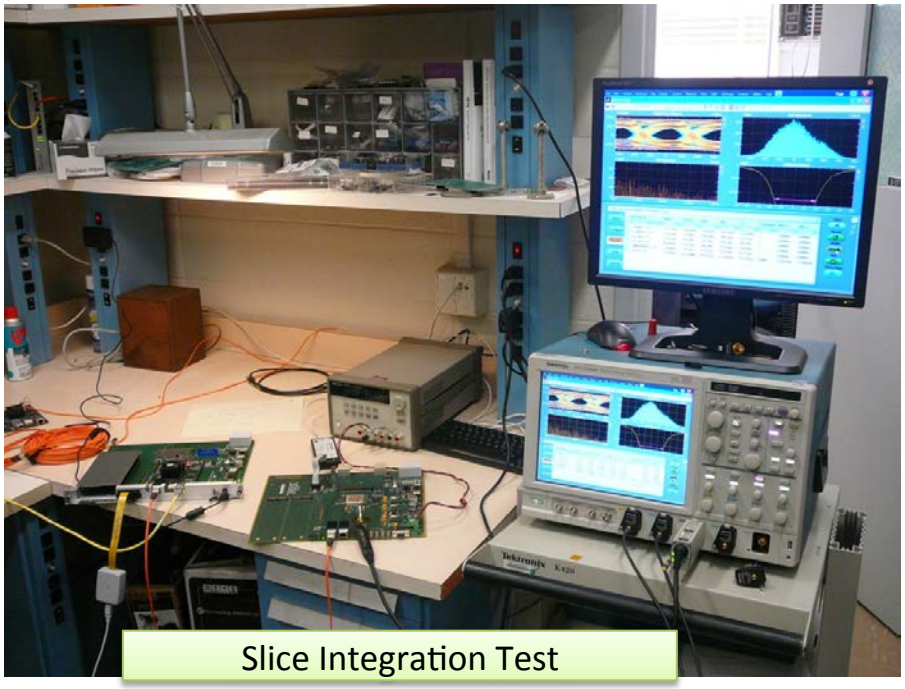
- LAr Phase-I Upgrade front-end development
  - LTDB can process up to 320 channels of super cell signals
  - LTDB mother board with ¼ Slice digital mezzanine card and integrated analog blocks
  - ~***200Gbp***s bandwidth for continuous digital trigger signal readout
- Initial demonstrator design is based on COTS component
  - TI ADS5272 ADC
  - Xilinx Kintex-7 XC7K325T FPGA
  - Avago PPOD
- Many technical challenges are being tackled
  - Mechanical, Powering and Cooling

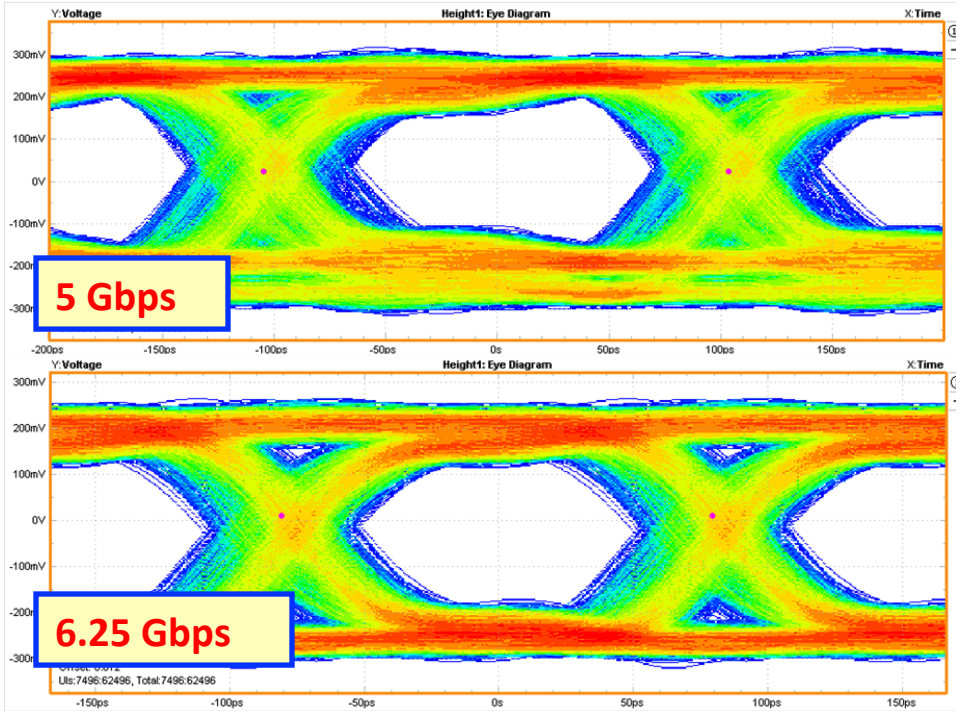
Back-End Development



- ROD R&D for LAr Calorimeter Phase-II Upgrade
  - Data bandwidth of entire LAr w. 1524 FEBs > ***150Tbps***
  - High speed parallel fiber optical transceiver (e.g. 12 fibers @ 10Gbps)
  - Address issues of bandwidth and achievable integration on the ROD
  - ROD based on FPGA high speed SERDES and FPGA based DSP to take advantage of parallel data processing
  - Perform trigger sum digitally after E-conversion with flexible and finer granularity within a realistic latency budget
- ROD development shares many ***common*** features with DPS in Phase-I Upgrade
  - Large data transmission over parallel optical links
  - Real time parallel data processing in modern FPGA
  - Industrial standard platform (ATCA, AMC etc.)

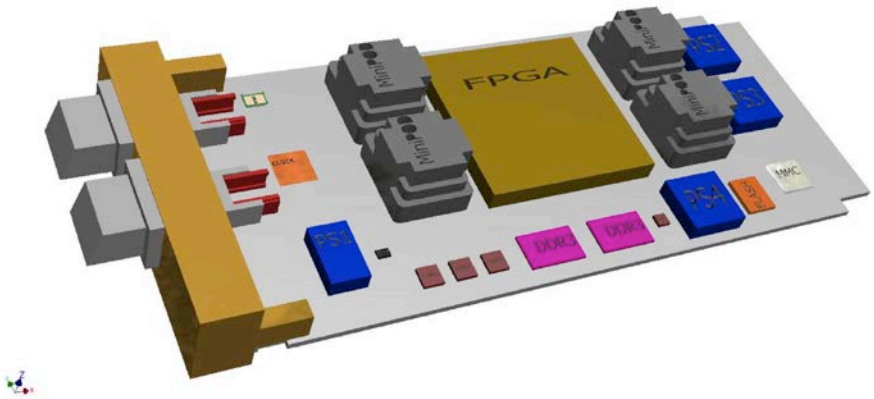
ATCA Sub-ROD Development

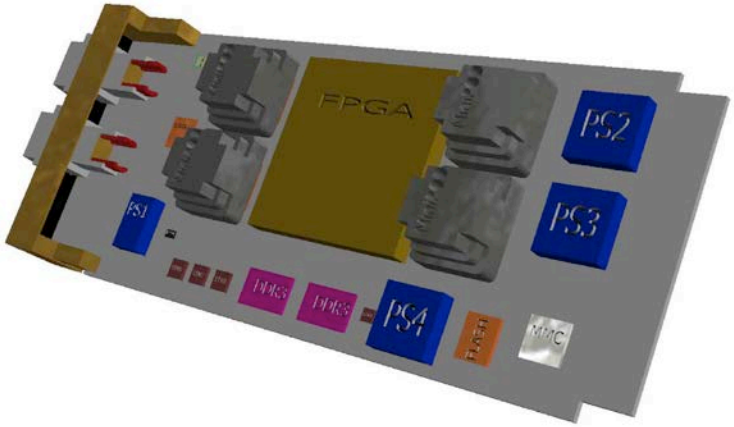


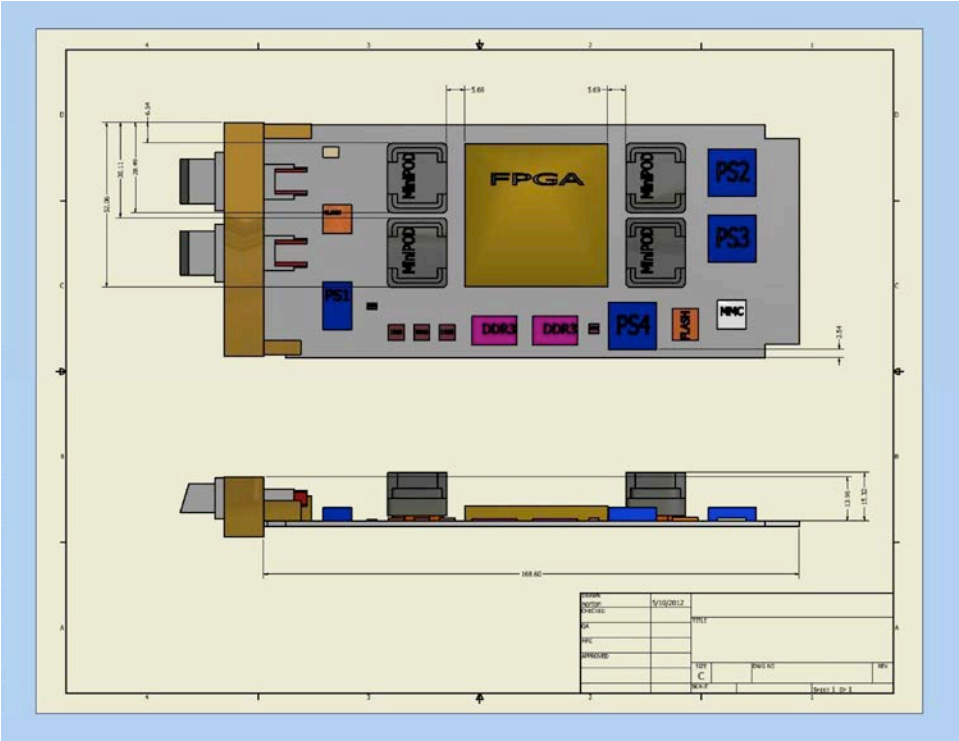


- Sub-ROD Development
  - ATCA form factor
  - 75Gbps parallel fiber optic links
  - FPGA SERDES: Xilinx Virtex 5 FX on Sub-ROD
  - Injector was designed by UAZ
- Slice integration test
  - SNAP-12 parallel optical transceiver from Emcore and Reflex Photonics
  - BERT from 2.4 to 6.25Gbps per link
  - Used as test stand for latency study and firmware development for interface to ROS

AMC sPU Development



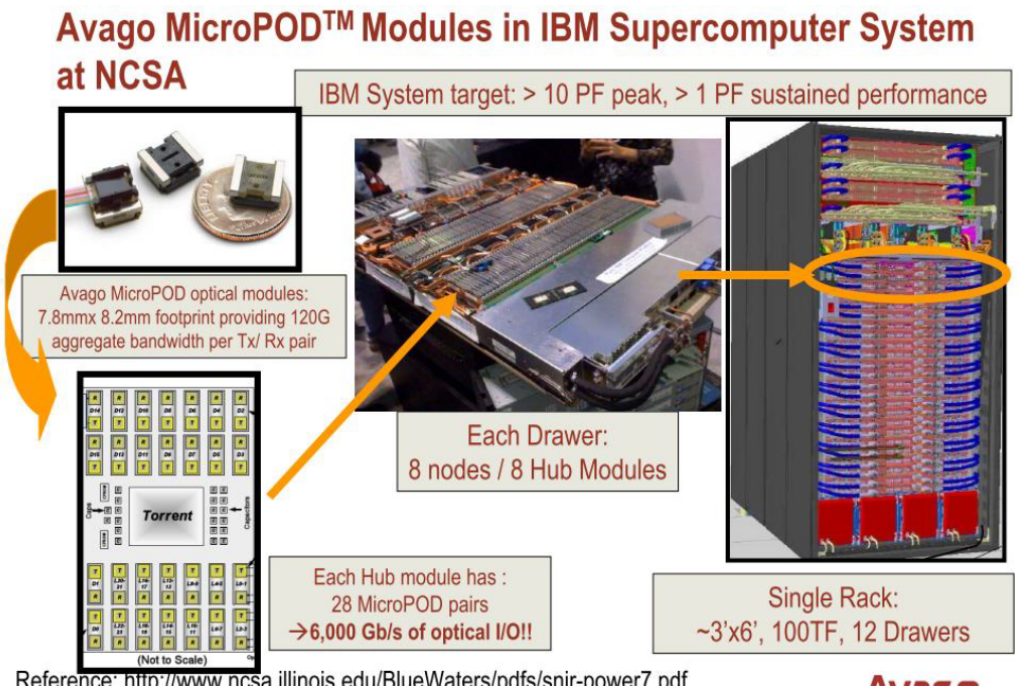


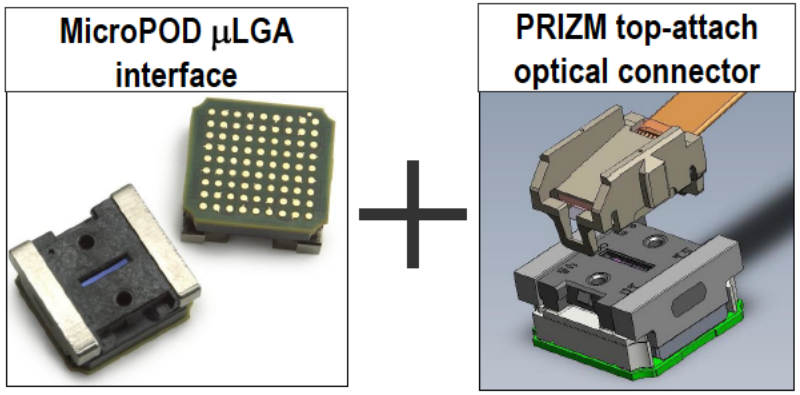


AMC sPU with Avago MiniPOD

- AMC module can be developed and tested in a low cost MicroTCA crate or on an ATCA carrier board
  - Modular design fits both Phase-I upgrade DPS and Phase-II upgrade ROD systems
  - Flexibilities for testing and maintenance
- Design with Avago MiniPOD
  - 4 MiniPODs (4x12 10Gbps) can be mounted on one AMC module
  - Optical transmitters are required to interface to L1Calo FEX from DPS
  - Stacking height of MiniPOD with FCI 55714 9x9 MEG-Array socket exceeds what mid-size face plate can cover
- Pursuing sPU design with Avago MicroPOD for ***higher density***

AMC sPU Development





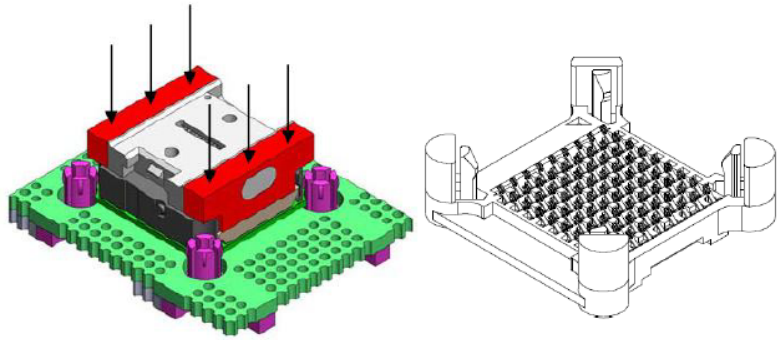
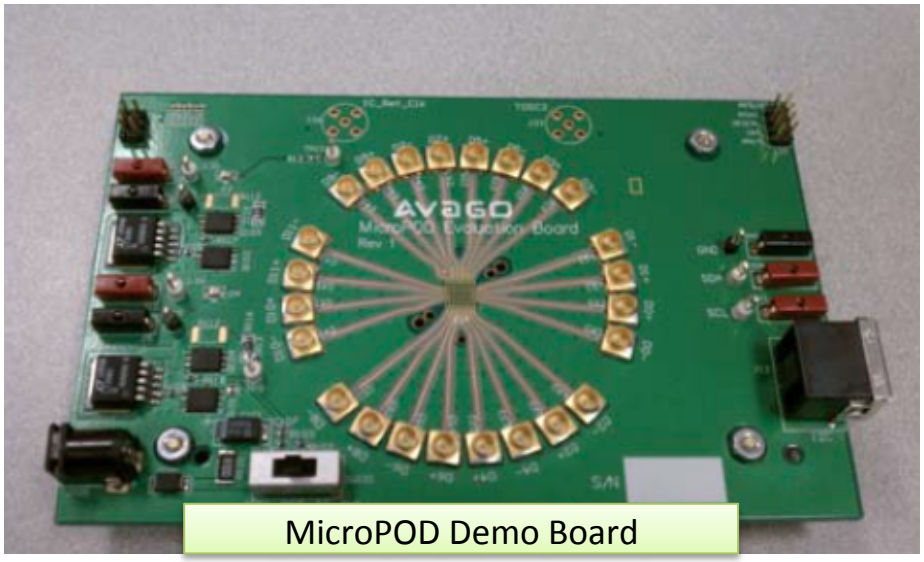


Illustration of force applied to MicroPOD in LGA socket

Example of µLGA interposer

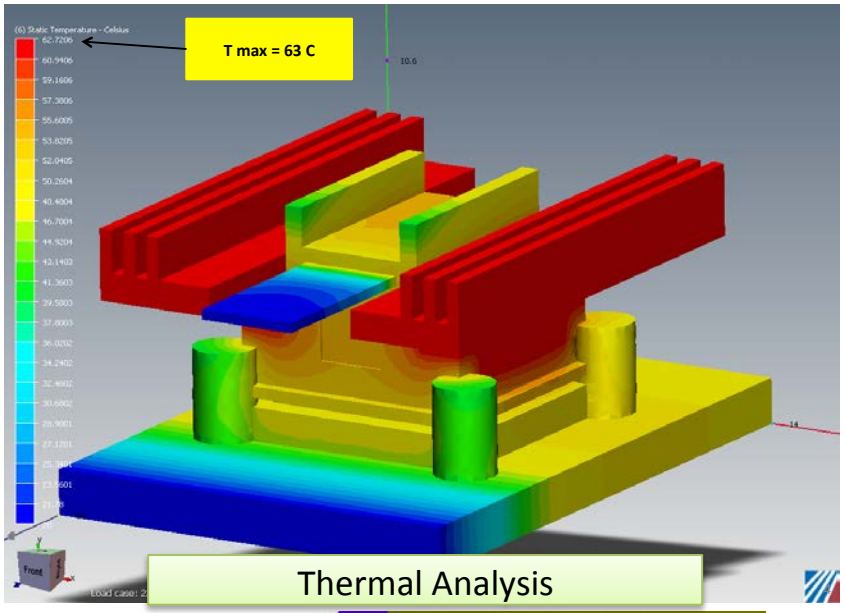
- MicroPOD has been used by other customers successfully (IBM etc.)
- MicroPOD is a nice choice of AMC sPU module
  - Large volume of data transmission with very small footprint
- ***However***
  - Very challenging in both mechanical and electrical designs
  - Cooling assembly needs to be developed

AMC sPU Development

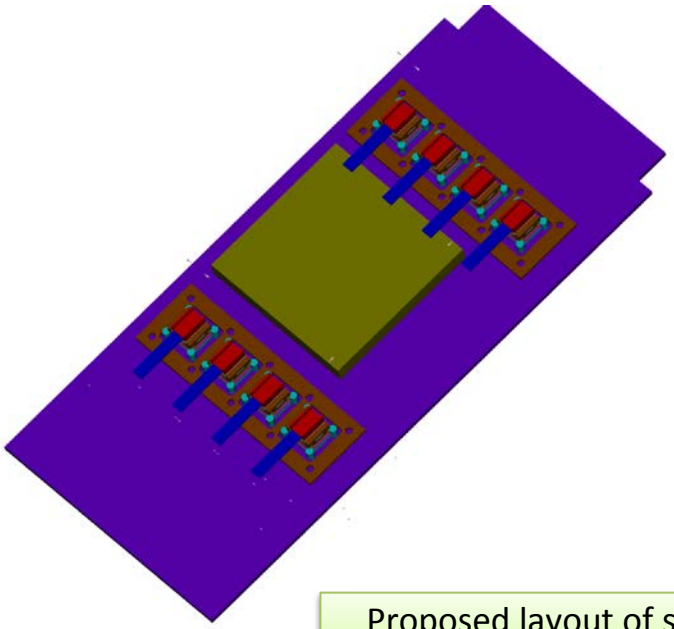


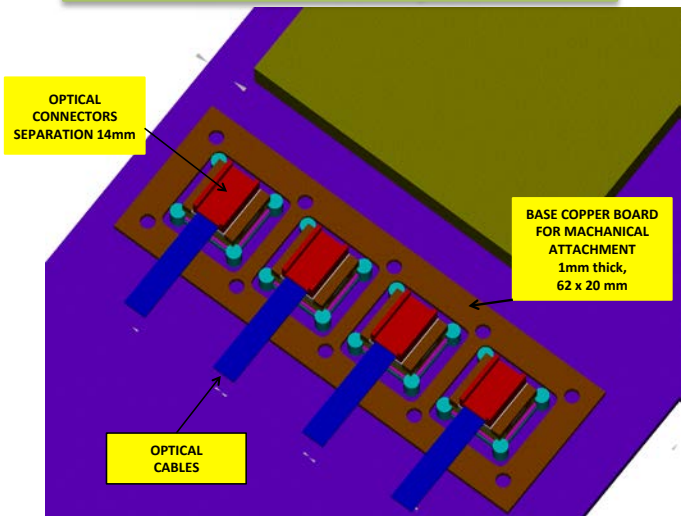
MicroPOD Demo Board

TOTAL POWER GENERATED = 0.8 W, AIR FLOW = 200mm/sec



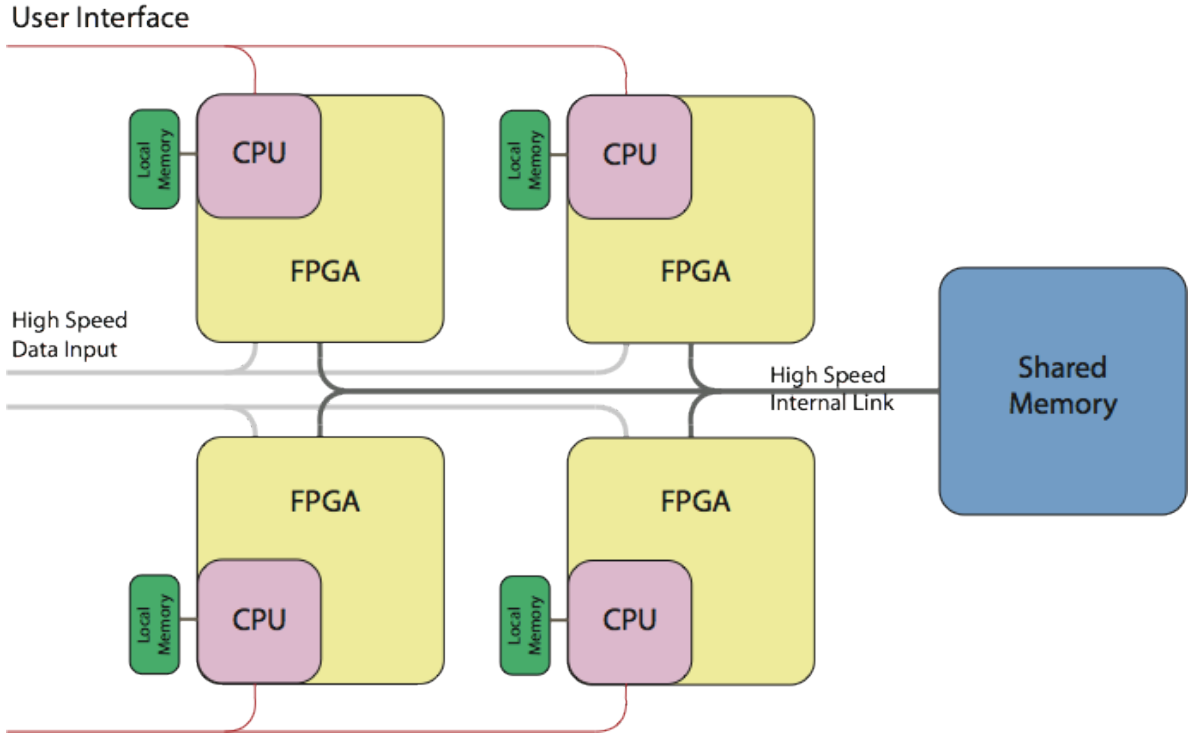
Thermal Analysis

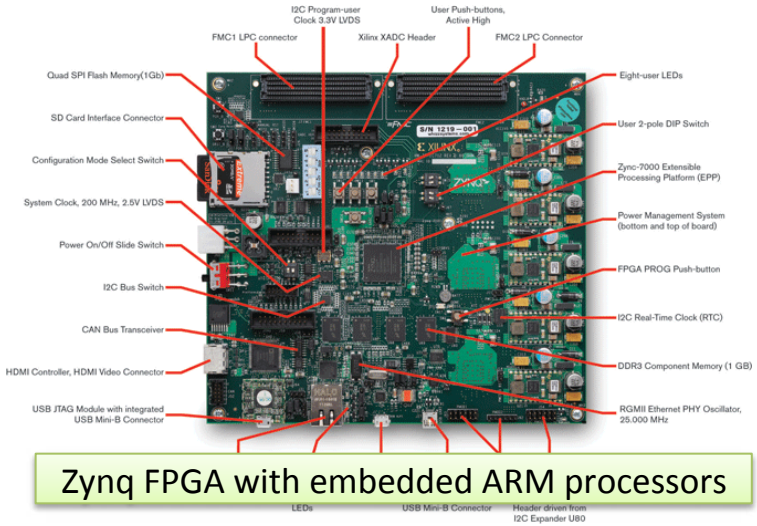




Proposed layout of sPU with ***eight*** MicroPODs

Extensible Computing Platform





Zynq FPGA with embedded ARM processors

- Extensible computing platforms, are integrated circuits that blends CPUs and FPGAs
- We aim to develop a scalable hybrid reconfigurable computer/conventional CPU
  - The user interaction is done via traditional CPUs
  - Data processing is done on FPGAs
- It has great potentials to be used in particle physics experiment
  - High level trigger farm
  - Trigger less DAQ system
- Initial test is based on Xilinx ZC702 evaluation board
  - ARM dual-core Cortex-A9 processor meets Xilinx 28nm programmable logic