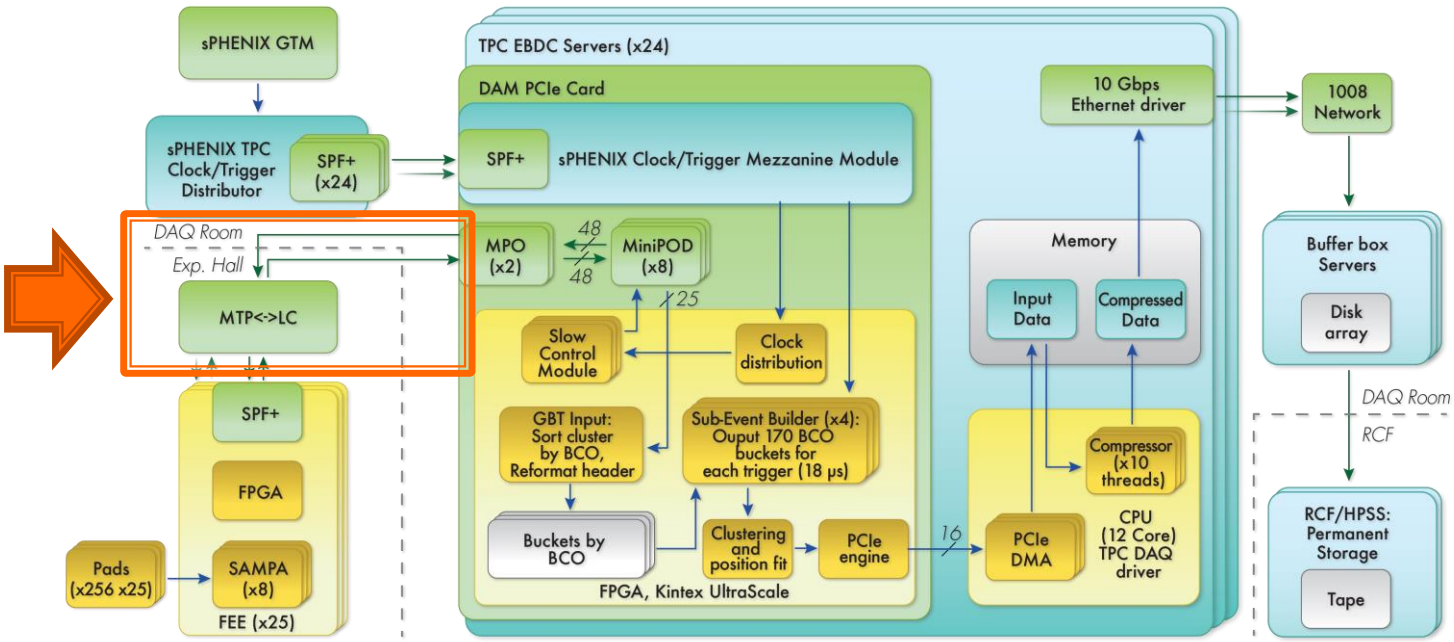
TPC DAM <-> FEE Cabling

Jin Huang (BNL)

Diagram

Live write up drafts online:
Rate estimation: https://docs.google.com/spreadsheets/d/1Q_uYf00_8pushSiYns29T_-ThIOqQaqpKbVS_LDqlAg/edit?usp=sharing
Data format: https://www.overleaf.com/read/wttbwnnynqwb



24 sectors, 144k Pads and 600 FEEs in total
1 sector, 25 FEEs per DAM for readout

Item			Rate Per unit		
	Unit	Count	Limit/Unit	Average/Unit	Max C./Unit
FEE SAMPA data	Gbps	4,800	1.28	0.20	0.51
FEE GBT fiber	Gbps	600	3.20	1.56	2.03
FPGA Input	Gbps	24	80.00	39.12	
Build hit - time table	Gbps	24	200.00	40.23	
After triggering	Gbps	24	200.00	11.47	
After clustering fitting	Gbps	24	101.70	5.73	
FPGA -> PCIex16 -> DMA	Gbps	24	101.70	5.73	
Lossless Compression	Gbps	24	4.80	3.44	
Server output to 1008 network	Gbps	24	10.00	3.44	
Buffer box servers	Gbps	1	120.00	82.56	

- Main update: cluster fitting in FPGA
- Necessary to bring down final data rate to 83 Gbps (<120Gbps)
- Quoting expectation of 50% reduction (~150bit/cluster->~72bit/cluster in payload)
- Need to support unfit and fit output in order to
- Operation can start with raw-hit output, switch to raw-hit + cluster-fit output later in operation

Cabling concept

TPC backplane <1 m> on sector patch panel <58 m> DAQ room

25 FEE with SFP / sector

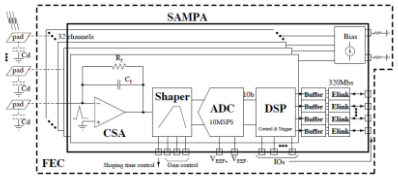
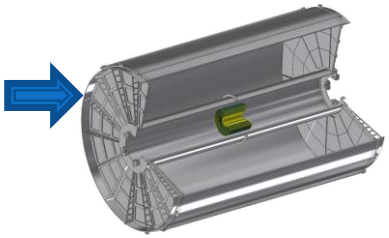


Figure 6.4: Schematic of the SAMPA ASIC for the GEM TPC readout, showing the main building blocks.

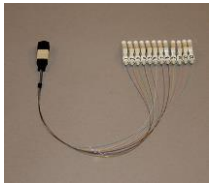


1 FELIX / sector

25 LC duplex
On FEEs

Option 1:
LC Duplex Uniboot

MTP (M) -> LC bare
+ coupler



58 M MTP fiber
72F, (F-F)

Option 1:
MTP, 72F (M)

Manufacture suggest to avoid:
High cost and high failure rate

MTP (M) -> LC Cassettes

Option 2:
MTP 12F (M) -> 6x LC

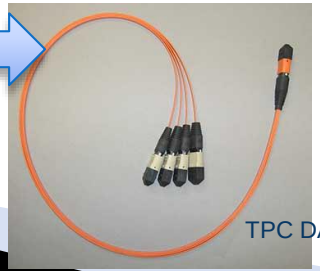
58 M MTP fiber
48F, (F-F)

Option 2:

MTP, 48F (M)

MTP, 48F (M)

MTP (M) -> MTP 12F (F)



Cabling options:

Counts are per-sector

On FEE (25 FEE/sector)	FEE <-> backplane (1 m)	On TPC backplane	TPC <-> FELIX (58 m)	FELIX (Need 50/96 Fiber IO)
25x LC duplex	5x (12-F MTP (M) <-> 6x LC duplex) Breakout cable or cassettes	72-F MTP (M) <-> 6x 12-F MTP (F) breakout cable	72-F MTP (F) <-> 72-F MTP (F)	72-F MTP (M) <-> 6x MiniPOD
25x LC duplex	LC duplex <-> LC duplex uniboot	72-F MTP (M) <-> 36x LC duplex bare or cassettes	72-F MTP (F) <-> 72-F MTP (F)	72-F MTP (M) <-> 6x MiniPOD
25x LC duplex	5x (12-F MTP (M) <-> 6x LC duplex) Breakout cable or cassettes	(48-F MTP (M) <-> 4x 12-F MTP (F) breakout cable) x2	(48-F MTP (F) <-> 48-F MTP (F)) x2	(48-F MTP (M) <-> 4x MiniPOD) + (48-F MTP (M) <-> 2x MiniPOD)
25x LC duplex	LC duplex <-> LC duplex uniboot	(48-F MTP (M) <-> 24x LC duplex bare or cassettes) x2	(48-F MTP (F) <-> 48-F MTP (F)) x2	(48-F MTP (M) <-> 4x MiniPOD) + (48-F MTP (M) <-> 2x MiniPOD)

Extra Information

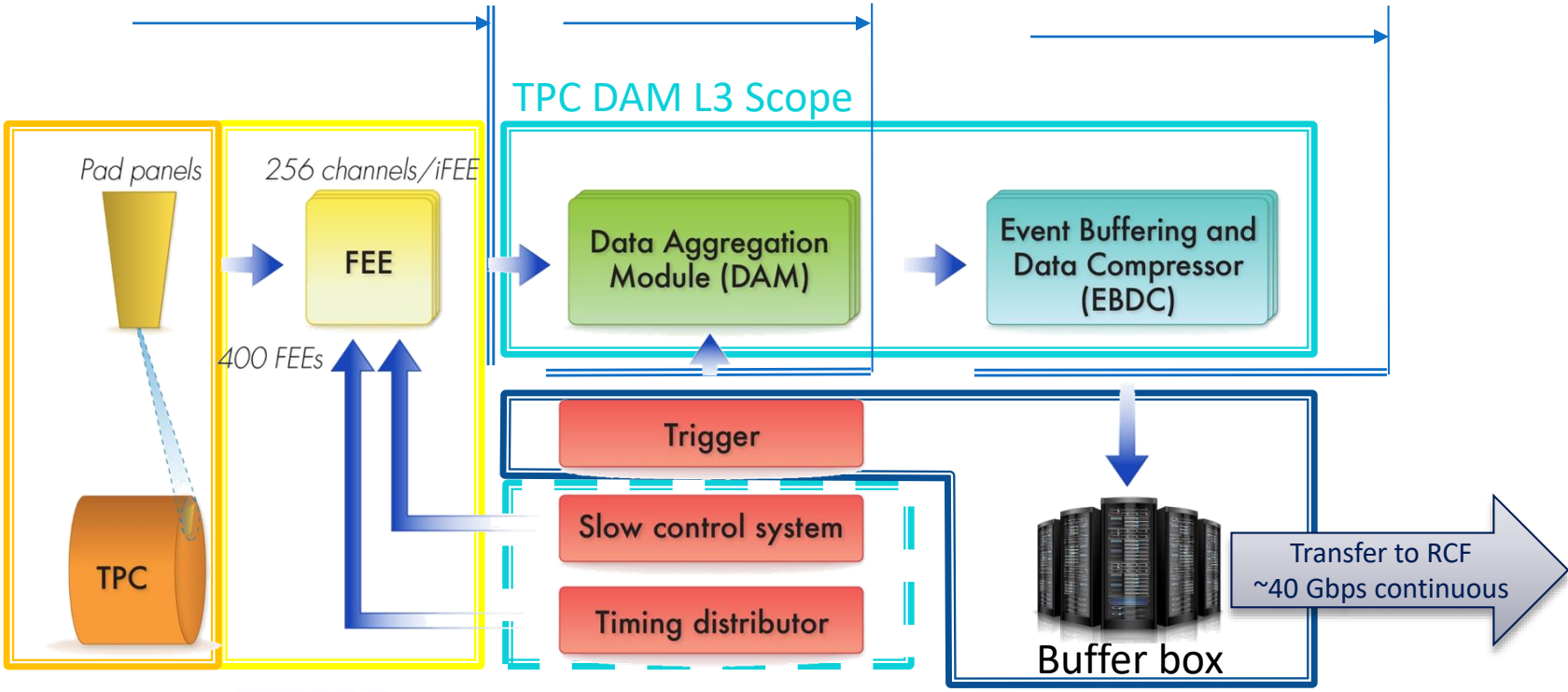
Envelop parameters for TPC DAM

Proposed KPP: demonstrate readout simulated data @ 1.56 Gbps x 600 fibers @ >99% LT

Input data stream:
600 4-Gbps fibers total
Max continuous: 2.87 Gbps / fiber
Average continuous: 1.43 Gbps x 600 fibers

Clock/Trigger input:
Fiber, protocol TBD
Clock = 9.4 MHz
Trigger Rate = 15 kHz

Output data stream to buffer box:
N x 10 Gbps Ethernet via fiber (N=10-50)
Total continuous limit: <120 Gbps (?)
i.e. 3x (Transfer rate to RCF ~ 40 Gbps)



Structure/ GEM L3 Scopes

FEE L3 Scope

Possible TPC DAM L3 Scope

DAQ L2 Scope

FPGA Choices

(a) PCie40.

CRU/ PCIe40

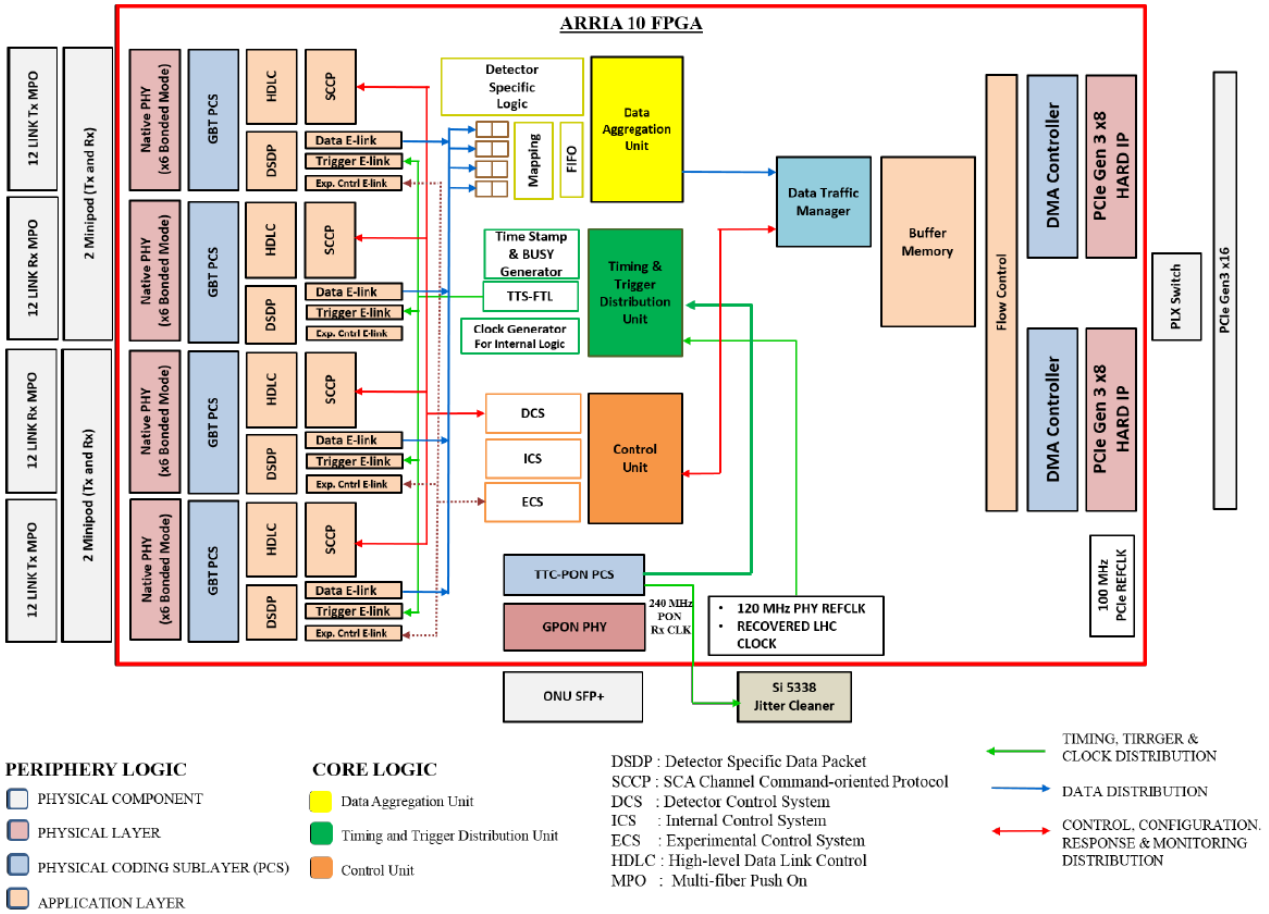
FELIX

FPGA Family Name	Xilinx Virtex 6	Altera Stratix V GX	Xilinx Virtex 7	Altera Arria 10 GX **	Xilinx Virtex Ultrascale	Altera Stratix 10	CRU Requirements #	Xlinux Kintex Ultrascale
Status		available	available	ES available from Q2'15	available	end of 2017		**Available**
FPGA part number	XC6VLX240T	5SGXEA7	XC7VX690T	**10AX115**	XCVU190	10SG280		**XCKU115**
Used in	C-RORC	AMC40	MP7	**PCIe40**				**FELIX v1.5 test boards**
Logic Elements / Cells [M]	0.241	0.622	0.693	1.15	1.9	2.8		**1.451**
FFs [M]	0.3	0.939	0.866	1.7	2.14			**1.3**
LUTs [M]	0.15	0.235	0.433	0.425	1.07			**0.66**
18/20 Kb RAM Blocks	832	2560	2940	**2713**	7560	11721	**1920 / 2560**	**4320**
Total Block RAM (Mb)	15	50	53	**53**	133	229	**40 / 53**	**75.9**
≥ 10 Gb/s Transeivers	24	48	80	**96**	60	144	**48**	**(48 input + 48 output fiber links in FELIX)**
PLLs	12	28	20	32	60	48		**48**
PCIe x8, Gen3	2 (Gen2)	4	3	4	6	6		**6**

TPC Detector is the majority user (>70%) of CRU boards. CRU requirements is measured against TPC detector specific logic occupancy.

** Altough the maximum number of links of the Arria10 family is 96 links, the FPGA equiping the PCIe40 board has only 72 links

CRU diagram


ARRIA 10 FPGA
12 LINK Tx MPO
12 LINK Rx MPO
12 LINK Rx MPO
12 LINK Tx MPO
2 Minipod (Tx and Rx)
2 Minipod (Tx and Rx)
Native PHY (x6 Bonded Mode)
GBT PCS
HDLC
DSDP
SCCP
Data E-lirk
Trigger E-link
Exp. Cntrl E-link
Detector Specific Logic
Mapping
FIFO
Data Aggregation Unit
Time Stamp & BUSY Generator
TTS-FTL
Clock Generator For Internal Logic
Timing & Trigger Distribution Unit
DCS
ICS
ECS
Control Unit
TTC-PON PCS
GPON PHY
240 MHz PON Rx CLK
120 MHz PHY REFCLK
RECOVERED LHC CLOCK
ONU SFP+
Si 5338 Jitter Cleaner
Data Traffic Manager
Buffer Memory
Flow Control
DMA Controller
PCIe Gen 3 x8 HARD IP
100 MHz PCIe REFCLK
PLX Switch
PCIe Gen3 x16
PERIPHERY LOGIC
PHYSICAL COMPONENT
PHYSICAL LAYER
PHYSICAL CODING SUBLAYER (PCS)
APPLICATION LAYER
CORE LOGIC
Data Aggregation Unit
Timing and Trigger Distribution Unit
Control Unit
DSDP : Detector Specific Data Packet
SCCP : SCA Channel Command-oriented Protocol
DCS : Detector Control System
ICS : Internal Control System
ECS : Experimental Control System
HDLC : High-level Data Link Control
MPO : Multi-fiber Push On
TIMING, TIRRGER & CLOCK DISTRIBUTION
DATA DISTRIBUTION
CONTROL, CONFIGURATION, RESPONSE & MONITORING DISTRIBUTION

SAMPA/STAR iFEE

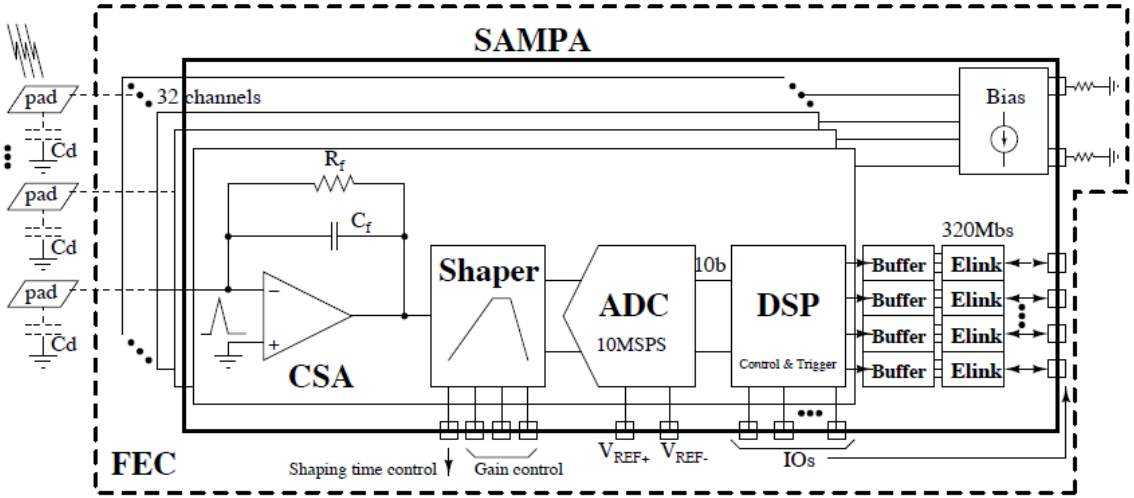
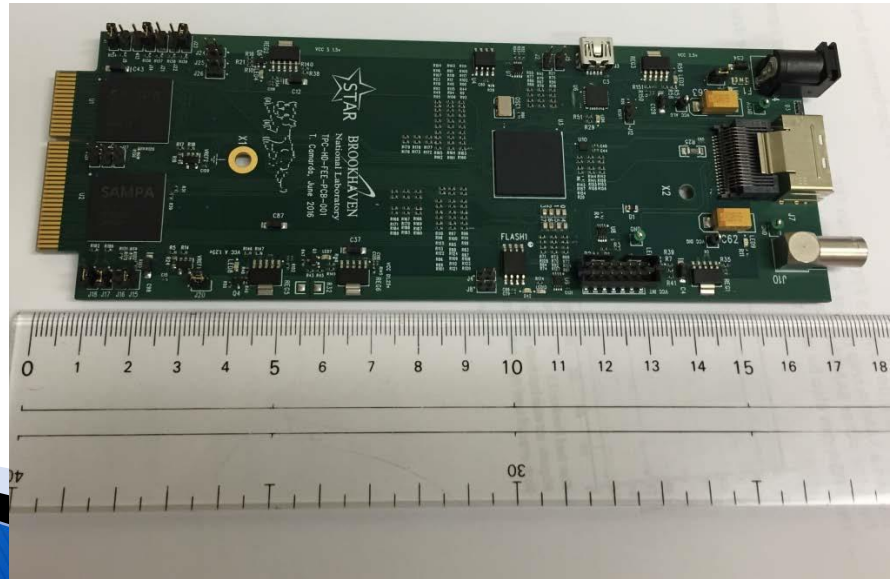



Figure 6.4: Schematic of the SAMPA ASIC for the GEM TPC readout, showing the main building blocks.