LAr Phase II Upgrade Interests

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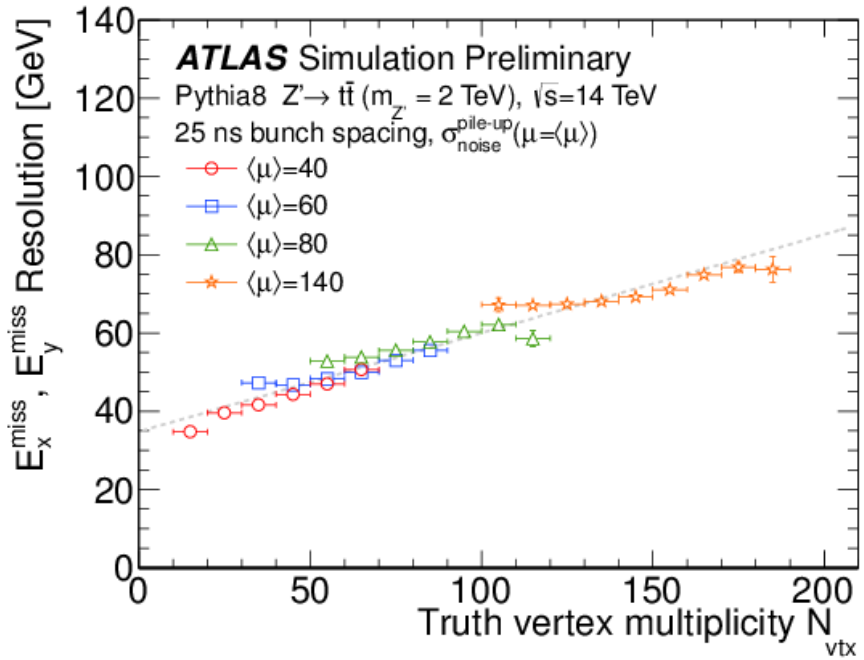
Phase-II LAr Backend Electronics Meeting
September 24, 2015

Physics Motivation

- MET triggers are essential to searches for new physics, in addition to benchmark physics processes
  - Any hint of new physics in Runs 2 or 3 must be investigated in detail & corroborated through complementary channels
- Jet substructure is likely to become increasingly important as a means to control rates for large-R jet triggers
- Calorimeter Triggers in Phase-II
  - Pileup mitigation in a harsh environment (up to μ=200) is critical to maintain the jet/MET trigger performance
  - The forward region is particularly challenging (sFCal?)
  - L1Global is especially important in the *low* & *middle* scenarios where the L1 rate is limited to 200 kHz

Topocluster-like Processing

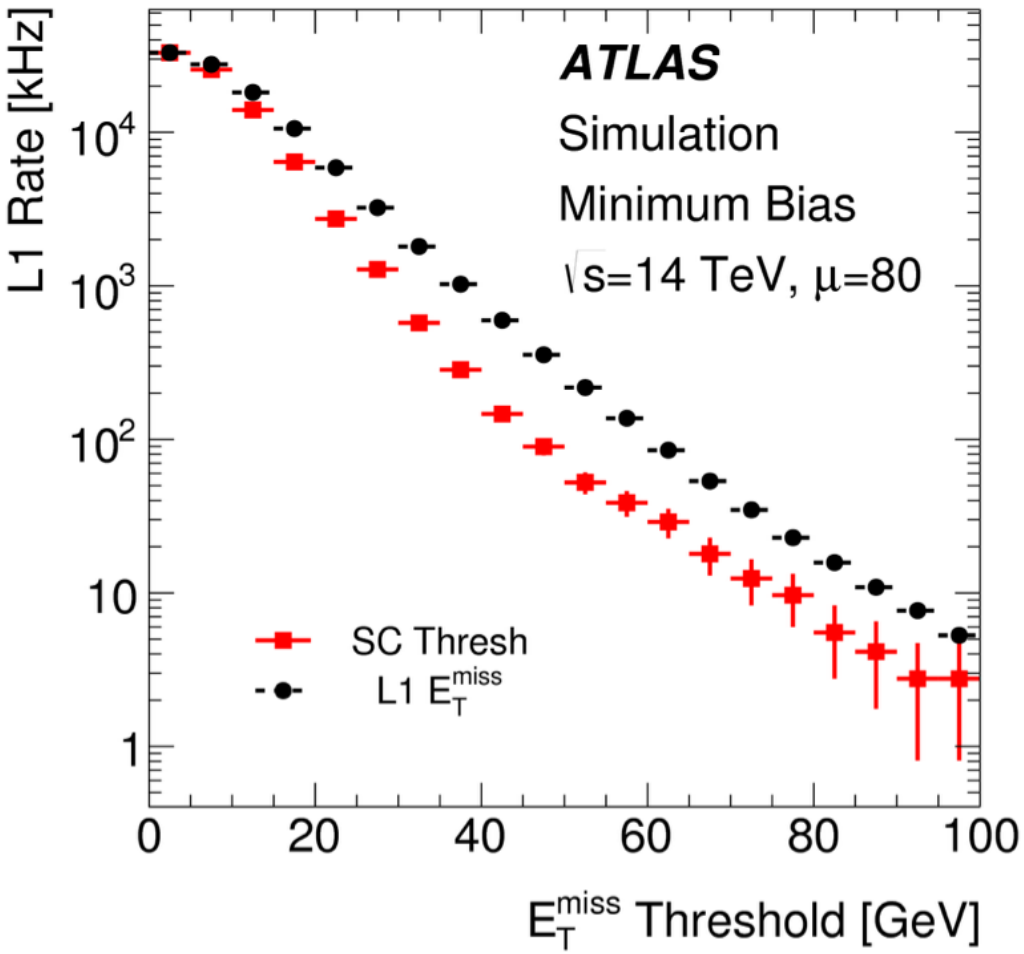
- Topoclustering has proven especially effective against pileup in offline jet reconstruction and in the HLT (EF) in Run 1 (2)
- $E_{x,y}^{miss}$ resolution increases linearly wrt the number of truth vertices, but is **independent of μ**
- σ_{noise} includes electronic ⊕ pile-up



https://twiki.cern.ch/twiki/bin/view/AtlasPublic/JetEtmissApproved2013HighMuEtmiss

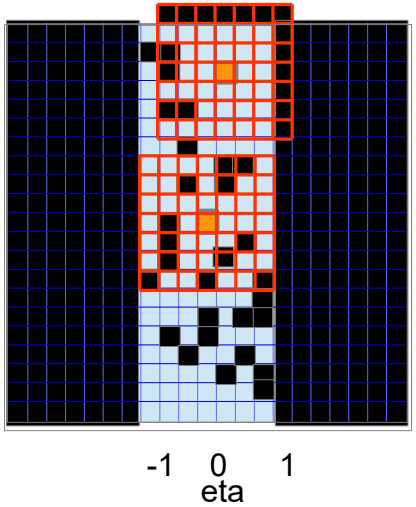
Topocluster-like Processing

- LAr Phase-I TDR Study only includes supercells in MET calculation if middle LAr layer satisfies $|E| > 2\sigma$
- ~20 GeV reduction in MET threshold for same rate ($|\eta| < 4.9$)
- "Easy" to implement in LAr DPS or after L1 Accept, even in Phase I [assuming FPGA resources]



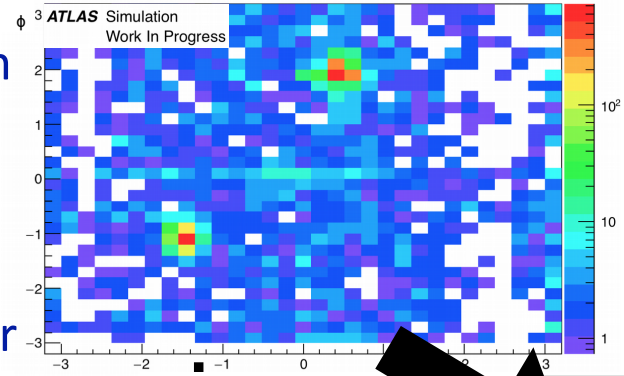
Possible Implementation(s)

- Potential granularities:
  - coarse (0.1x0.1 or 0.2x0.2) towers in (super?)FEXs
  - over LAr SuperCells, before or after L0 accept
  - over full granularity (high data volume!), before or after L0 accept
- R&D Stage (recent MSU involvment):
  - investigating range of granularities in simulation, benchmarking against offline topoclustering & jet/MET trigger performance (see next slide)
  - development of analogous non-sequential algorithm suitable for implementation in FPGA (& feedback to understand impact on performance) C. Dudley (Oregon), P. Plucinski (MSU)

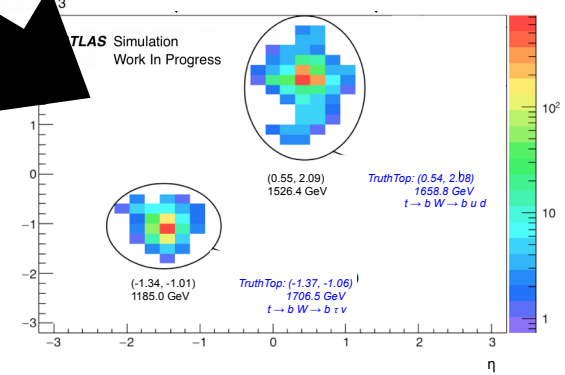


Standalone Algorithm Development

- 2-D topoclustering algorithm implemented in standalone simulation over coarse (0.2x0.2) granularity
- Simple local maximum finder in lieu of split/merge
- Fixed threshold optimization performed; relative threshold (using noise) optimization in progress

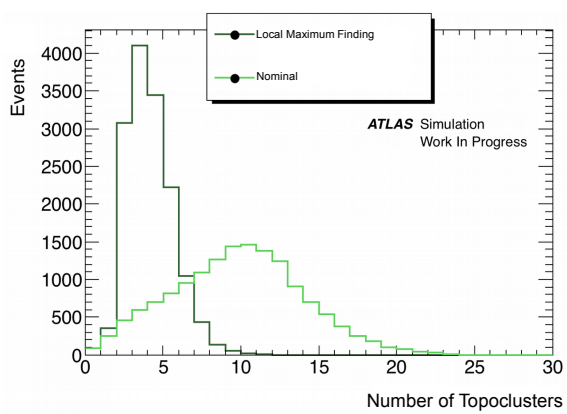


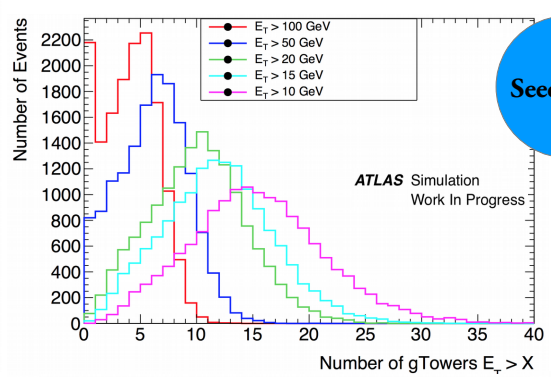
Oregon undergrads:
Luc Lisi,
Elliot Parrish,
Brianna Stamas

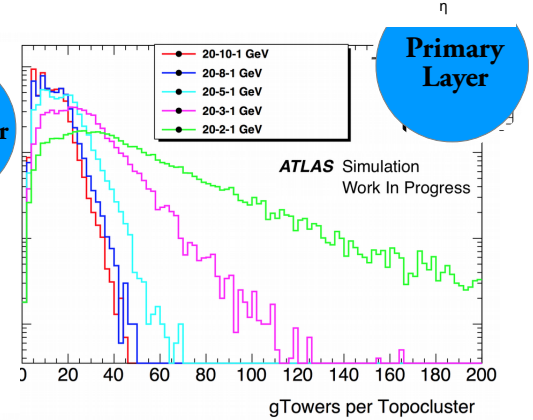


$Z' (5\ TeV) \rightarrow t\,\bar{t}$

$\langle\mu\rangle = 80$

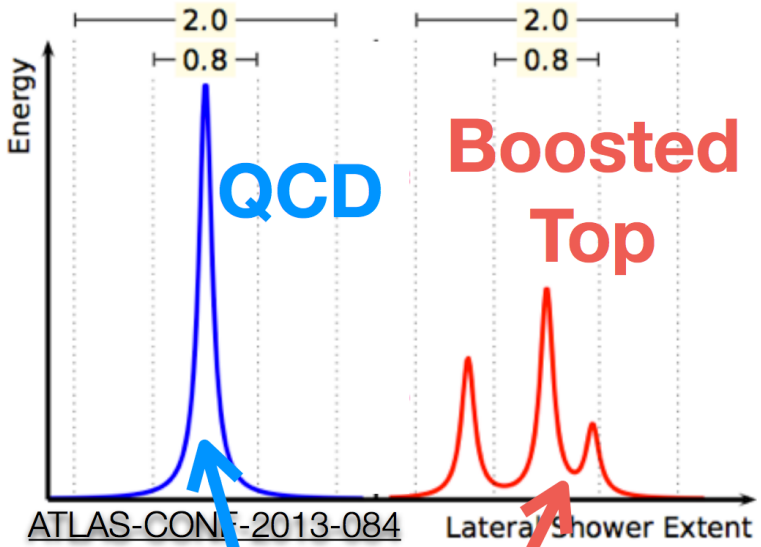






Jet Substructure in FEX System

- In addition to MET trigger applications, topoclusters can provide a natural input to jet substructure identification algorithms
  - Input to (or calculation in) Phase-1 or Phase-2 gFEX provides a powerful background rejection tool.
  - Ideally clustering is performed at finest available granularity & at 40 MHz
- Seeding topoclusters to jFEX/gFEX algorithms also provides potential for improved tau identification



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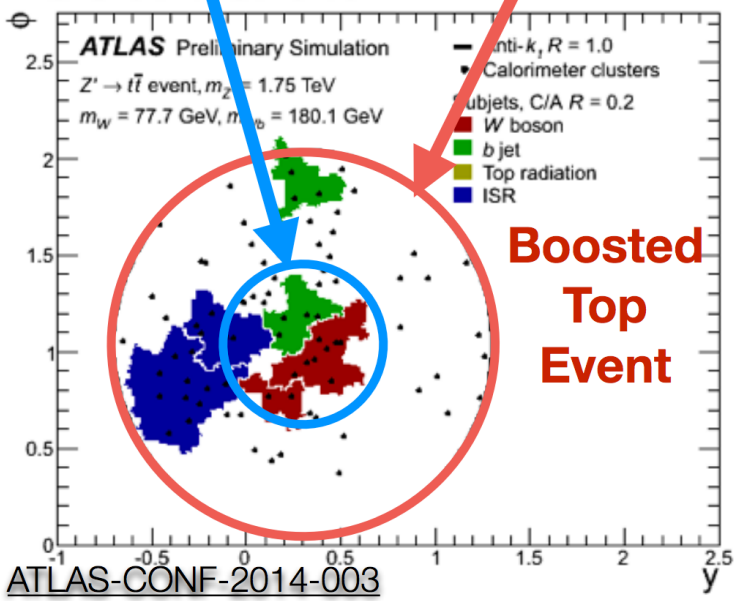

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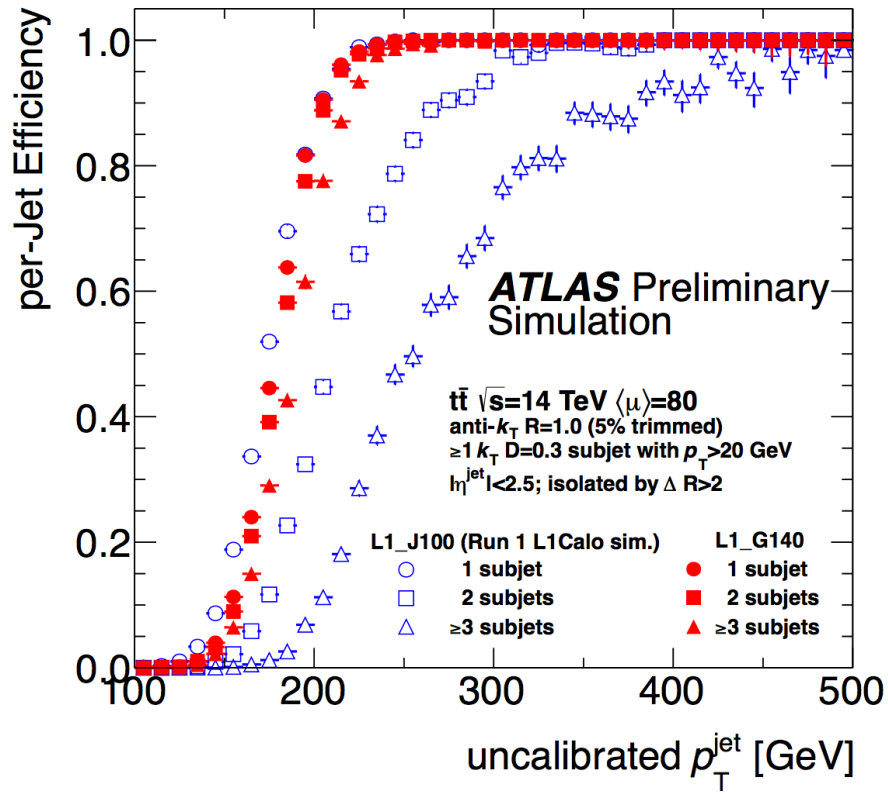
Jet Substructure in FEX System

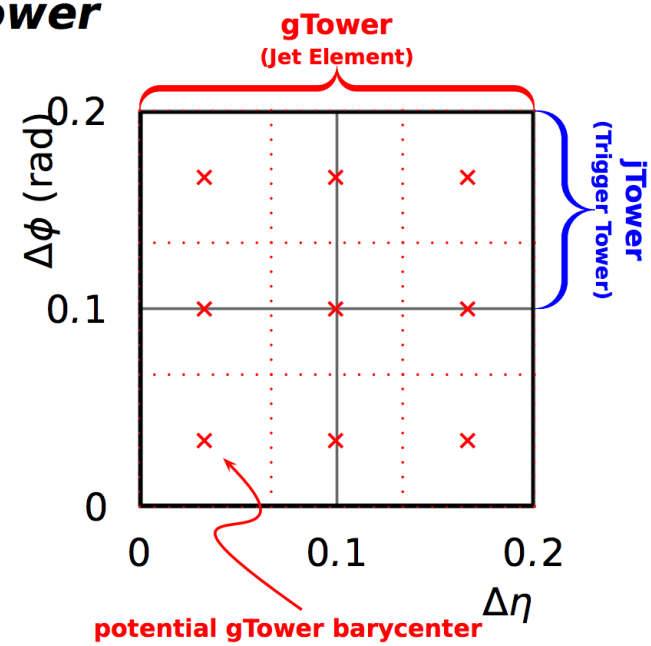
- gFEX large-R jet algorithms already planned to operate in phase space where substructure is important
  - Performance of these algorithms at Run-3 luminosities studied
  - Run-4 luminosity environment may stress gFEX trigger rates

- Substructure provides background rejection that would otherwise have to be addressed by increased pT thresholds



Jet Substructure in FEX System

- ***Improved angular resolution within gTower for mass and substructure calculations***
  - calorimeter has finer granularity than gTower
    - except EMEC $2.5 < |\eta| < 3.1$ and Tile (Phase I)
    - FCAL treatment?
  - nine positions (3 × 3) with little latency cost
  - fifteen positions (5 × 3) at some latency
  - **location within gTower requires 4 bit number**
  - can a similar scheme be implemented for jTowers?

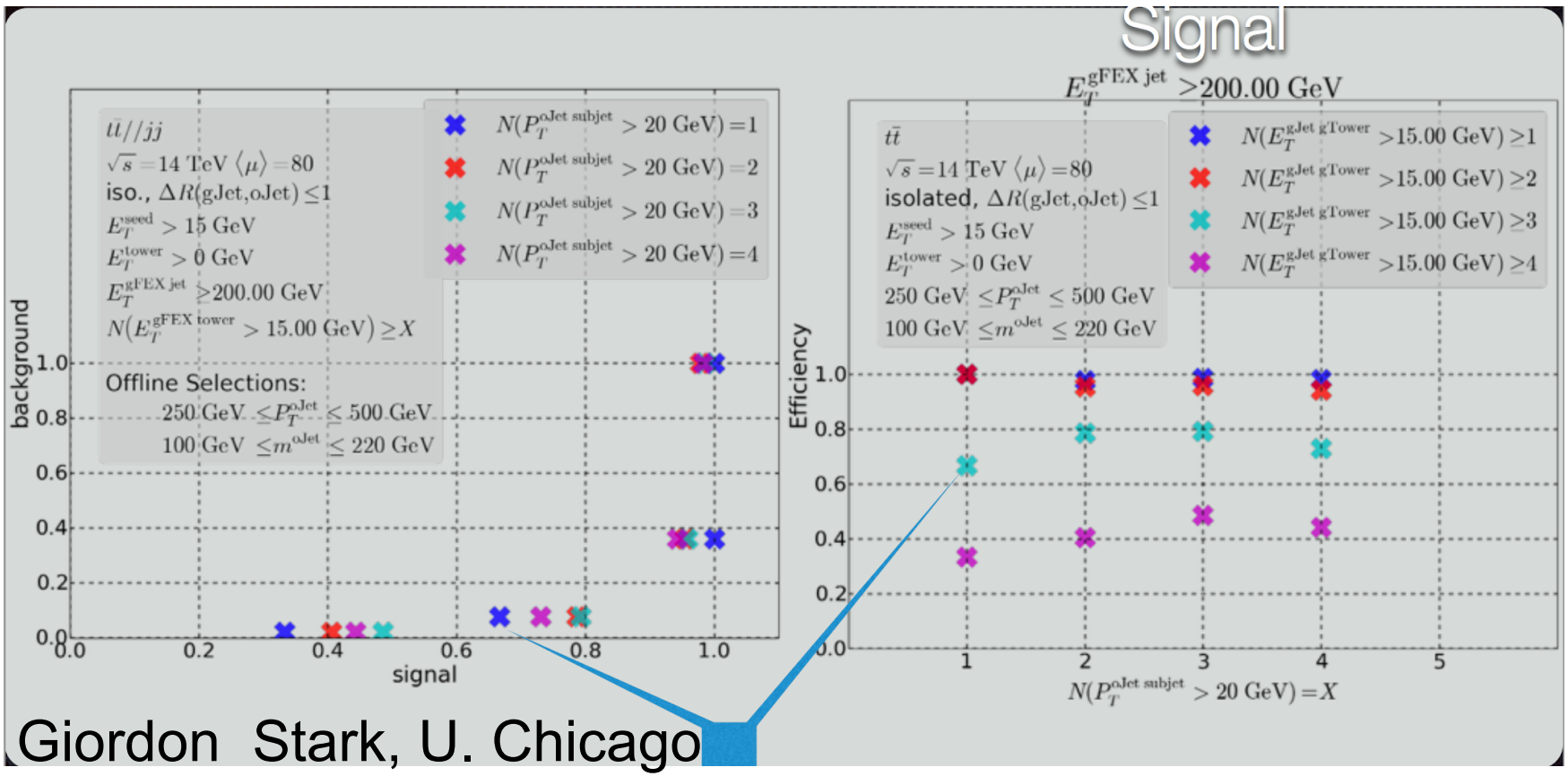


- ***More calorimeter information available***
  - tower quality, noise, timing, etc
  - layer with maximum energy
  - shower shape information
  - additional quantities possible
    - useful for both jFEX and gFEX
  - **final content depends on utility, link speed, and latency**

November 5, 2014

Jet Substructure in FEX System

- Background rejection already being studied using gTowers as a proxy for subjects
  - Dijet rejection of >50% at 95+% ttbar efficiency already promising



Giordon Stark, U. Chicago

Project Goals / Questions

can exploit synergy with US ATLAS TDAQ deliverables from Phase-I Construction Project - see MSU (W. Fisher)

- Prepare for Phase-II TDRs
  - R&D on topoclustering option needed to design the system!
- Outstanding questions
  - Can a clustering-like option (or one with similar performance) be implemented on a FPGA?
  - What is the latency of such an algorithm?
  - What is the optimal granularity to achieve performance goals (& can this be traded for latency?)
- Context within international ATLAS
  - project at the border between LAr & TDAQ
  - progress being reported in gFEX meetings

Current Status

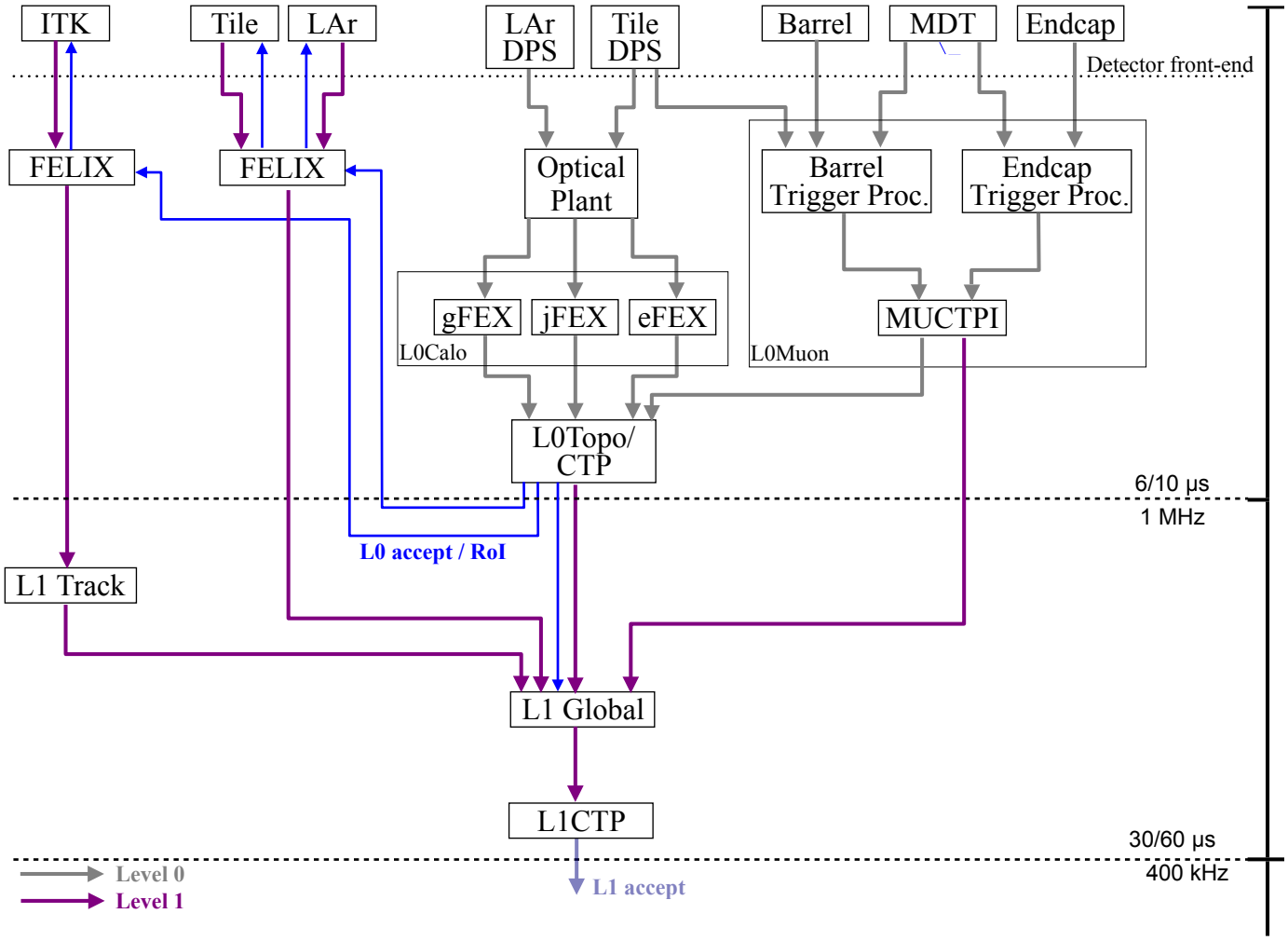
- Oregon (Stephanie):
  - Currently L3 mgr for Phase-1 LAr DPS hardware / firmware
  - Modest TDAQ R&D funds allocated for Phase-2 efforts
- MSU (Wade):
  - Currently L3 mgr for Phase-1 TDAQ ATCA Hub module / firmware
    - N.B.: Reinhard Schwienhorst also involved in Phase-1 upgrade (L3 mgr for TDAQ fiber plant project). Not certain of his plans for Phase-2 yet. But it's still early.
  - $560k Phase-2 R&D funds award from MSU foundation
- Primary interests
  - MSU: Hardware preference, but R&D studies need to support plans
  - Oregon: HW/FW projects, guided by R&D

Manpower Estimates

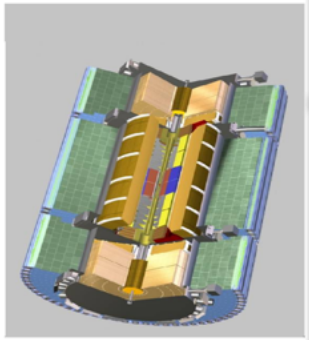
	Oregon	MSU
R&D Hardware Design	0.5 FTE/yr, engineer or technician	1.5 FTE/yr, engineer + postdoc
R&D Firmware Design	0.5 FTE/yr engineer, 1.5 FTE/yr technician	1.5 FTE/yr, engineer + postdoc
Construction Hardware	1 FTE/yr engineer, 1 FTE/yr technician	3 FTE/yr engineer
Construction Firmware	1 FTE/yr engineer	2 FTE/yr engineer

- Overlap between HW/FW implied
- Assume R&D = FY16-FY19, Construction = FY19-FY23
- Simulation / physics studies
  - Physicist effort (undergraduates, partial postdoc(s), PIs)

Phase-II ATLAS Trigger



LAr Phase II Architecture



Phase-II Upgrade Front-End Board
Shaper
2,3 Gains
ADC & Gain Selec
MUX/Serializer
Preampl.
Linear Mixer
Optical Links
CLK Fanout
Layer Sum Boards [LSB]
80-100m fibers
Phase-II Upgrade ROD
FPGA
Ped Sub
E,t N-tap FIR
ORx Arrays
OTx
L1-buffers
Output OTx
DAQ
L0-pipelines
L0 Accept Logic & L1 Trigger Feature Extractor
L1 Accept Logic
TTC Partition Master
Controller Board
Timing Trigger Control Distribution
Tower Builder Board [TBB]
PZ+Dly
Trigger Tower Sum and Drivers
$\Sigma\alpha_i S(t-\tau_i)$
Monitoring Stations
Baseplane
L1 Trigger Processor
Level-0,1 Calorimeter Trigger System
LAr Trigger Digitizer Board (LTDB)
ADC
CLK Fanout
ORx
MUX/Serializer (FPGA)
Optical Links
~250 Gbps/board
Crate Monitoring
LAr Digital Processing System (LDPS)
OTx CLK & Clg.
Optical Receiver Deserializer
480Gbps/module
1.92 Tbps/board
Timing Trigger Control Rx
L0 Trigger Processor
SDRAM