Basic IP blocks

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Outline

- IO pads with ESD
- Rx and Tx circuits
- Band-gap
- Chip seal-ring library
- Conclusion

IO pads with ESD

- Motivation / need
  - Standard TSMC65 IO pads use radiation soft 3.3V transistors
  - We also need a fast analog input IO pads
- Solution is to take 1.2V IO pads developed by SOFICS for Cern
- Problem: IO pads are designed for 7+1 metal stacks
- Nevis will convert it to 9+1 metal stack

Rx and Tx circuits

- Motivation / need
  - Standard, fast, rad hard TSMC65 Rx/Tx do not exist
  - To be compatible with Cern digital environment we need SLVS signaling
- Solution is to take a RD53 Rx/Tx circuits
- There is no problem with using them.
- We have a library

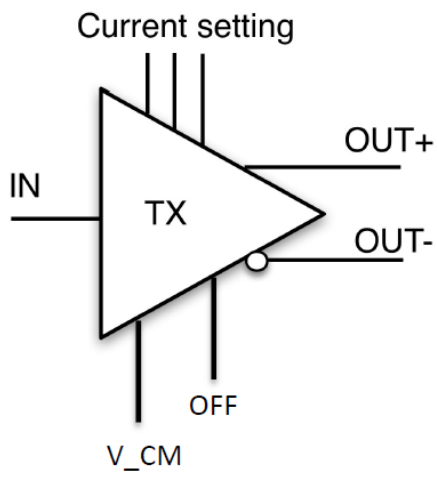
RD53 SLVS Driver

IP Block: BG-PV Scalable LVDS driver

Parameter	Value
Size	150 µm X 200 µm
Supply voltage	1.08V - 1.32V
Power	2.8 mW
Temperature range	-40°C +80°C
Frequency of operation	1.2 Gbps
Metal layers	M1-M2-M3
Special options	None
Capacitor	NMOS
Active element used	NMOS, PMOS, LVT_NMOS, LVT_PMOS, rppolywo, rnpolywo
Status	First prototype characterized at 1.2Gbps Abstract, verilog and liberty files ready Characterized up to 550 Mrad with X-rays
Future activity	
Designer (Email)	gianluca.traversi@cern.ch francesco.de.canio@cern.ch

I/O signals	Function
Input signals (Signal name)	IN
Output signals (Signal name)	OUT+, OUT- , V_CM, OFF, B0, B1, B2
VDD, GND	Supply voltage, ground

Block Diagram



V_{CM} = 200mV

V_{DM} = 200mV

V_{OUT} is equal to +100mV or +300mV

I_{OUT} = 0.5mA, 1mA, 1,5mA, 2mA, 2.5mA

Schedule

Status	Date
Prototype 1 submission	Q2 2015
Prototype 1 characterized	Q4 2015
Prototype 1 irradiated	Q1 2016
Full IP available	Q2 2016

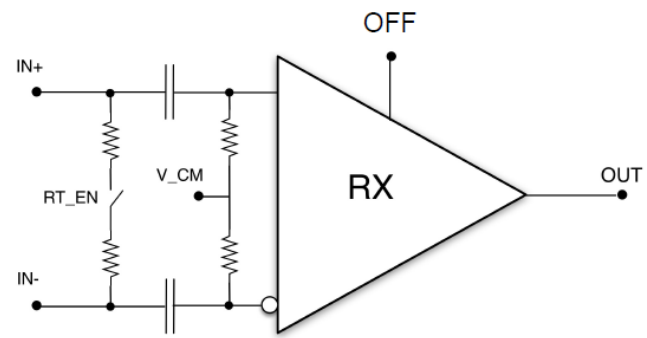
RD53 SLVS Receiver

IP Block: BG-PV Scalable LVDS receiver

Parameter	Value
Size	90 µm X 115 µm
Supply voltage	1.08V - 1.32V
Power	2.5 mW
Operating temperature	-40°C + 80°C
Bandwidth	1.2 Gbps
Metal layers used	M1-M2-M3-M4
Capacitor	crtmom
Active element used	NMOS, PMOS, LVT_NMOS, LVT_PMOS, rppolywo
Status	First prototype characterized at 1.2Gbps Abstract, verilog and liberty files ready
Future activity	Characterized up to 550 Mrad with X-rays
Designer (Email)	francesco.de.canio@cern.ch gianluca.traversi@cern.ch

I/O signals	Function
Input signals (Signal name)	IN+, IN-
Output signals (Signal name)	IN+, IN- , OUT, RT_EN, V_CM for the AC coupled version, OFF
VDD, GND	Supply voltage, ground

Block Diagram



Schedule

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Prototype 1 submission	Q2 2015
Prototype 1 characterized	Q4 2015
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Band-gap unit

- Motivation / need
  - Radiation hardness unit needed
- We are looking into a RD 53 unit
- It was produced and characterized to be rad hard to very, very high rad levels
- Problem: ~100 DRC errors due to the enclosed NMOS transistors used
- Question: how these DRC issues compromise the yield? We would need to produce ~50000 ADC devices with one bandgap in each of them.

Band-gap unit

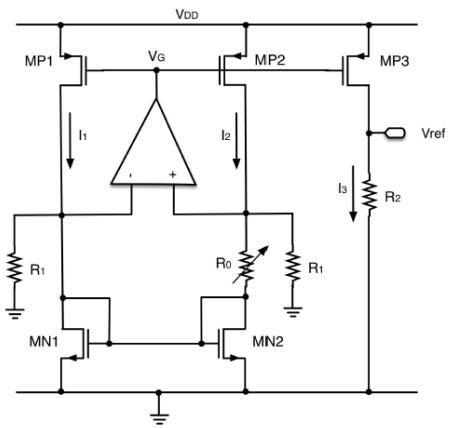
- Answer from IMEC: "There is no easy answer to such question. First of all, there is indeed a yield-related aspect why TSMC does not allow bended poly gates, but that information will not be publicly available. Secondly, yield loss could very well be the result of bad/insufficient modeling of the enclosed layout device, e.g. lower matching, different VT effects, different mobility, .."
- What is the solution ?
  - To use another device
  - To modify the transistors to normal one as we do not need to be in such a high radiation
  - We are looking into both options

Band-gap

IP Block: Bandgap

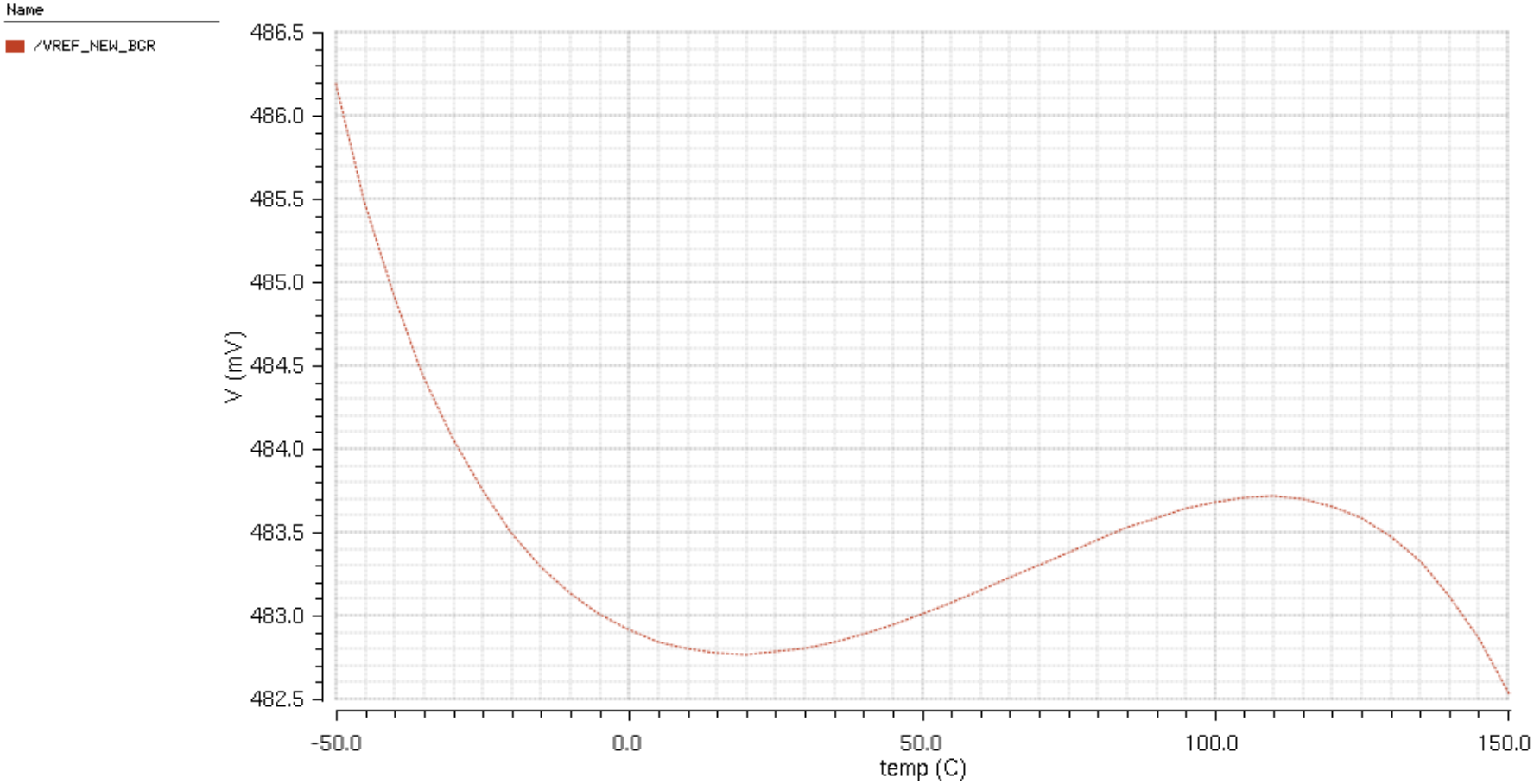
Parameter	Value
Size	100 um X 280 um
Supply voltage	1.08-1.32 V
Power	46 uW **(V1)** 180 uW **(V2)**
Temperature range	-40°C + 110°C
Bandgap voltage	650 mV @ 30°C **(V1)** 395 mV @ 30°C **(V2)**
Temperature Coefficient	255 ppm/K **(V1)** 18 ppm/K **(V2)** (after trimming, best case)
Metal layers used	M1-M2-M3-M4
Special options	None
Capacitor	MOMCAP
Active element used	NMOS, PMOS
Irradiation status	Irradiated with: - Xrays up to 250 Mrad, 10MeV protons (chip unbiased, room temp.) that are equivalent to 800 Mrad and $5{,}56*10^{15}$ 1MeV n.eq/cm^2 and 3MeV protons up to 1Grad and 10^{16} n.eq/cm^2
Status	Samples characterized in temperature chamber -40°C ÷ +100°C Layout, Abstract, Verilog (Vout vs T) are ready
Designer (Email)	gianluca.traversi@cern.ch francesco.de.canio@cern.ch

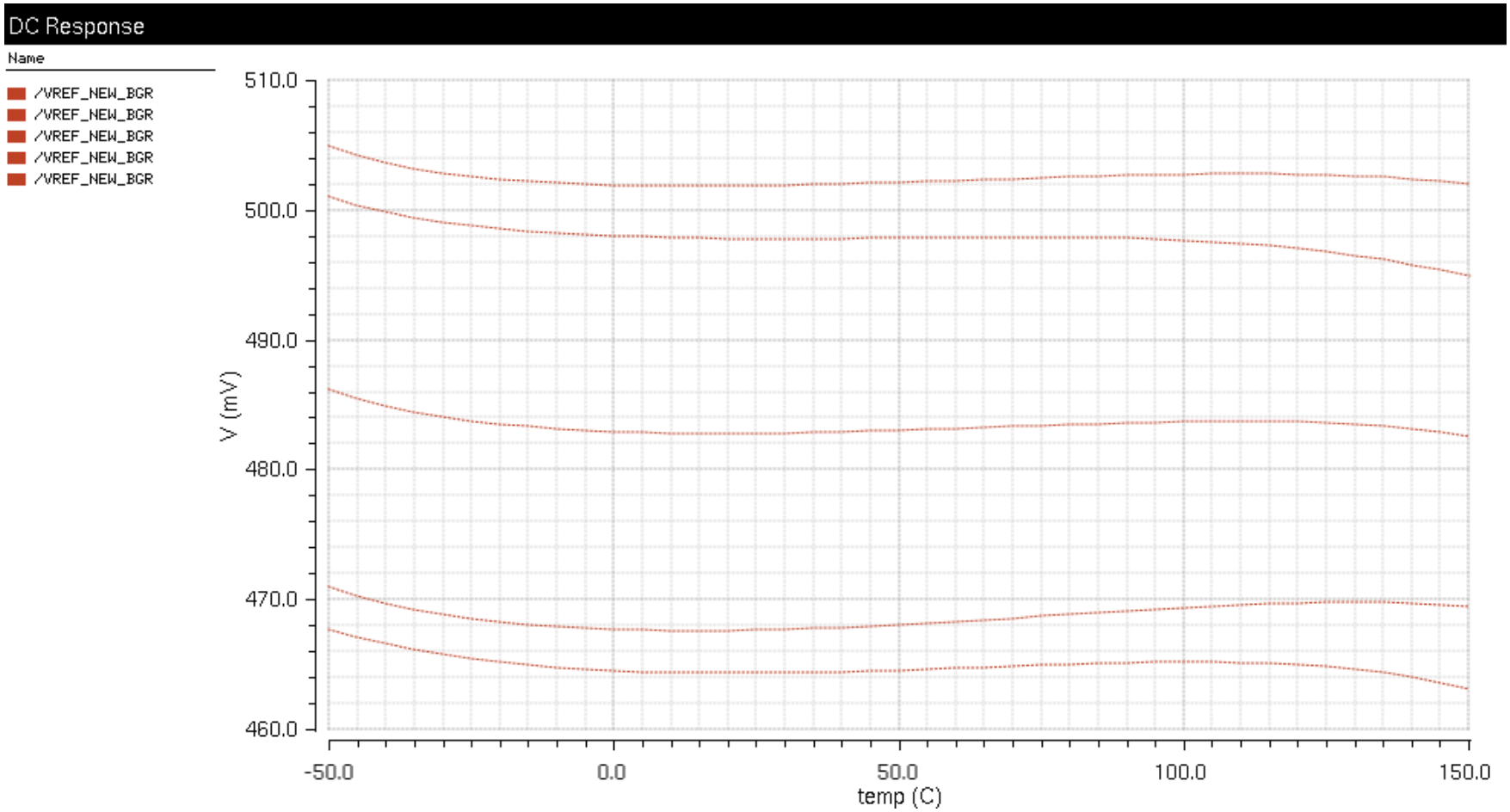
Block Diagram



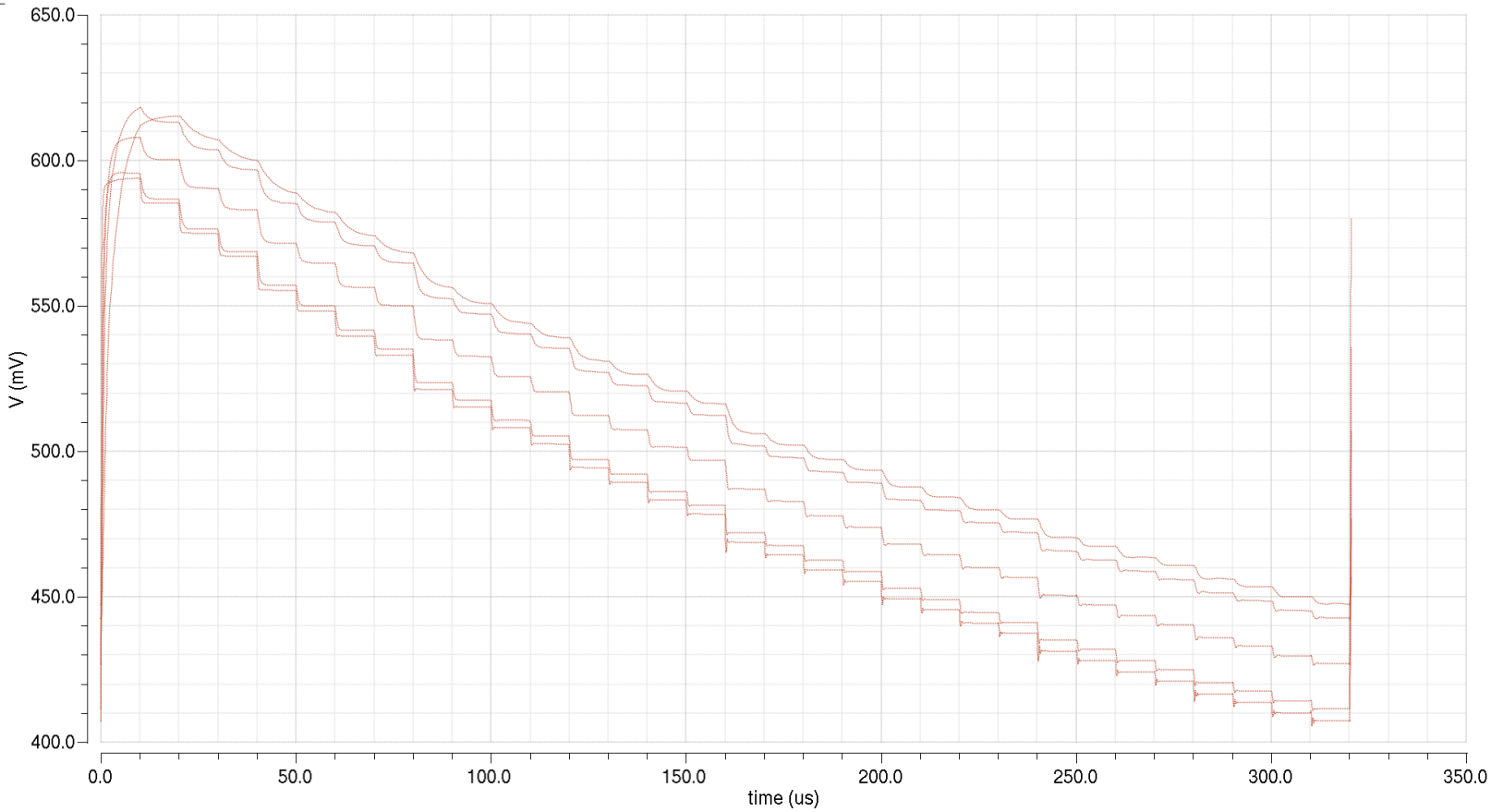
I/O signals	Function
Input signals (Signal name)	Startup, 5bit for trimming
Output signals (Signal name)	Vref
VDD, GND	Supply voltage, ground

DC Response


Name
/VREF_NEW_BGR
486.5
486.0
485.5
485.0
484.5
484.0
483.5
483.0
482.5
V (mV)
-50.0
0.0
50.0
100.0
150.0
temp (C)


DC Response
Name
/VREF_NEW_BGR
/VREF_NEW_BGR
/VREF_NEW_BGR
/VREF_NEW_BGR
/VREF_NEW_BGR
510.0
500.0
490.0
480.0
470.0
460.0
V (mV)
-50.0
0.0
50.0
100.0
150.0
temp (C)

Transient Response



Seal-ring library

- Seal ring library as distributed by Cern has quite a few problems
- We have now “corrected” library which allows to make a chip ring without drc errors

Conclusion

- Problems with basic IP blocks needed for radiation hard and Cern signaling environment identified
- We are on the way to have these IP blocks ready for the chip submission