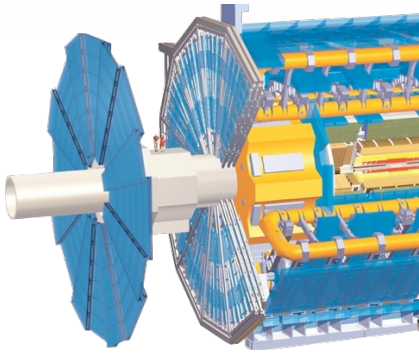


Layout & Verification Update

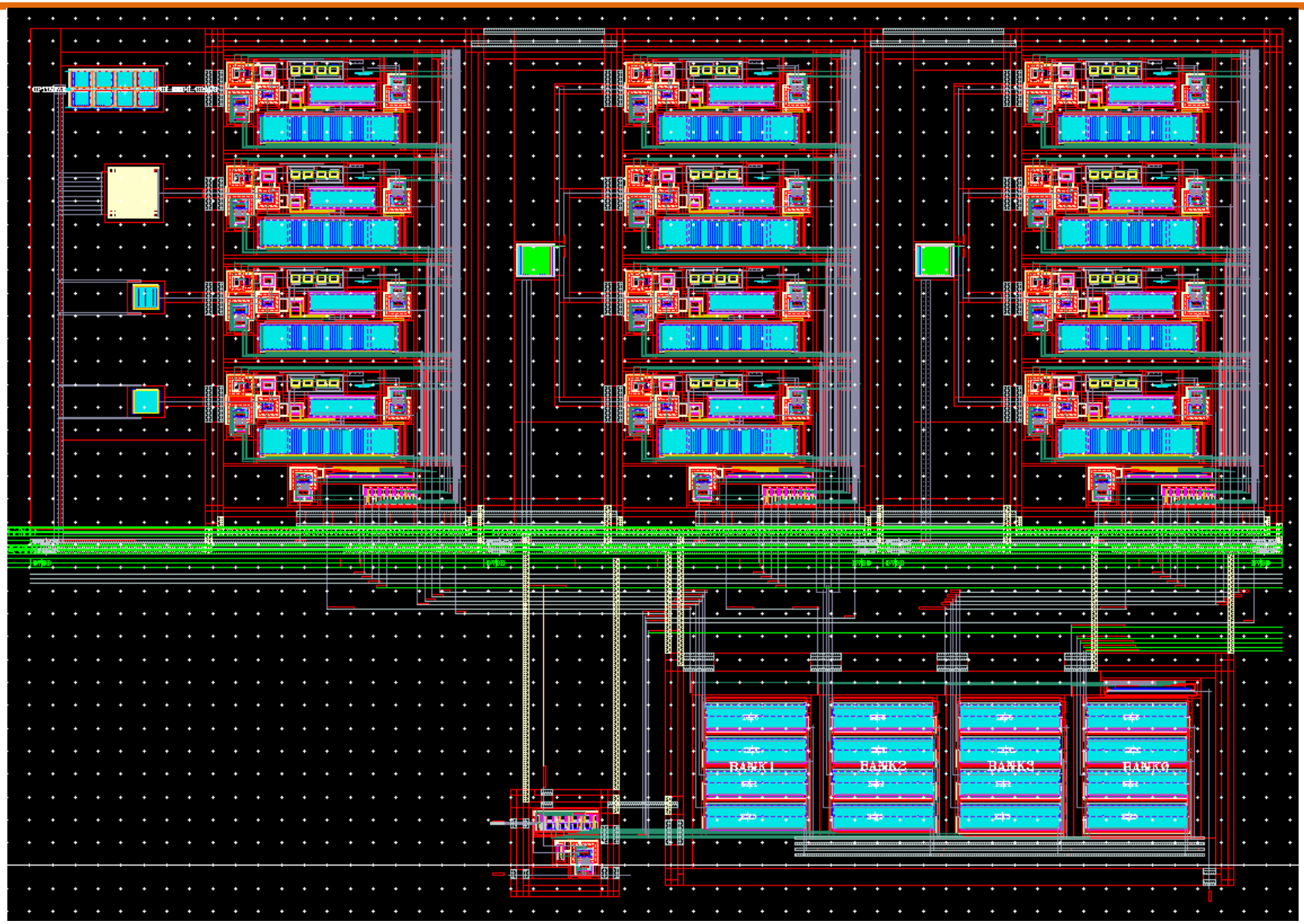
Ray Xu

Mar 12, 2017

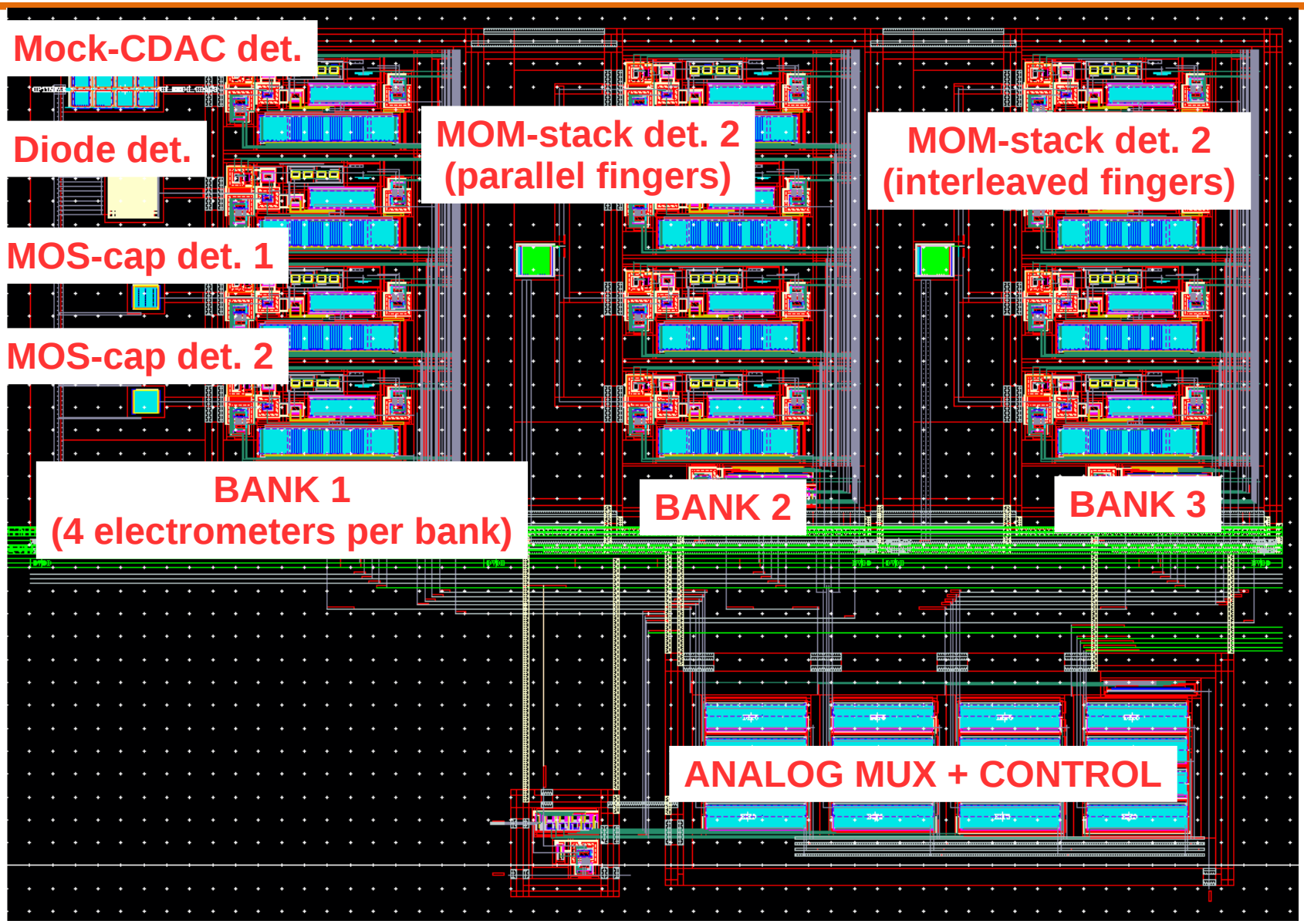
Outline

- Layout of SEU test structures + core
- R+C+CC Simulation with mock SEU (of reasonable energy)
  - SEU hit on the detector
  - SEU hit on the readout circuitry

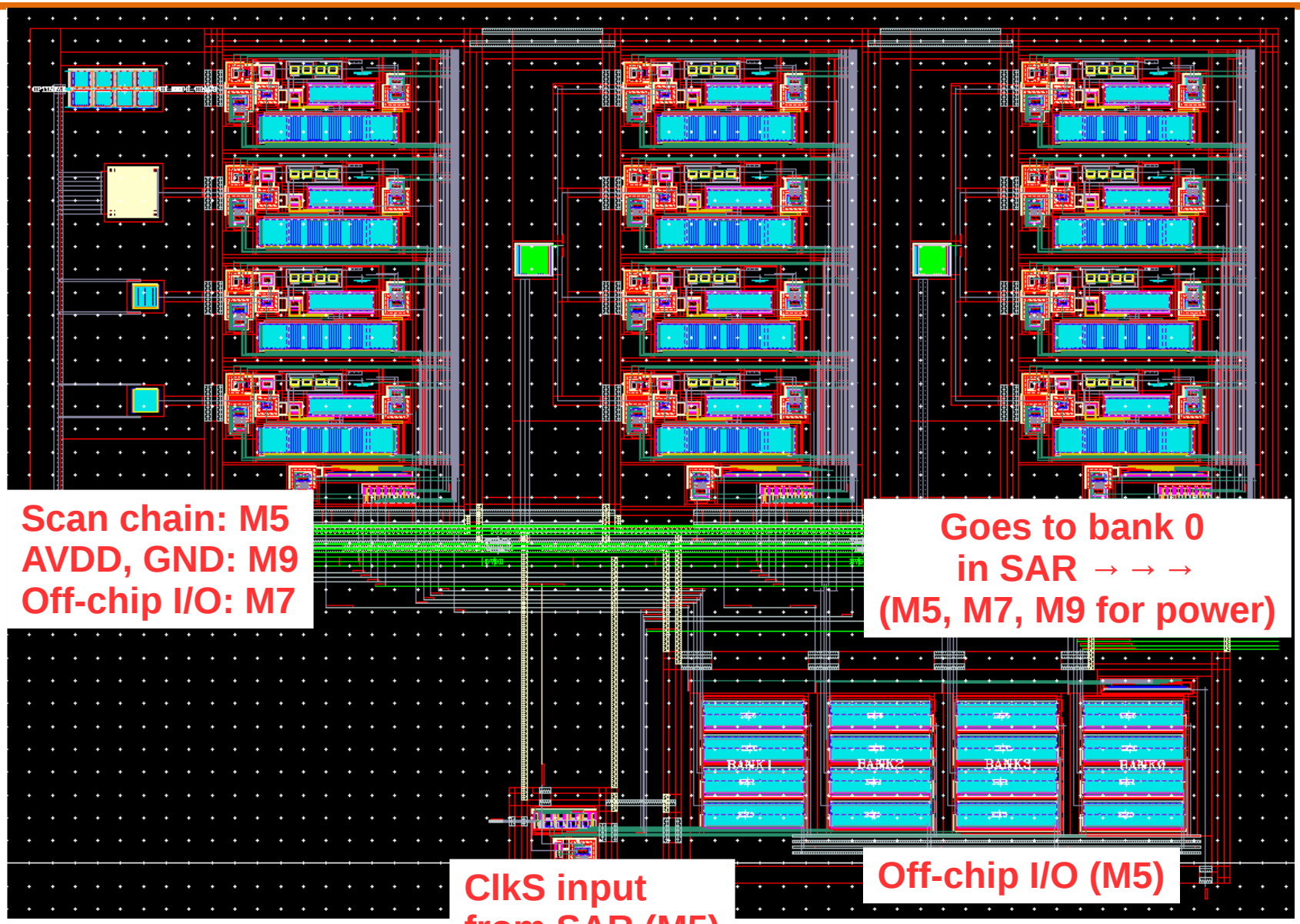
SEU Test Structure Topcell



SEU Test Structure Topcell



SEU Test Structure Topcell



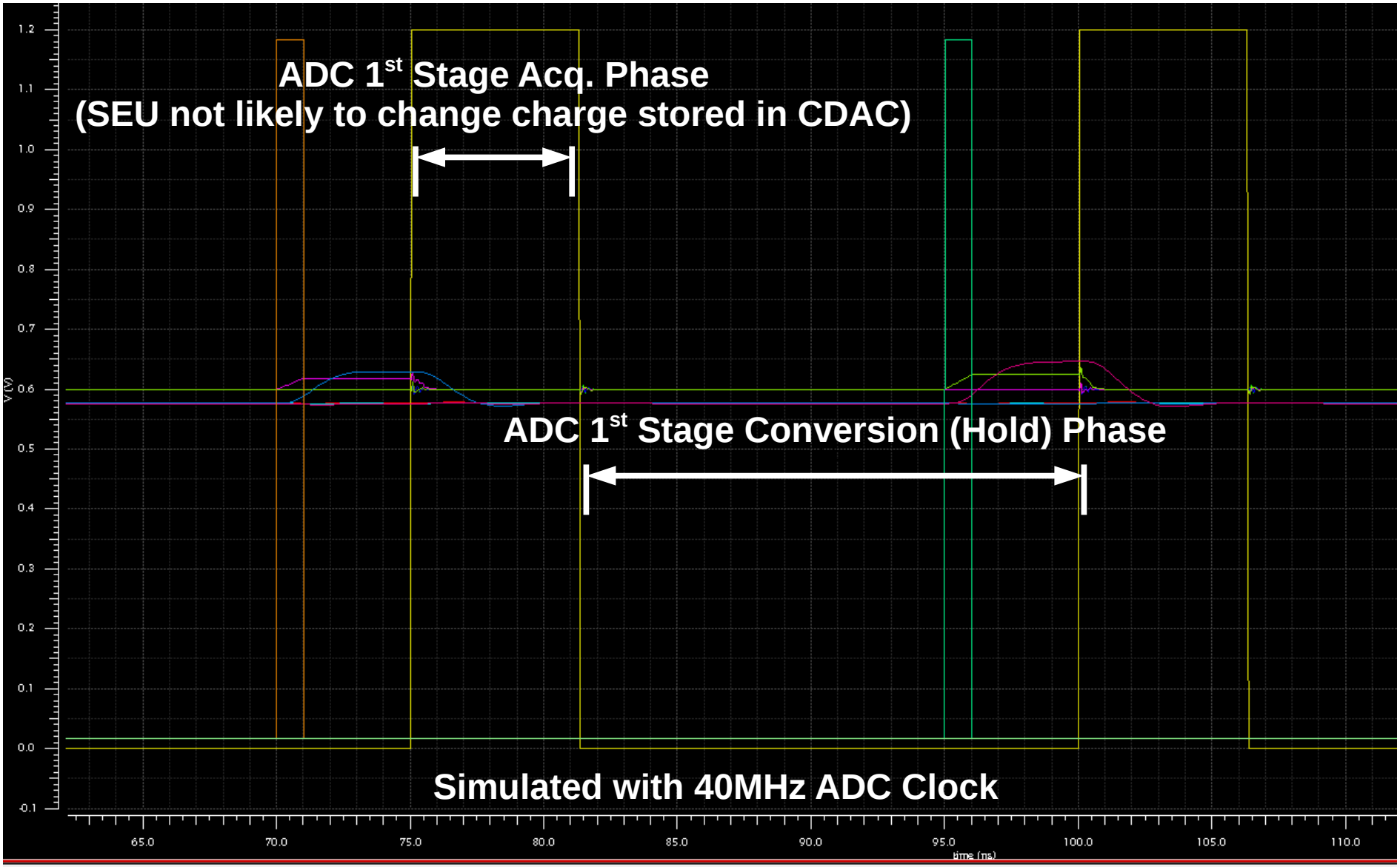
SEU Test Structure Topcell

- ~ 300 um x 200 um
- Horizontal: odd metals
- Vertical: even metals
- 16 total SEU Readouts; only 4 simultaneous
- DRC & LVS clean (sans metal density, ESD, seal ring, etc)

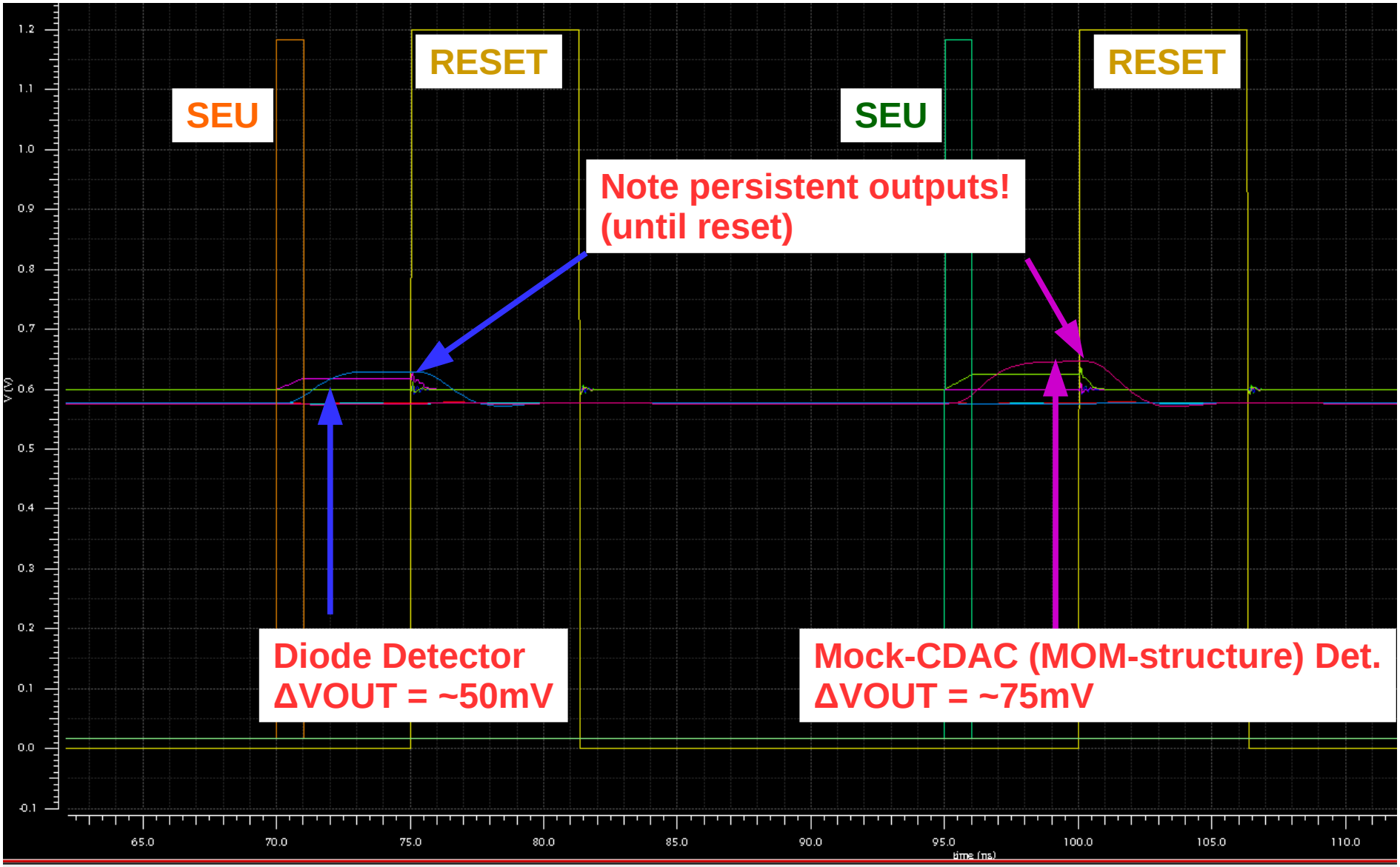
Post-extraction Simulation

- Emulating an SEU:
  - Current pulse source in between detector nodes
  - 1uA for duration of 1nS (unless otherwise stated)
- R+C+CC Extraction, 10 pF off-chip load
- Worst-case package parasitics included on off-chip nodes
- Drawback: Cadence simulation only considers disturbance of charge

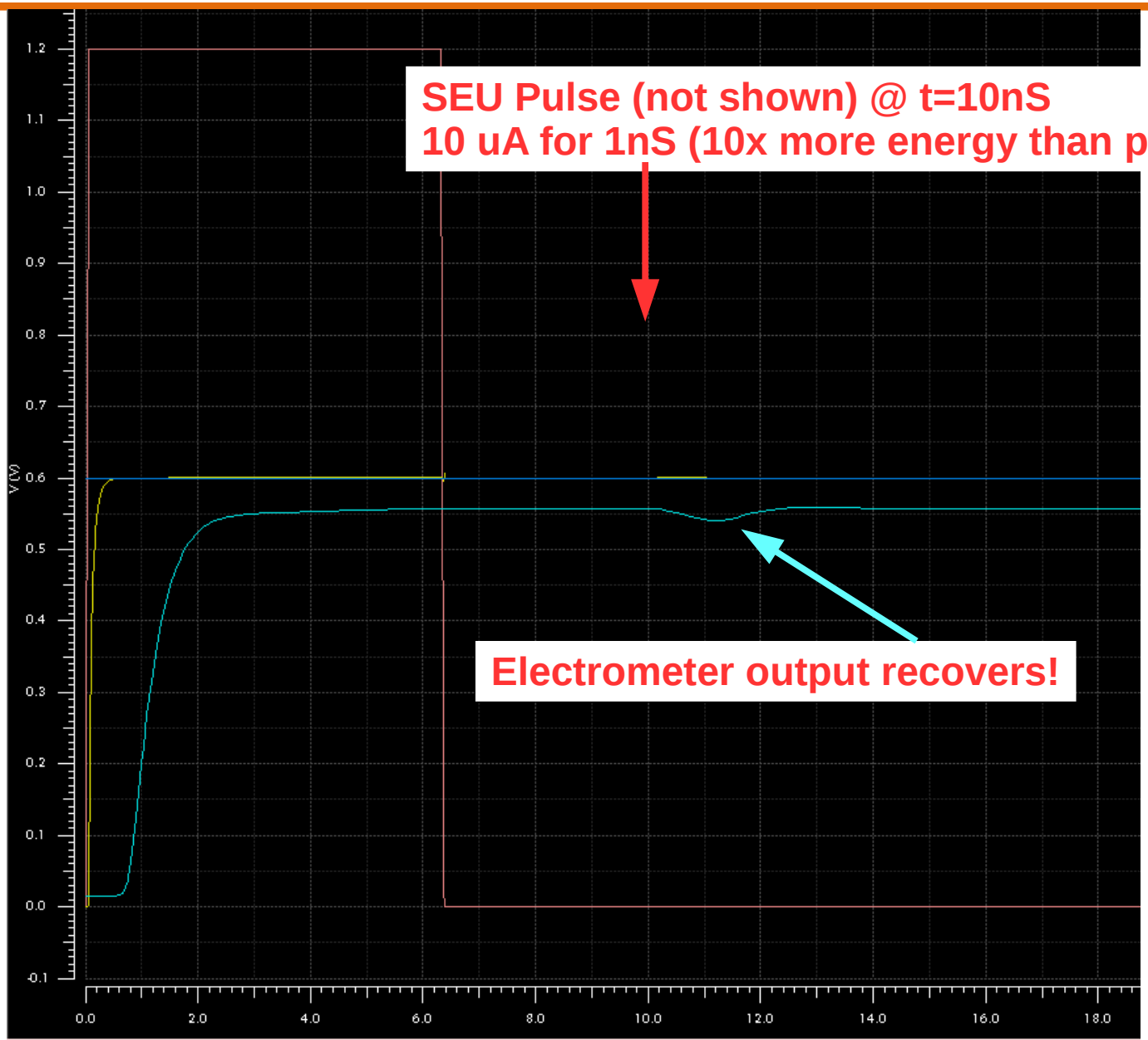
Notable Results



Notable Results



SEU Hit on Electrometer



To-do

- Make changes to CDAC capacitors to match detector cap metal pitch and width (not critical, but preferred)
- Connect CDAC detector to SEU core