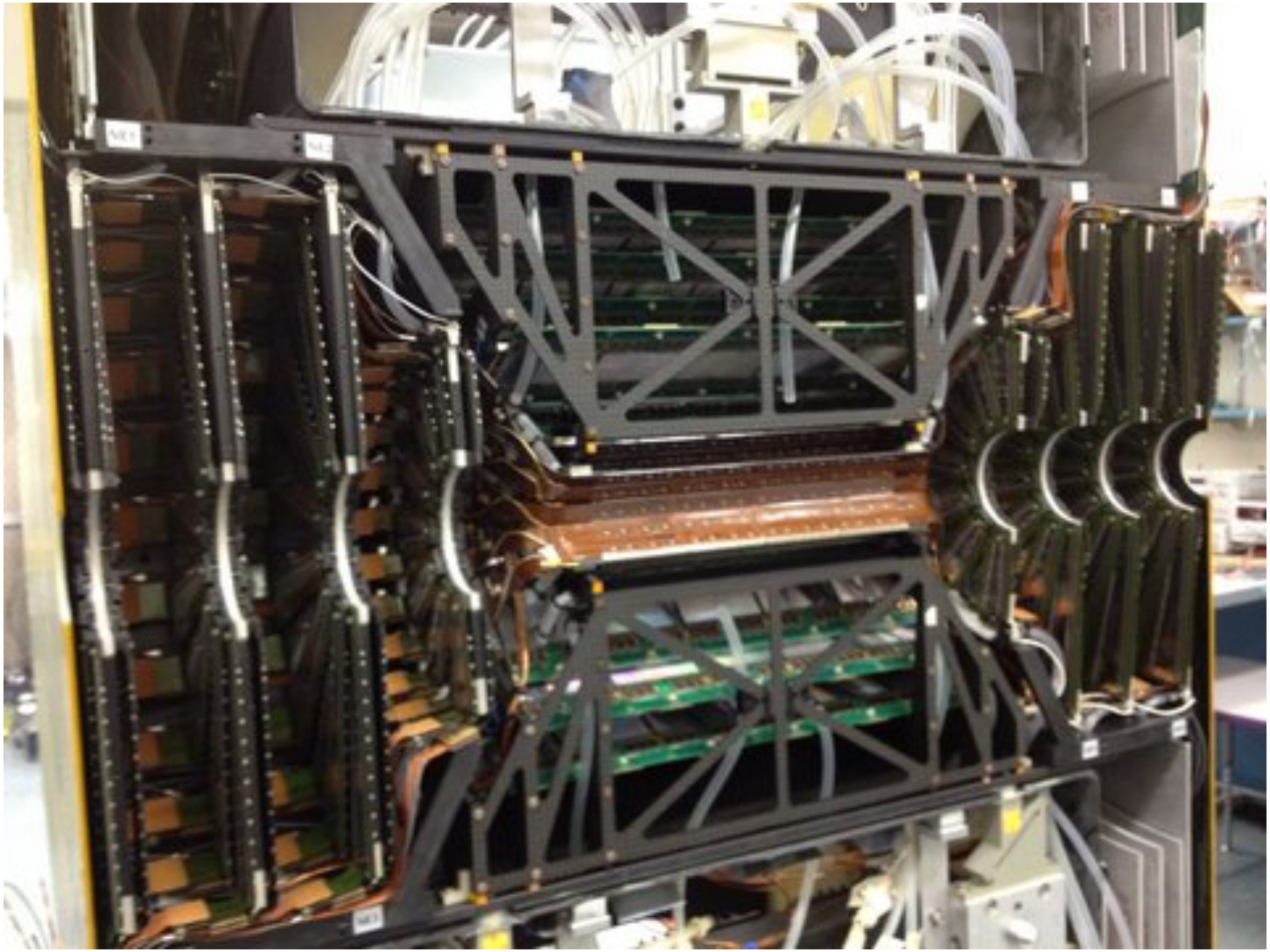
sPHENIX Intermediate Tracker Status

RIKEN/RBRC
Itaru Nakagawa
for the INTT group

Basic Project Philosophy

Basic Project Philosophy

PHENIX FVTX Detector



Developed mainly by LANL and NM Universities

RIKEN + Rikkyo Univ.+J-Parc	Work
Itaru Nakagawa	Design, management
Yasuyuki Akiba	Design, Consultant
Students (Rikkyo)	FPGA program, test bench activities
Shoichi Hasegawa(J-Parc)	FPGA programmer

Procurement

Japanese Companies

Si-Sensor (Hamamatsu Co.)
HDI (Yamashita Co.)

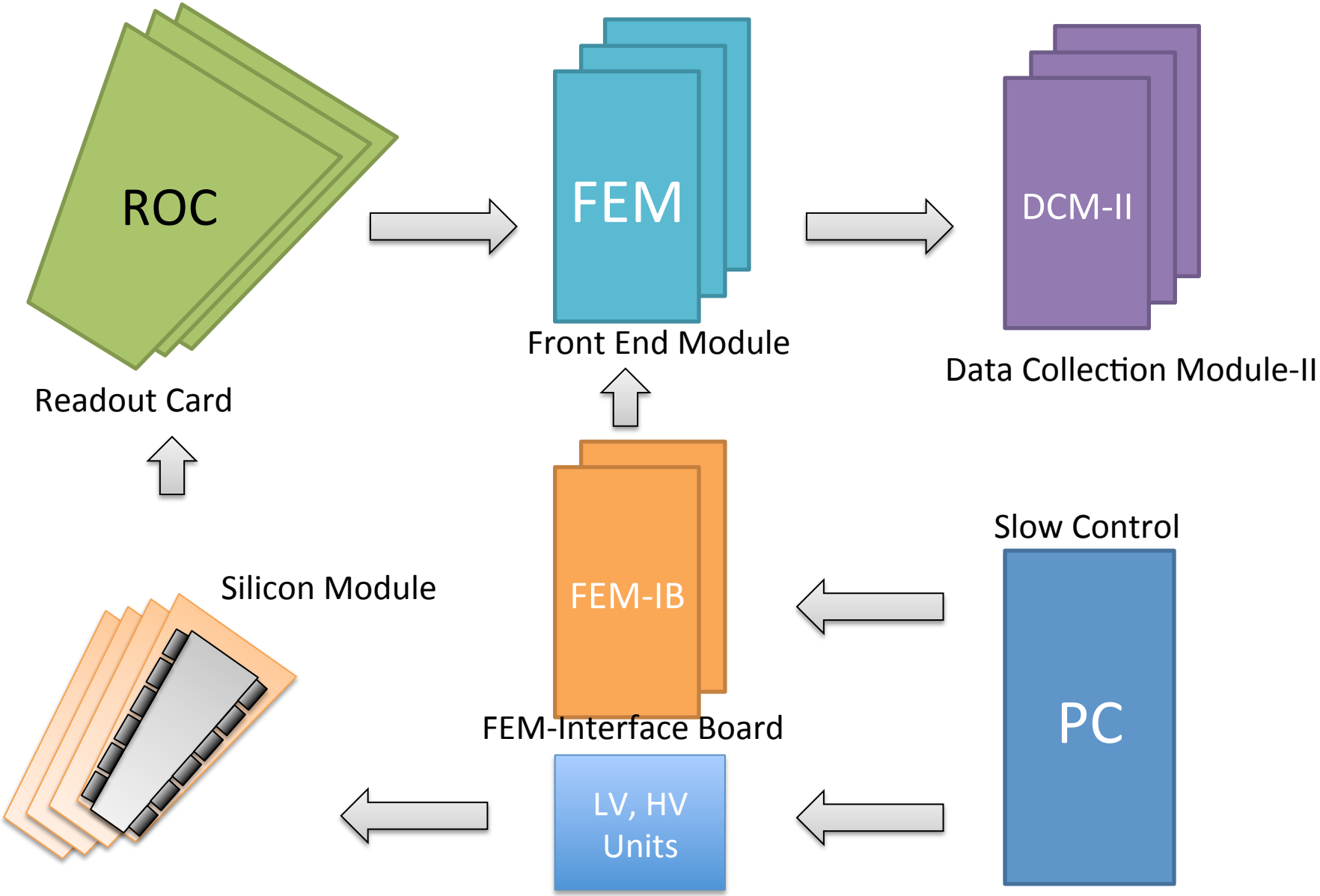
Provision of resources,
Technical support

BNL	Work
Y. Yamaguchi G. Mitsuka	Test bench activities, Simulation
Rachid Nouicer	Design, assembly, management
Eric Mannel	FPHX chip, test bench support
Jin Huang	Software, analysis…
Engineer	Support structure design

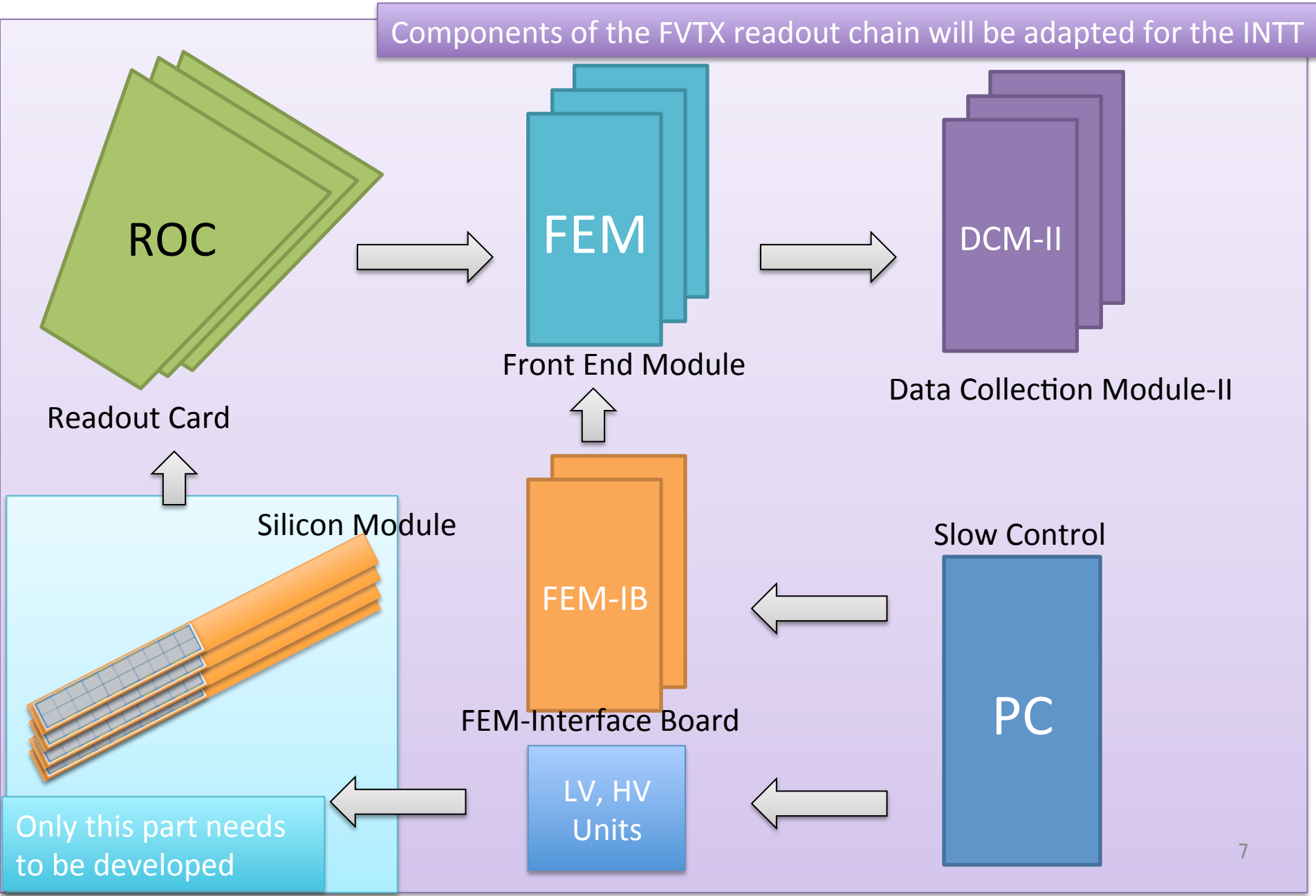
LANL + UNM
Melynda Brooks
Ming Liu
Walter Sondheim
Doug Fields

Technical Support

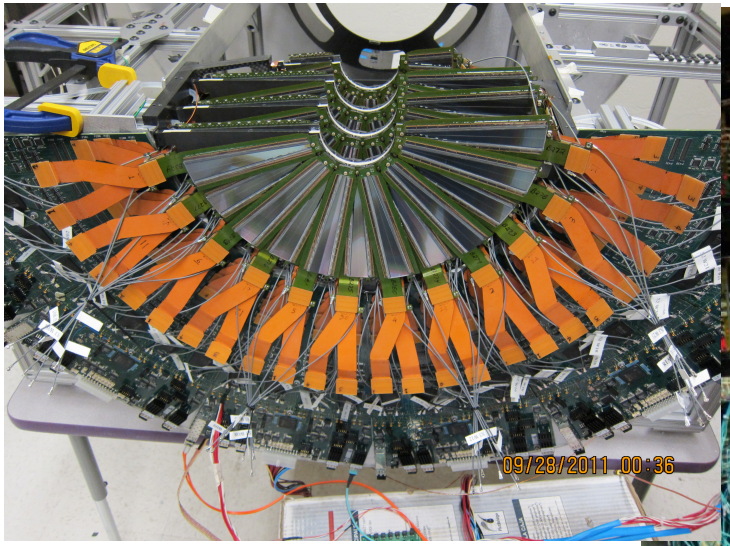
FVTX Readout Chain

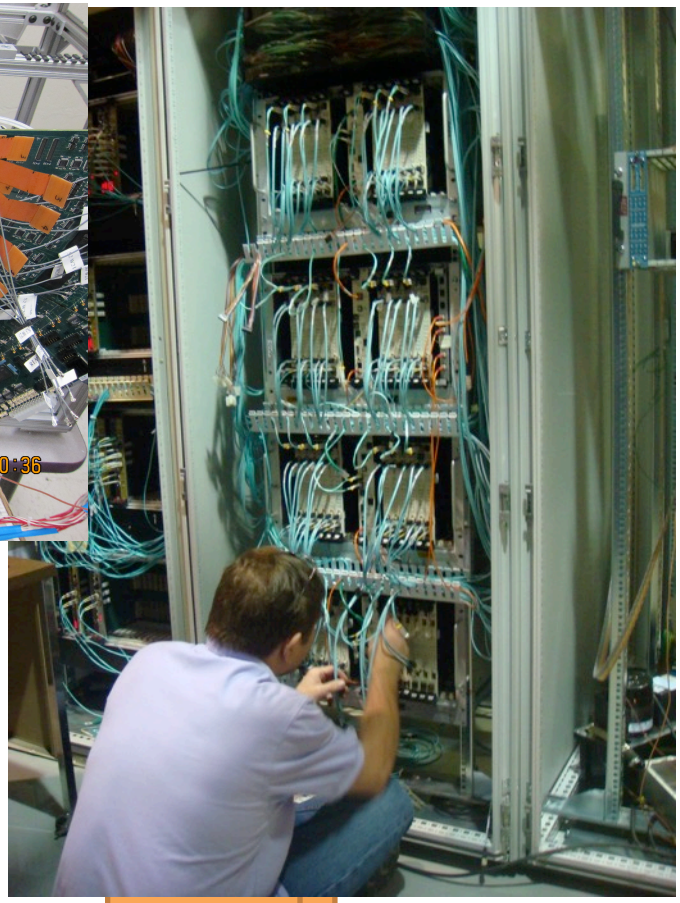


INTT Readout Chain



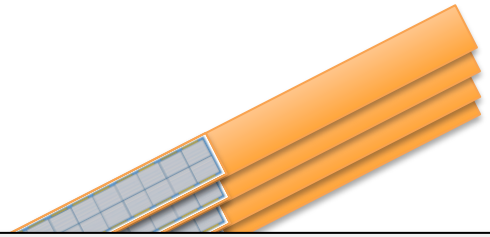
INTT Readout Chain





DCM-II

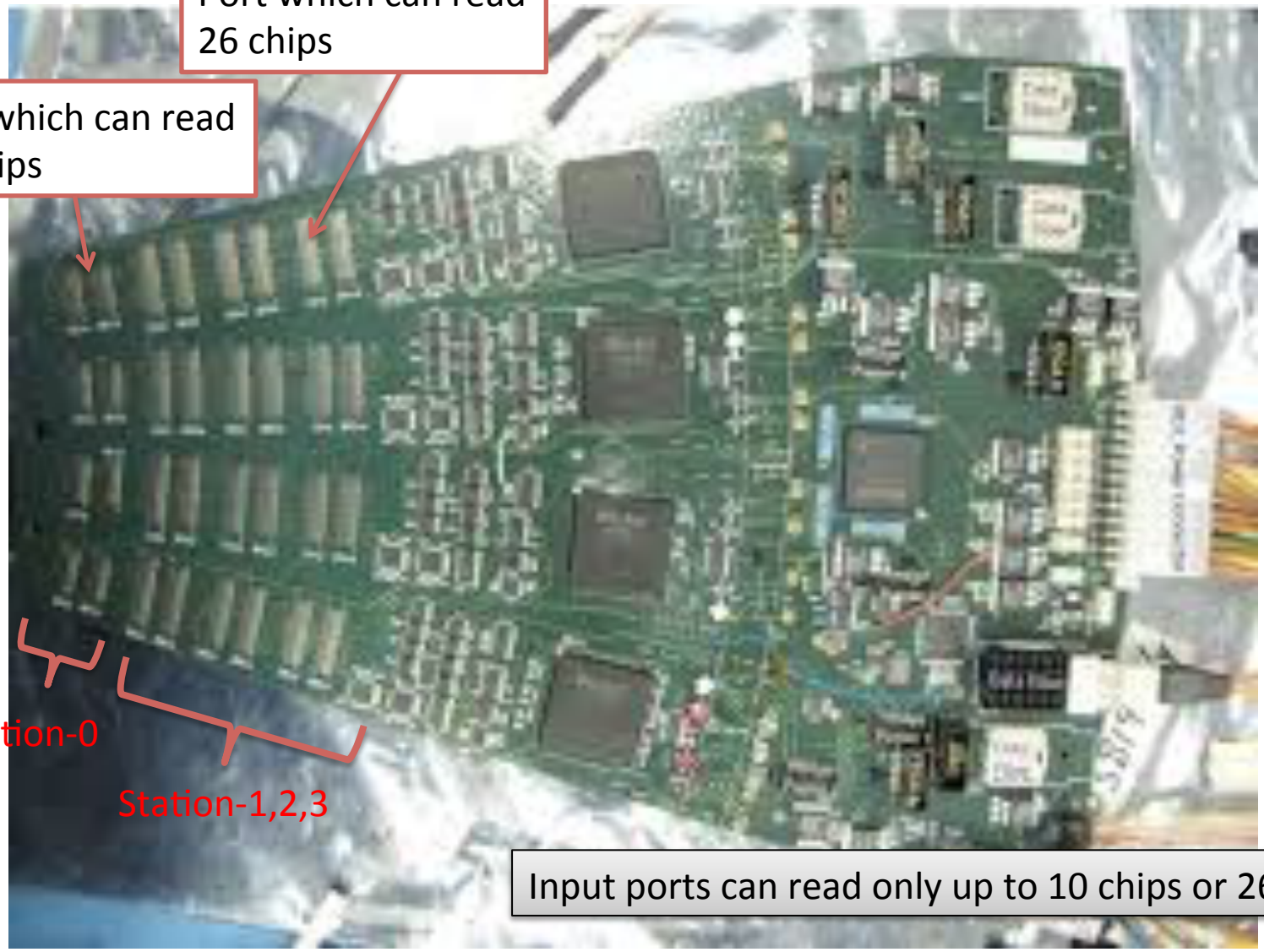
Slow Control



The entire read-out chain of FVTX system will be re-used in INTT. This will reduce the cost by half and save 2 years of R&D phase.

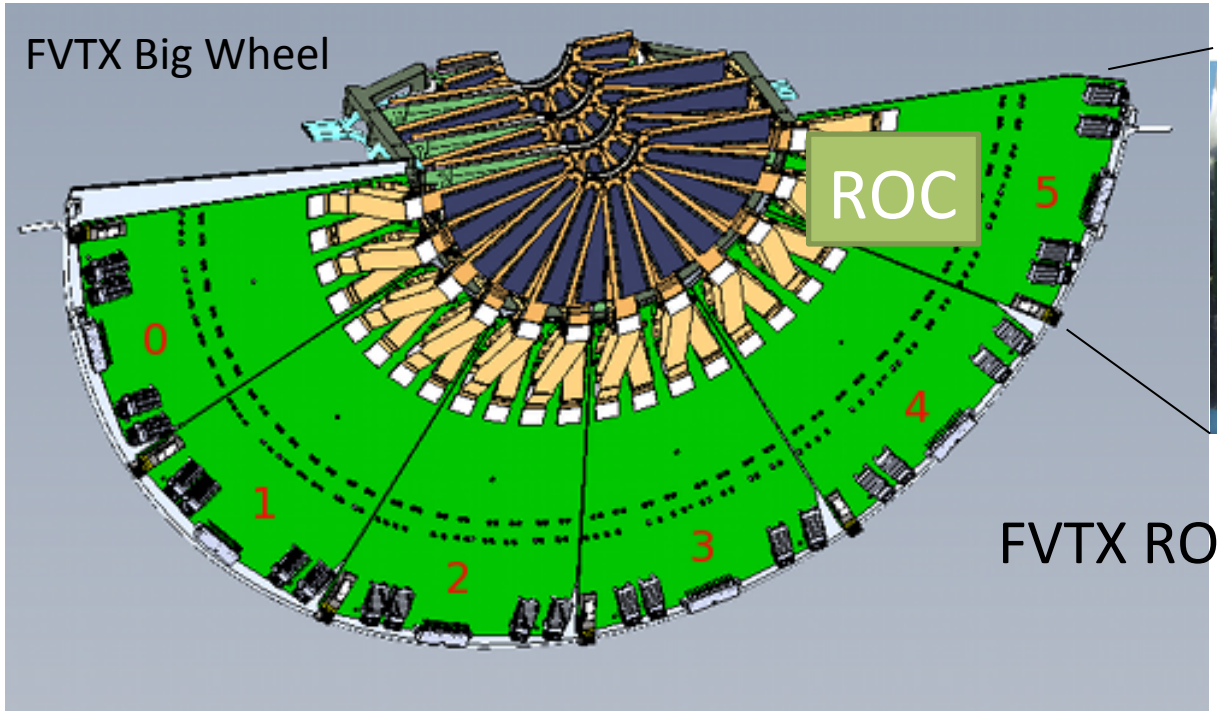
Silicon Module

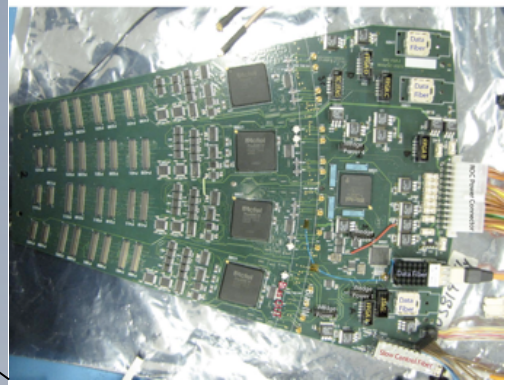
Constraints from FVTX Input ports of ROC



Input ports can read only up to 10 chips or 26 chips.

Total Number of Ports Available





FVTX ROC boards to be reused

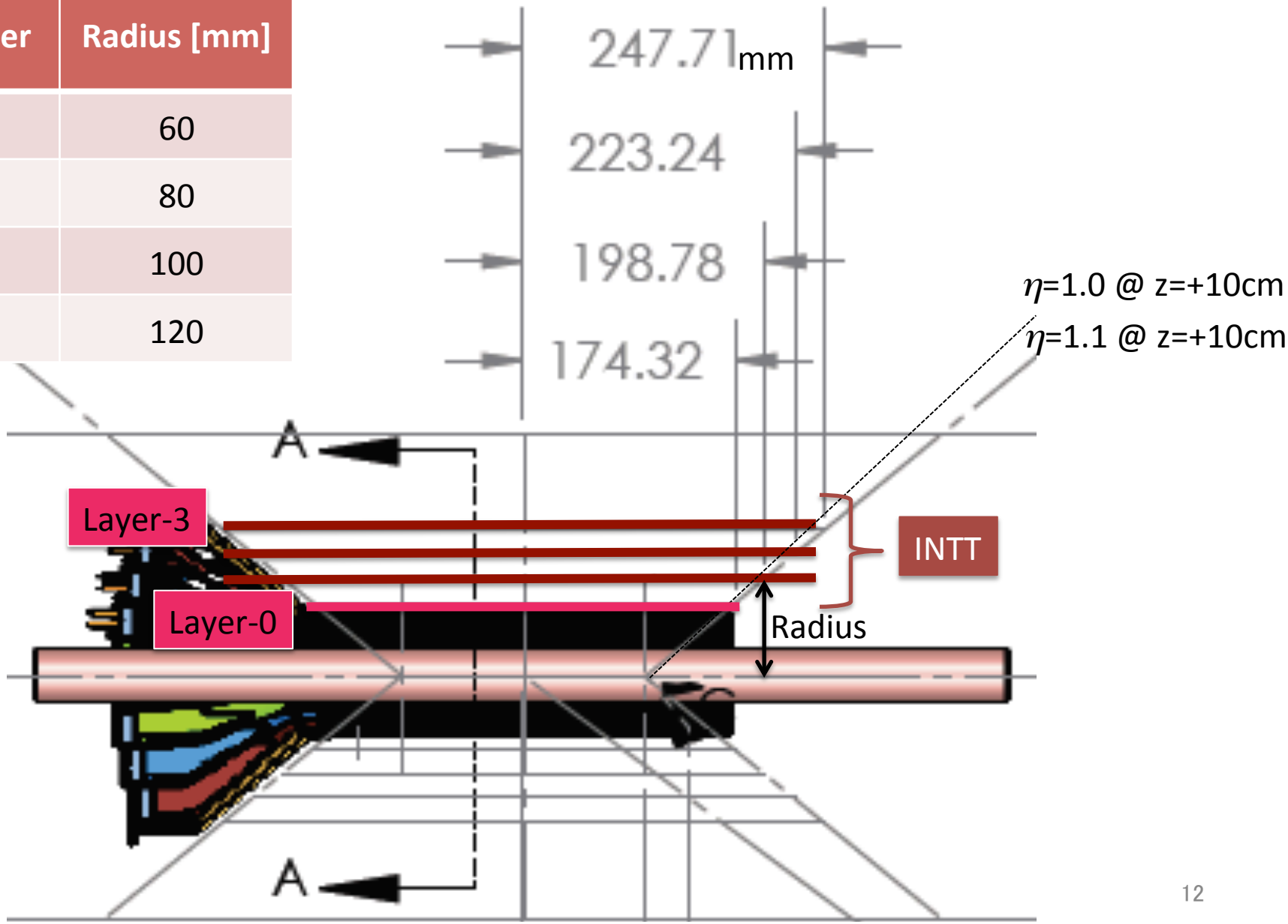
	Per Arm	Total (2 arms)
Station-0	4 ports × 12ROCs = 48	96
Station-1,2,3	4 × 3 ports × 12ROCs=144	288

Total number of INTT readout ports should be less than the available # of ports.

CONFIGURATION

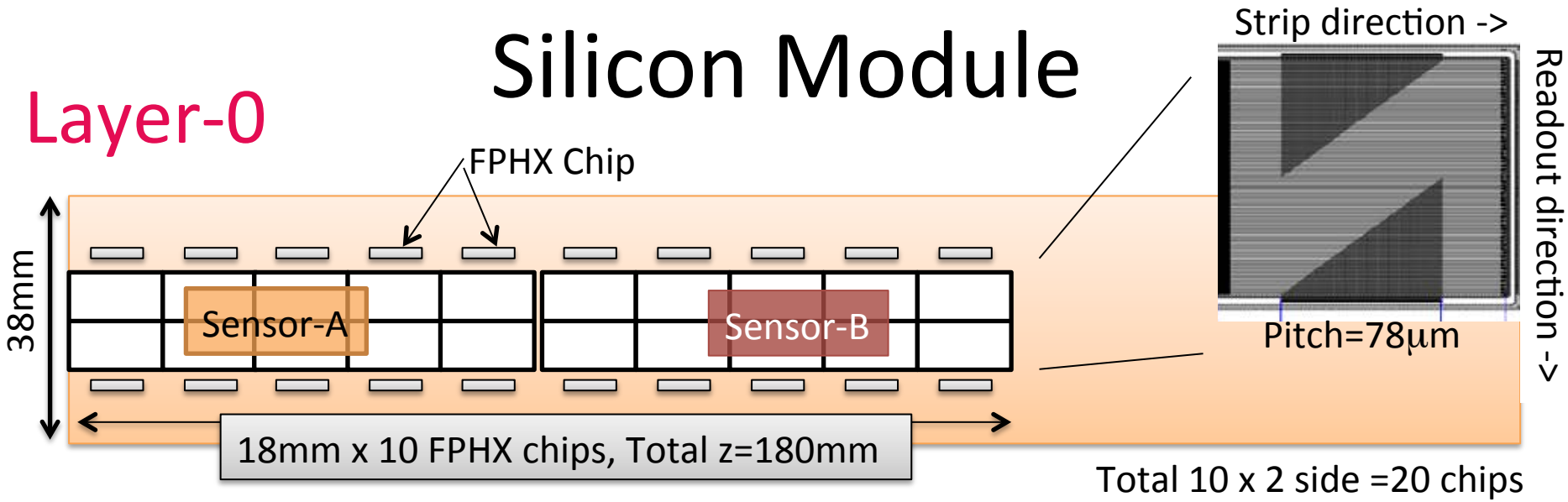
Detector Layout

Layer	Radius [mm]
0	60
1	80
2	100
3	120

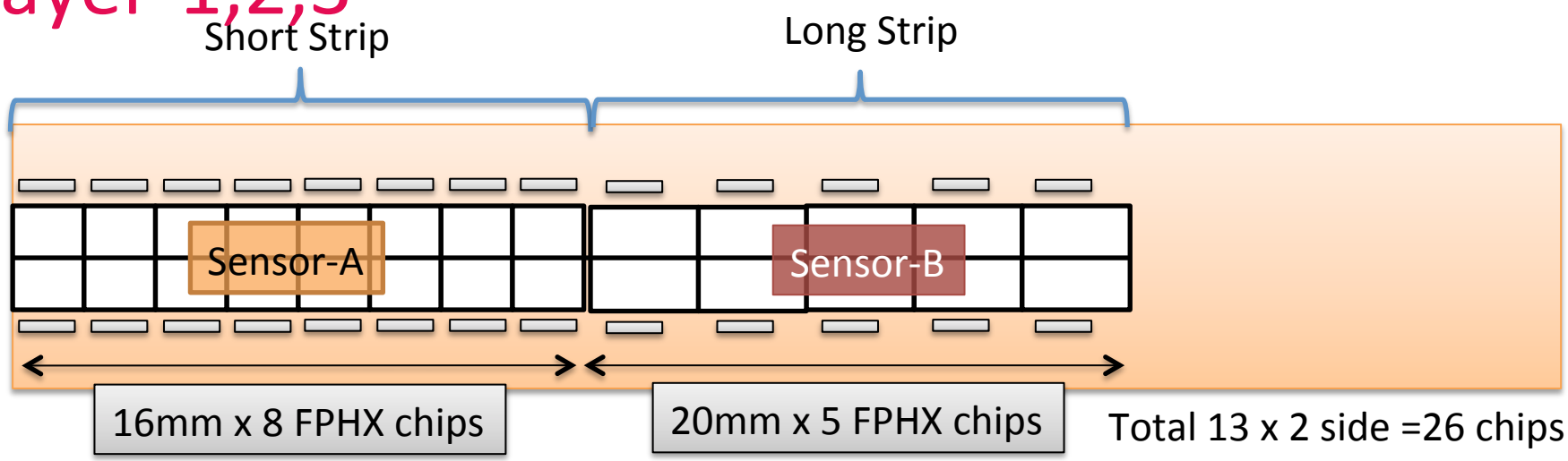


Silicon Module

Layer-0



Layer-1,2,3



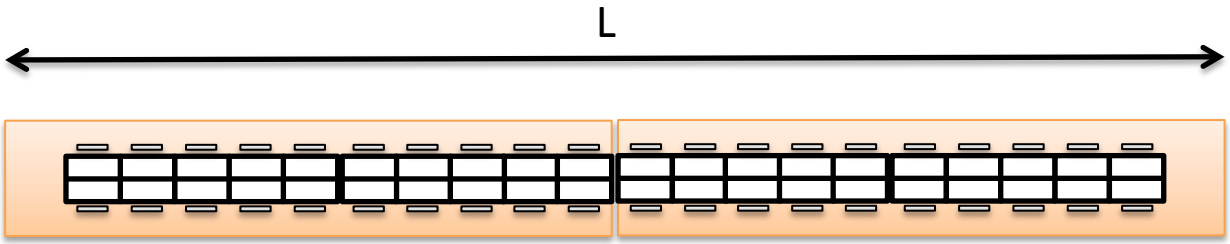
Sensor Module

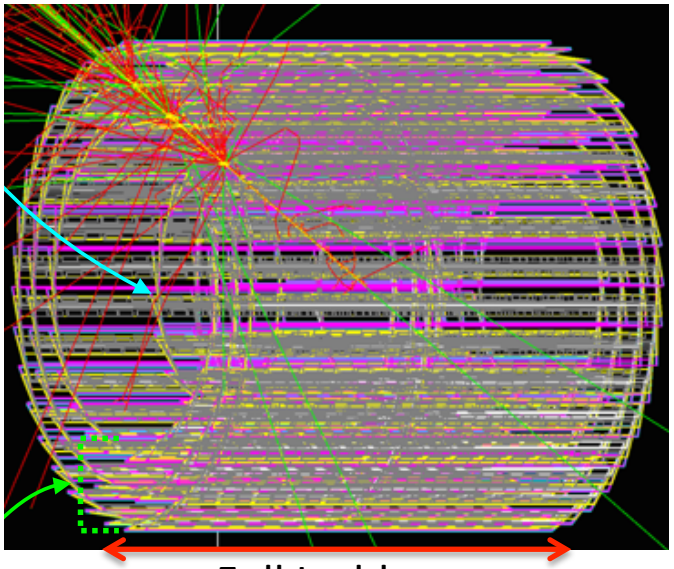
- Composed by 2 silicon strip sensors
- Employ FPHX Chip developed for FVTX
- High Density Integrated Circuit (HDI) is designed based on the HDI of FVTX

Layer	Sensor-A	Sensor-B	Z-Total [mm]	η=1.1 [mm]
0	18 mm x 5 chips	18 mm x 5 chips	180	174
1	16 mm x 8 = 128 mm	20 mm x 5 = 100 mm	228	198
2				223
3				247

Full Ladder

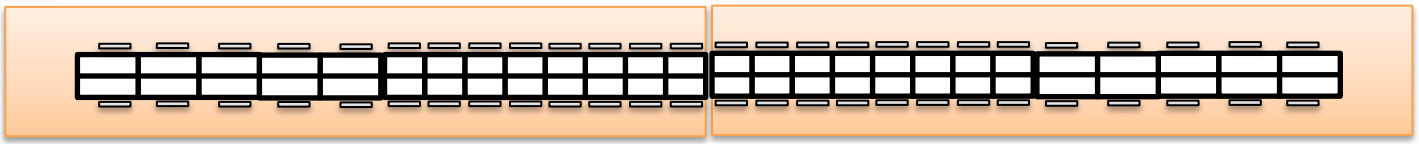
Layer-0



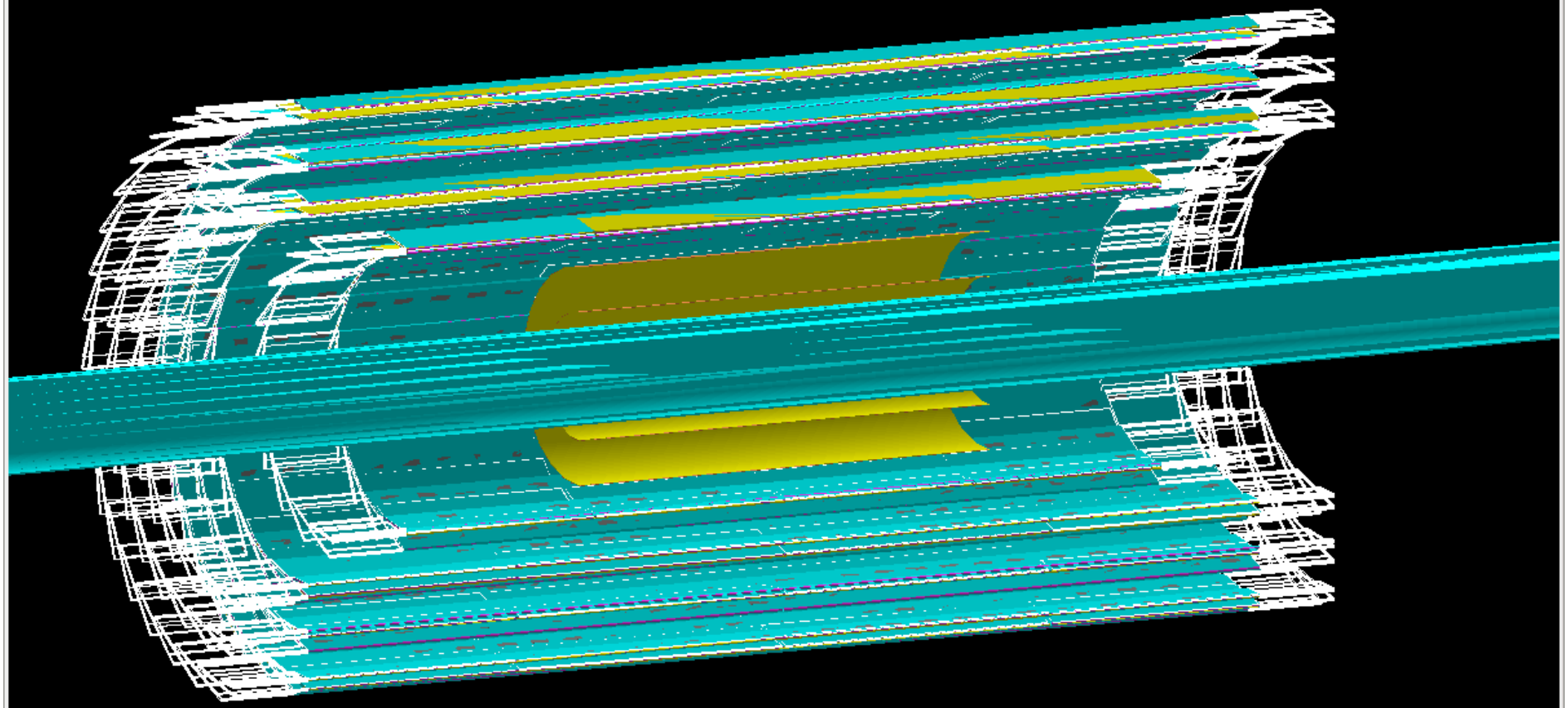


Layer	L [mm]
0	440
1	536
2	
3	

Layer-1,2,3

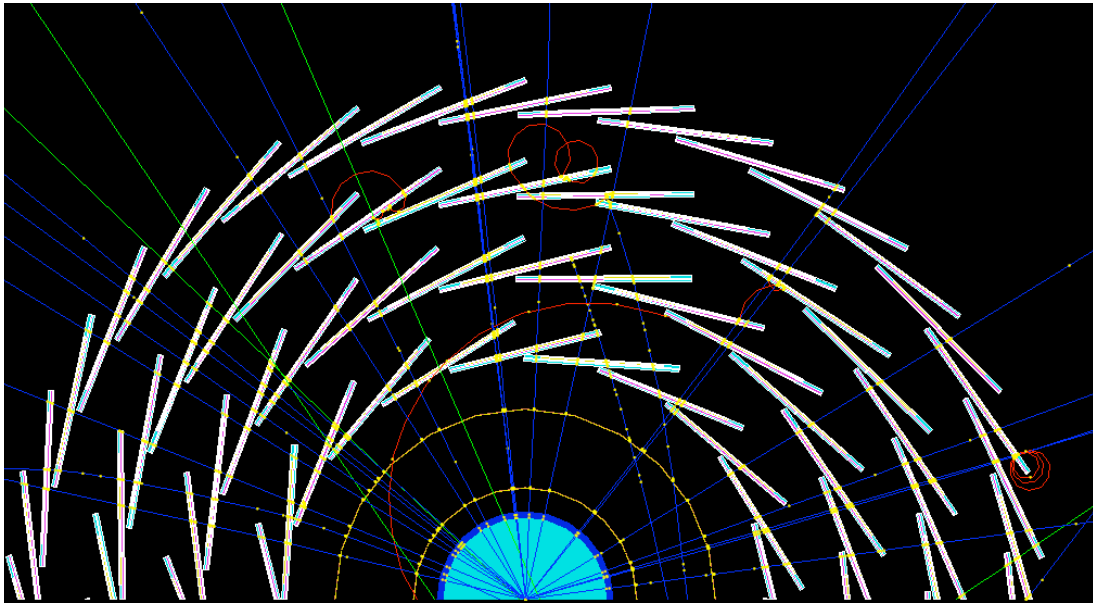


Barrel Design

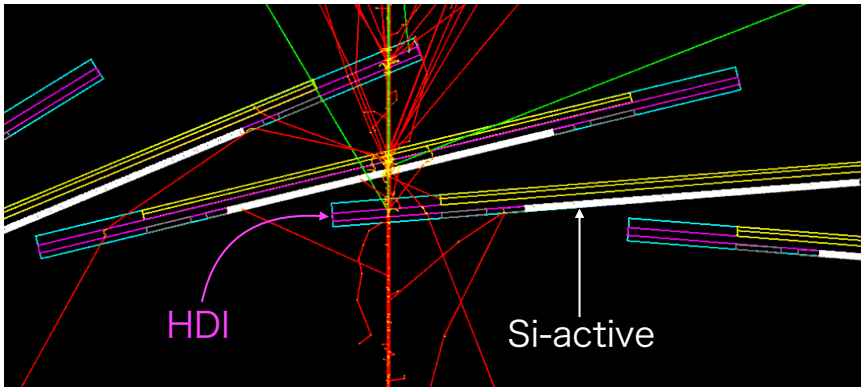


Courtesy of Jin Huang.
GEANT Model for INTT is implemented by Gaku Mitsuka

Barrel Structure



Courtesy of Jin Huang



Layer	# of Ladders	Rotation Angle [deg]
0	20	14.0
1	26	14.0
2	32	12.0
3	38	11.5

ROC Ports Configuration

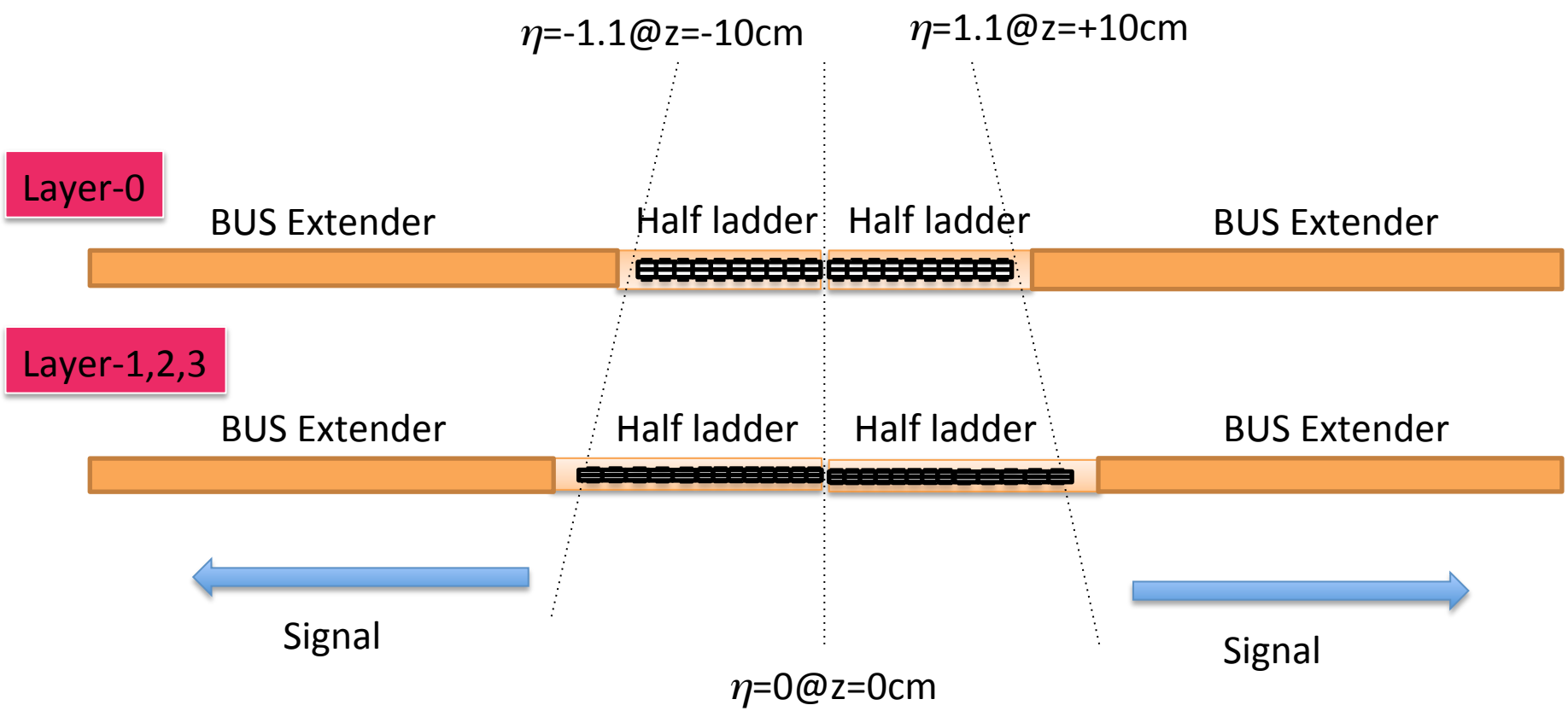
- For one arm

	INTT		Available # of Ports
Layer-0	36	<	48
Layer-1,2,3	90	<	144

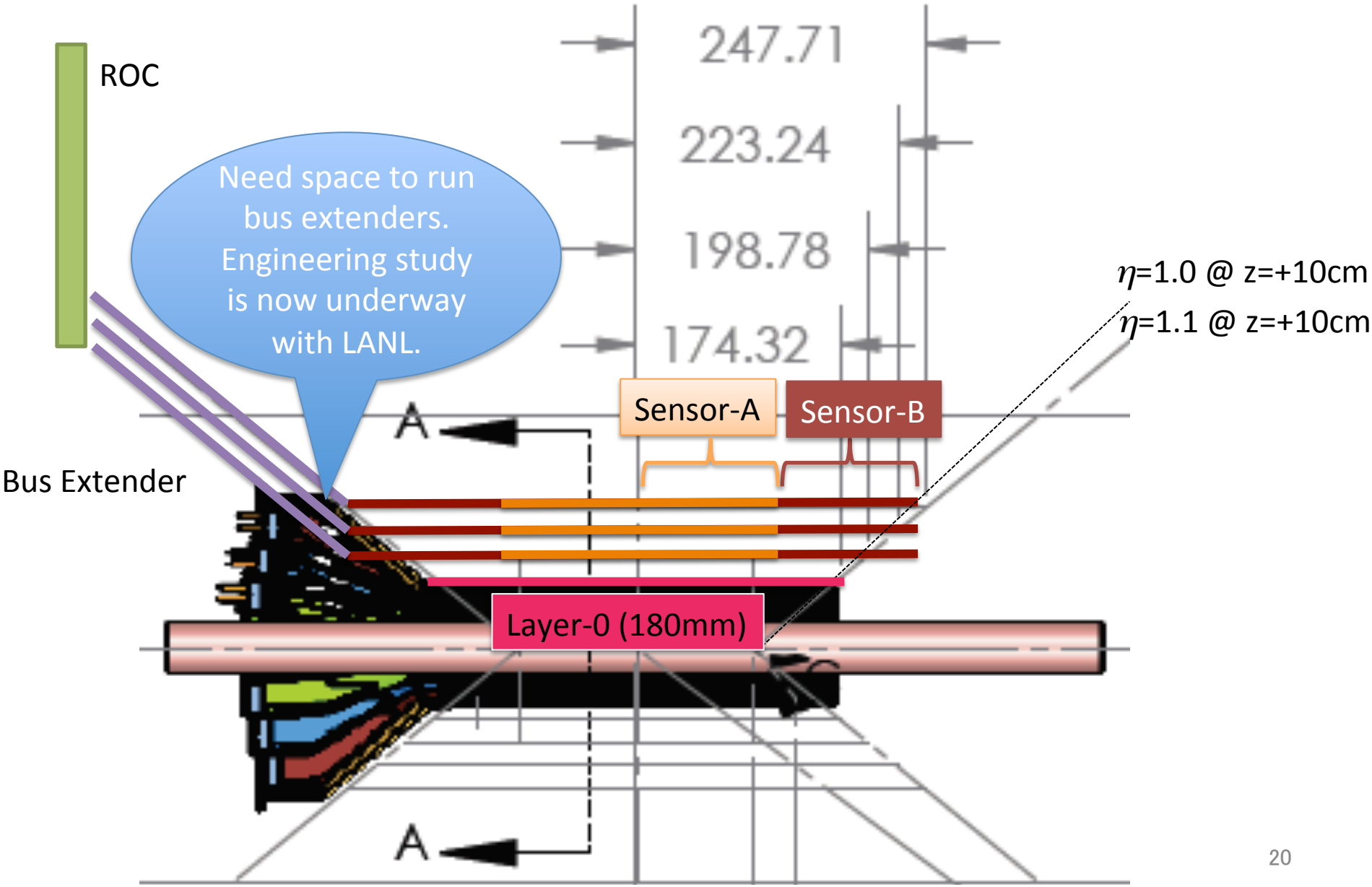
Number of ports to be used nicely fits within available number of ports

Readouts from Both North and South Sides

Signals are transferred from HDIs to outside TPC by BUS extenders

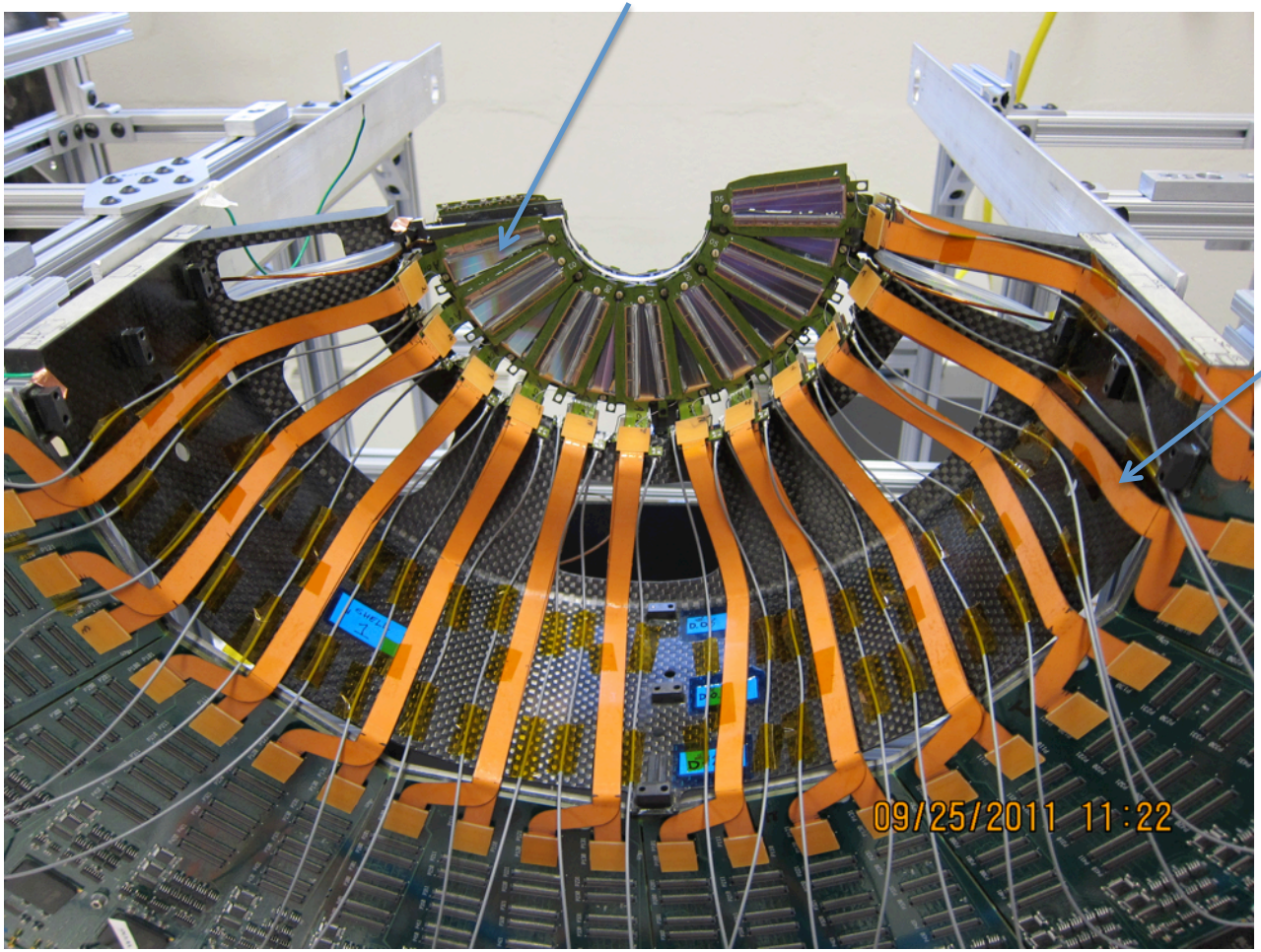


Spatial Conflict with MAPS Readout



FVTX Station-0 Bus Extenders

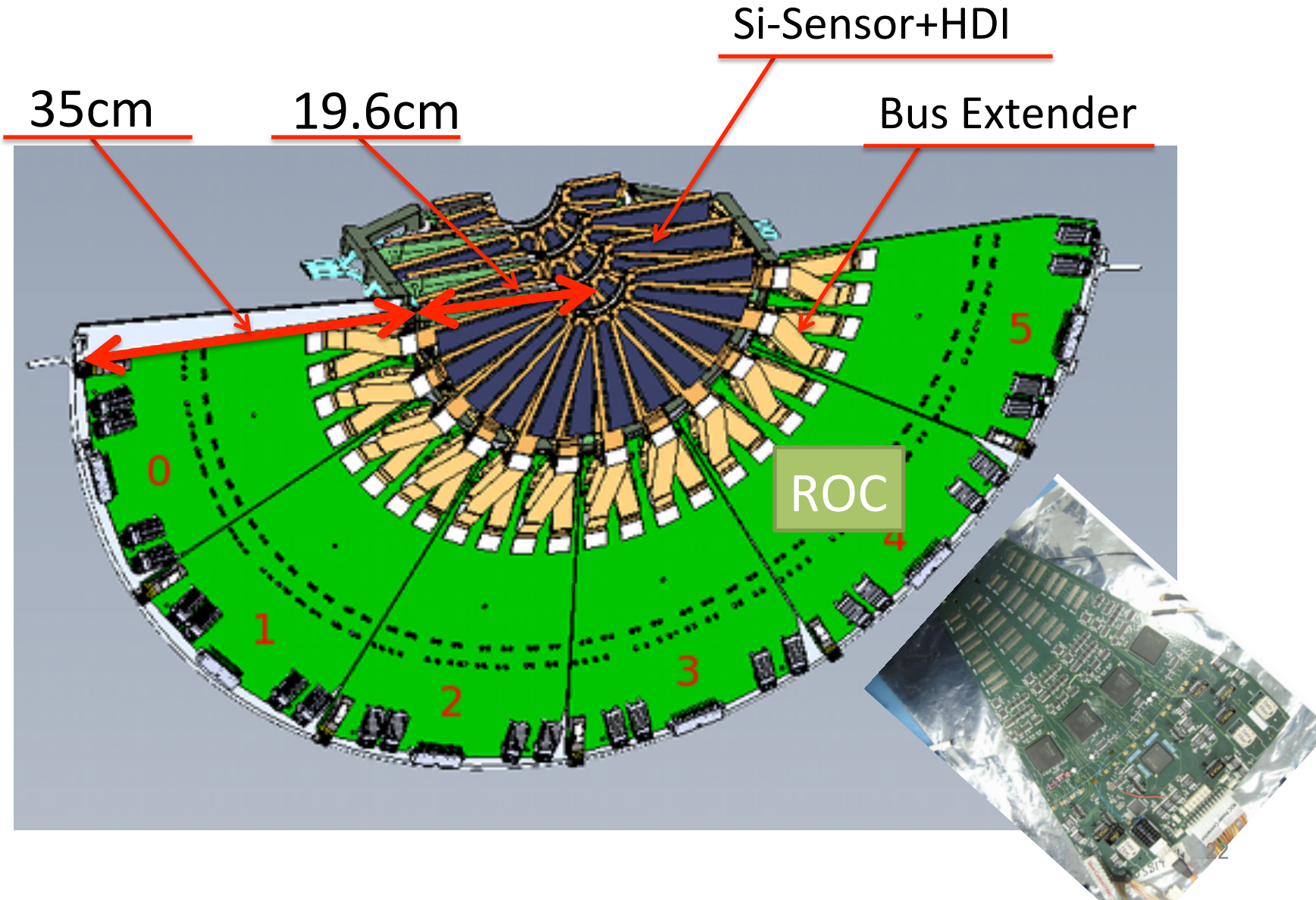
FVTX Station-0 Silicon Module



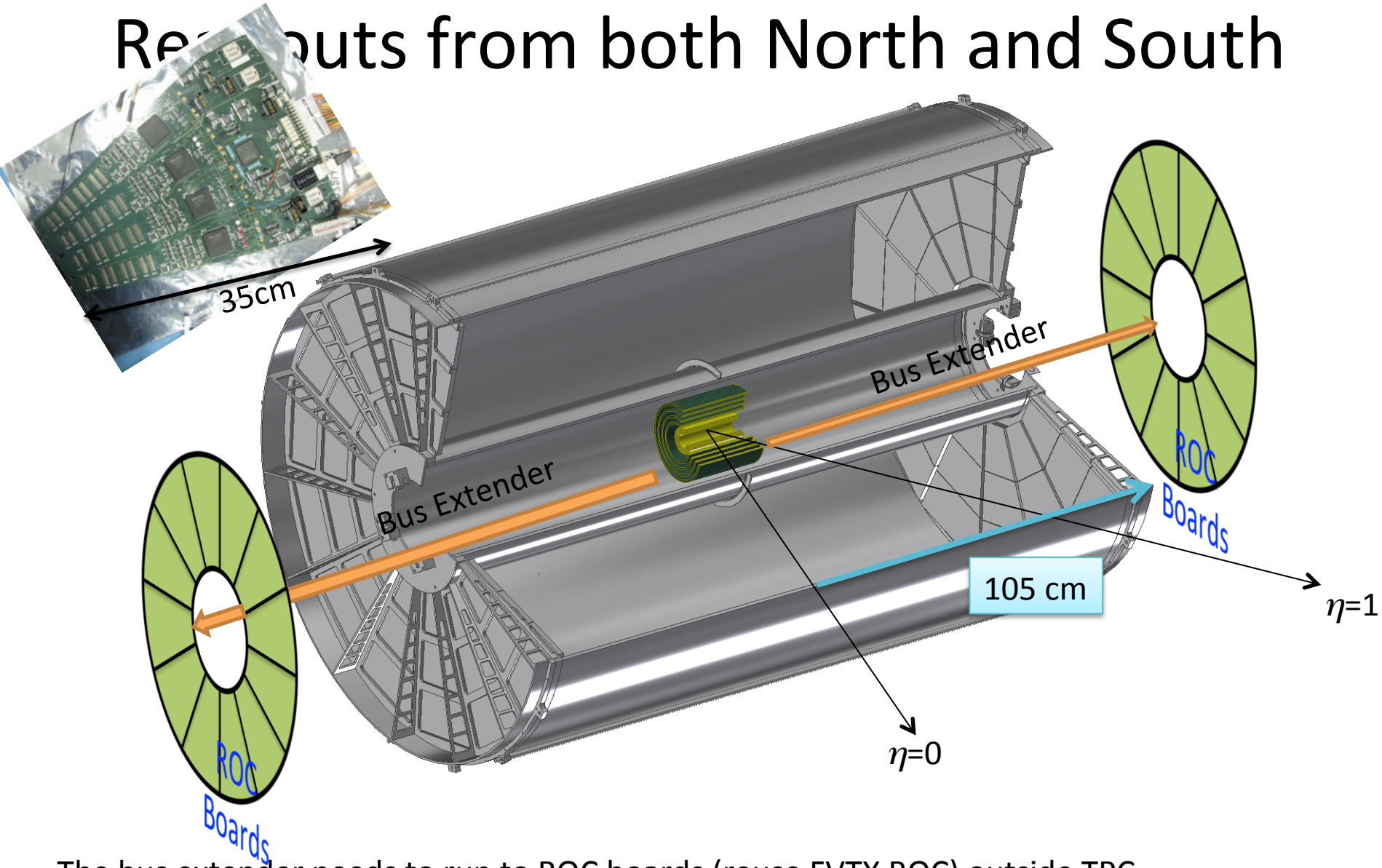
Bus Extender

ROC

FVTX Big Wheel

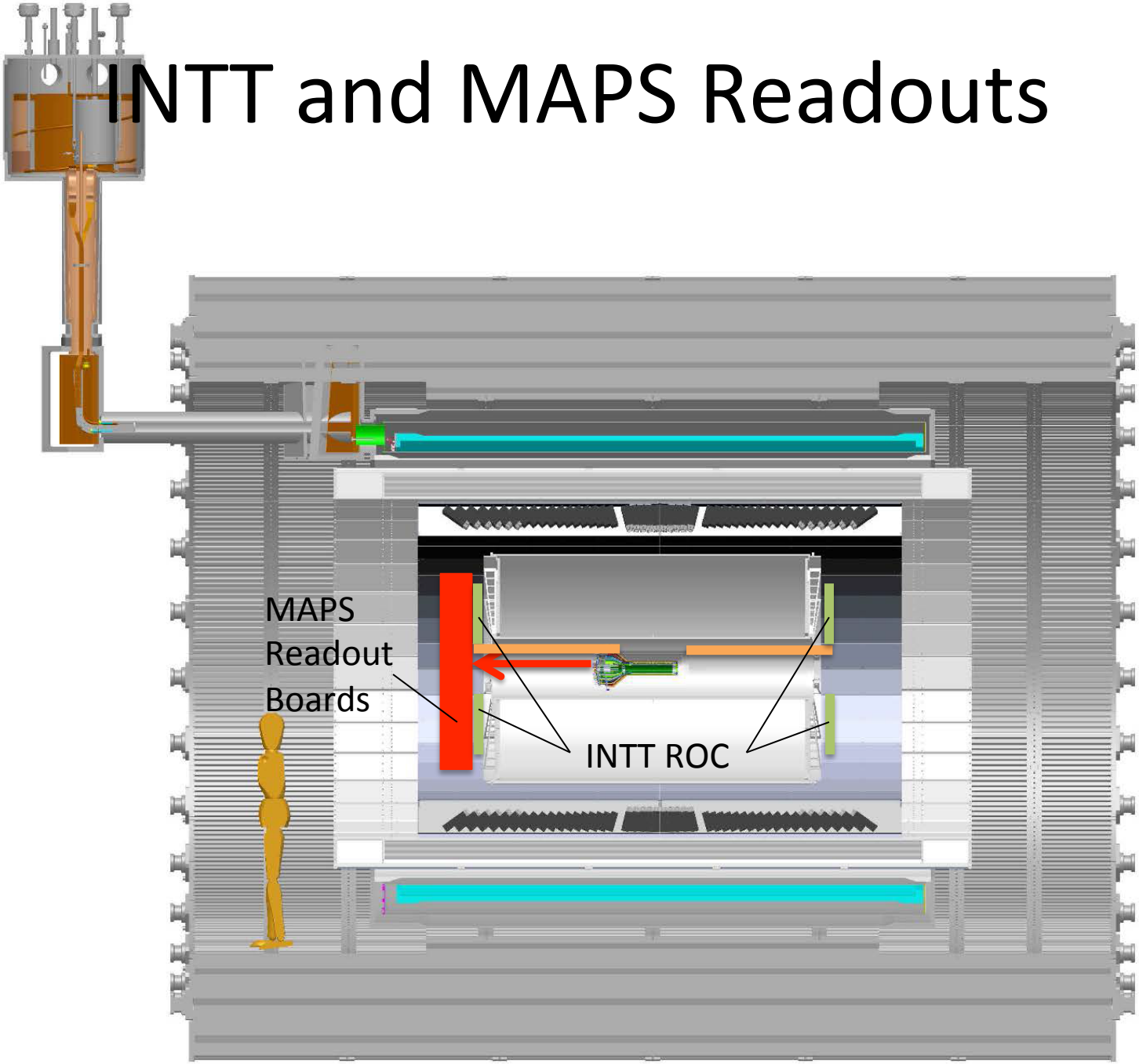


Readouts from both North and South



The bus extender needs to run to ROC boards (reuse FVTX ROC) outside TPC.
Minimum length is 105cm – ladder length + distance to ROC board.

INTT and MAPS Readouts



Geometrical Acceptance (Simulation)

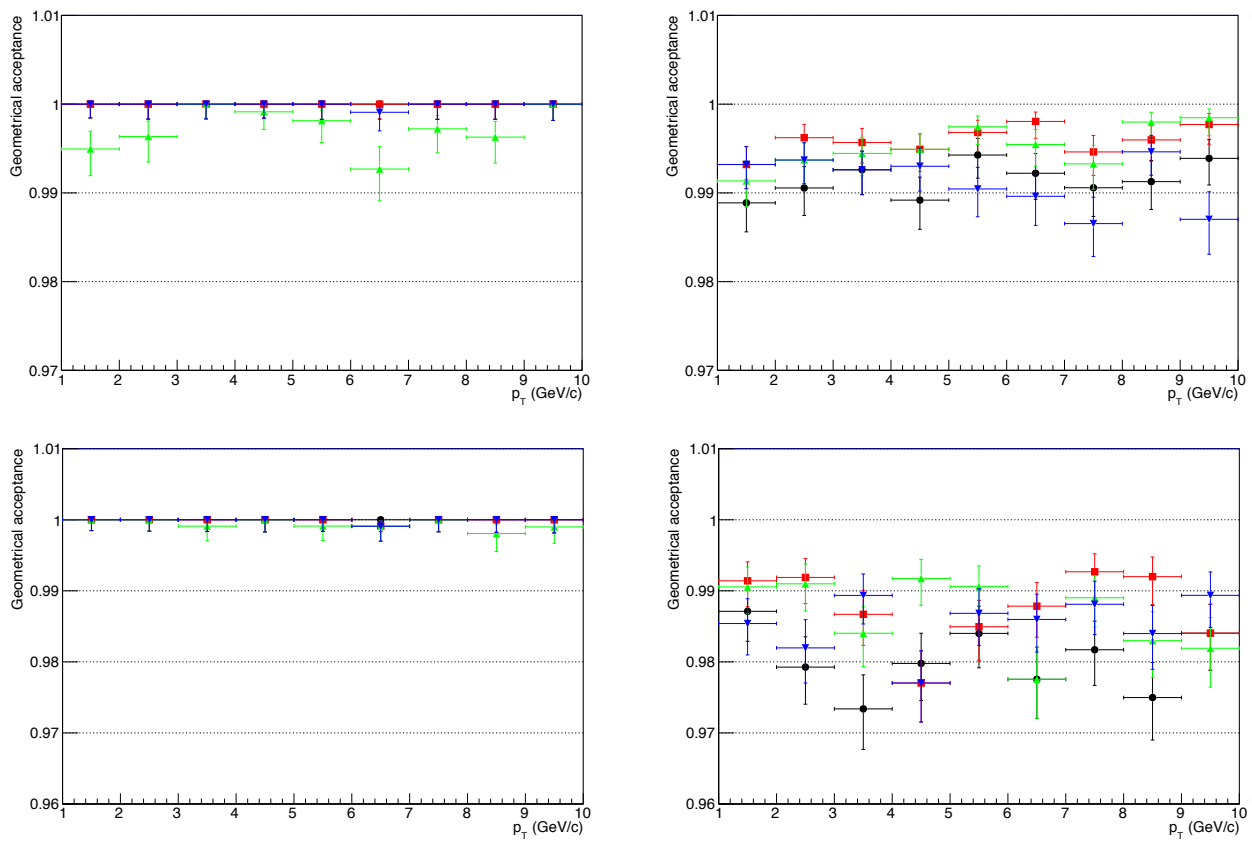
- Ideal case: firing from (0, 0, 0.5cm) to η=0 (0.5cm shift avoids sensor gap.)
- Realistic case: firing from (0, 0, 0) to |η|<1 (verified for |vtx-z|<10cm.)

Layer0 (R=6cm) Layer2 (R=10cm)
Layer1 (R=8cm) Layer3 (R=12cm)

η=0 from the vertex (0,0,0.5cm) |η|<1 from the vertex (0,0,0)

electron

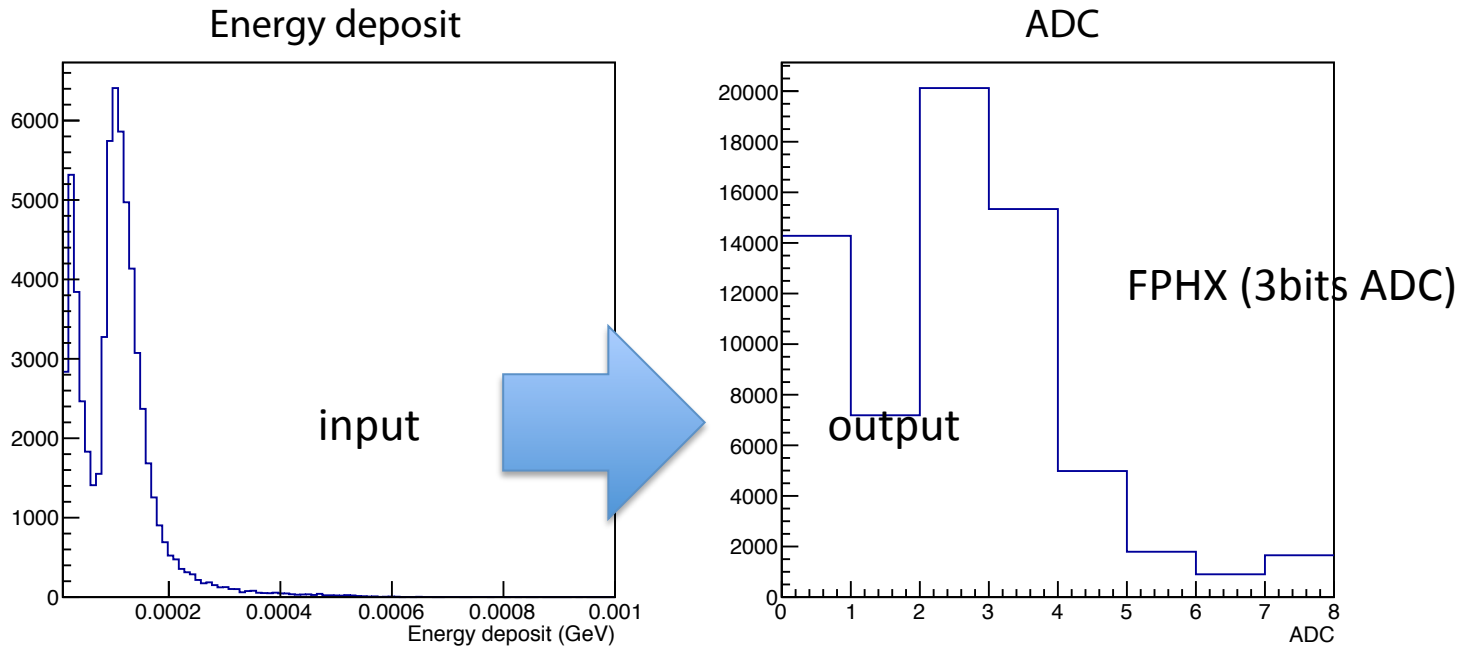
positron



Confirmed to be very high

GEANT Model Development

Deposit energy and ADC distributions



The Edep/ADC factor = 0.39MeV/ADC is temporarily used for visibility. This factor will be modified later by taking account of the FPHX's non-linear ADC thresholds.

Development of the GEANT model is in progress. Once modeling is done, then the tracking algorithm will be developed.

R & D STATUS

INTT Activities at BNL: Detector Construction

- **In 2016:**

  - We built and tested successfully two silicon modules type S1 (SM-S1)
  - SM-S1 will not be used for INTT. SM-S1 corresponds to an old detector configuration.
  - SM-S1 modules provide excellent inputs for the HDI bus and silicon sensor for the silicon module prototype for INTT detector.

  → Our finding's/issues from SM-S1 (sensor and HDI) and requests for improvements have been sent to the companies HPK (sensor) and Yamashita (HDI) in Japan.

- **Beginning 2017:**

  - We will receive prototype sensors and HDI bus to build first prototype silicon modules SM-S0 for INTT detector

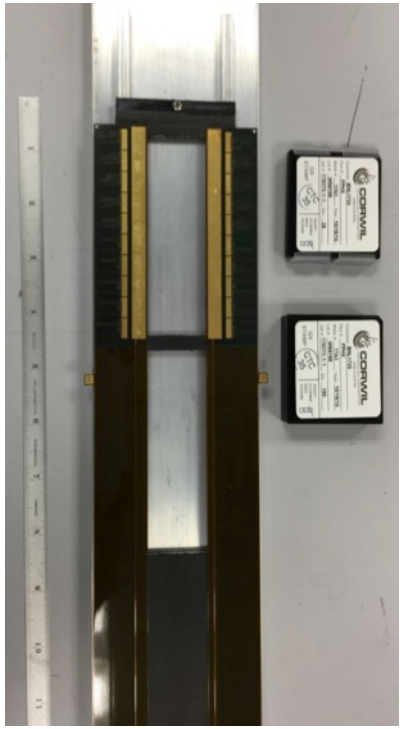
INTT Activities at BNL: Detector Construction

Construction steps:

Step 1

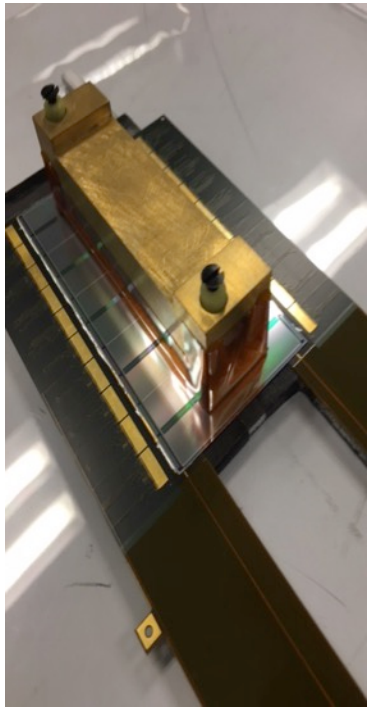
mechanical support stave made of CFC by M. Lenz

Step 2



Assembly/gluing HDI/Chips (20) by RN

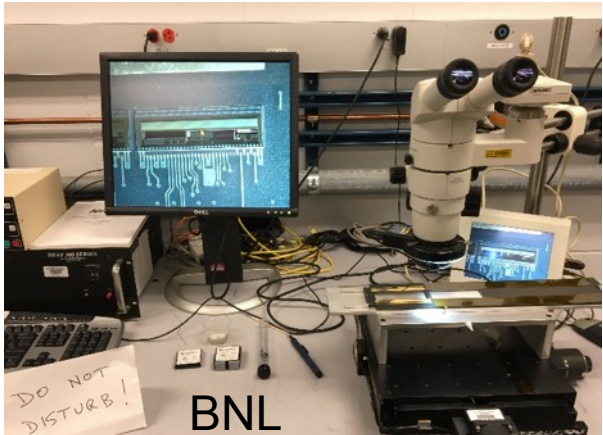
Step 3



Assembly/alignment/gluing sensor on HDI by RN

Step 4

Wire-bonding chips to HDIs and sensor to chips by D. Panelli at Instrumentation Division

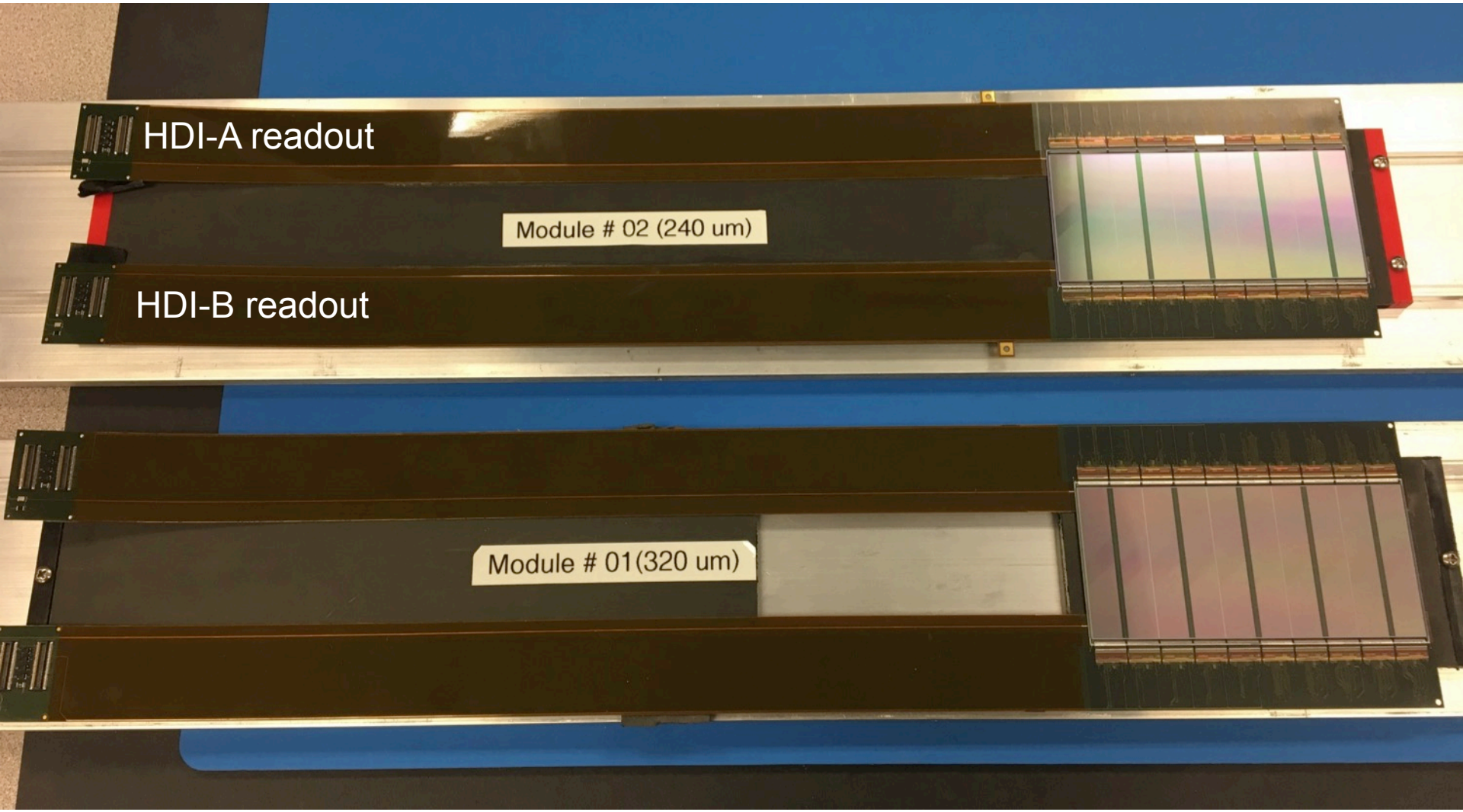


BNL

INTT Activities at BNL: Detector Construction

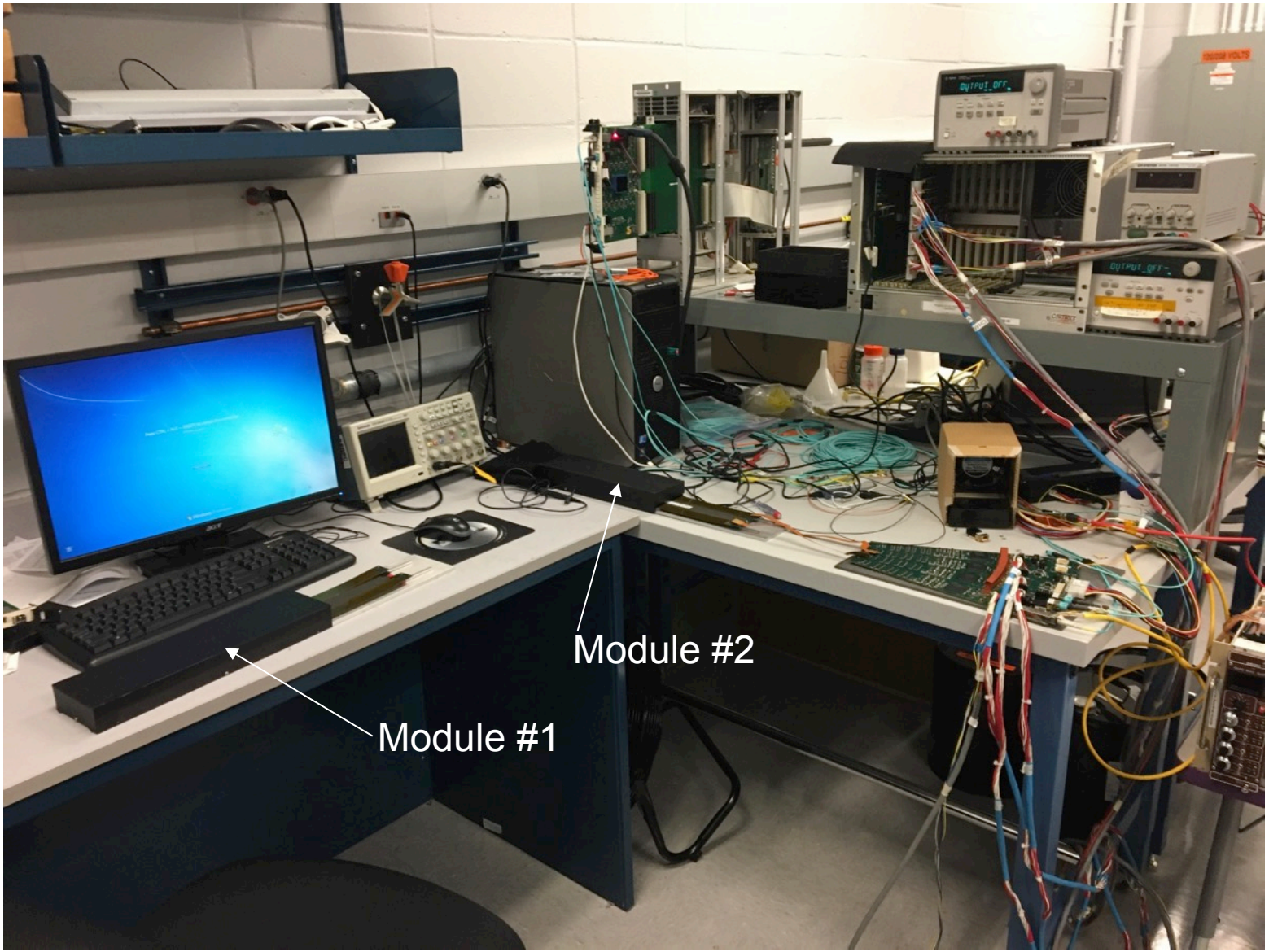
We built two silicon modules with two different silicon sensor thicknesses:

Module #1: 320 um silicon sensor and Module #2 : 240 um silicon sensor



INTT Activities at BNL: Detector Construction

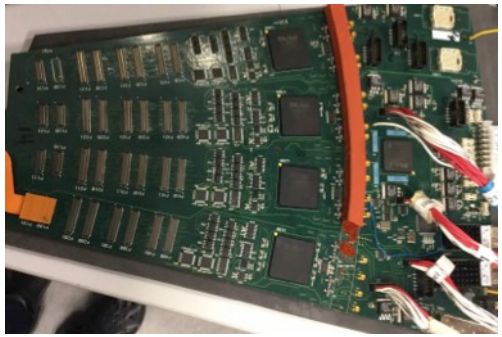
Module Test Bench at BNL



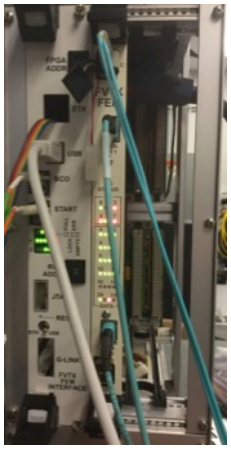
Readout system for tests

Silicon Module
(Si+FPHX chips+HDIs)

Readout Controller (ROC)



Front End Module (FEM)



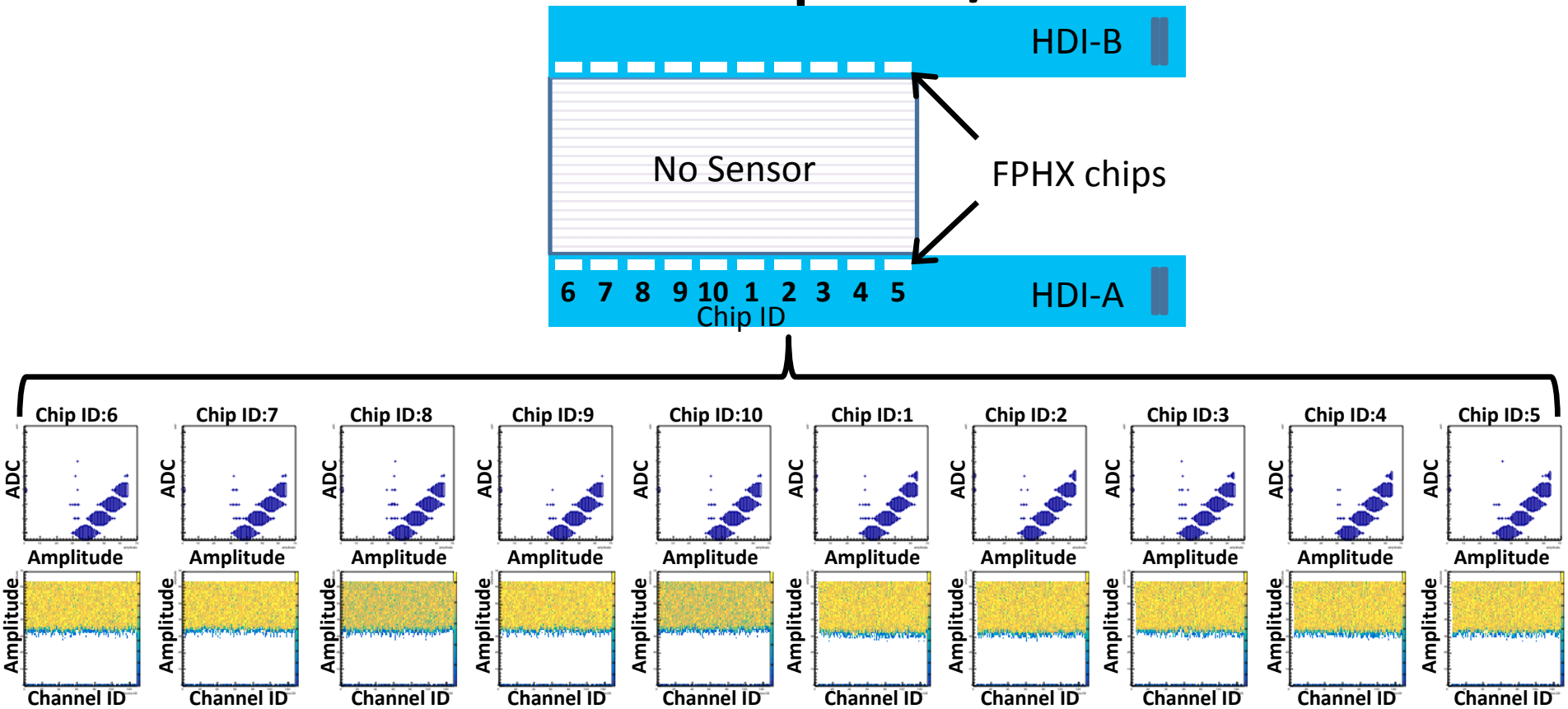
- Entire readout system including DAQ is the one used for FVTX.
  - ✓ Only Silicon module is exception.
- HDI has 10 FPHX chips + 1 connector.
- Slow control is made through FEM-Interface Board (FEM-IB) by PC.
- Test procedure:

  Step1: Check if FPHX chips on HDI work with calibration pulses
  - ✓ Then, Si sensors are mounted on HDI and wire-bonded to FPHX chips.

  Step2: Do step1 again after wire-bonding of Si sensors to FPHX chips.

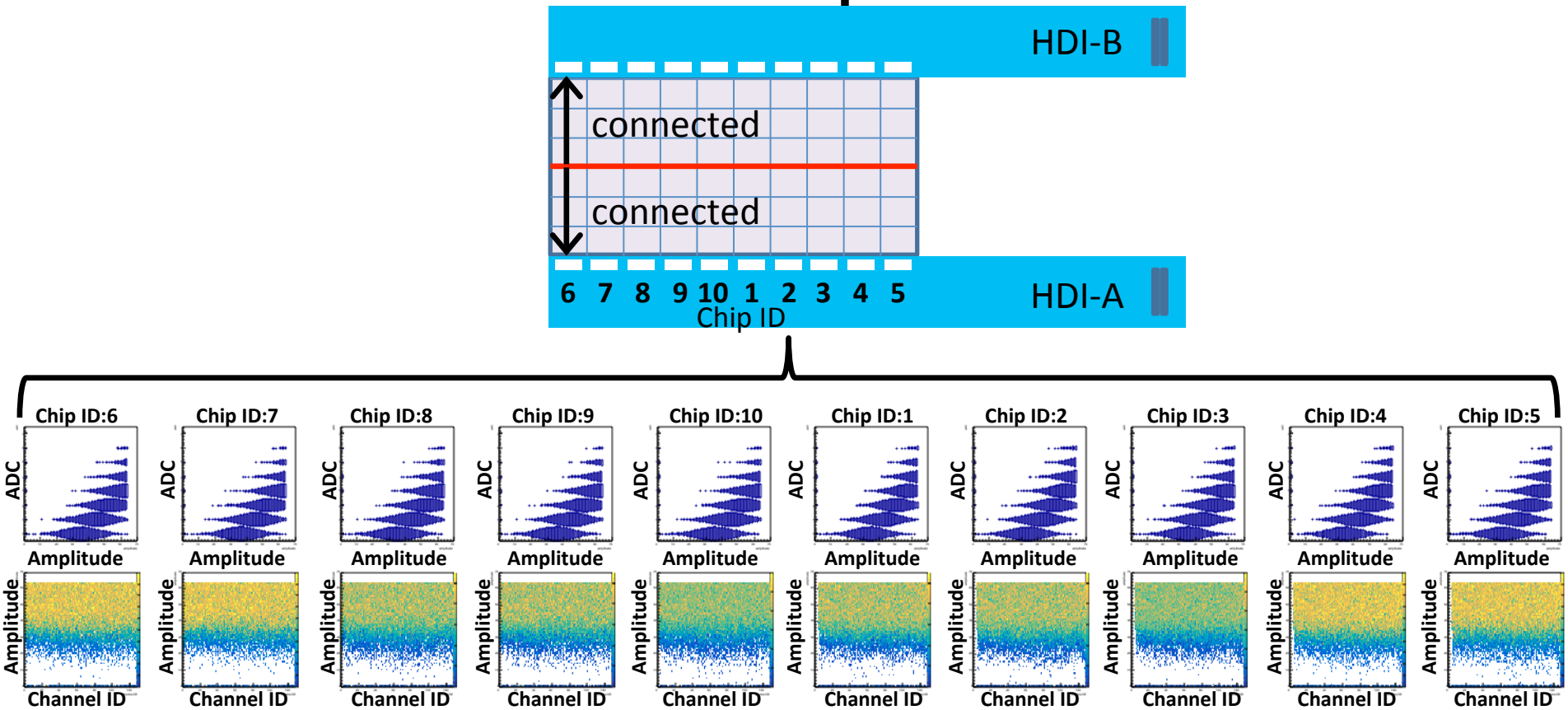
Testing done by Yorito Yamaguchi, Gaku Mitsuka, Hidekazu Masuda

Check1: FPHX chips w/o Si sensors



- Check if FPHX chips on HDI are working correctly with calibration pulses.
  - ✓ Upper: Pulse amplitude vs ADC, Bottom: Channel ID vs Pulse amplitude
  - ✓ Clear correlation between pulse amplitudes and ADC (with linear charge-ADC configuration)
  - ✓ All channels (128 channels for each chip) look good.

Check2: FPHX chips w Si sensors

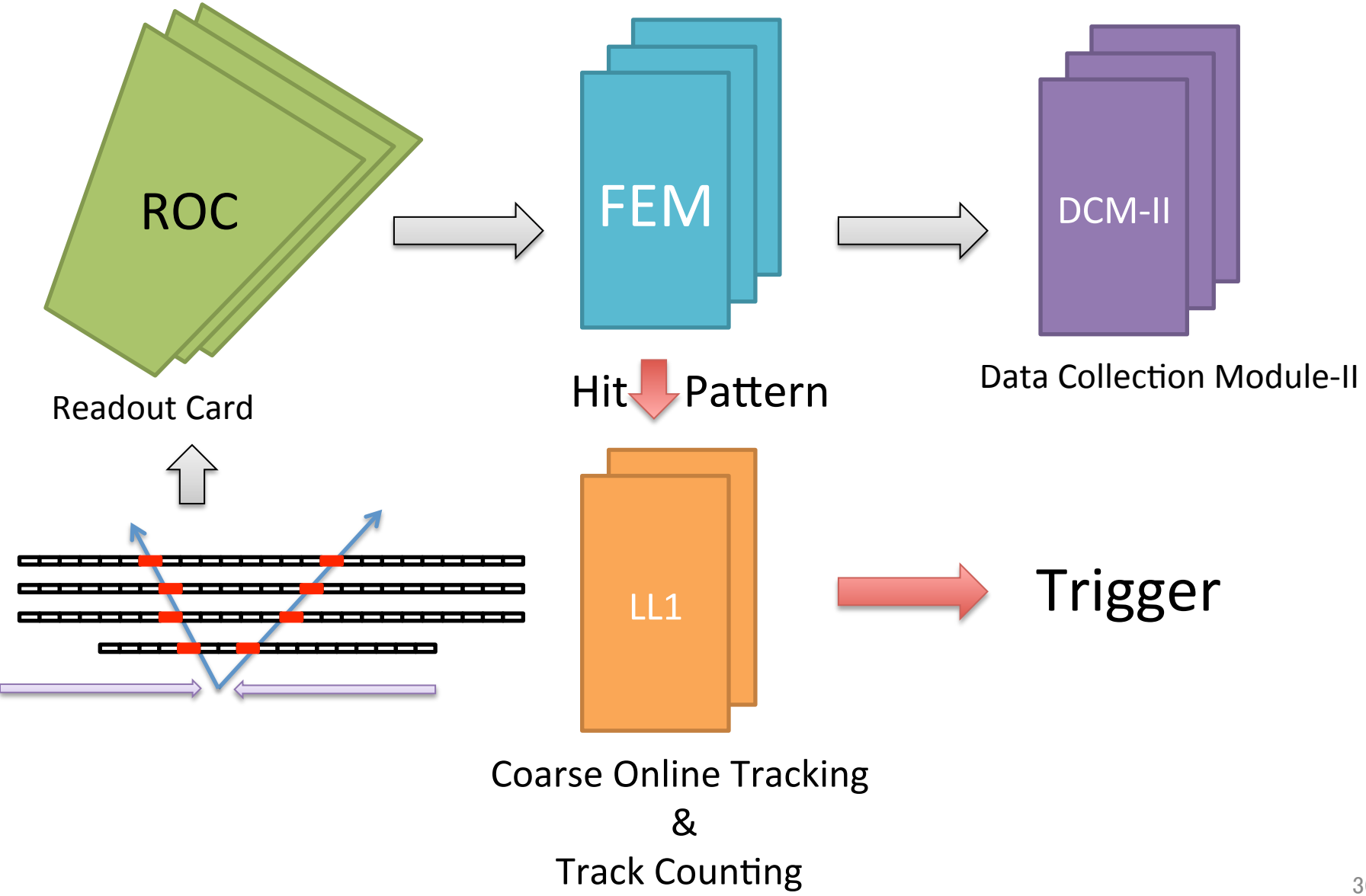


- Check the status of the FPHX chips after the Si sensors was bonded.
  - ✓ Bias voltage (100V) was applied to the Si sensors for both HDIs.
  - ✓ Get more noisy, but still can see clear correlation between pulse amplitudes and ADC

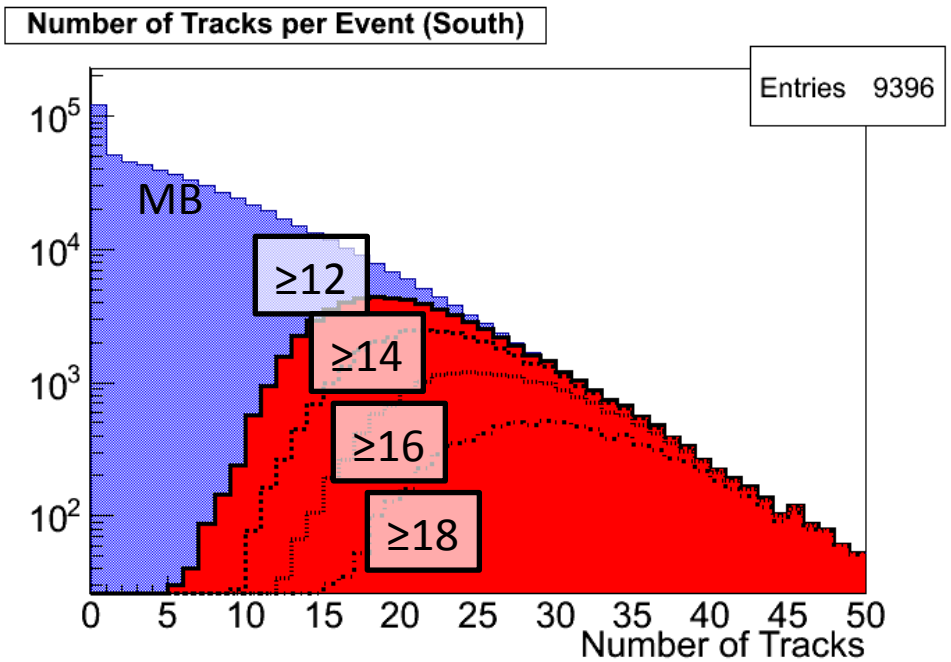
INTT Activities at BNL: Detector Construction

New facility for wire-bonding and encapsulation at Instrumentation Division, BNL

Tracking Trigger

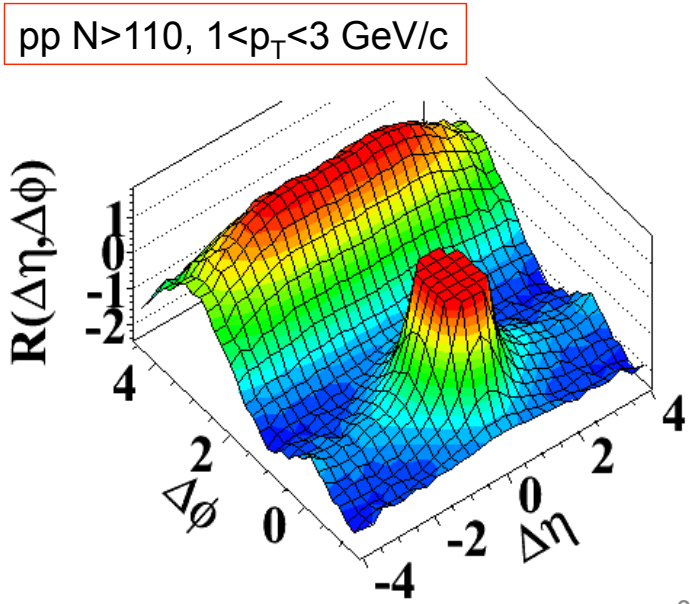


High Multiplicity and MB Trigger



FVTX High Multiplicity Trigger in pAu

Two particle Correlation in small systems



Takashi Hachiya, Hidekazu Masuda, Itaru Nakagawa

R&D Schedule JFY2016

2016 Month	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	Resource	Design
s1 Prototype-I															Production
Silicon Sensor														RIKEN	Test
HDI														RIKEN	
Silicon Module														RBRC,BNL	
s0 Prototype-I															
Silicon Sensor														RIKEN,BNL	
HDI														RIKEN	
Silicon Module														RBRC,BNL	

Today

Summary

- INTT is designed to be low cost with established technology by re-using FVTX readouts.
- Prototype Si+HDI were successfully readout with calibration pulse.
- Confirmed the prototype gives consistent output data format with FVTX Readout chain
- Developments in the engineering and tracking algorithm are to be proceeded in the next phase.

BACKUP

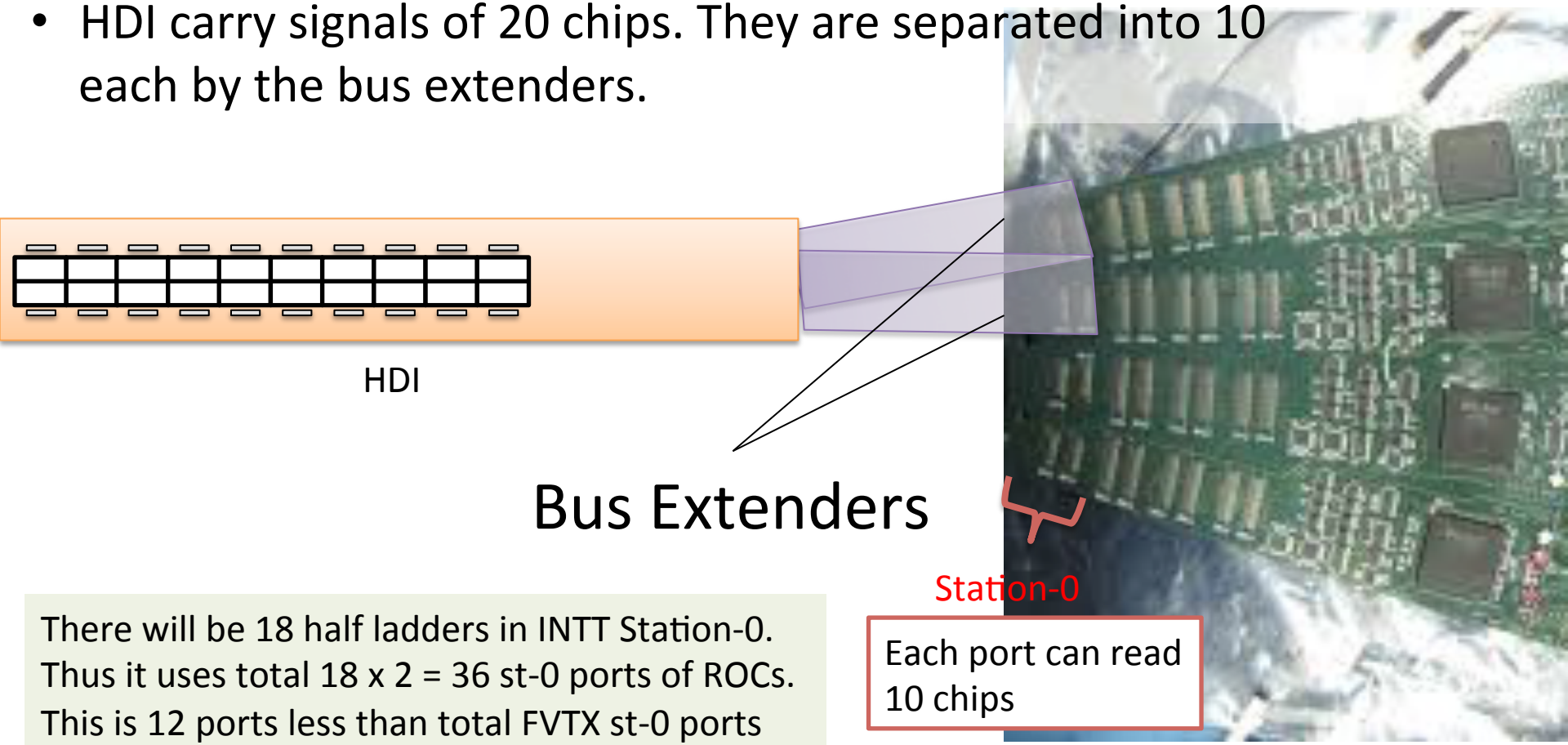
Collaboration

- RIKEN (Y. Akiba, I. Nakagawa)
- RBRC (T. Hachiya, G. Mitsuka,Y. Yamaguchi)
- BNL (J. Huang, M. Lenz, E. Mannel, R. Nouicer, R. Pisani)
- Rikkyo (H. Masuda, D. Nemoto, Y. Kawashima)
- Nara woman's university (M. Shimomura)
- LANL (M. Brooks, M. Liu)
- New Mexico (D. Field)
- J-Parc (S. Hasegawa, H. Sako)

*FVTX expert

ROC Port Allocation for Layer-0

- Layer-0 signals are connected to Station-0 ports of FVTX.
- HDI carry signals of 20 chips. They are separated into 10 each by the bus extenders.



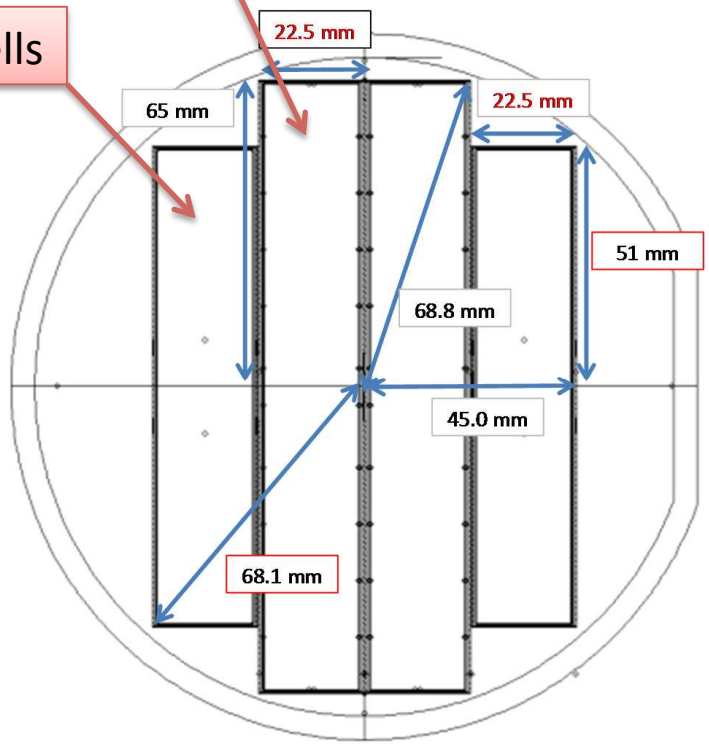
There will be 18 half ladders in INTT Station-0. Thus it uses total 18 x 2 = 36 st-0 ports of ROCs. This is 12 ports less than total FVTX st-0 ports (48 ports)

Layer-1,2,3 Silicon Sensors

Sensor Layouts in 6 inch Wafer

16mm strip x 8 cells

20mm strip x 5 cells



Maximum Sensor length is 135mm for 22.5mm width sensor

※左図

赤字（幅）：記載ミス

赤枠：修正

Strip length = 20mm
Number of cells = 5

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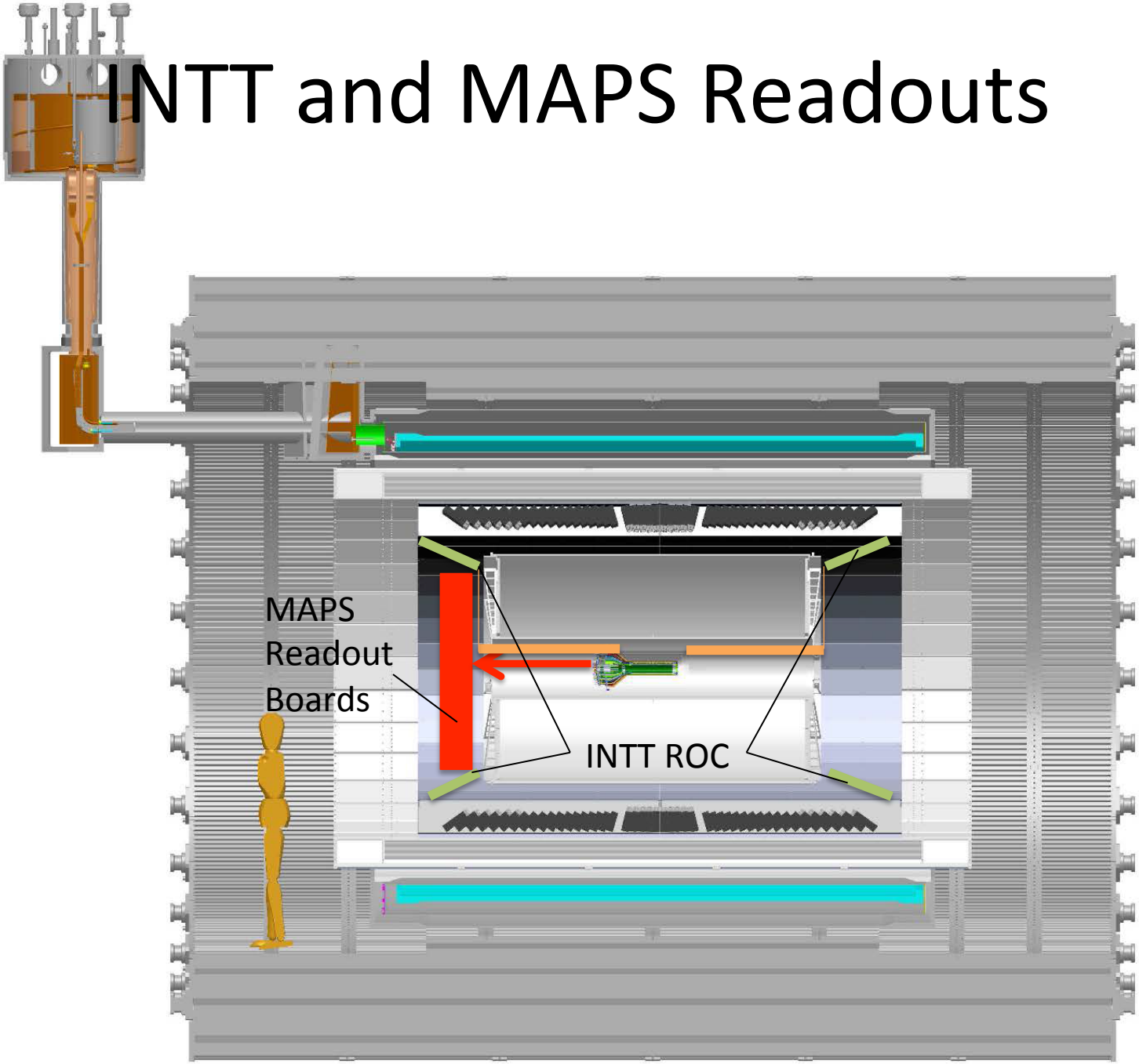
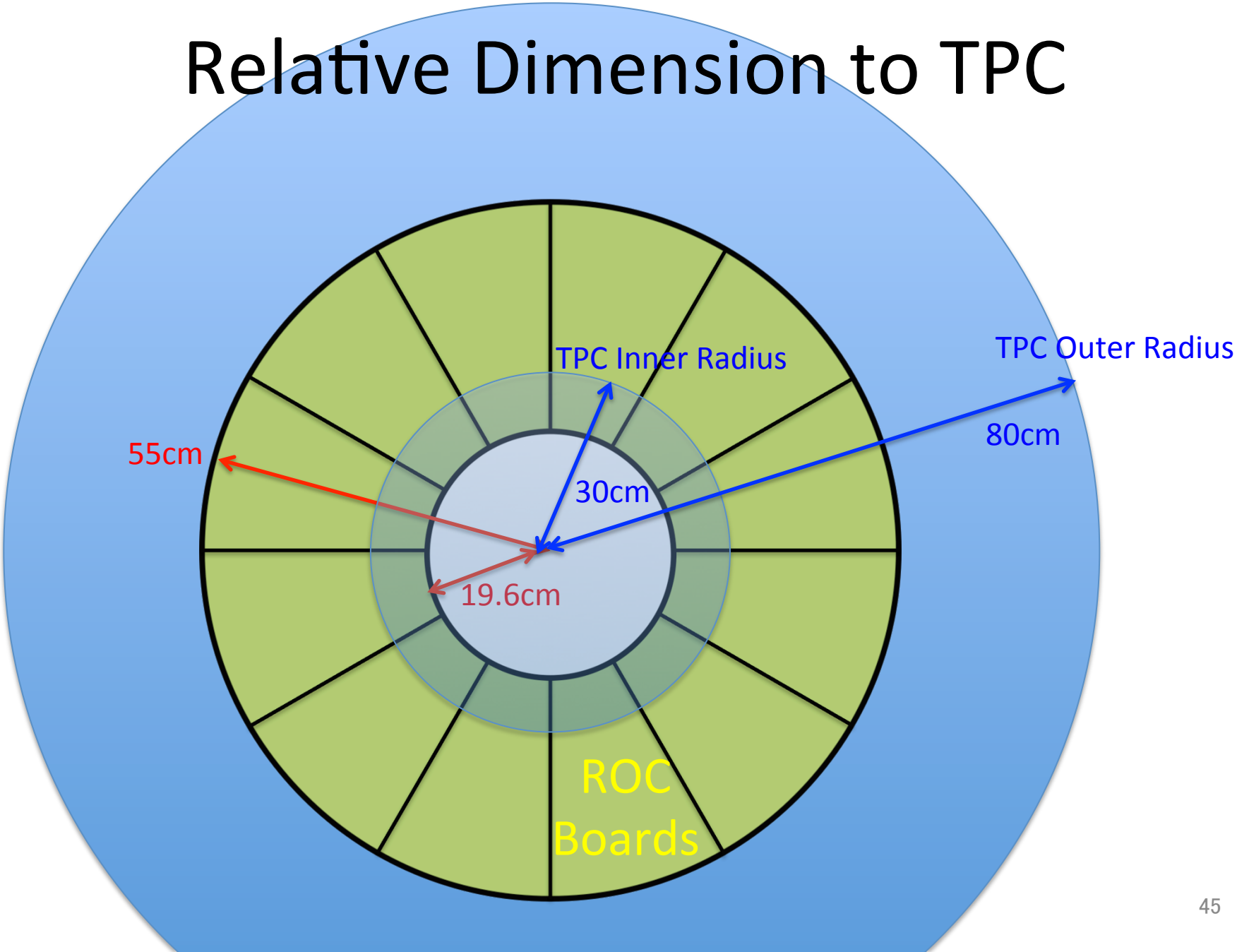
Strip length=16mm x 8 cells = 64mm
Strip length=20mm x 5 cells = 10mm

x 2 sensors will fit in 1 wafer

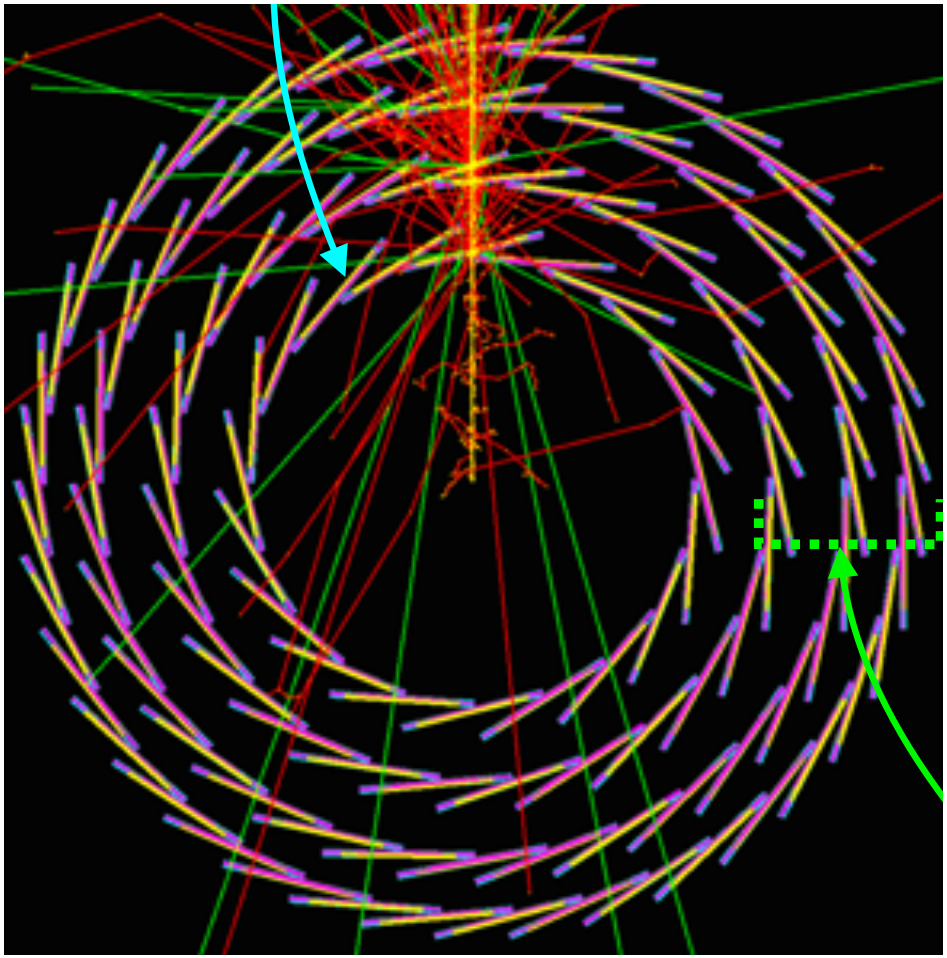
INTT and MAPS Readouts

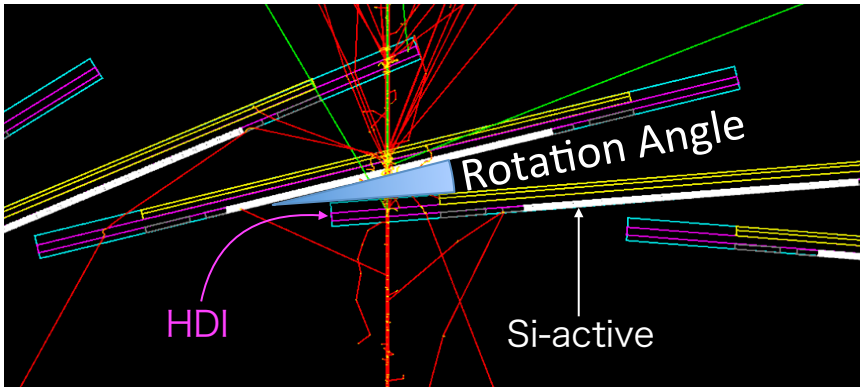


Relative Dimension to TPC



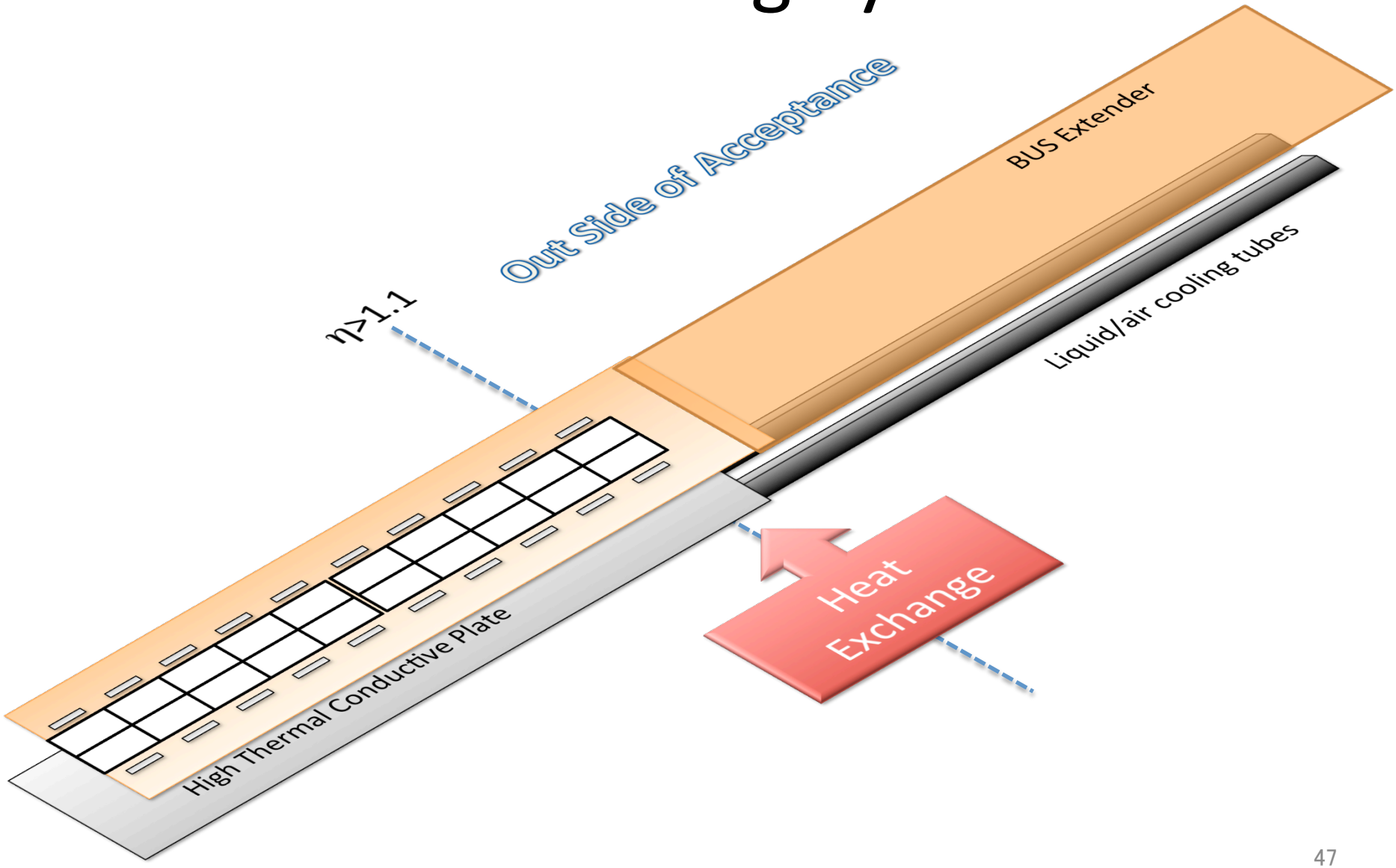
Barrel





Layer	# of Ladders	Rotation Angle [deg]
0	20	14.0
1	26	14.0
2	32	12.0
3	38	11.5

INTT Cooling System



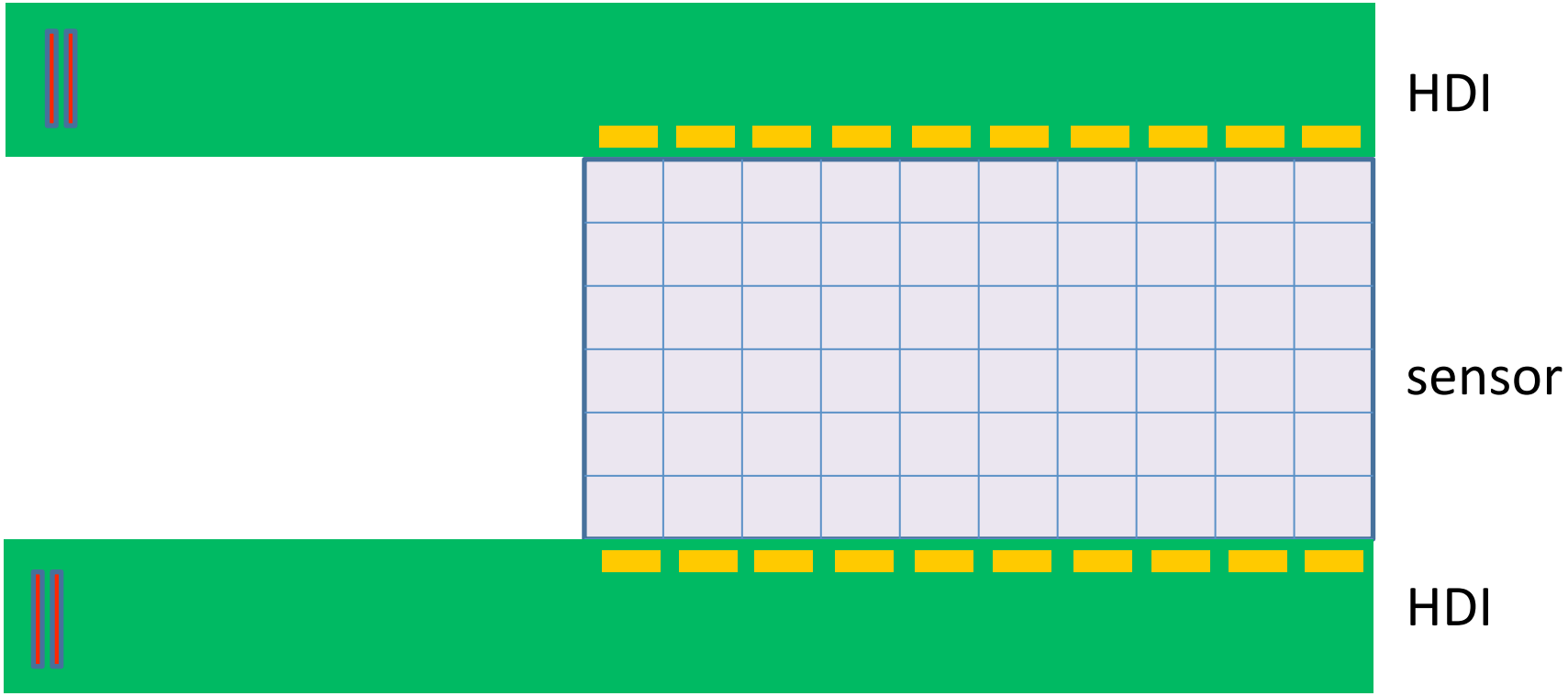
ROC Total Number of Ports/Arm

	Per Arm	Total (2 arms)
Station-0	48	96
Station-1,2,3	144	288

Number of Ladders for sPHENIX INTT

R [cm]	Per Arm	Total (2 arms)
6 (Layer 0)	18	36
8 (Layer 1)	24	48
10 (Layer 2)	30	60
12 (Layer 3)	36	72
Total	**108 (116?)**	**216**

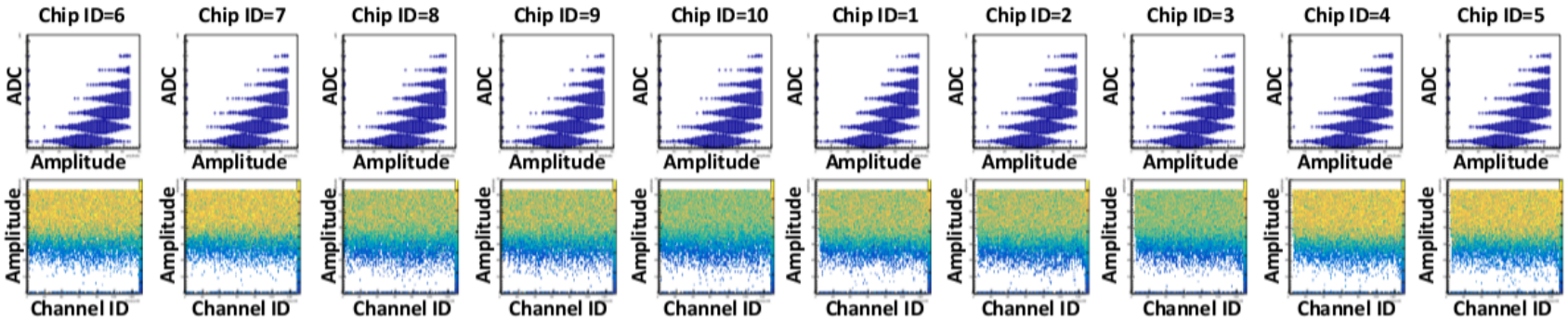
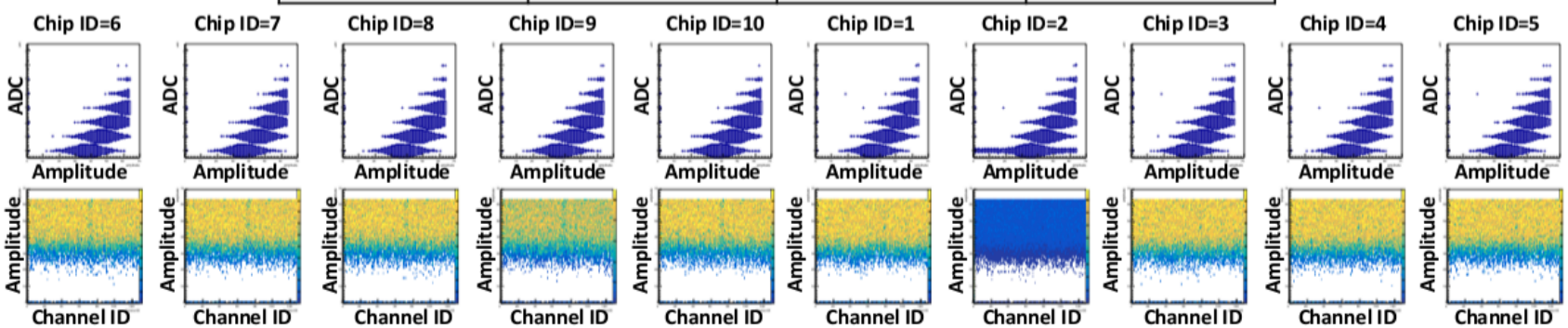
Basically, all INTT readouts can be fit within Station-1,2,3 ports of the ROC.


HDI
sensor
HDI

INTT Activities at BNL: Detector Construction

Test Results of Module #2 at BNL (HDI-A and HDI-B tested independently) by Gaku and Yorito

Test #	Readout	Bias-A	Bias-B
2	A	100V	100V



Test #	Readout	Bias-A	Bias-B
3	B	100V	100V