WBS 6.4
Liquid Argon Calorimeter System Technical Overview of 6.4.x.1 (FE) and 6.4.x.2 (Optics)

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Columbia University

NSF Conceptual Design Review of the U.S. ATLAS HL-LHC Upgrade
National Science Foundation
Arlington, VA
March 8 - 10, 2016

US LAr WBS Structure and Institutions

6.4 Liquid Argon WBS (NSF)	
Deliverable/Item	**Institution**
FE Electronics	
6.4.1.1 FE Electronics	Columbia (John Parsons)
6.4.2.1 FE Electronics	UT Austin (Tim Andeen)
Optics	
6.4.3.2 Optics	SMU (Jingbo Ye)
BE Electronics	
6.4.4.3 BE Electronics	Stony Brook (John Hobbs)
6.4.5.3 BE Electronics	U Arizona (Ken Johns)

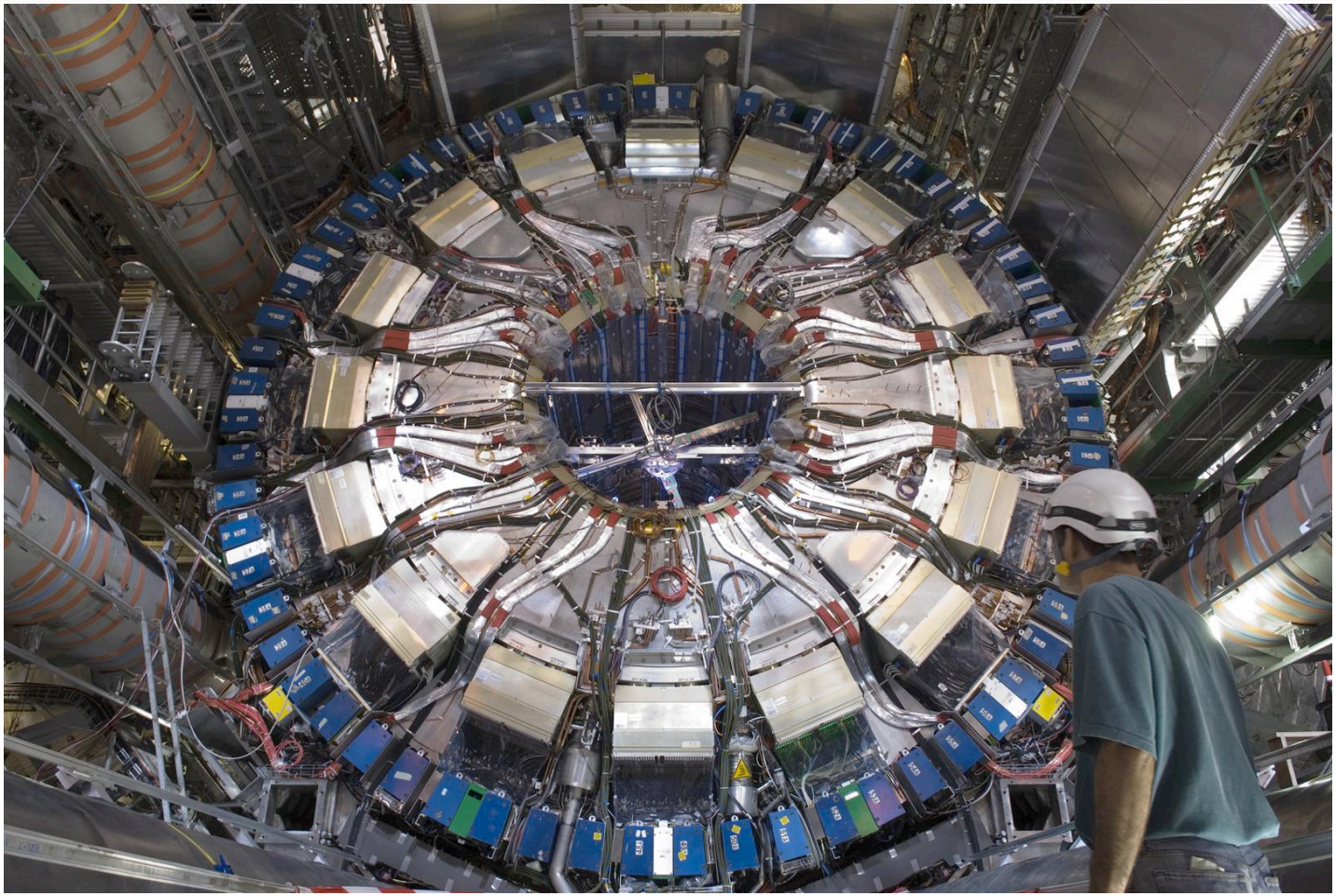
- NSF deliverables organized into 3 BOEs, including efforts by 5 university groups
- DOE scope includes PA/shaper ASIC and System Integration

HL-LHC LAr FE Readout Specifications

- Main functionality:
  - Receive raw detector signals, apply analog filtering (amplification and shaping) to optimize signal-to-noise, digitize the signals at 40 MHz, serialize the data and transmit off detector via 10 Gbps optical links

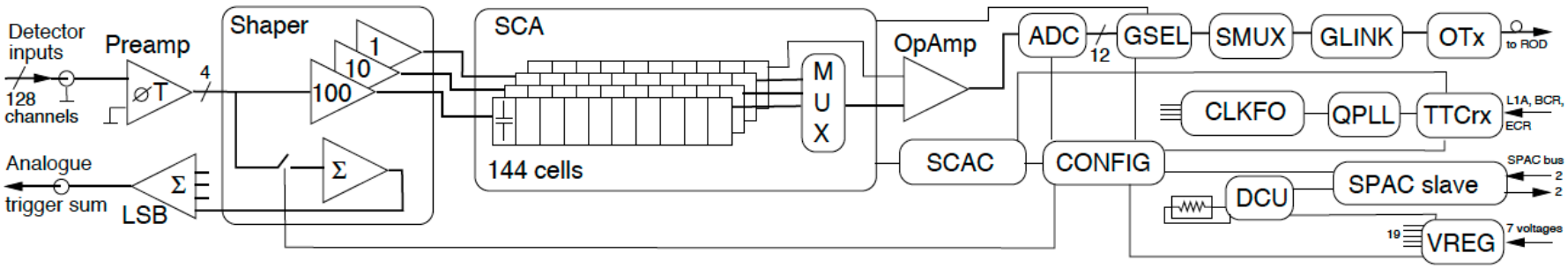
- Some of the specifications:
  - ~170k channels (1524 FEB2 boards installed, each handling 128 LAr channels)
  - 16 bit dynamic range (baseline is to use 2 overlapping 14-bit gain scales)
  - Measure deposited energies with resolution < 0.25%
  - Measure time of energy deposition with resolution ~ 100 ps
  - Coherent noise < 5% of total noise
  - Read out full granularity (preferably both gains) at 40 MHz bunch crossing rate
  - Power not to exceed that of current FEB (~ 0.8 W/channel)
  - Radiation tolerant to levels anticipated at HL-LHC (see table in backup)
  - High reliability (can access no more than once/yr, and more likely once/3 yrs)

LAr FE Electronics Installed



- FEBs and other FE boards (CALIB, Control, Trigger) placed in crates mounted directly on to the calorimeter cryostat feedthroughs

Current LAr Frontend Board (FEB)



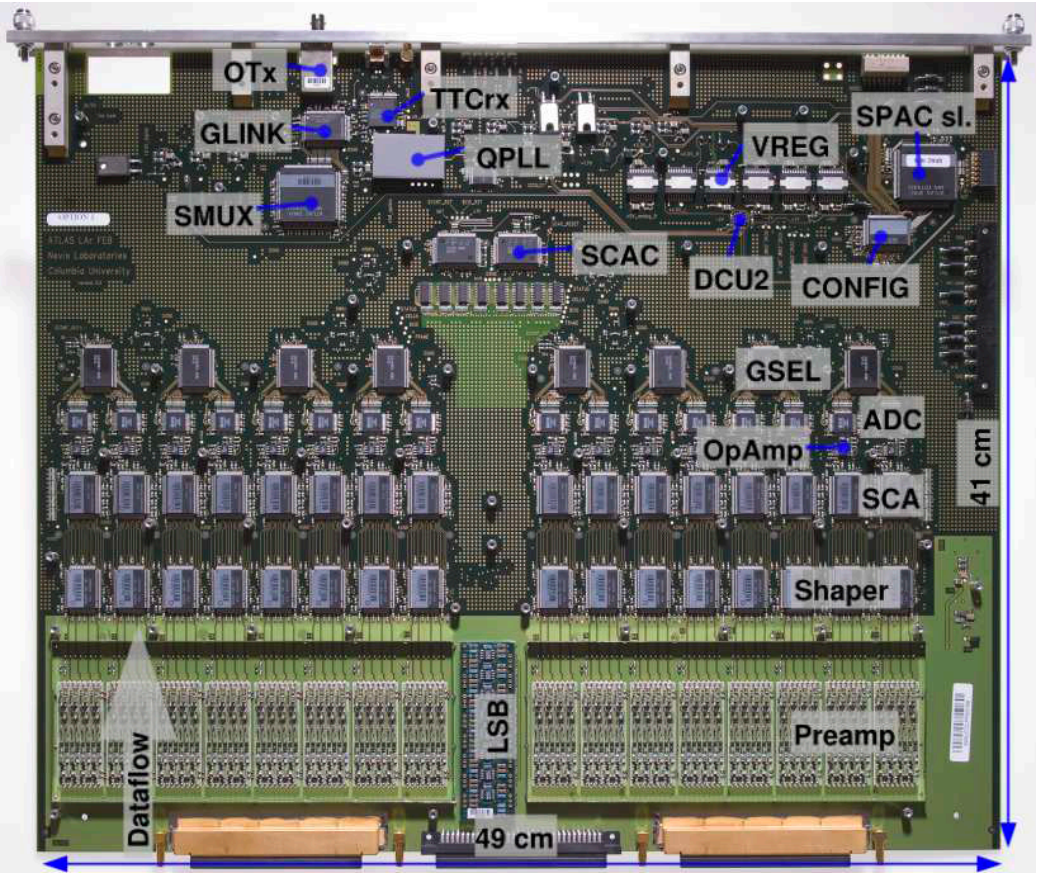
- Current FEB uses 11 different custom radiation-tolerant ASICS, in a variety of technologies
  - Columbia developed FEB, as well as 5 radiation-tolerant ASICs
- 19 on-board radiation-tolerant voltage regulators used to generate 12 different voltages from 7 input voltage levels
- Power ~ 80 W/FEB (< 0.7 W/channel)
  - Under-pressure ("leakless") water-cooled plates attached on both sides of FEB for cooling

Table 3. The acronyms of the main active components of the FEB, the number of each component per 128-channel FEB, and the component's functionality. The components are grouped according to the semi-conductor technology used in their production.

Production Process	Component Name	Number per FEB	Description of Functionality
Hybrid	Preamp	32	First stage amplification
	Preshaper	32	Amplification, preshaping for HEC
AMS BiCMOS	Shaper	32	Amplification and shaping
DMILL	SCA	32	Sampling and analog pipeline
	SMUX	1	32:16 multiplexor
	SPAC slave	1	Serial control interface
	CONFIG	1	Configuration controller
	TTCrx	1	Trigger and timing control receiver
DSM	GSEL	8	Gain selection, data formatting
	CLKFO	7	Clock fanout
	SCAC	2	SCA controller
	DCU2	2	Temperature and voltage monitor
	QPLL	1	Quartz-crystal phase-locked loop
STm RHBip1	VREG	19	Radiation-tolerant voltage regulator
COTS	OpAmp	32	Match SCA output to ADC input
	ADC	16	12-bit digitization
	GLINK	1	1.6 Gbps Serializer
	OTx	1	VCSEL-based optical transmitter

Current LAr Frontend Board (FEB)

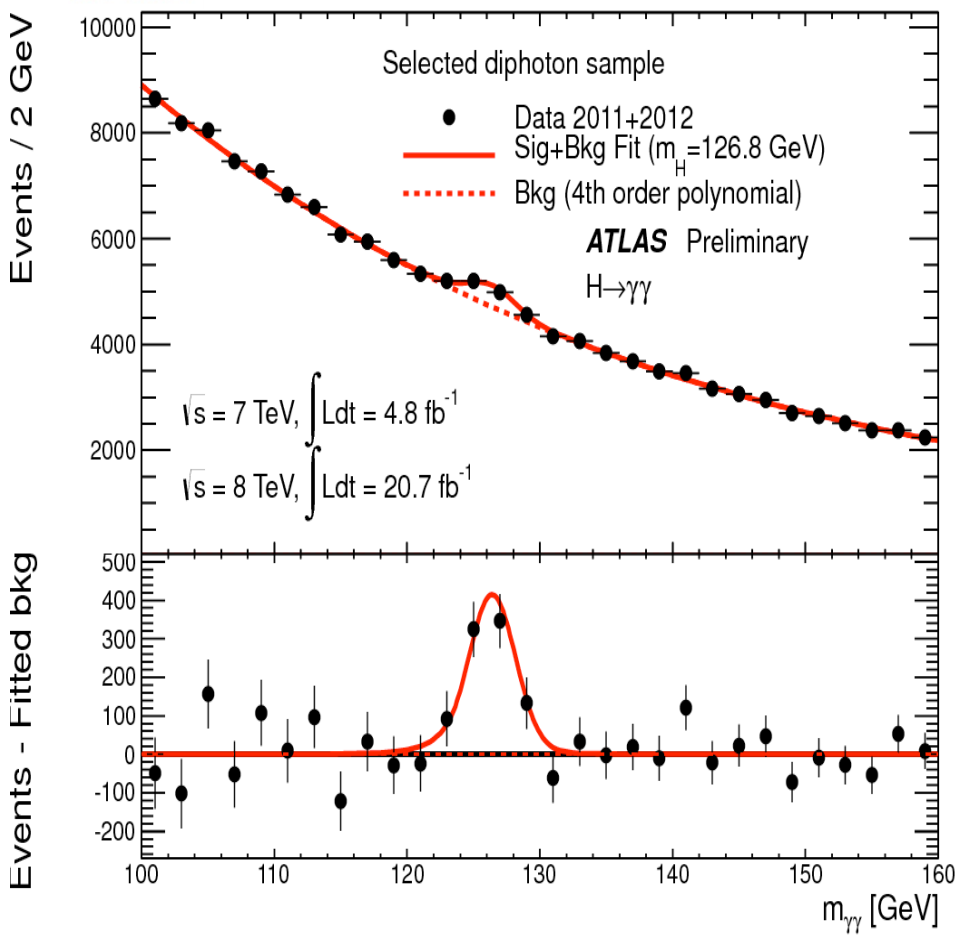
- The FEB2 analog specifications are essentially the same as those of the original FEB (since need to maintain current performance at HL-LHC conditions to meet physics goals)
- However, on current FEB signals are sampled at 40 MHz and stored in analog memories, with digitization and readout only done for L1 triggered events, at max. rate of 100 kHz (and after max. latency of 2.5 μs)

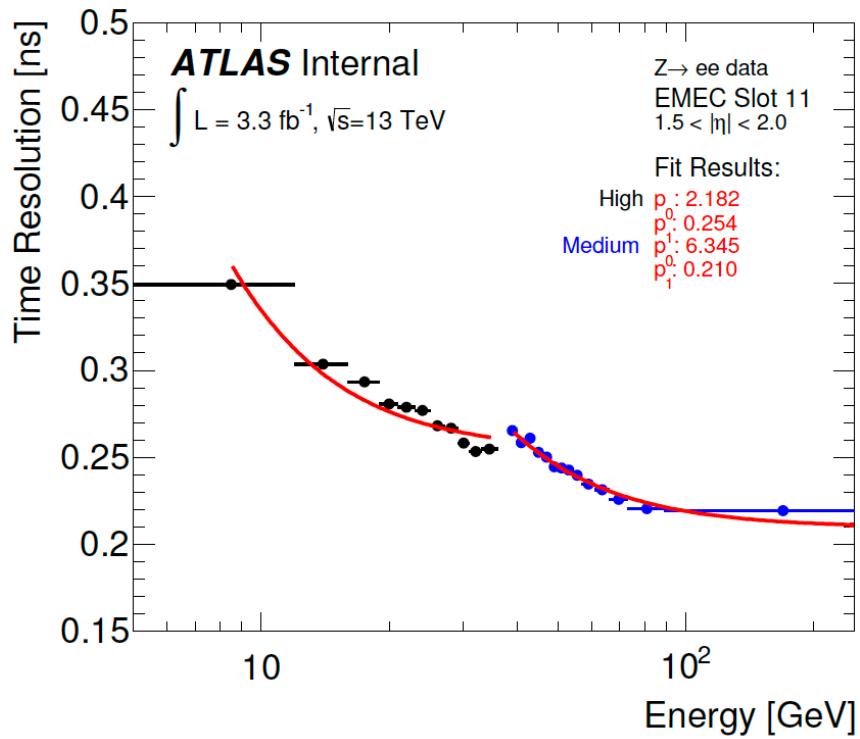


- Current FEB meets or exceeds all original ATLAS specifications
- At end of Run 1, all 1524 FEBs were functional

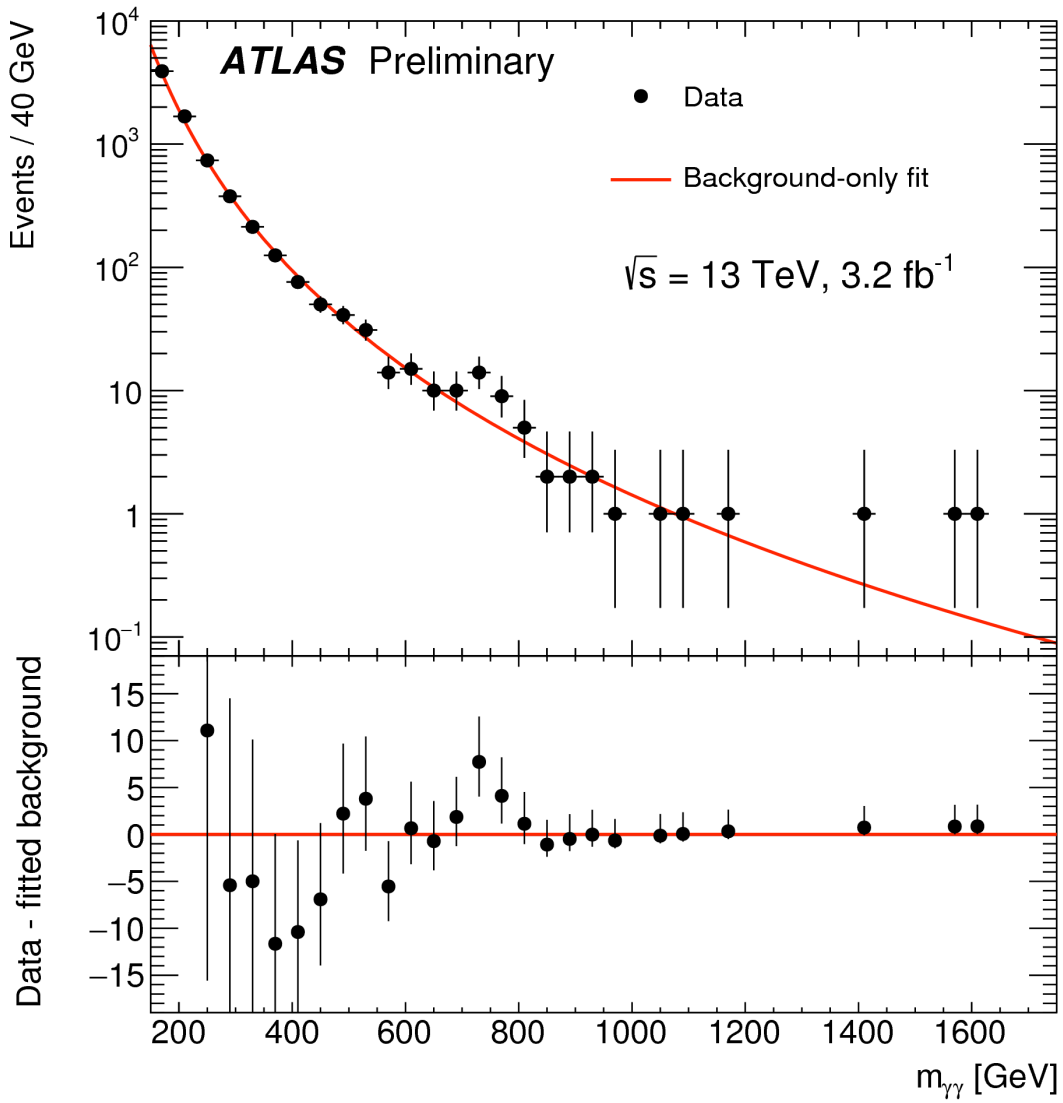
  (despite not being serviced for ~ 2 yrs)

Some Examples of LAr Performance

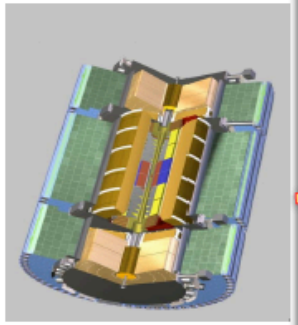


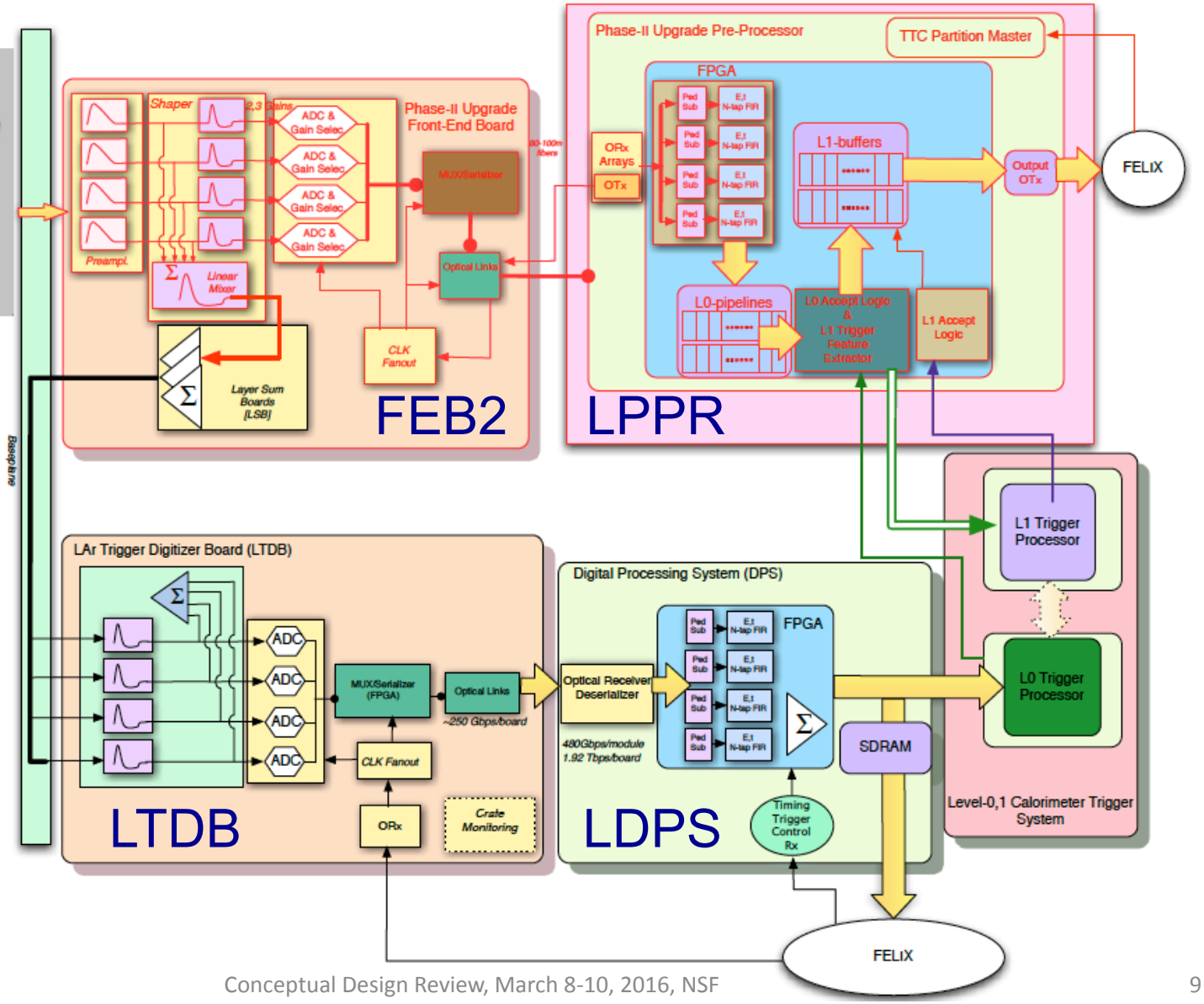


Some Examples of LAr Performance



HL-LHC LAr Readout Architecture

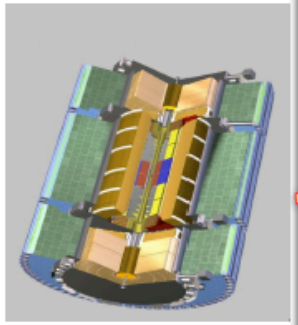


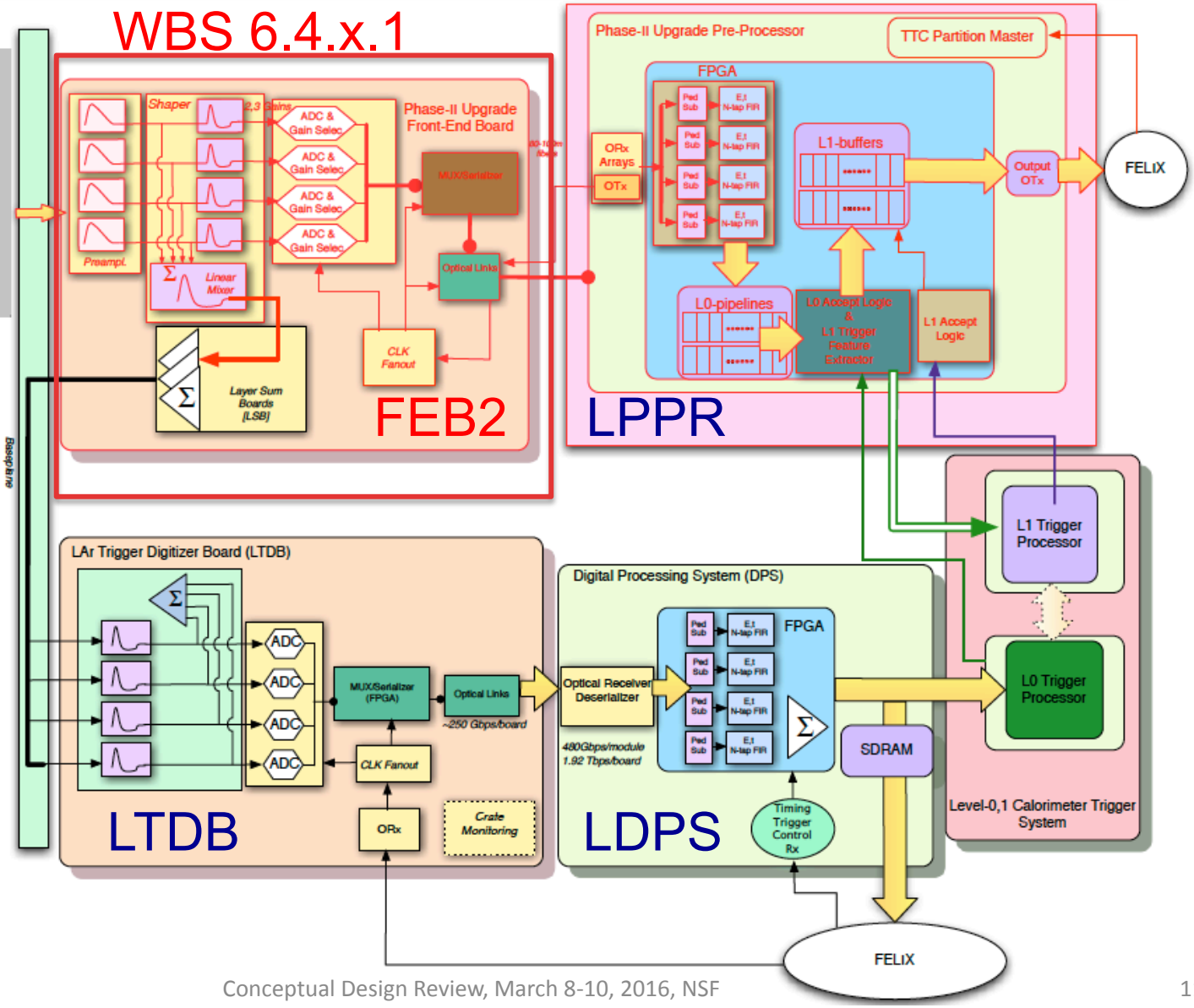


HL-LHC LAr FE Electronics

- NSF scope includes playing the leading role in development of the FE electronics for the HL-LHC, and leverages the expertise of the university groups involved
- WBS 6.4.x.1 (FE Electronics)
  - Columbia – development of FEB2, custom dual-range 12-bit 40 MHz ADC
    - Developed original FEB, as well as 5 out of 11 custom ASICs
    - Developed custom radiation-tolerant 12-bit 40 MHz ADC for Phase I upgrade
  - UT Austin – ASIC testing/validation, including radiation qualification
    - Tim Andeen (as Columbia postdoc) led Phase I ADC testing effort
    - Tim will discuss the testing program in the next talk
- WBS 6.4.x.2 (Optical links)
  - SMU – development of 10 Gbps optical links, incl. Serializer ASIC
    - Was responsible for optical links (1.6 Gbps) of original FEB
    - Developing 5 Gbps Serializer ASIC + optical links for Phase I upgrade

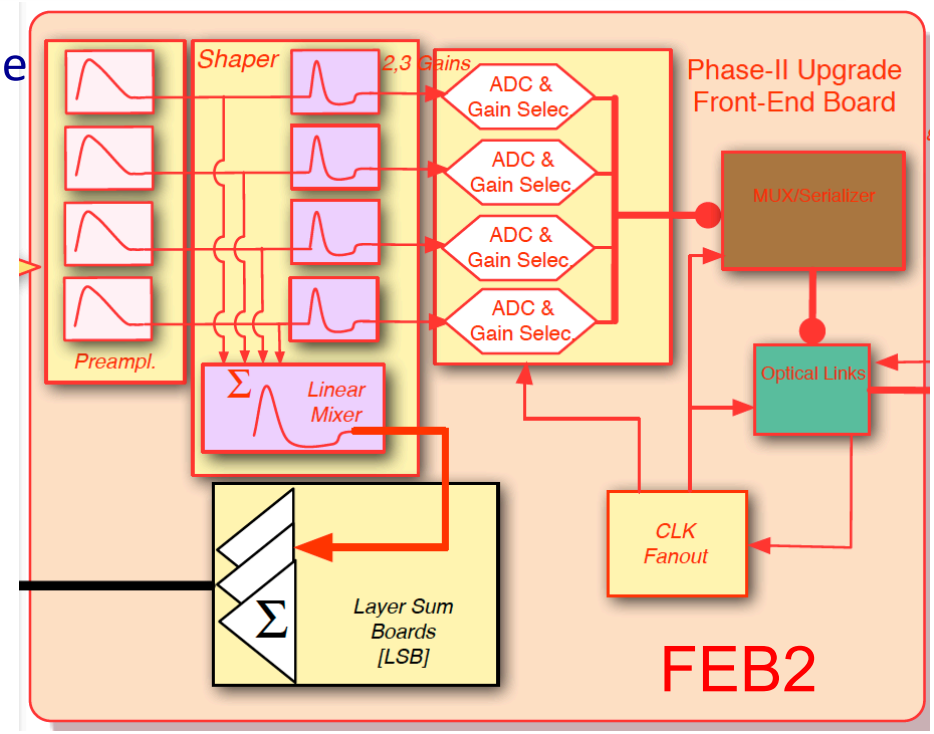
WBS 6.4.x.1 - FE Electronics





WBS 6.4.x.1 - FE Electronics

- Deliverables under WBS 6.4.x.1 include
  - Radiation-tolerant (65 nm) dual-range 40 MHz ADC ASIC
  - Frontend Board (FEB2)



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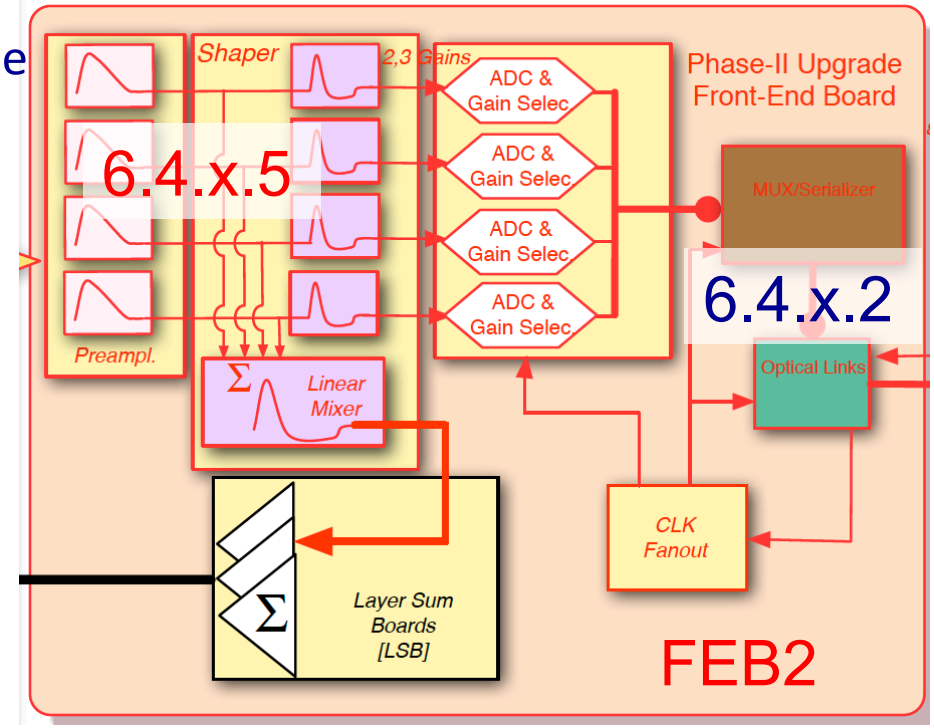
- Deliverables under WBS 6.4.x.1 include
  - Radiation-tolerant (65 nm) dual-range 40 MHz ADC ASIC
  - Frontend Board (FEB2)
- FEB2 design must incorporate also PA/shaper ASIC (WBS 6.4.x.5 in DOE scope) as well as multiple 10 Gbps optical links (WBS 6.4.x.2)



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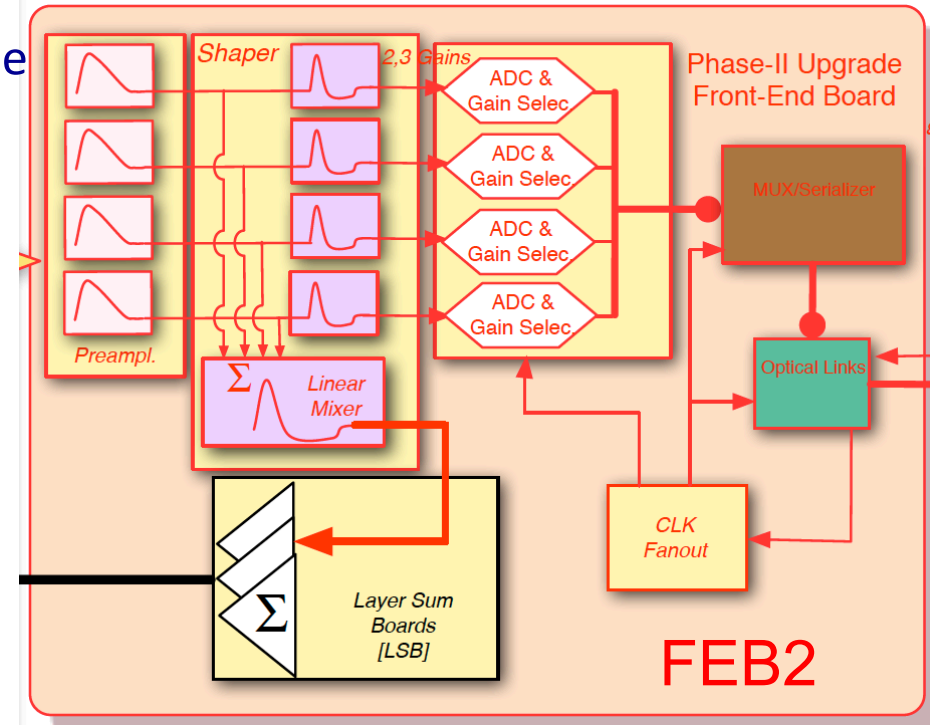
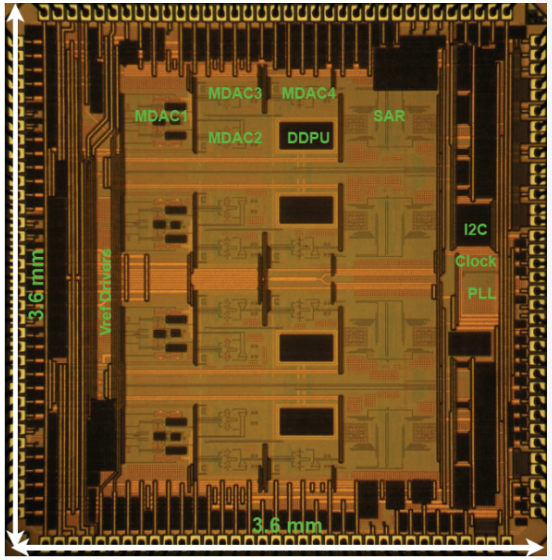
- Deliverables under WBS 6.4.x.1 include
  - Radiation-tolerant (65 nm) dual-range 40 MHz ADC ASIC
  - Frontend Board (FEB2)
- FEB2 design must incorporate also PA/shaper ASIC (WBS 6.4.x.5 in DOE scope) as well as multiple 10 Gbps optical links (WBS 6.4.x.2)
- FEB2 power must not exceed that of current FEB (~80 W for 128 channels)



- Full system requires installation of 1524 FEB2 boards (128 channels each)
  - As in original construction, planning to produce total of 1627

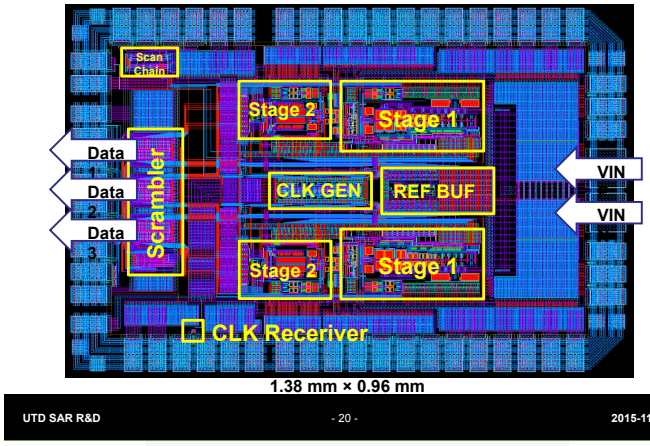
Radiation-Tolerant ADC

- Columbia ADC R&D (collaboration between Physics and EE Depts) over past several years
  - Developed 12 bit 40 MHz ADC in 130nm CMOS for Phase I LAr trigger upgrade
- UTD (EE Dept) recently joined R&D effort, with strong experience in ADC design
- UTD has prototyped Successive Approximation Register (SAR) ADC building block with SEE/SEU mitigation, in 65 nm CMOS
  - Prototype in GF process submitted 8/15. Prelim. test results from UTD show ENOB = 12.1 bits
  - Tests boards are being prepared at UTD and Columbia for TID and SEE/SEU in 2016
  - Next prototype, migrated to TSMC 65nm CMOS, planned for FY17
- Columbia investigating using this as "IP block" in development targeted at dual-range 12-14 b ADC



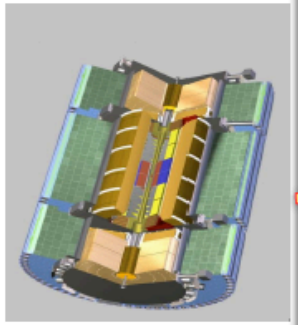
Nevis13 for Phase-I Upgrade

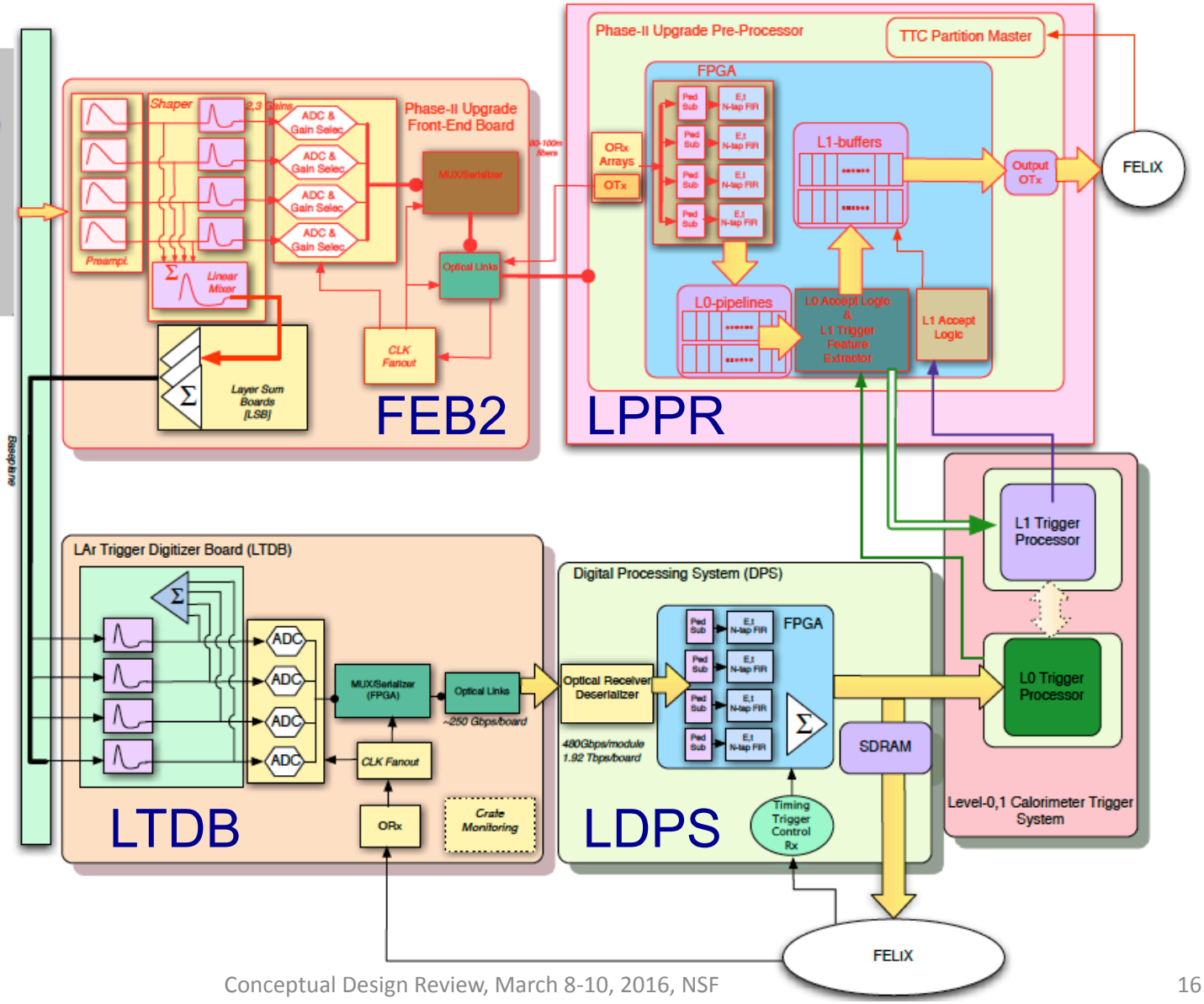
ADC Layout (GF 65nm CMOS)



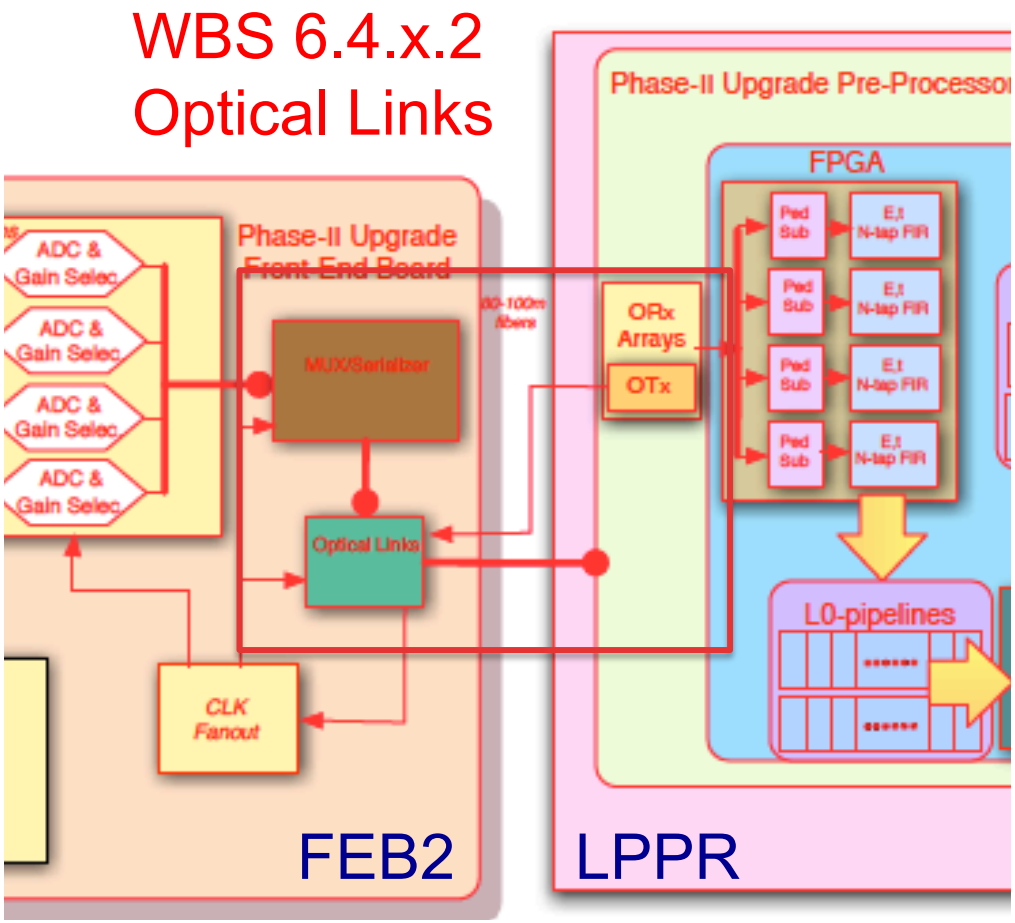
UTD prototype 2015

HL-LHC LAr Readout Architecture





WBS 6.4.x.2 – Optical Links

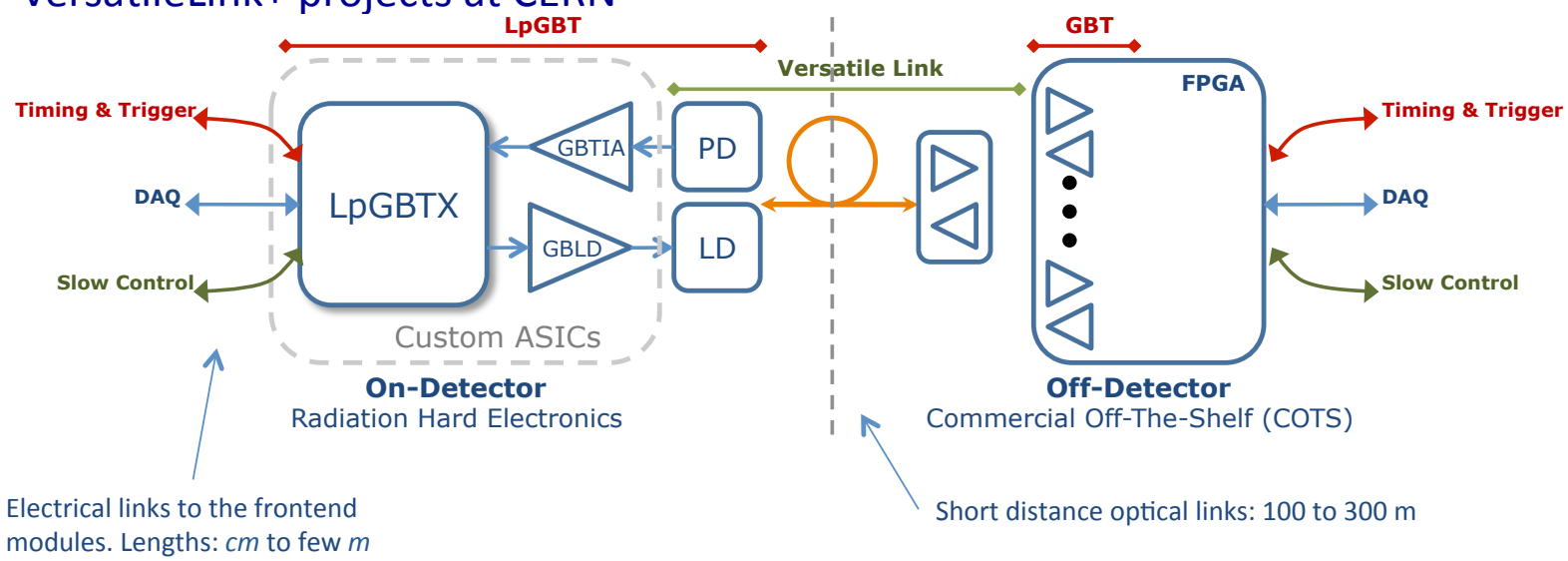


WBS 6.4.x.2 – Optical Links

- Assuming full readout of 2 x 14-bit gain scales per channel, plus 20% overhead for framing, bunch crossing ID, forward error correction, etc., need 172 Gbps of optical bandwidth per FEB2 board

- For HL-LHC, SMU developing a 10 Gbps optical link system, including 2 ASICs in 65 nm CMOS (Serializer, VCSEL Array Driver) as well as optical transmitter (OTx) module

- SMU performing this development as part of their collaboration in lpGBT and VersatileLink+ projects at CERN

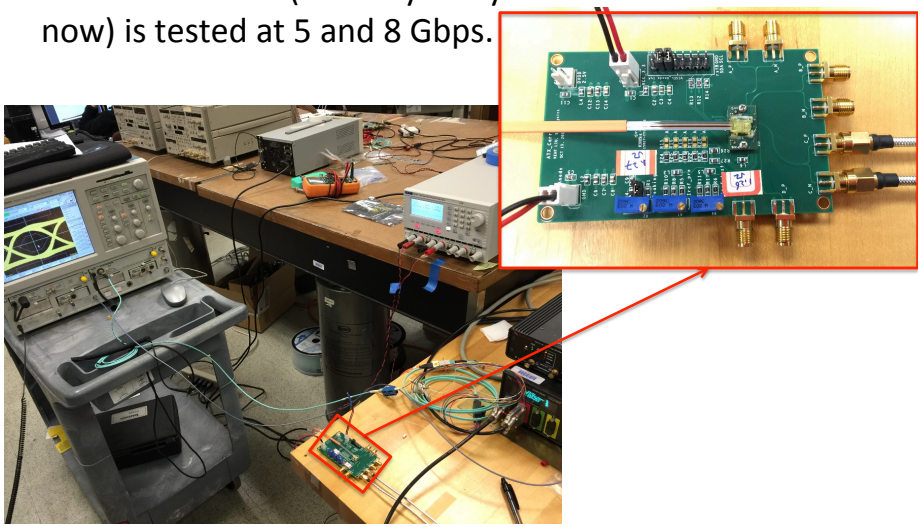


Optical Link R&D

- Development of 10 Gpbs Serializer (lpGBT) proceeding in collab. with CERN
- Within VersatileLink+, SMU developed two designs of 4-channel VCSEL array driver ASIC (VLAD and lpVLAD). Prototypes will be submitted next month.
- SMU also working on optical transmitter module (ATx) which would satisfy the space and other constraints of the FEB2

Testing ATx with LOCld4

- ATx with LOCld4 (the only array driver we have as of now) is tested at 5 and 8 Gbps.



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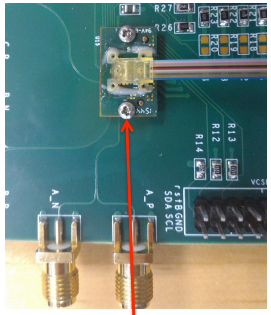
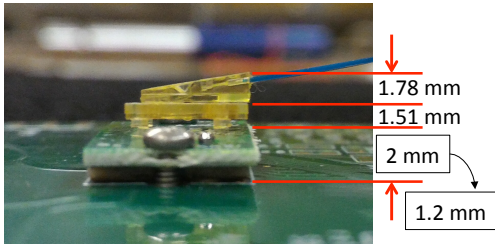
ATx prototype with Samtec ZA8

- The final ATx module is chosen to be with VLAD or/and lpVLAD. The electric connector under investigation is ZA8 from Samtec (https://wwws.samtec.com/technical-specifications/default.aspx?SeriesMaster=ZA8)
- Dimensions of ATx with ZA8 are shown below.



ATx foot print: 10 mm x 15 mm. MOI with a Prizm connect to a 12-way fiber ribbon.



The base will be reduced from 2 mm to 1.2 mm. ATx modules will be 5.3 mm tall for now. In the final design we hope to reduce the height to 4.5 mm.

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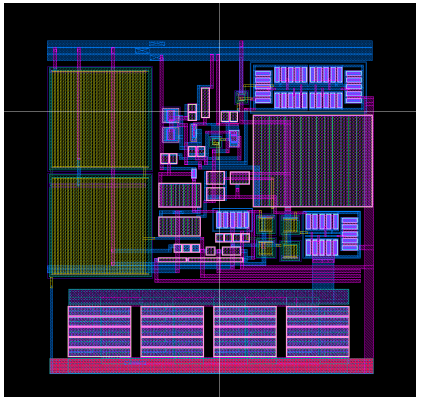
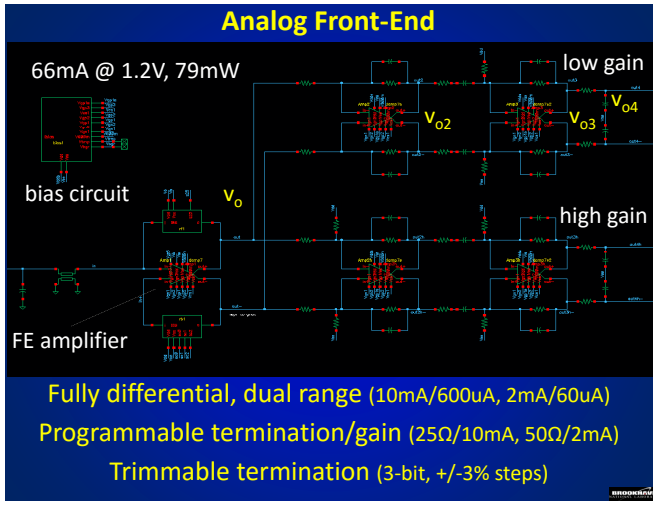
DOE Scope: PA/shaper ASIC

- PA/shaper ASIC is key component of FEB2, with design profiting from BNL expertise (DoE scope)
- Developed SiGe PA/shaper prototypes since 2009. Recently UPenn completed layout for SiGe preamp in IBM's 7WL, potential backup solution
- Proof of principle schematic design of 65nm CMOS preamp+shaper completed. Investigating an improved design with 2 gains x 14 bits
  - Joint effort by BNL/Penn. First prototype layout to be completed by May 2016, fabrication by end of FY16.
- In close communication with the French effort on a different approach in CMOS analog frontend design (current prototype in 130nm)
  - Meetings at Orsay in May 2015, and at CERN Dec 2015
  - BNL is designing common test boards for both ASICs.
  - Will compare performance by the end of 2016
  - Aim for an optimal design by the TDR time in 2017



Layout for SiGE PA/shaper in IBM 7WL



Schematic for preamp in 65nm CMOS

Closing Remarks

- The NSF groups are proposing to play the leading role in the development of the readout electronics (ASICs as well as FEB2 board) for the LAr HL-LHC upgrade

- NSF scope deliverables for LAr follow directly from our expertise and experience from the original ATLAS construction project and the ATLAS Phase I Upgrade project

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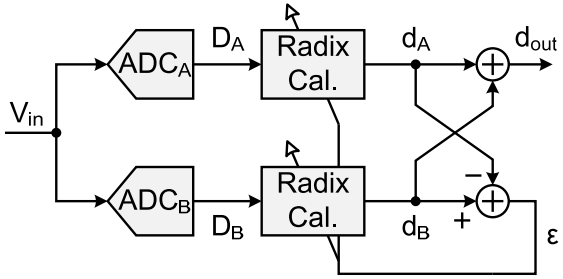
- Next, Tim Andeen (UT Austin) will discuss in more detail the planning for ASIC testing (both performance and radiation) as well as production FEB2 testing/validation

Backup Slides

UTD SAR ADC

Architecture – Split ADC (Dig. Cal.)



$$d_A = \sum_i w_{A,i} \cdot D_{A,i}$$

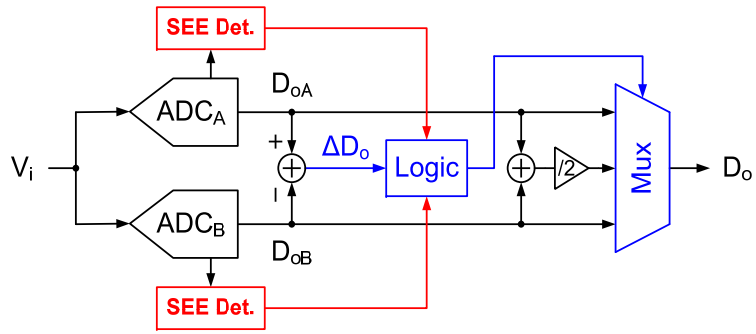
$$d_B = \sum_i w_{B,i} \cdot D_{B,i}$$

- Split-ADC enables digital background calibration
- LMS update:

$$w_{A,i}(n+1) = w_{A,i}(n) - \mu \cdot \varepsilon \cdot D_{A,i}$$

$$w_{B,i}(n+1) = w_{B,i}(n) + \mu \cdot \varepsilon \cdot D_{B,i}$$

Split ADC (SEE Protection)



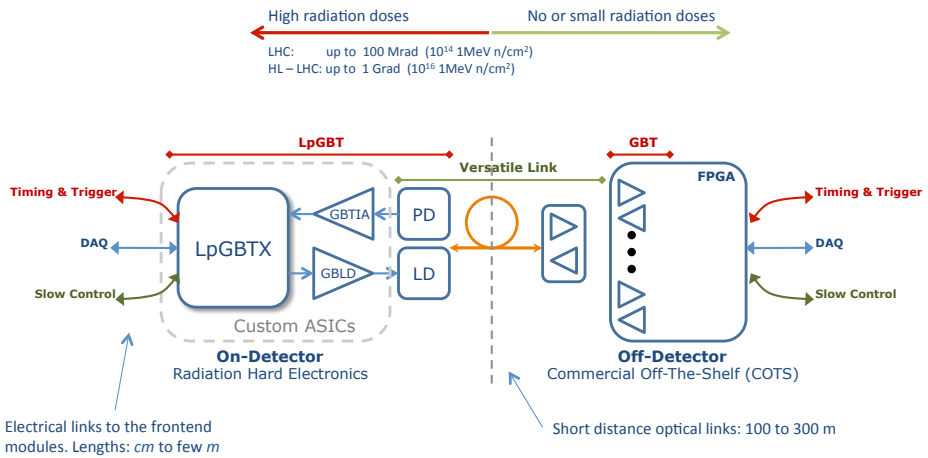
- If ΔD_o is large, chose the output of the ADC that is not hit
- A 3-dB SNR gain with normal operation (i.e., no hit)

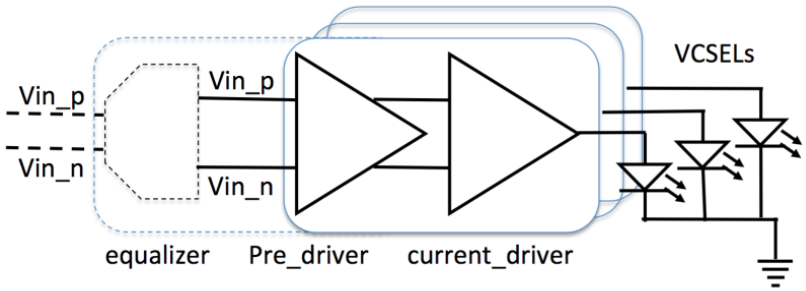
Split ADC design for digital calibration for SEE protection

Serializer and Optical Link

- SMU has extensive experience in optical links
  - Responsible for original LAr FEB links and current Phase I trigger upgrade
- SMU collaborating in lpGBT and Versatile Link+ projects at CERN, both in 65nm CMOS
- lpGBT: designing the phase aligner for the deserializer; first prototype expected in the coming year; expect to use lpGBT IP blocks for Serializer for use on FEB2
- VL+: pursuing two designs in a 4-channel VCSEL array driver (VLAD and lpVLAD). Prototypes will be submitted as part of VL+ project next month. Tests to follow with ATx optical module.
  - Will then develop 10 or 12 channel VLAD prototype for use on FEB2

LpGBT & VL+ Link Architecture





BOE Table: 6.4.x.1 FE Electronics

6.4.x.1 LAr FE Electronics						
WBS	Description	Labor FTE	Labor Ayk$	M&S Ayk$	Travel Ayk$	TOTAL Ayk$
6.4.x.1	**LAr FE Electronics**	**34.9**	**5,370**	**4,948**	**95**	**10,414**
	Instr. Physicists	5.6				
	Engineers	14.9				
	Techs	13.4				
	EE PhD Students	1.0				
6.4.1.1	**LArFE_Columbia**	**29.9**	**4,947**	**4,816**	**55**	**9,818**
	Instr. Physicists	5.6				
	Engineers	12.4				
	Techs	10.9				
	EE PhD Students	1.0				
6.4.2.1	**LArFE_UTAustin**	**5.0**	**423**	**133**	**40**	**596**
	Instr. Physicists	-				
	Engineers	2.5				
	Techs	2.5				
	EE PhD Students	-				

BOE Table: 6.4.x.2 Optics

6.4.3.2 LAr Optical Links						
WBS	Description	Labor FTE	Labor Ayk$	M&S Ayk$	Travel Ayk$	TOTAL Ayk$
6.4.3.2	**LAr Optical Links**	**20.2**	**2,374**	**981**	**40**	**3,396**
	Engineers	10.7				
	Techs	2.5				
	Students	7.0				

LAr Electronics Radiation Tolerance

Table 14. Radiation tolerance criteria of the LAr electronics for operation at HL-LHC for a total luminosity of $3000\ \mathrm{fb}^{-1}$, including safety factors for background estimation, given in brackets. For COTS, an additional safety factor of 4 is included in case of production in unknown multiple lots. Furthermore, the ATLAS policy specifies annealing tests that allow reducing the enhanced low dose rate safety-factor to 1, which currently is set to 1.5 for ASICs and 5 for COTS.

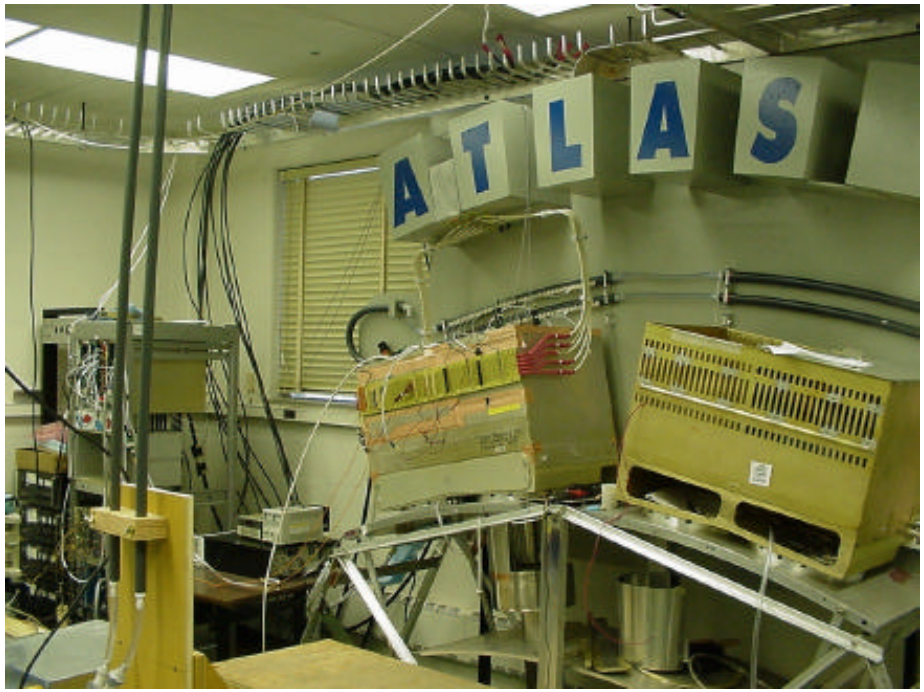
	TID [kGy]		NIEL [n_{eq}/cm^2]		SEE [h/cm^2]	
ASIC	0.75	(2.25)	2.0×10^{13}	(2)	3.8×10^{12}	(2)
COTS (multiple lots)	9.9	(30)	8.2×10^{13}	(8)	1.5×10^{13}	(8)
COTS (single-lot)	2.5	(7.5)	2.0×10^{13}	(2)	3.8×10^{12}	(2)
LVPS (EMB and EMEC)	0.58	(30)	9.2×10^{12}	(8)	2.4×10^{12}	(8)
LVPS (HEC)	0.17	(2.25)	4.7×10^{12}	(2)	2.7×10^{11}	(2)

LAr Electronics CORE Costs

WBS ID	Upgrade Item	All Cost Scenarios [kCHF]
3.1	**LAr Readout Electronics**	**31,394**
3.1.1	**LAr Front-end Electronics**	**20,427**
3.1.1.1	Front-end Boards (FEB-2)	9,743
3.1.1.2	Optical fibres and fibre plant	4,306
3.1.1.3	Front-end power distribution system	3,123
3.1.1.4	HEC LVPS	622
3.1.1.5	Calibration System	2,484
3.1.1.6	Shipping and Logistics	150
3.1.2	**LAr Back-end Electronics**	**10,967**
3.1.2.1	LAr Pre-processor Boards (LPPR)	10,212
3.1.2.2	Transition modules	122
3.1.2.3	ATCA shelves	66
3.1.2.4	ATCA switches	76
3.1.2.5	Server PC	22
3.1.2.6	Controller PC	8
3.1.2.7	FELIX/TTC System	460

System Integration

- WBS 6.4.x.4 covers "System Integration" task at BNL, which is part of DOE scope
- Work involved includes:
  - Frontend Crate System Test, performed to validate the FE system integration and overall performance before PRRs of the various FE crate boards (including FEB2)
  - Validation and final analog tests of 50% of the FEB2 boards
  - Integration and combined system test of FE and BE electronics



- The equivalent tests were performed at BNL during the original ATLAS construction

Phase I LAr Trigger Digitizer Board

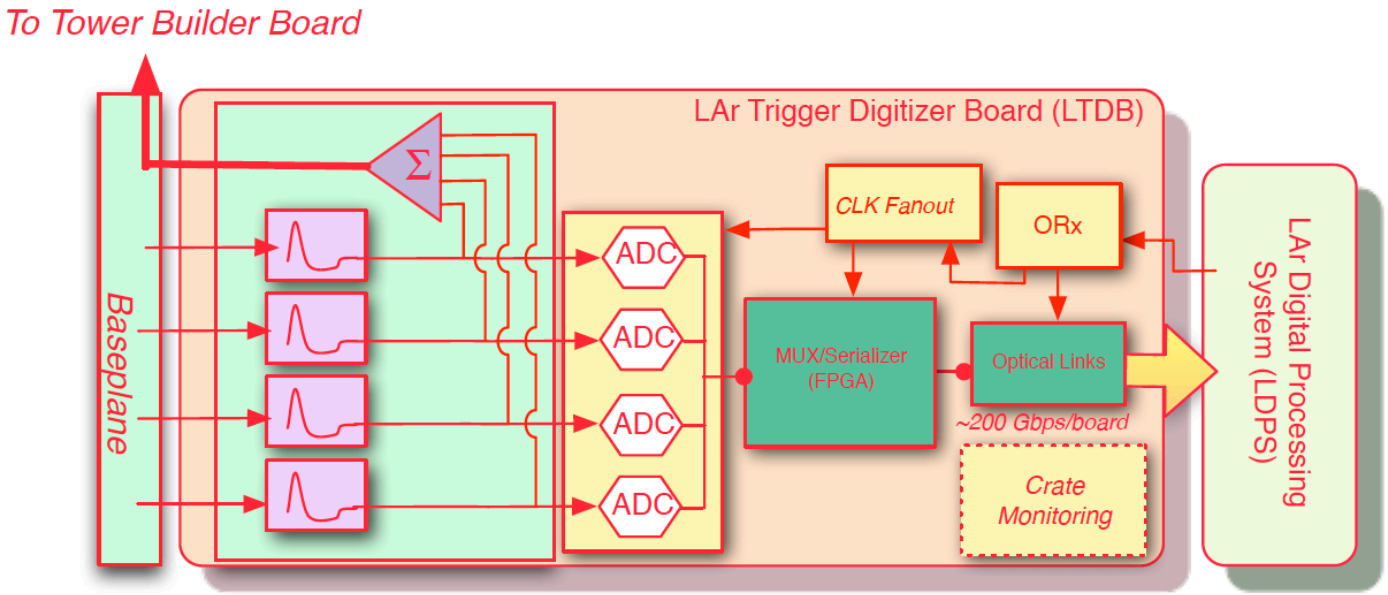
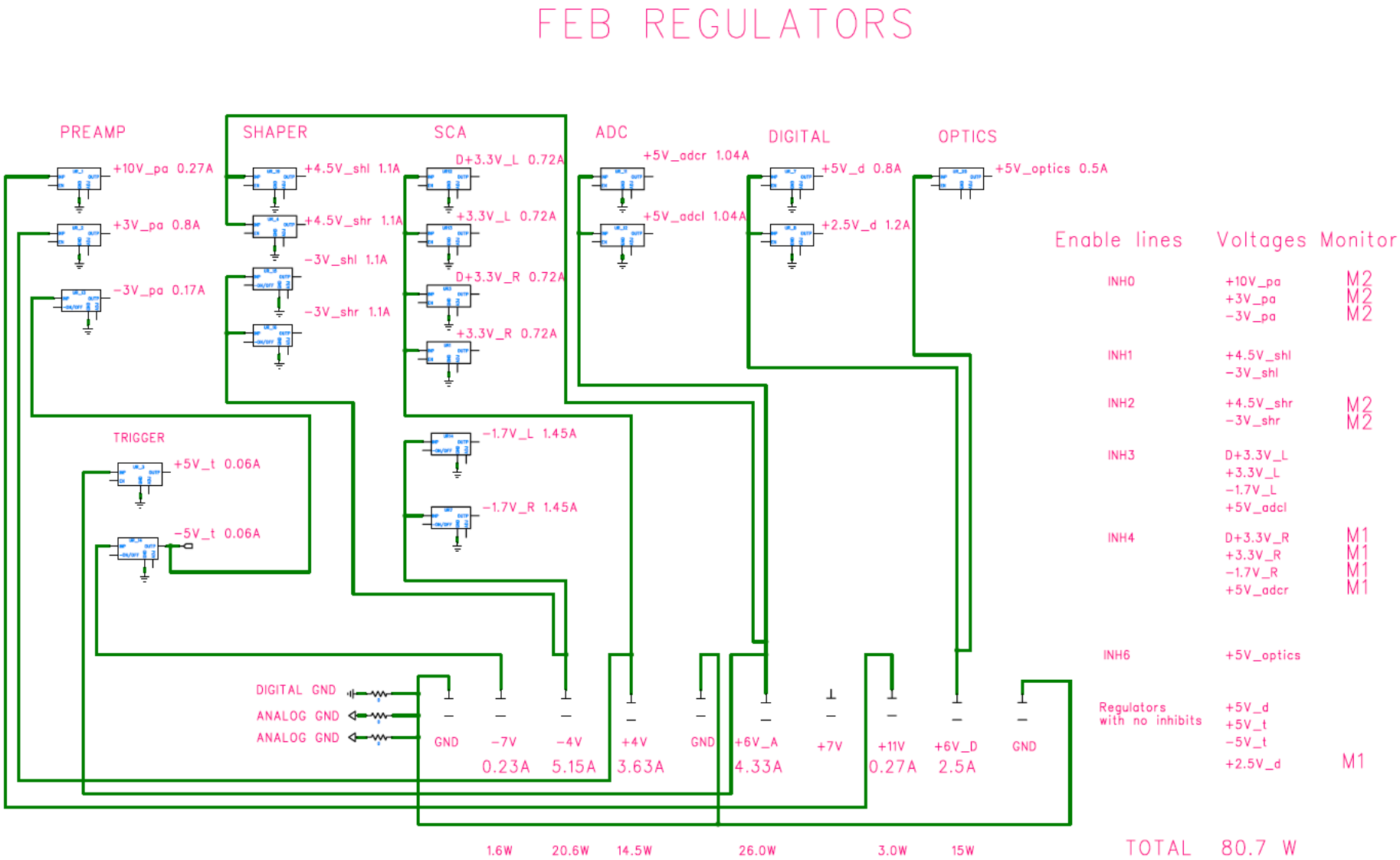
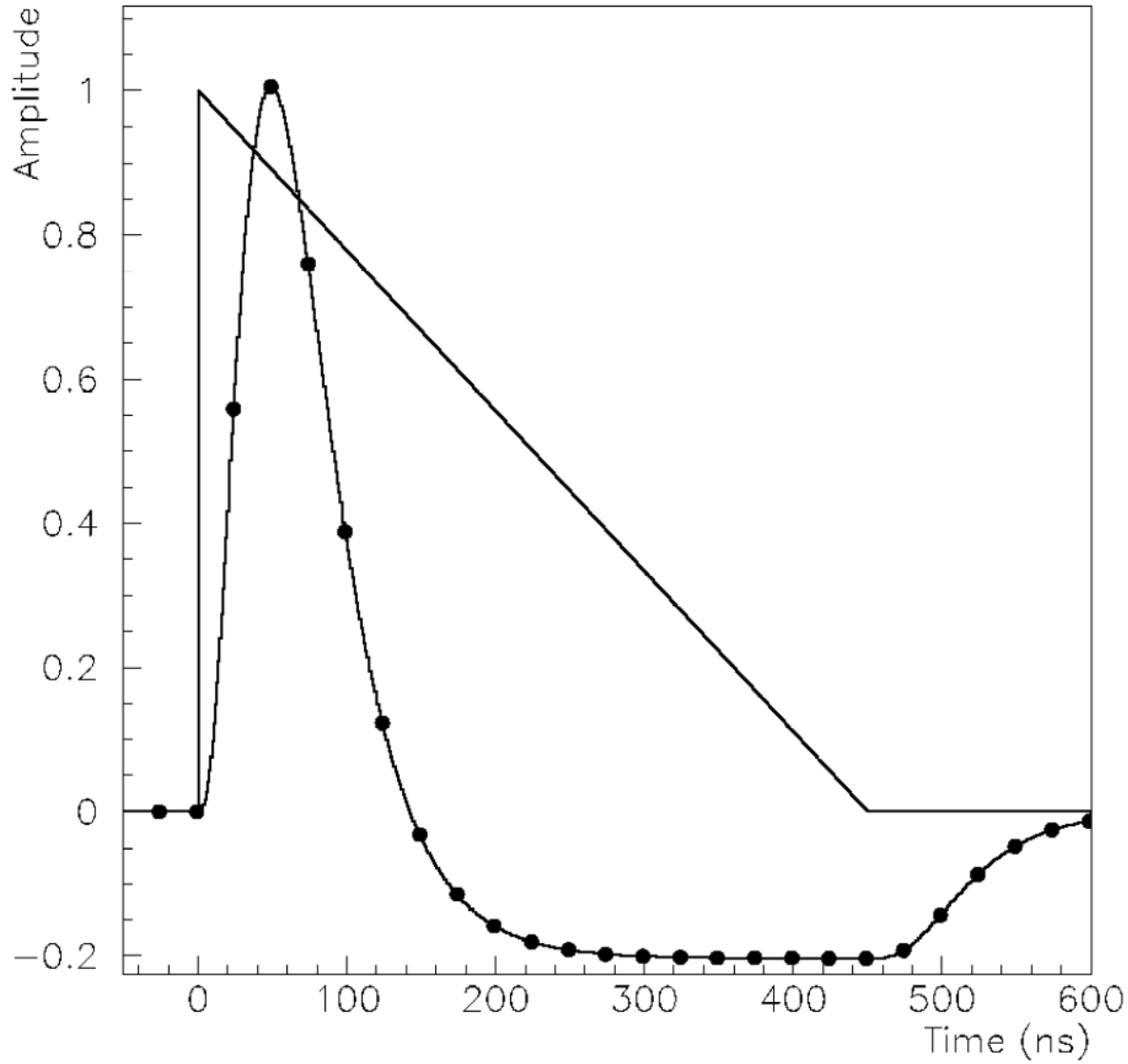


Figure 29. Schematic block diagram of the proposed LAr Trigger Digitizer Board (LTDB).

Power Distribution on Current LAr FEB



LAr Pulseshape