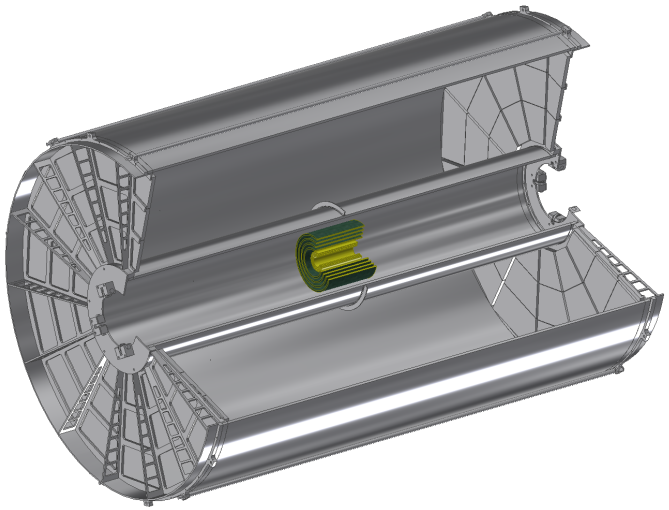
Intermediate Silicon Tracker Overview

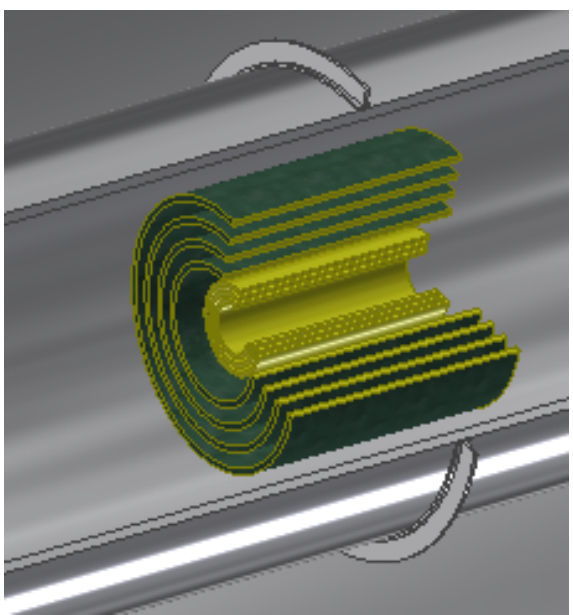
RIKEN/RBRC
Itaru Nakagawa

Quick Overview of Intermediate Silicon Tracker (INTT)

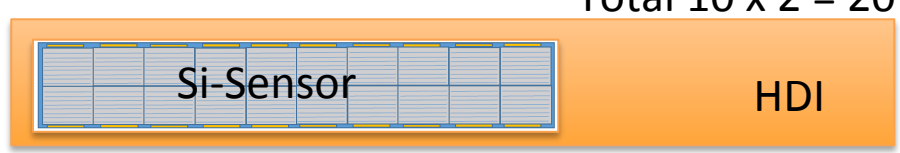


	R [cm]	# of Ladders
MAPS	2.3	
	3.1	
	3.9	
INTT	**6**	18
	8	24
	10	30
	12	36
TPC	20 ~ 78	

Total Number of Ladders=108



Total 10 x 2 = 20 cells/ladder



Role of INTT

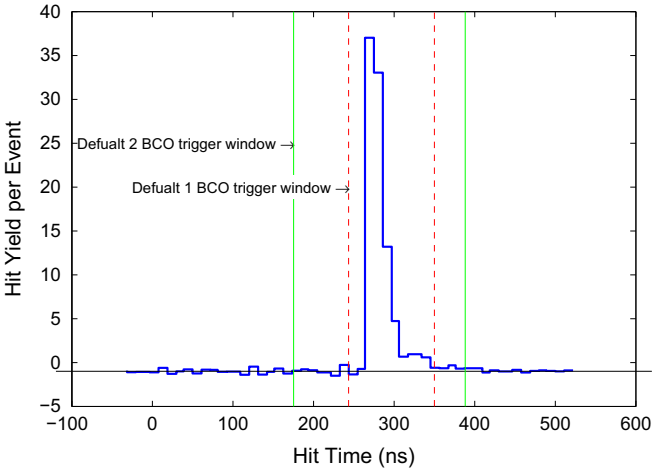


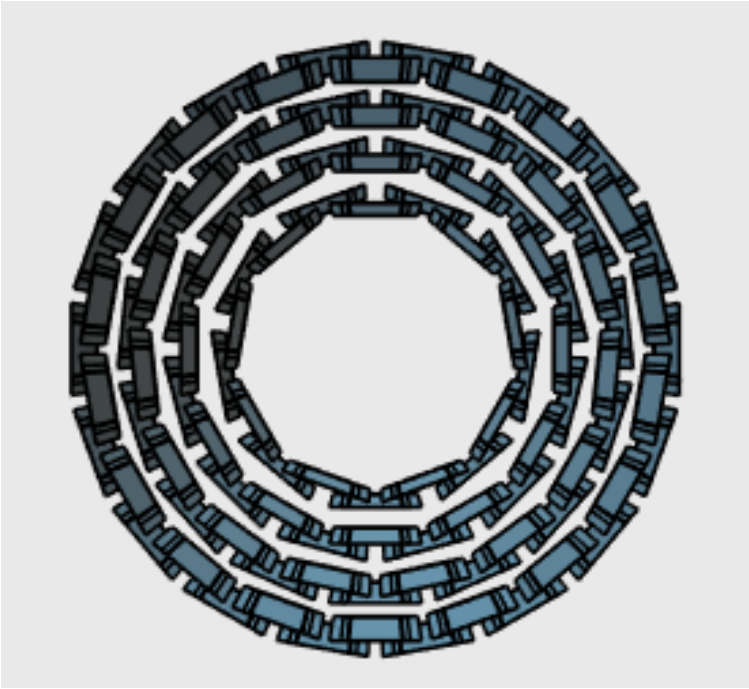
Fig. 32. Timing distribution of the FVTX hits relative to the RHIC beam clock.

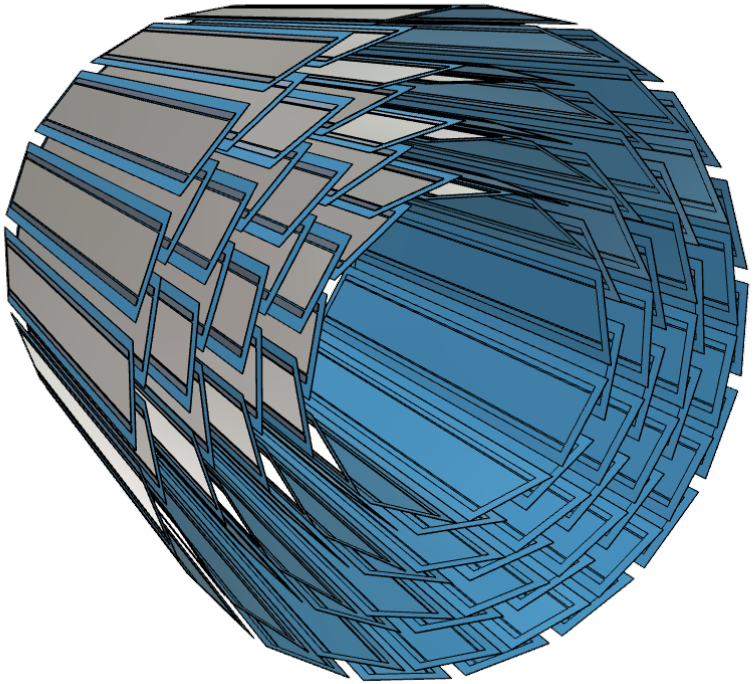
1. Improved DCA measurements
   - Connect MAPS tracklets and TPC track
   - Reduce backgrounds in DCA
2. Disentangle Pile up at high collision rate
   - Improve track finding efficiency in central Au-Au
   - Memory time of INTT is less than 1 crossing. (MAPS, TPC are multiple beam clocks).
3. Contribute to TPC position calibration
   - Identify track position for the space-time calibration of TPC

Boundary condition :

- Goal of material budget is **1% rad. Length** per layer.
- Minimum technical risk to be in time for day-1.

INTT Barrel Tracker

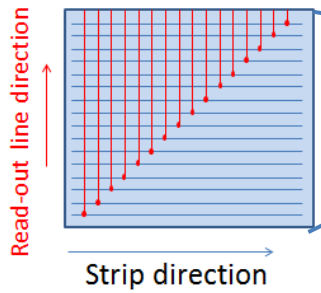




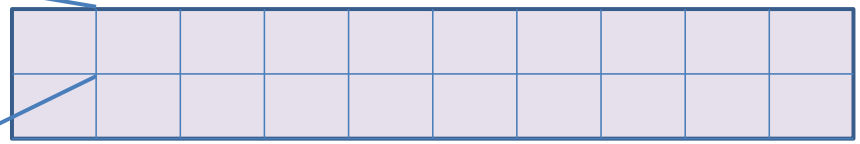
- Identical ladders form 4 barrels at R=6, 8, 10, and 12 cm
- Made of 108 ladders of 2cm wide x 24 cm active area

Silicon Sensors, Silicon Module and Ladder

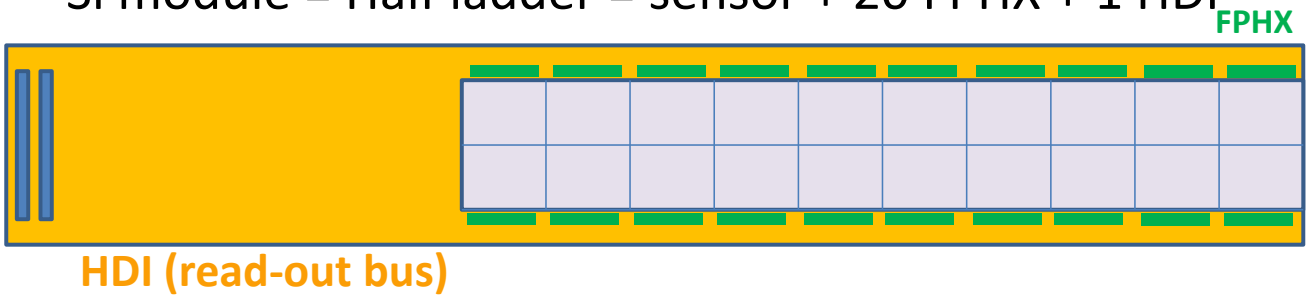
cell = 128 mini-strips



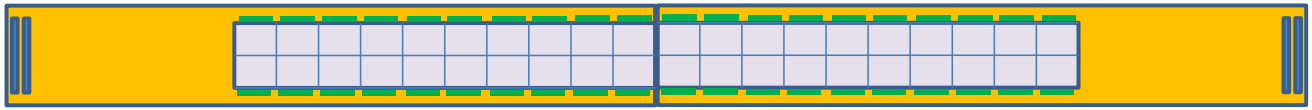
Sensor = 2x10 sensor cells



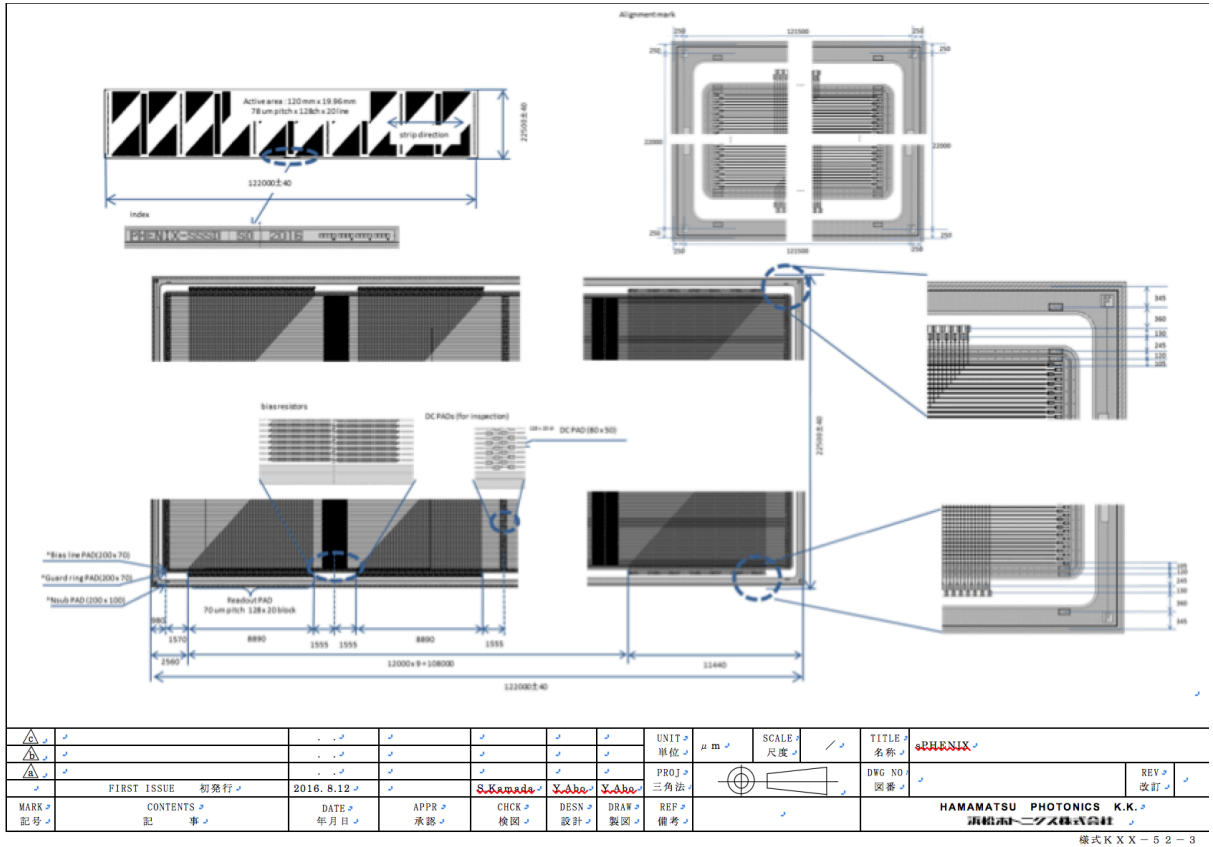
Si module = Half ladder = sensor + 20 FPHX + 1 HDI



Ladder = 2 half ladder + stave (cooling/support)



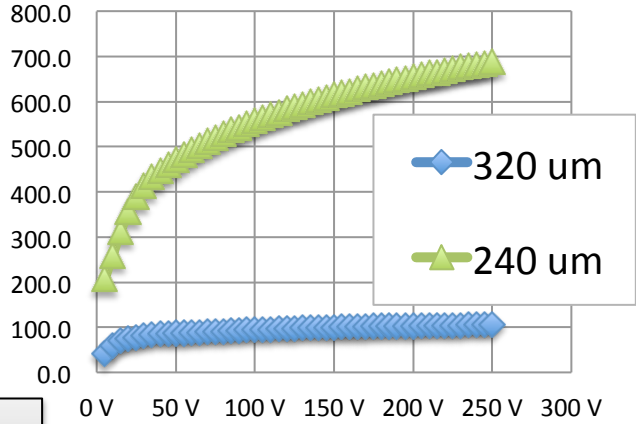
Leading Sensor Options



Prototype single sided silicon strip sensor design by Hamamatsu Co.

Well established technology
single sided silicon strip sensors
(Hamamatsu Co.)

Dark Current [uA]

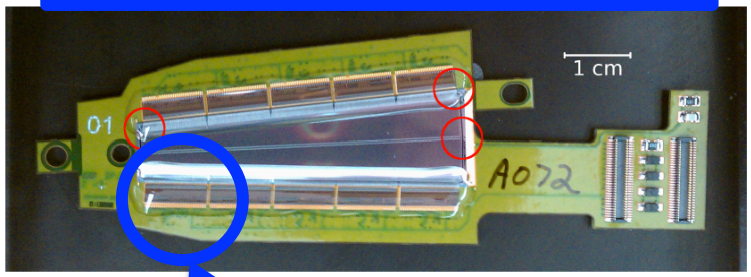


At a cost of S/N

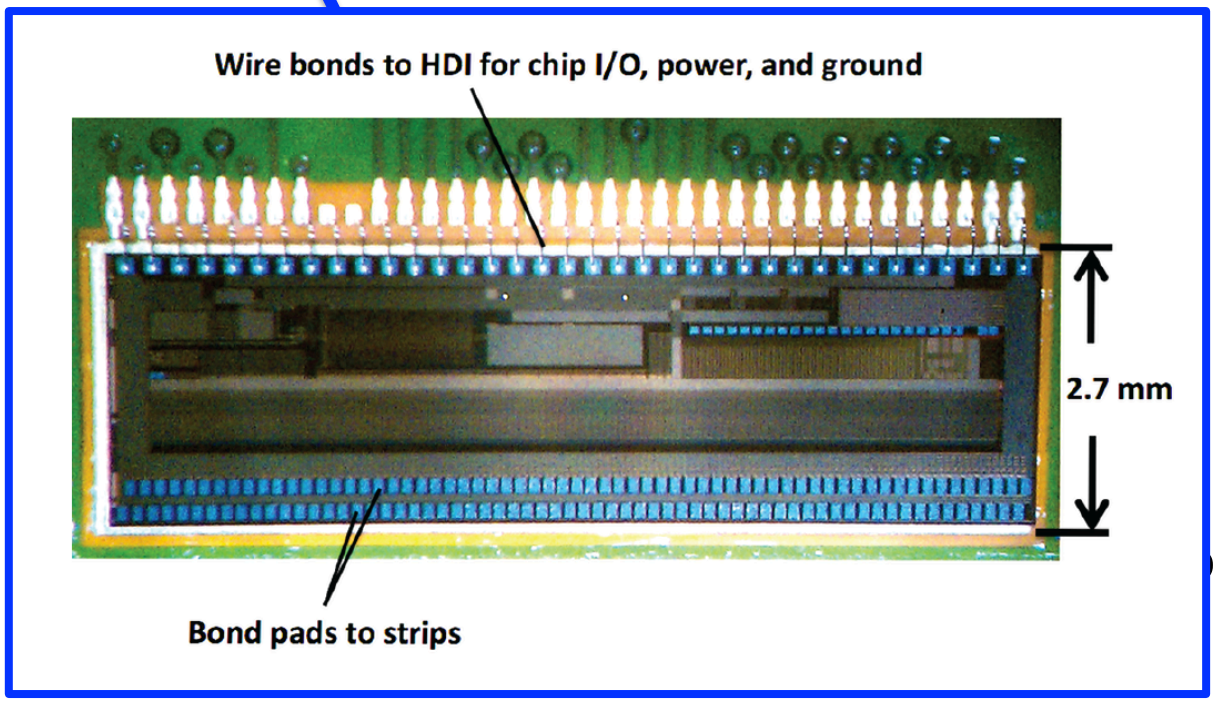
Challenge to develop thinning sensor to reduce material budgets.
Standard thickness 320μm -> Thinned sensor 200 – 240 μm?

Readout Chip Selection

FVTX Silicon Module for PHENIX



- **FPHX** Chip is to be used.
- Designed by FNAL for PHENIX FVTX
- Low power consumption compared to SVTX4 by factor of 5.



FPHX Specifications

Channel	128
dimension	9 x 2.7mm
Input capacitance	1.5pF
Gain	50 – 200mV/fC

FPHX Power Consumption

Specification	FPHX
ADC/channel	3 bits
Power Consumption	64 mW
Cooling	Solid conductive

Material Budget for cooling options

Liquid > Air > Solid conductive

X_{rad} [μm]	X_{rad}/X_0 [%]
100 - 500	0.05 – 0.25

High thermal conductive sheet:

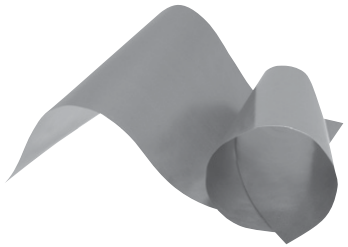
- Factor of 2 to 5 higher Conductivity than Al
- Widely used for heat dilution of smart phones
- To be glued on the back side of HDI to remove the heat from FPHX chips efficiently.

Panasonic **"PGS" Graphite Sheets**

"PGS" Graphite Sheets

Type: **EYG**

"PGS (Pyrolytic Graphite Sheet)" is a thermal interface material which is very thin, synthetically made, has high thermal conductivity, and is made from a higly oriented graphite polymer film. It is ideal for providing thermal management/heat-sinking in limited spaces or to provide supplemental

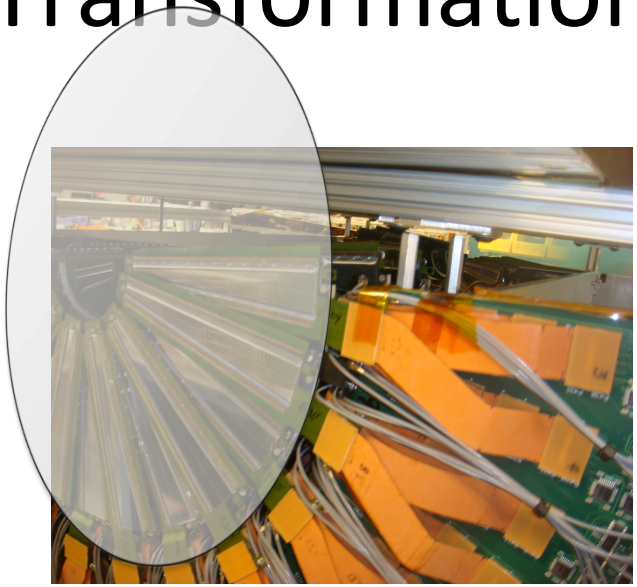


Features

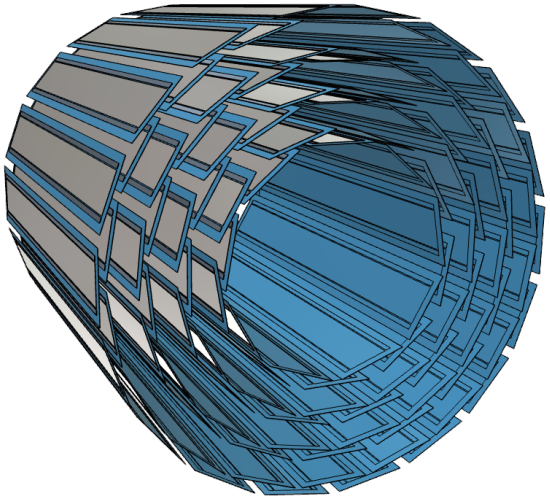
- Excellent thermal conductivity : 700 to 1950 W/(m·K)
  (2 to 5 times as high as copper, 3 to 8 time as high as aluminum)

Owing to low power consumption of FPHX chip, the cooling system can be simplified. This helps to reduce the material budget comes from the cooling system.

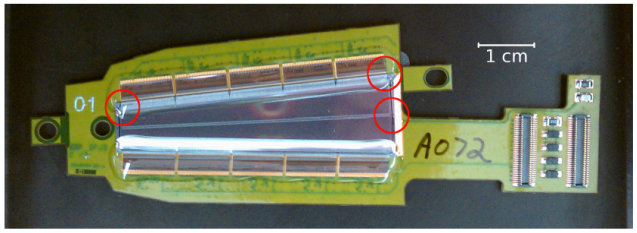
Transformation of FVTX to Barrel Tracker



Disk Type



Barrel Type



Trapezoid Shape

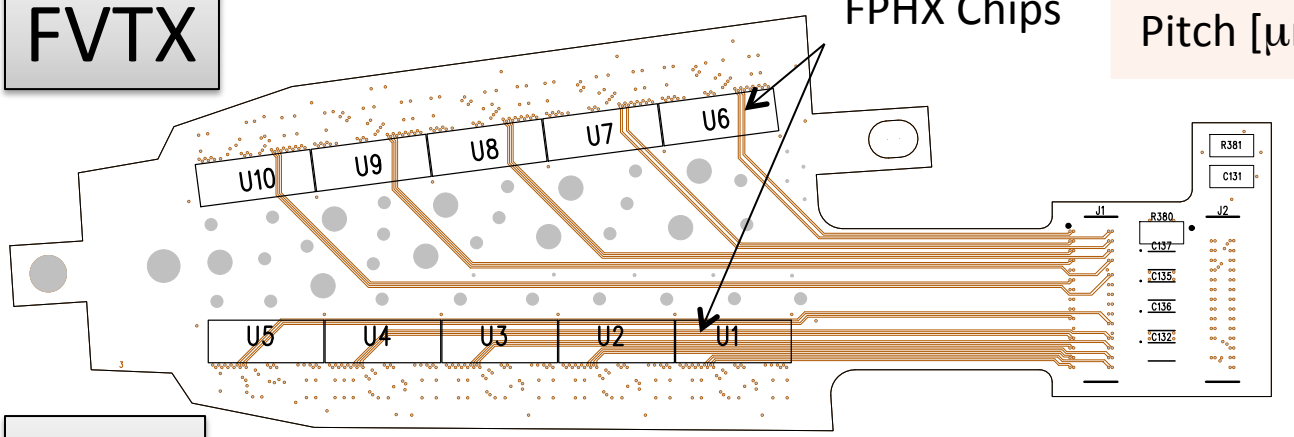
Rectangular Shape

The shape of the sensor and readout HDI needs to be re-designed in order to form the barrel type geometry. This doesn't mean the electrical circuit has to be re-designed from the scratch. The electrical design will be the same.

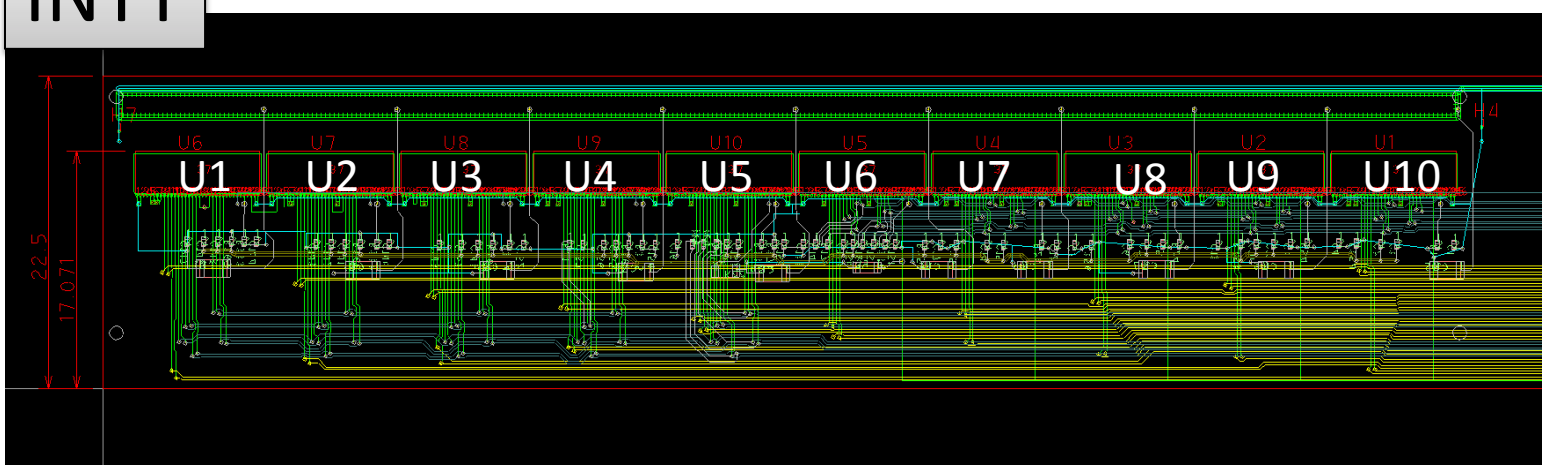
HDI Design

	FVTX	INTT
# Layers	7	7
Pitch [μm]	40	60 -> ?

FVTX

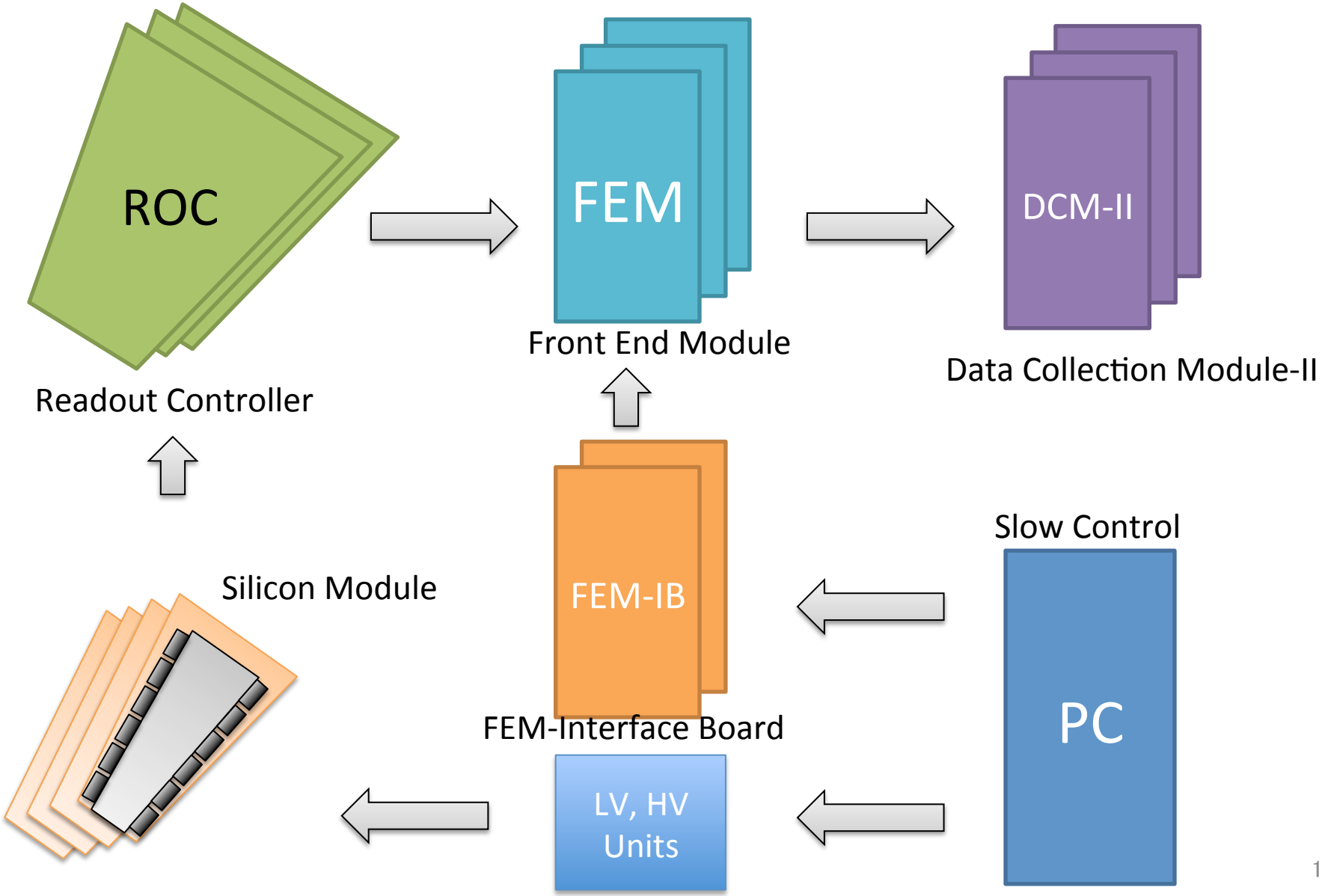


INTT



The INTT HDI prototype circuit is designed based on the FVTX circuit drawing. The line spacing pitch for FVTX was the cutting edge 40μm, but this can be relaxed for INTT due to relatively relaxed geometrical constraint.

FVTX Readout Chain



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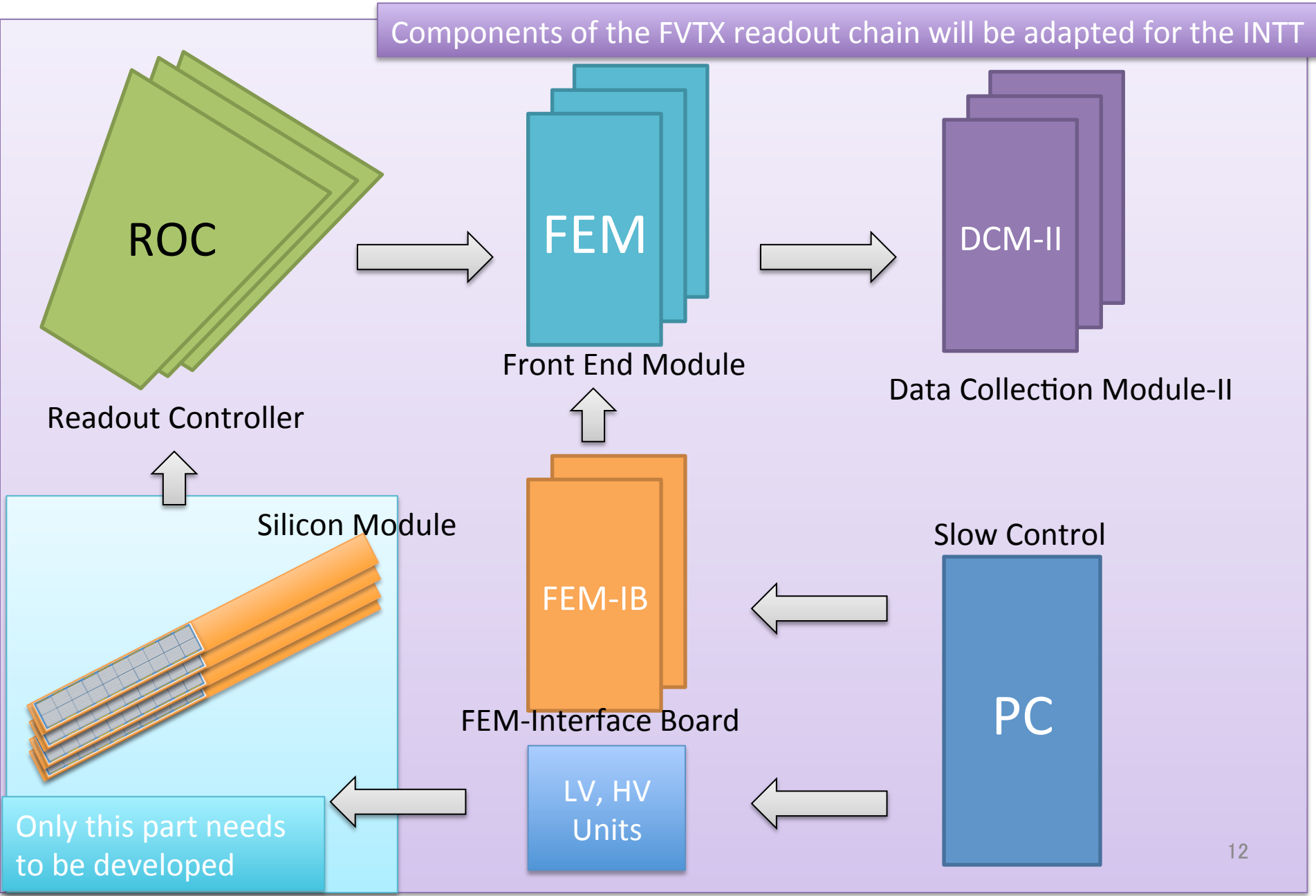

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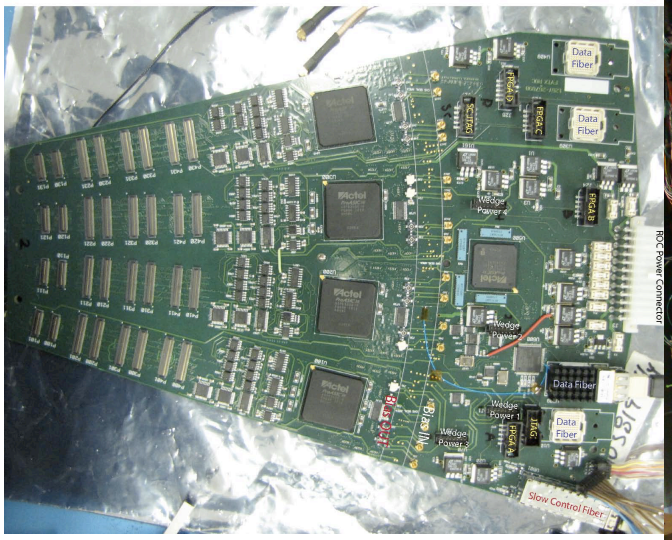
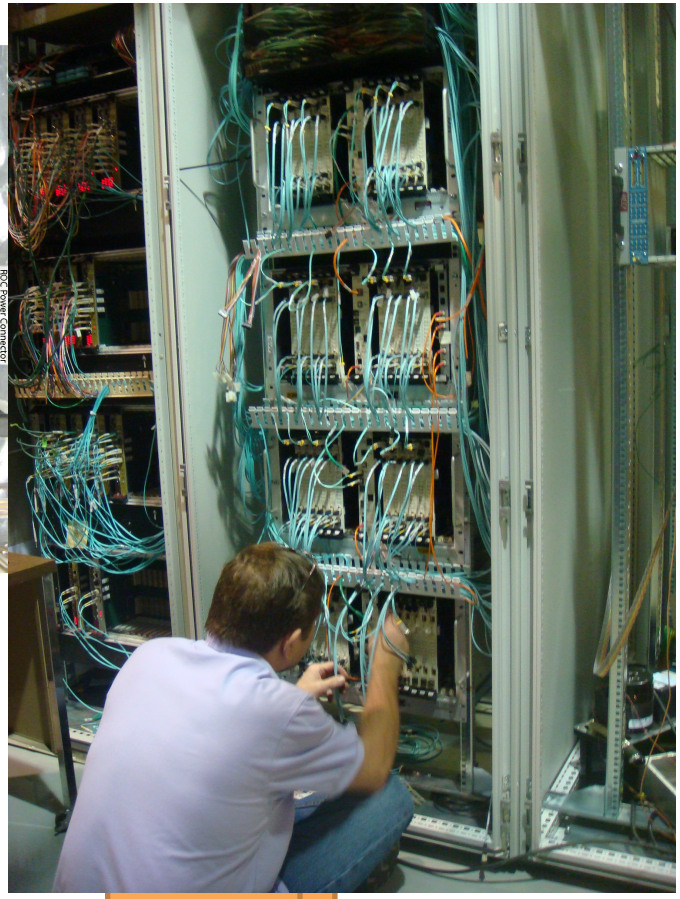




DCM-II

Slow Control

PC

The entire read-out chain of FVTX system will be re-used in INTT. This will reduce the technical risk and cost.

Silicon Module

Collaborating Institutes and Expertise

- **RIKEN (Y. Akiba, I. Nakagawa)**
  - Conducted the PIXEL detector for PHENIX. In charge of design work and procurements of silicon sensors and HDIs with Japanese companies.
- **RBRC (T. Hachiya, G. Mitsuka,Y. Yamaguchi)**
  - Assembly and testing silicon module. Physics simulation and configuration optimization. Adapt FVTX readout electronics.
- **BNL (J. Huang, M. Lenz, E. Mannel, R. Nouicer, R. Pisani)**
  - Engineering and assembly of the ladder and support structures.
- **Rikkyo (H. Masuda)**
  - FPGA coding in readout electronics and slow controls and testing prototypes.
- **Nara Woman's University (M. Shimomura)**
  - Testing prototypes and productions.
- **LANL (M. Brooks, M. Liu)**
  - Played leading role in FVTX detector development. Consultant for the application of FVTX electronics to INTT.
- **J-Parc (S. Hasegawa, H. Sako)**
  - Additional funding and co-development of silicon sensors.

*FVTX expert

R&D Schedule JFY2016

2016 Month	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	Resource	Design
s1 Prototype-I															Production
Silicon Sensor														RIKEN	Test
HDI														RIKEN	
Silicon Module														RBRC,BNL	
s0 Prototype-I															
Silicon Sensor														RIKEN,BNL	
HDI														RIKEN	
Silicon Module														RBRC,BNL	

Today

Issues and concerns

- Mechanical engineering
- Radiation monitoring, radiation environment
- Thinner silicon sensors than the standard thickness.
- High thermal conductivity plate cooling (to be proven by R&D)
- Known issues of FVTX readout (data packets drop off in the middle of run) to be resolved.

Summary

- Intermediate tracker to improving the tracking performance in high multiplicity circumstance.
  - Multi-layers tracking.
  - INTT tracker is to be built with small material budget ~1% for the tracking performance.
  - Thinner silicon sensor and high thermal conducting plate for cooling to save material budget.
- Stay with well established technology to minimize technical challenge to be in time for day-1 experiment.
  - Single sided silicon sensors
  - Reduce the cost of R&D and production.
    - Reuse FPHX Chip
    - Reuse FVTX readout electronics (ROC, FEM, DCM-II, Slow control systems).

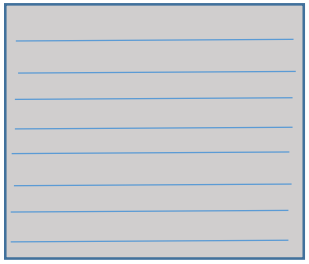
Challenge

Minimize Risk

BACKUP SLIDES

s0 Sensor Design

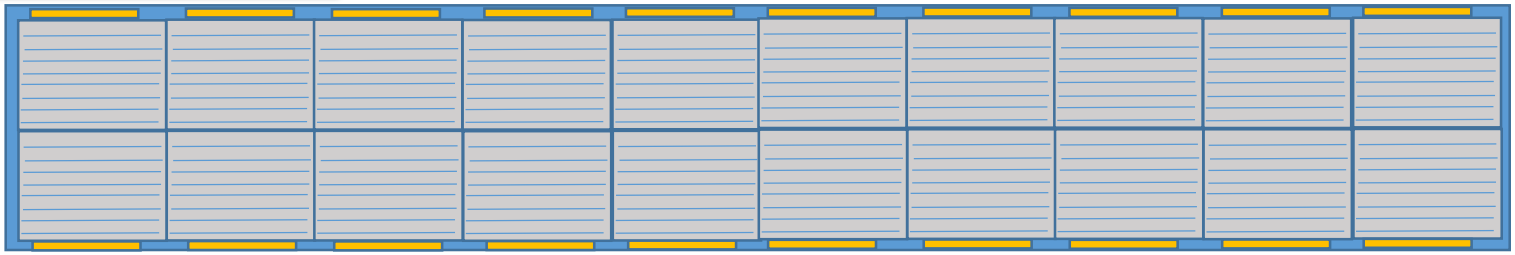
Silicon Cell



Number of Strips	**128**
Strip width	84 um
Strip length	12 mm

Block Width	**128 × 84 um = 10.752 mm**
Block Length	12 mmm

Silicon Sensor



Number of Blocks	**12 × 2 =24**
Active Are	(2 × 10.752) mm × (12 × 10) mm

Design by Yasuyuki Akiba

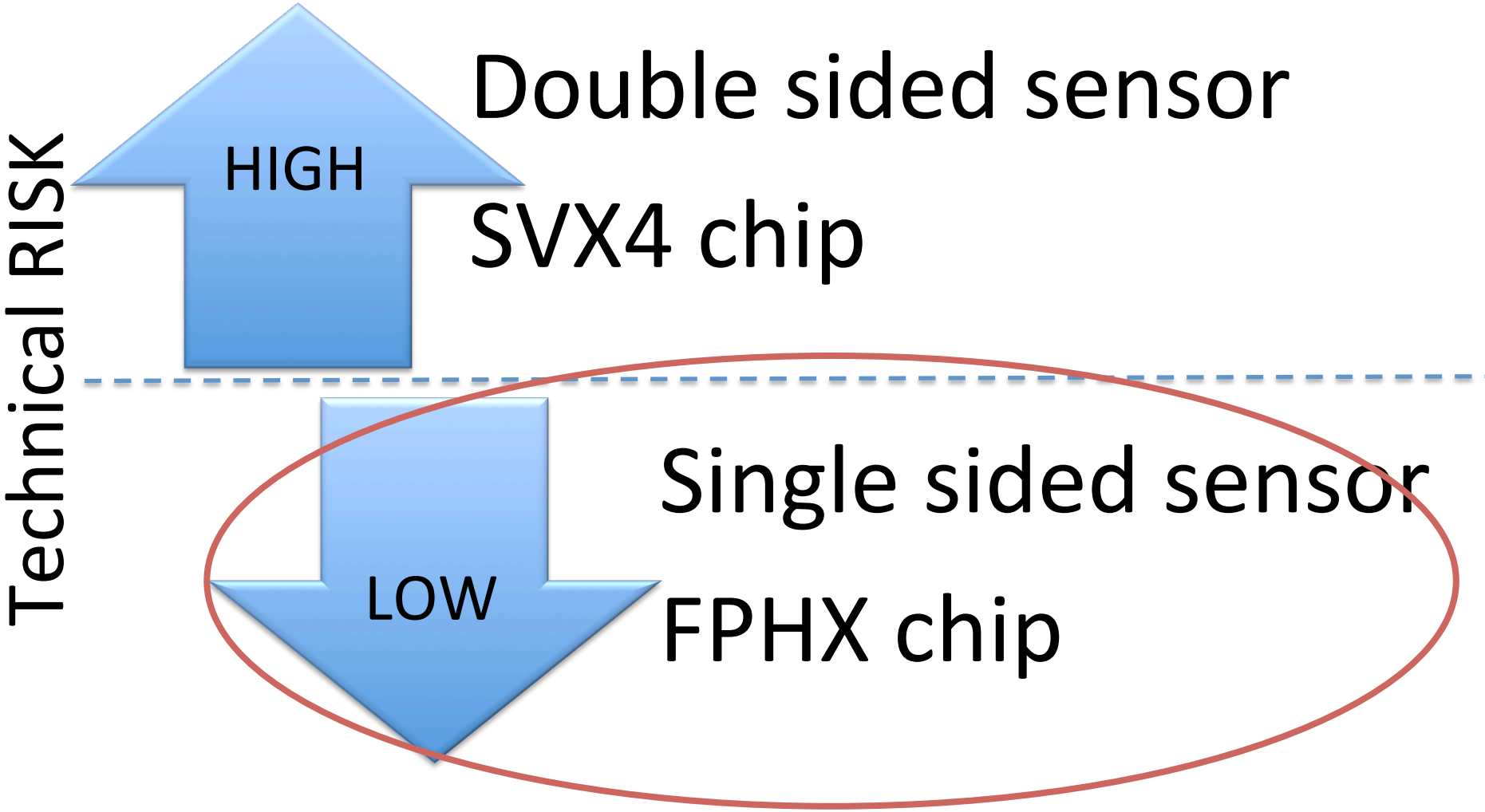
Managements

- Project manager (Itaru Nakagawa)
- deputy manager (Rachid Nouicer)
- Subsystem managers
  - Detector assembly and construction (Rachid Nouicer)
  - Mechanical and integration (Rob Pisani)
  - Electronics and readouts (Eric Mannel and Takashi Hachiya)
  - Software (Gaku Mitsuka)
  - LV + HV and Slow control (Yorito Yamaguchi)

Outline

- Role of the intermediate tracker (INTT)
- INTT concept
  - Configuration
  - Technology
  - Cost

Technological Choice



Collaboration

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- RBRC (T. Hachiya, G. Mitsuka,Y. Yamaguchi)
- BNL (J. Huang, M. Lenz, E. Mannel, R. Nouicer, R. Pisani)
- Rikkyo (H. Masuda, Kazu Kurita?)
- Nara woman's university (M. Shimomura)
- LANL (M. Brooks, M. Liu)
- New Mexico (D. Field*)
- J-Parc (S. Hasegawa, H. Sako)
- Tsukuba (S. Esumi)

*FVTX expert

Basic Project Philosophy

Basic Design Philosophy

Technology

- Employ existing technology
- Employ technology we are familiar with

Man Power

- Collaborate with Institutes which have the experience and infrastructure

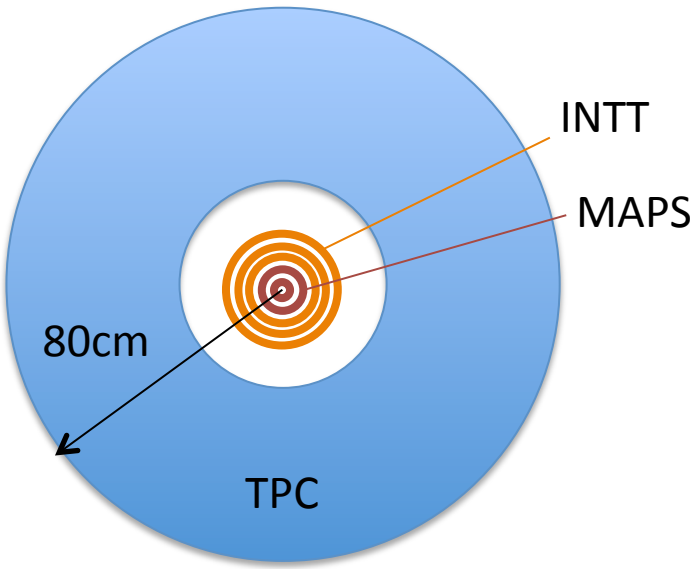
Minimum Cost

- Little “R” and rather focus on “D”
- As compact as possible

Schedule

- **To be in time for 2022**

Quick Overview of Intermediate Silicon Tracker (INTT)



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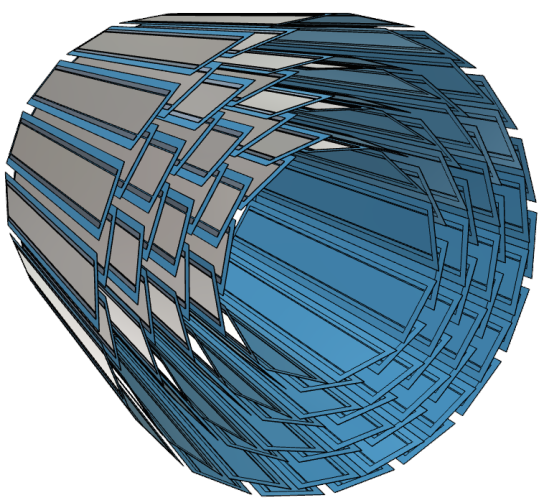

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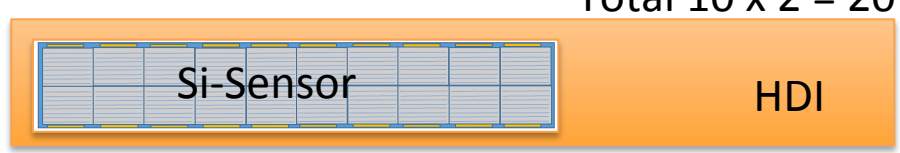
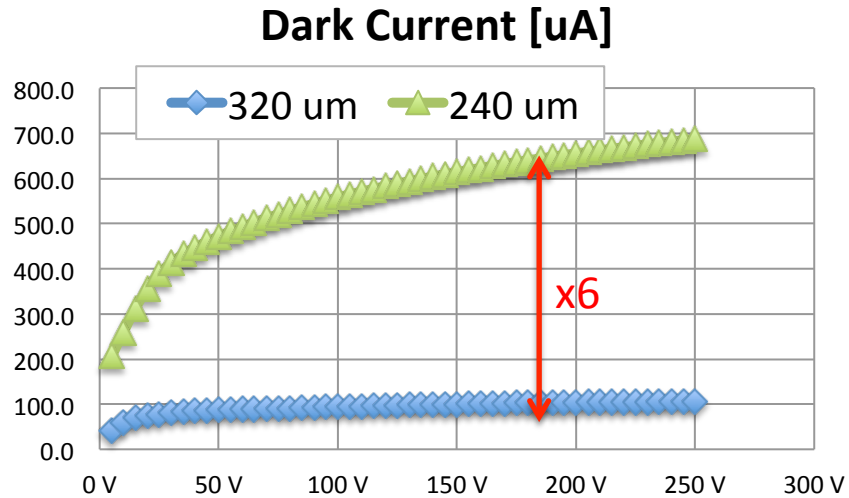
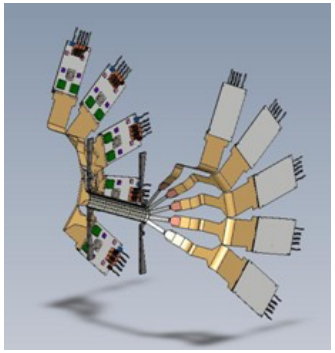
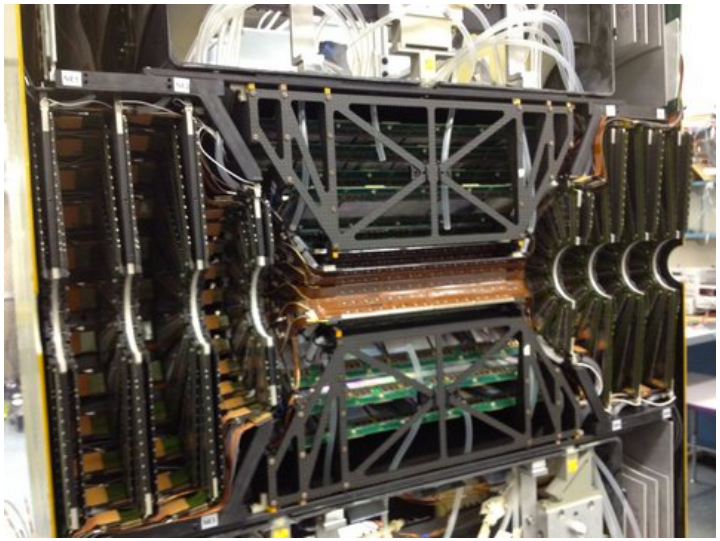
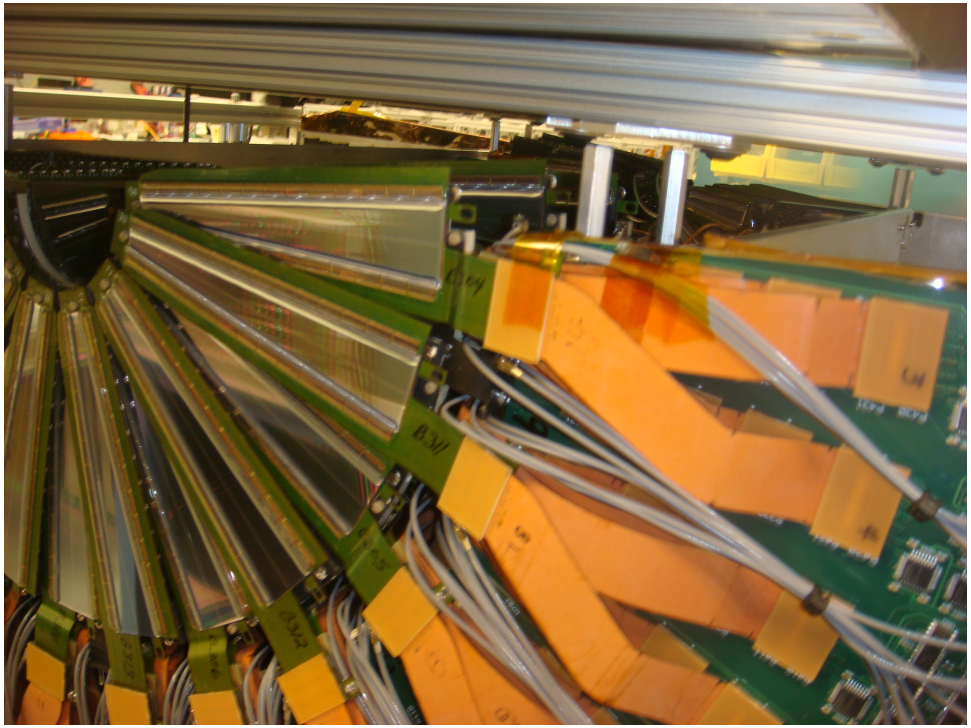
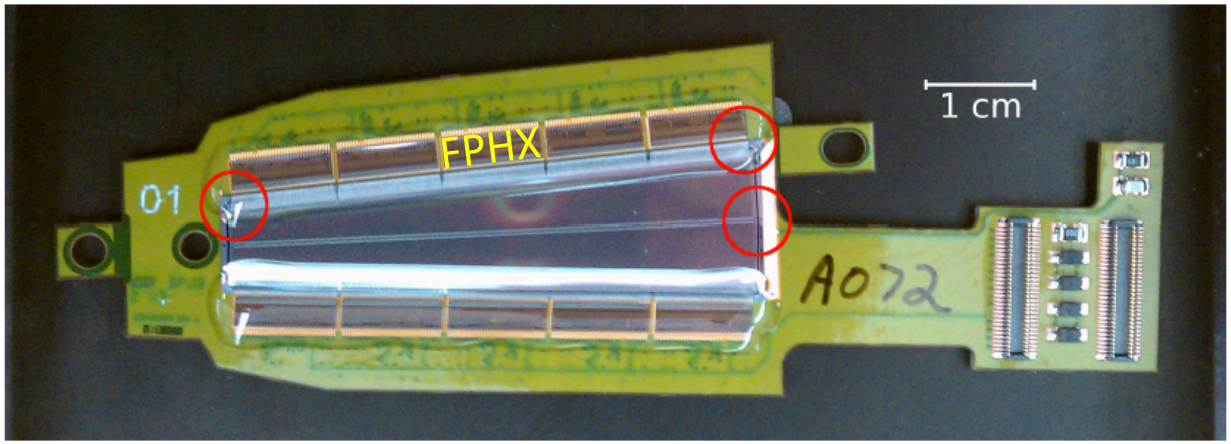


Technical Challenge

- Thinner Silicon Sensor
  - Trade off of S/N ratio
- Solid Coolings





- Adaption of FVTX Electronics to INTT.

FVTX Detector