LAr Calorimeter Upgrades for Phase-I

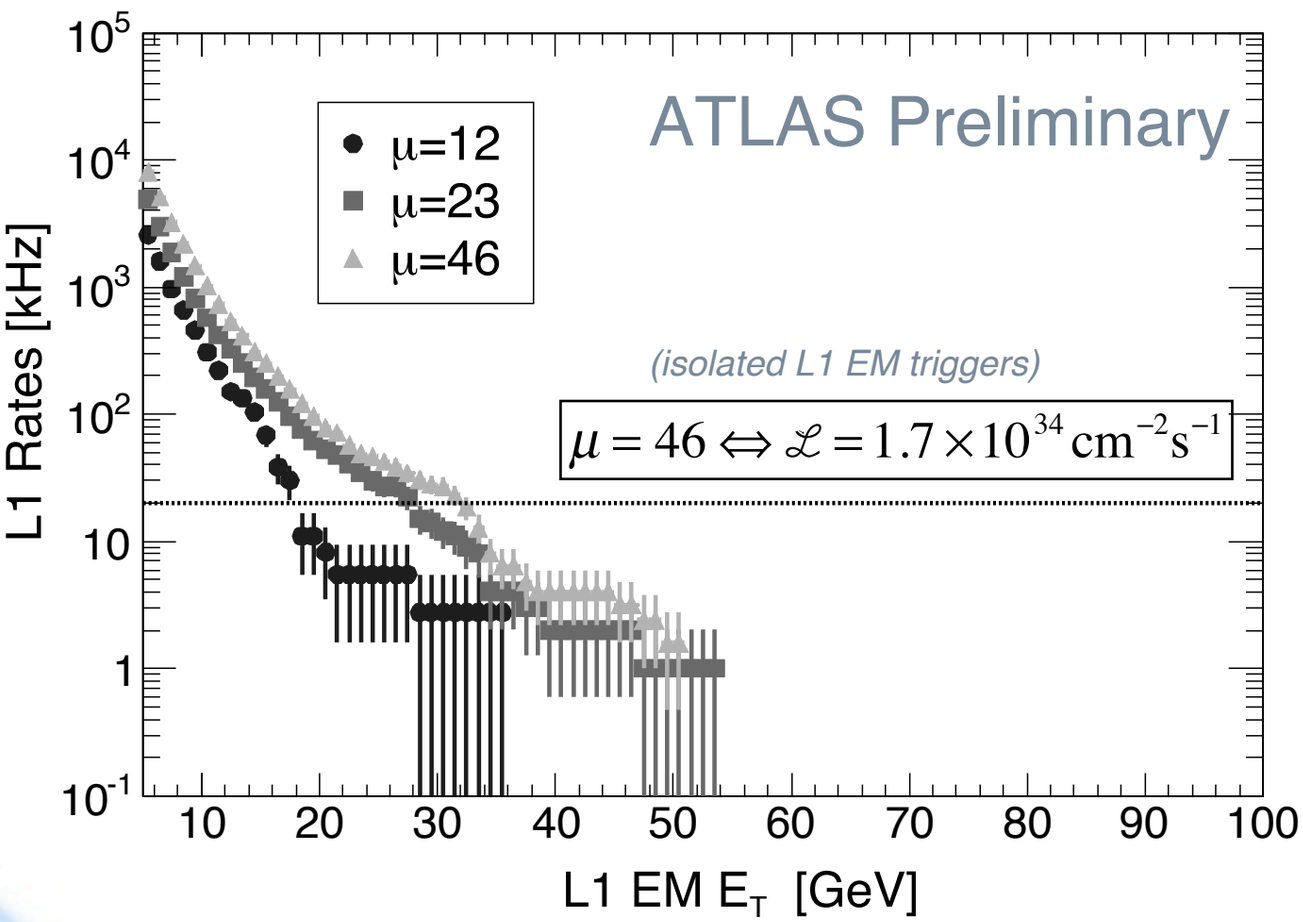
F. Lanni

Outline

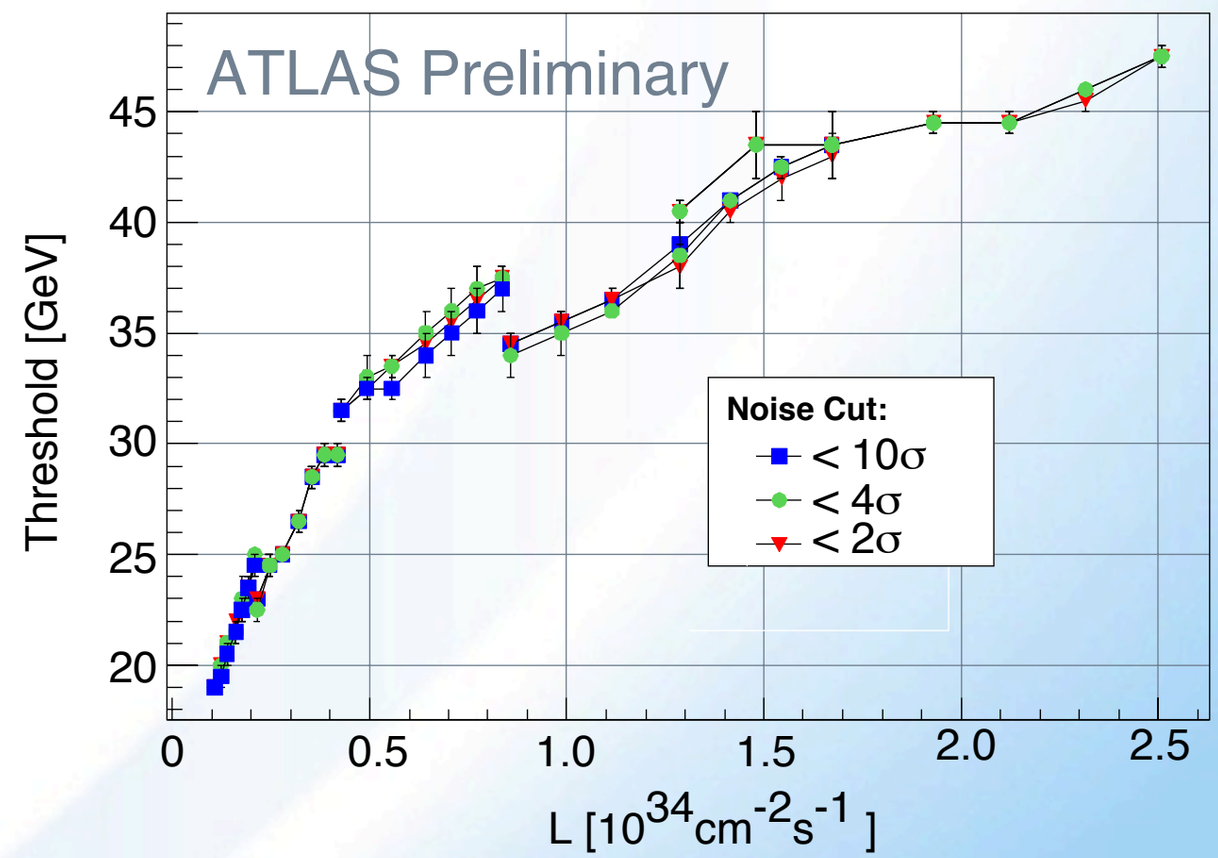
- Motivations
- Upgrades of the LAr EM Calorimeter Trigger Readout
- Options for LAr HEC and FCal
- LAr Phase-I Upgrade Project: plan and milestones
- Core Cost Estimates of the project
- U.S. participation and resource estimates in the US

Motivations

- New challenges for hardware-based triggers involving calorimeter readout information beyond nominal luminosity design:
  - Rates increase (linearly in the best cases)
  - Resolution are degraded ⟹ worse turn-on curves



Thresholds for non isolated EM objects vs. Inst. Luminosity @ 20kHz Level-1 Trigger rate



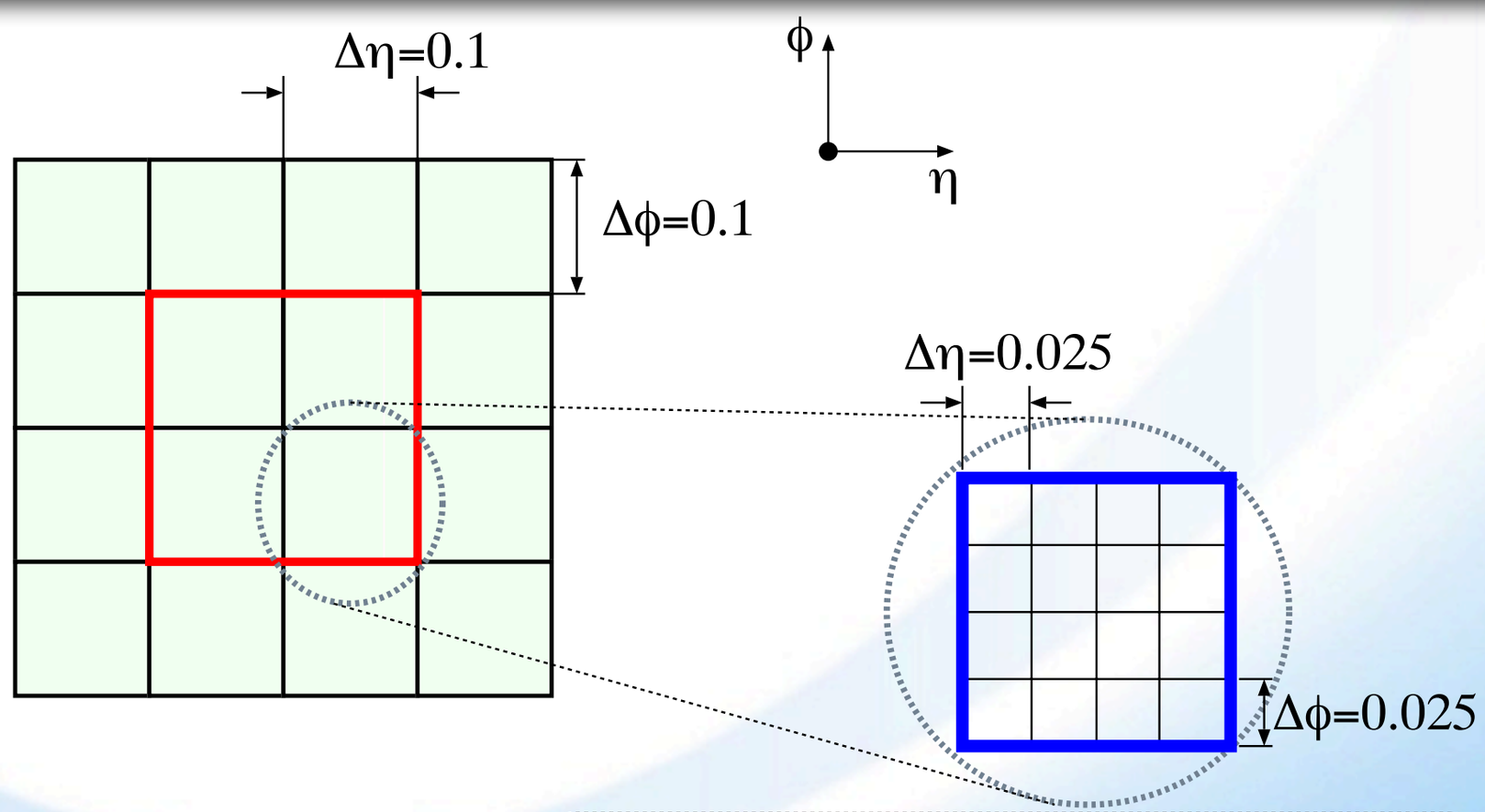
- **Need to improve trigger system to maintain adequate performance as luminosity increases beyond nominal design value**
- **Otherwise, higher thresholds would have to be deployed to control the rates, which would significantly reduce the efficiency of the physics channels**
  - and compromise ATLAS capability to search for new phenomena and for precision measurements of established processes.

Motivations in the US

- US groups have led the construction of the LAr calorimeter readout electronics and retain the scientific leadership and technical expertise to extract and process the calorimeter information for either trigger, reconstruction and analysis.
- Until recently 6-12 months ago our focus was on R&D progresses towards Phase-II with the possibility of introducing a demonstrator concept on-detector on a shorter timescale.
  - Since then we have studied in details the rates for EM triggers, and we have come to the conclusion that the current Level-1 system will not be able to cope with the upgraded luminosity. We devised algorithms, based on finer granularity information sent to the Level-1 processors to better control the rates.
- **The ideas and strategies proposed in the ATLAS Letter of Intent (and here) have been initiated and led by US scientists.**
- **We are strongly motivated to pursue and realize their implementation.**
- Currently active in the upgrade R&D program
  - U. Arizona
  - BNL
  - Columbia/Nevis Lab.
  - U. Pennsylvania
  - SMU Dallas
- New groups:
  - SUNY Stony Brook
  - U. Iowa (?)

Current and Proposed Solution

- **Goal: Preserve un-prescaled Level-1 thresholds for single electron triggers at p_T~25 GeV for LHC operation beyond the nominal design (Phase-I LHC and HL-LHC)**
  - Improve rejection against jets faking electrons, implementing algorithms similar to the ones used in HLT and offline
  - Shower shape using high granularity data from the EM calorimeters (2nd layer and possibly 1st layer as well)



In the 2nd layer of the EM calorimeter a single trigger tower is made of 16 calorimeter cells.

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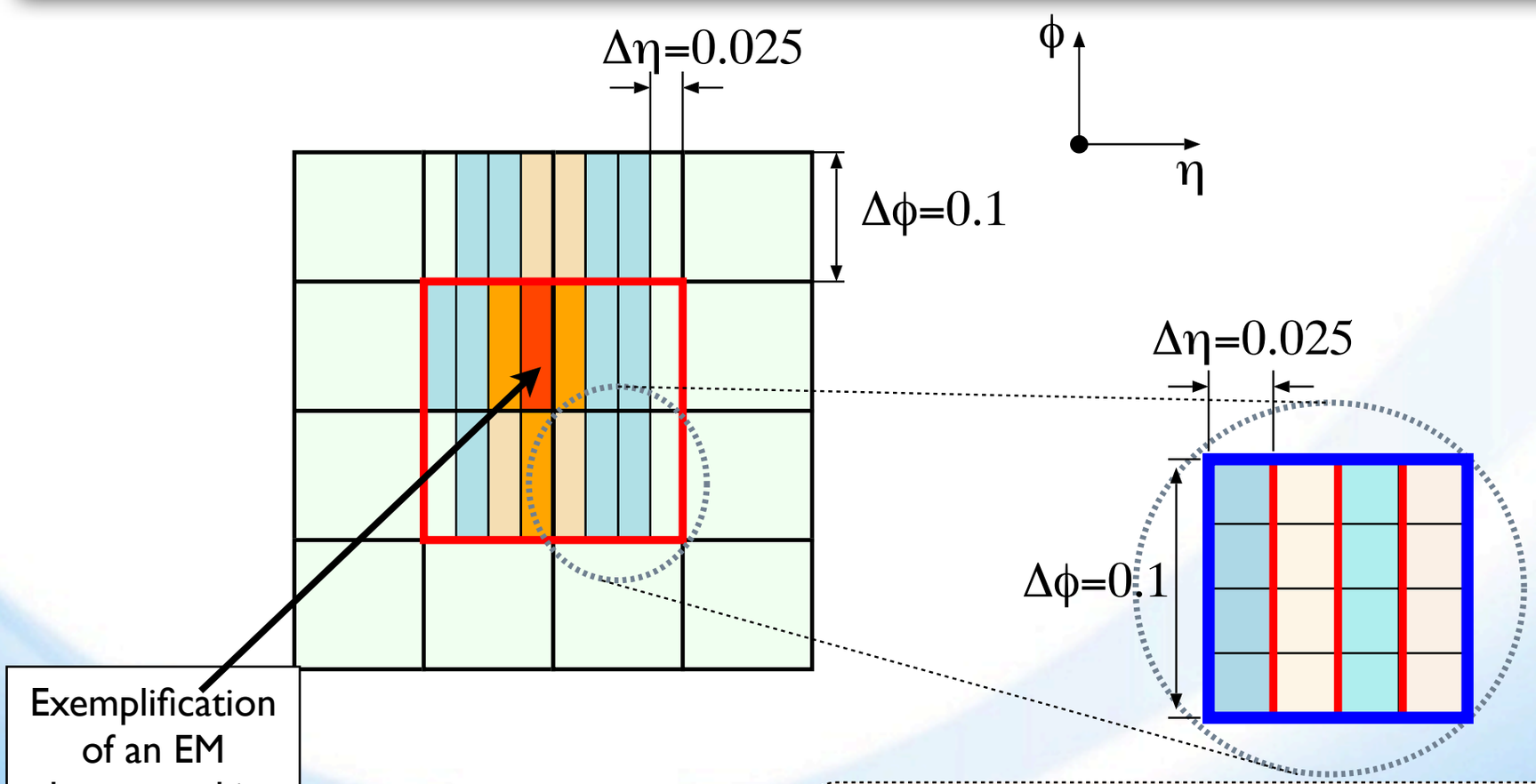


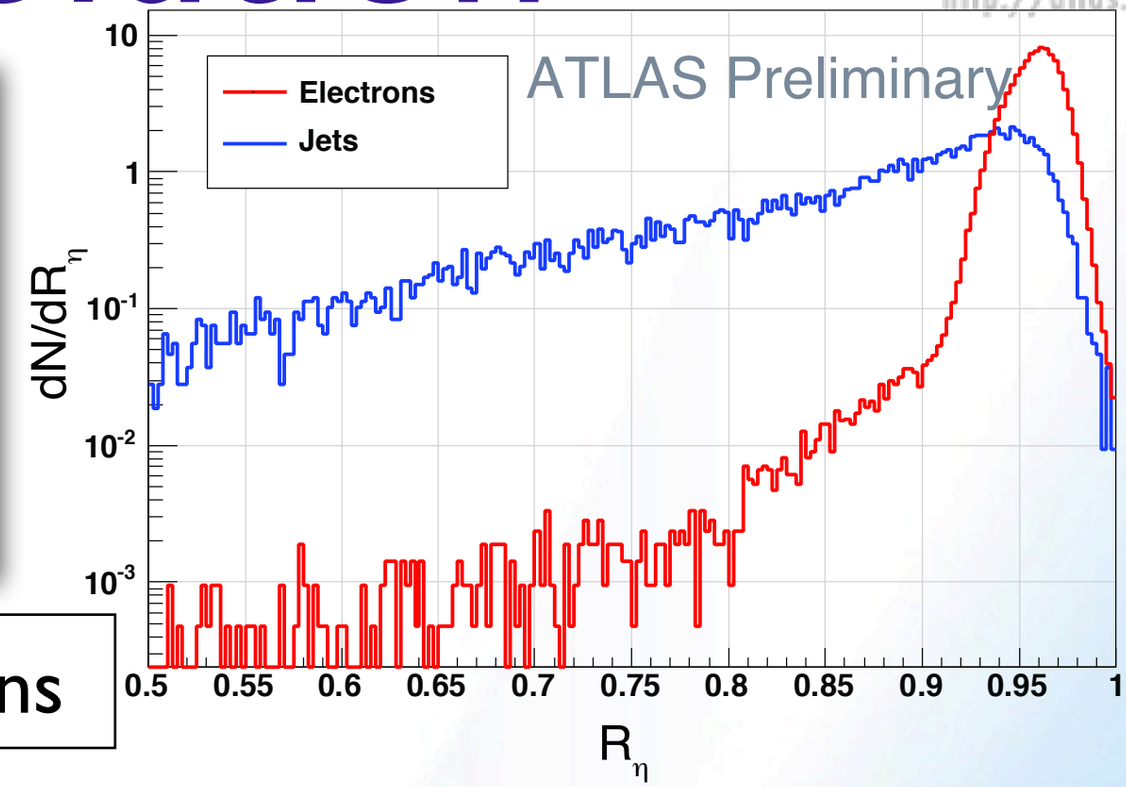
Exemplification of an EM shower and its lateral energy profile across the Super-Cells

"Super-Cells" are formed by grouping 4 cells in φ inside the Front-End Boards. The signals of the SuperCells are digitized in the new TBB

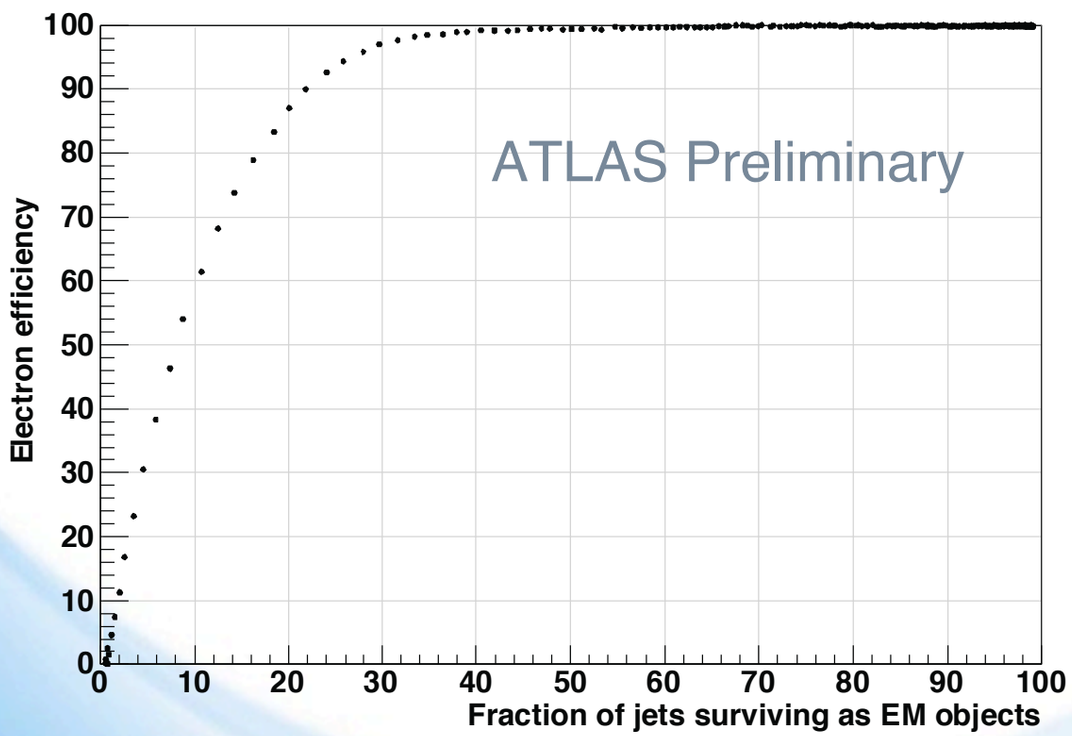
Proposed solution

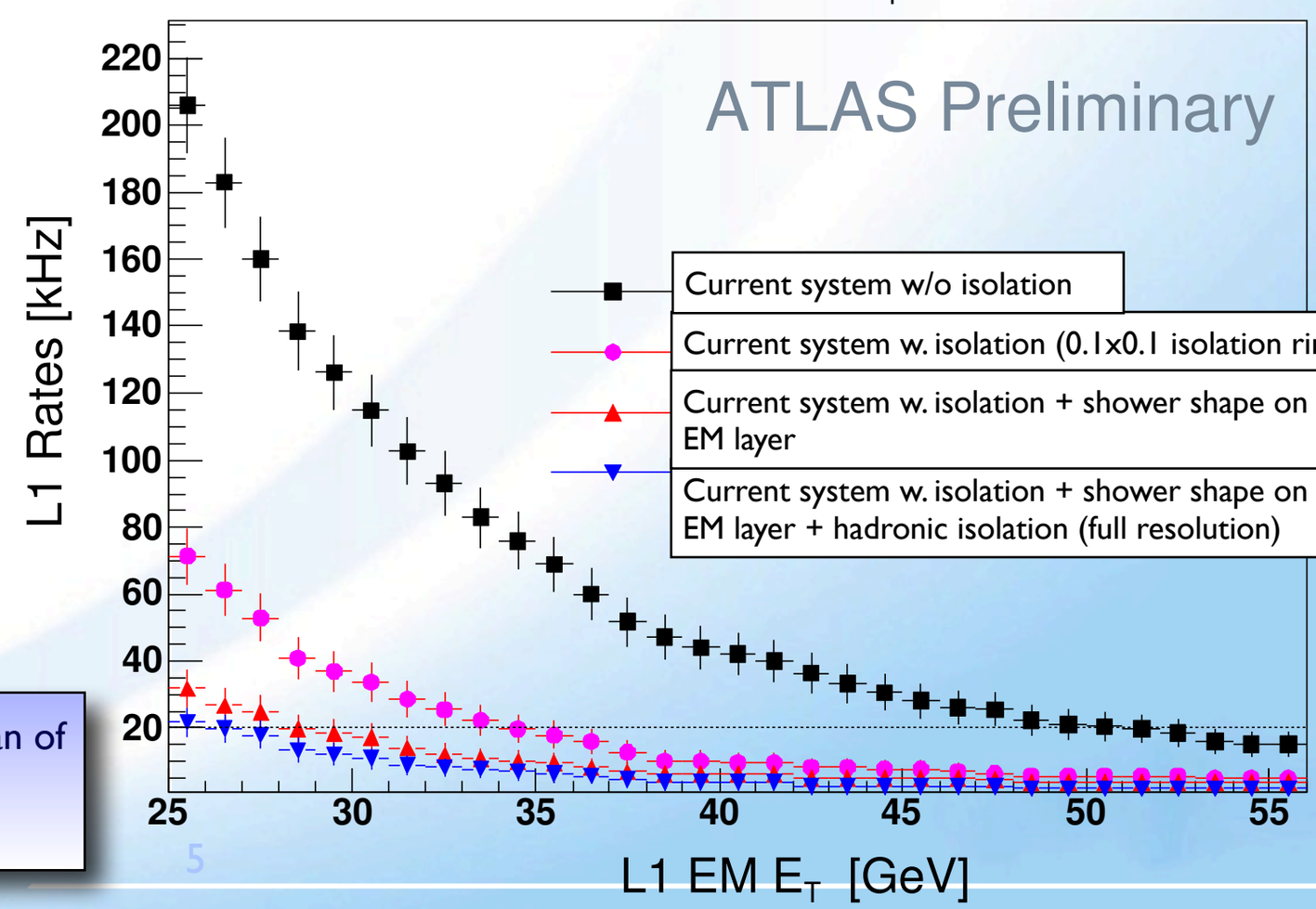
Shower shape cut on R_η:
ratio of energy in clusters of two sizes

$$R_\eta = \frac{E_{3\times 8}}{E_{7\times 8}}$$



Simulations for $\mathscr{L}$ = 1.7x10^{34}cm^{-2}s^{-1} @25ns

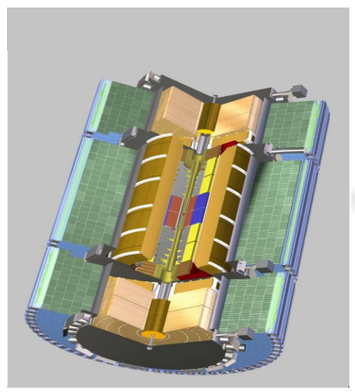


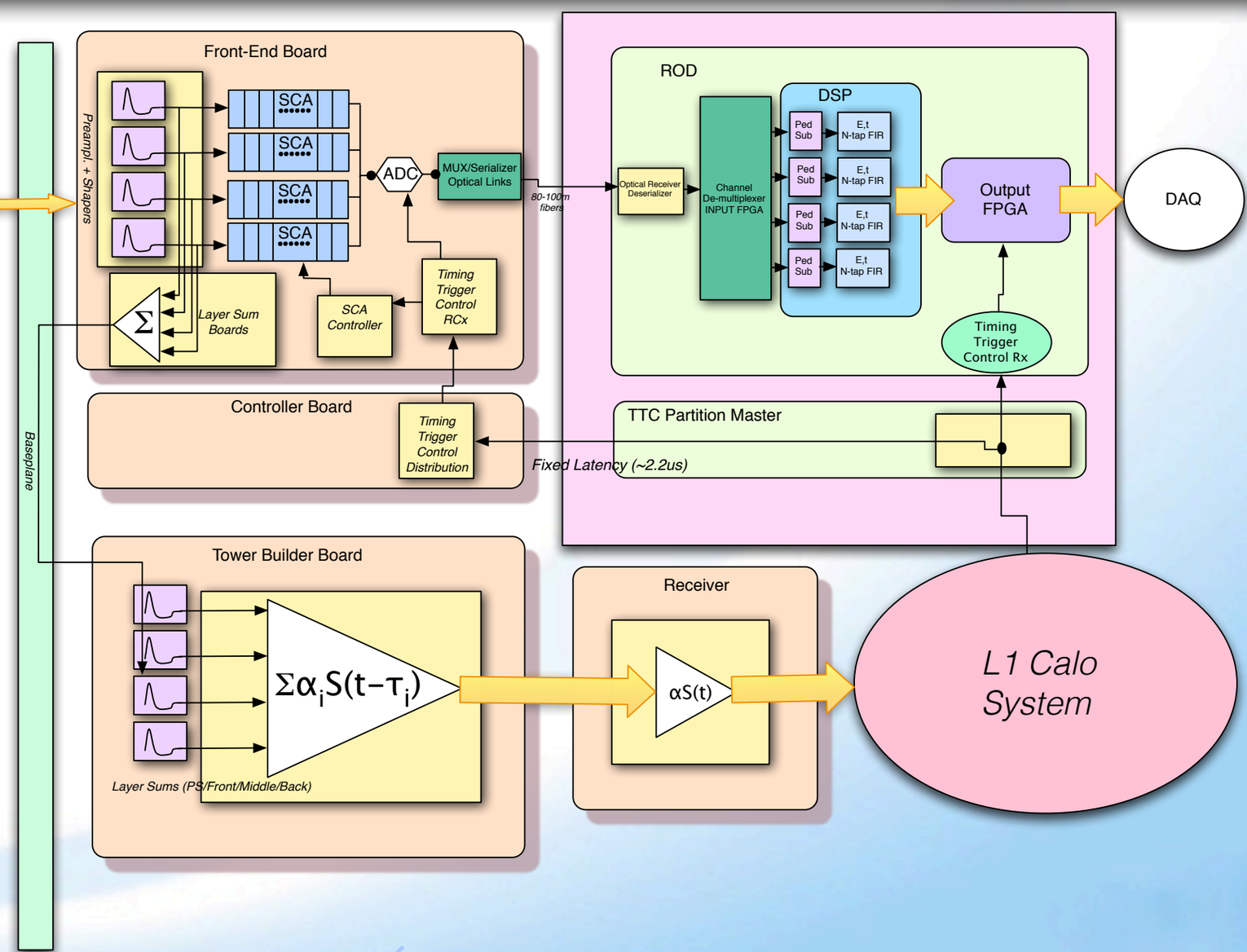


"**Receiver operating characteristics curve**": scan of the Rη parameter in the electron efficiency vs. "fake" rejection power.

LAr Calorimeter Readout: Current System and Trigger Interface

- **Currently** on-detector summing stages of analog signals in the Front-End Board (FEB) and trigger Tower Builder/Driver Boards (TBB/TBD)
  - $\Delta\eta\times\Delta\varphi=0.1\times0.1$ layer sums at the output of the Front-End Boardss
  - trigger towers at the output of the Tower Builder Board/Tower Driver Board
  - processed by the Level-1Calo processors





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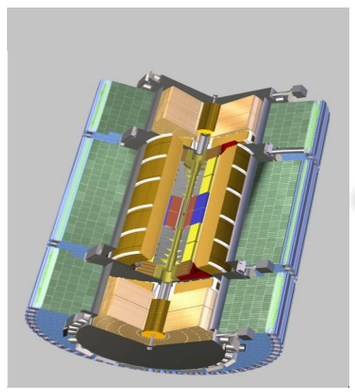
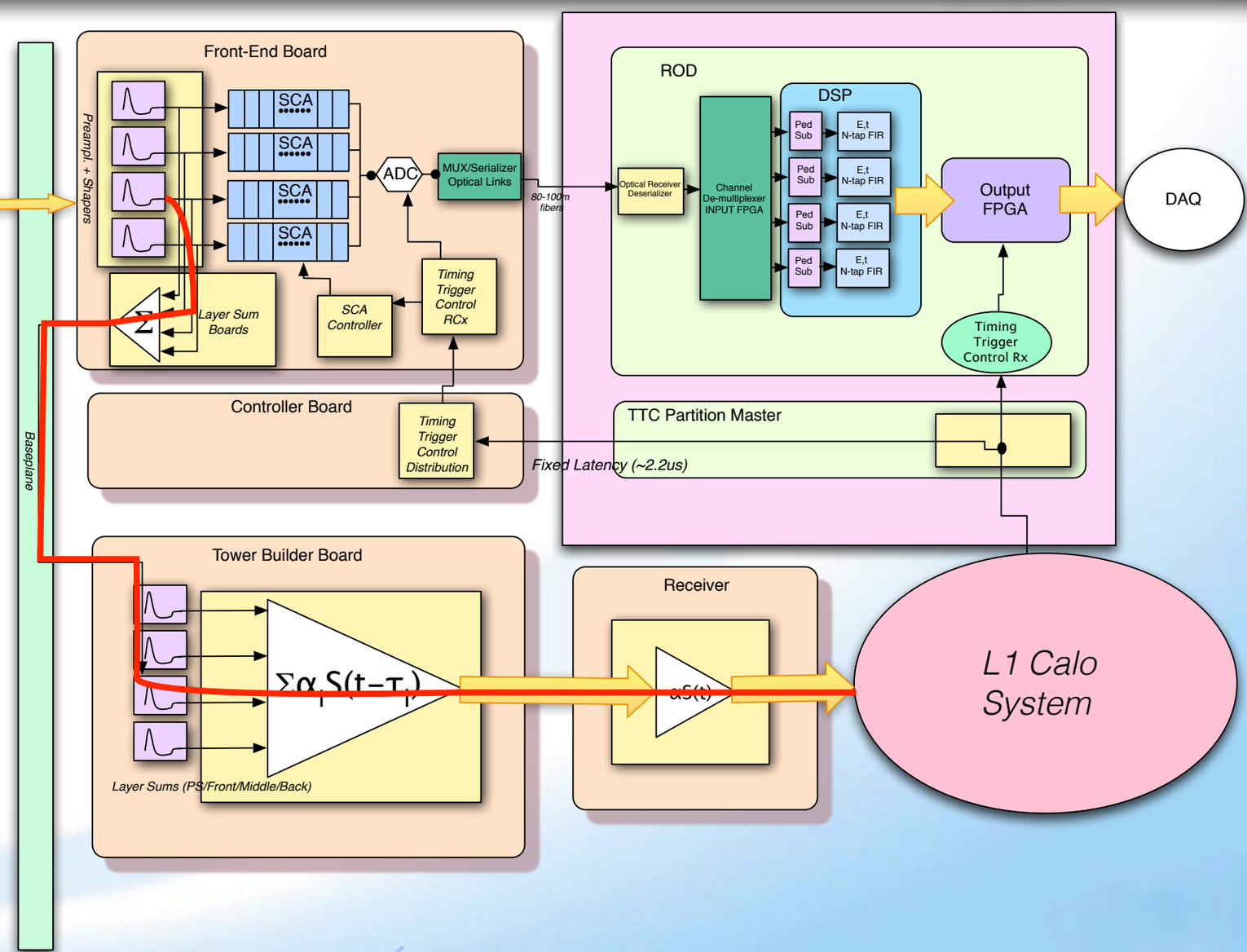
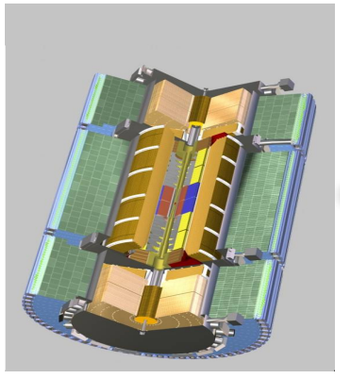
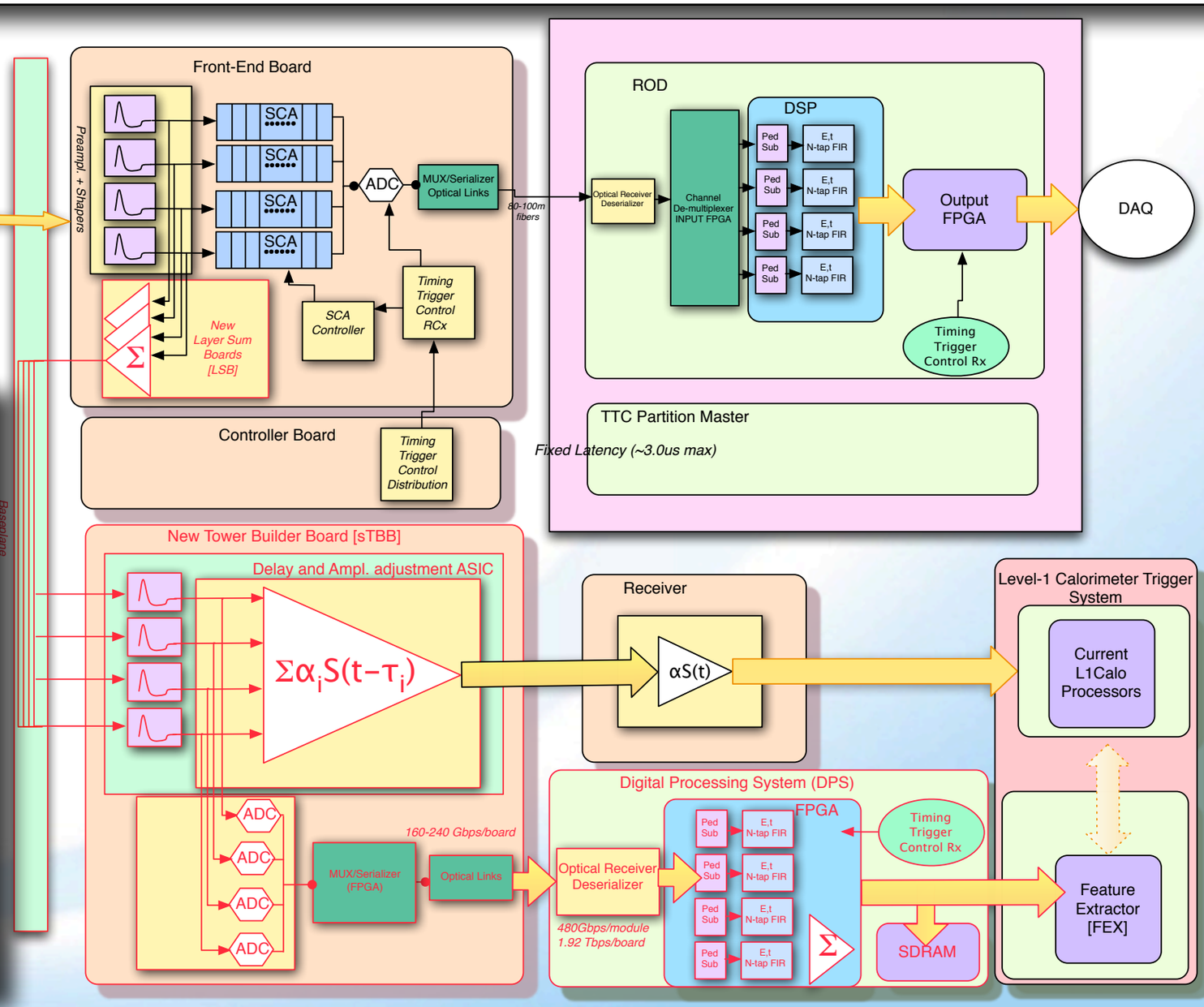




LAr Calorimeter Readout: Phase-I Upgrades

- **Proposed architecture for EM calos**:
  - Analog section implemented by ASICs (shaping, summing stages and delay lines)
  - Layer sums of $\Delta\eta\times\Delta\varphi=0.1\times0.1$ (PS, 3rd EM layer) and "super-cells" $\Delta\eta\times\Delta\varphi=0.025\times0.1$ (1st, 2nd EM layers) individually digitized and transmitted via high bandwidth optical links
  - Digital Processing Systems reconstruct fully calibrated energy reconstruction (each BC) and send the results to the new components in the L1Calo processors (Feature Extractors...)





- Baseplanes
- Layer Sum Boards (on FEBs) [*US collaborating*]
- New high-density Tower Builder Boards [*US leading*]
- Digital Processing system [*US collaborating*]

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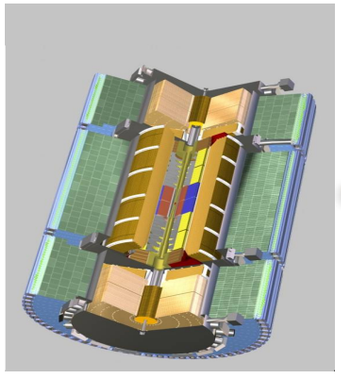

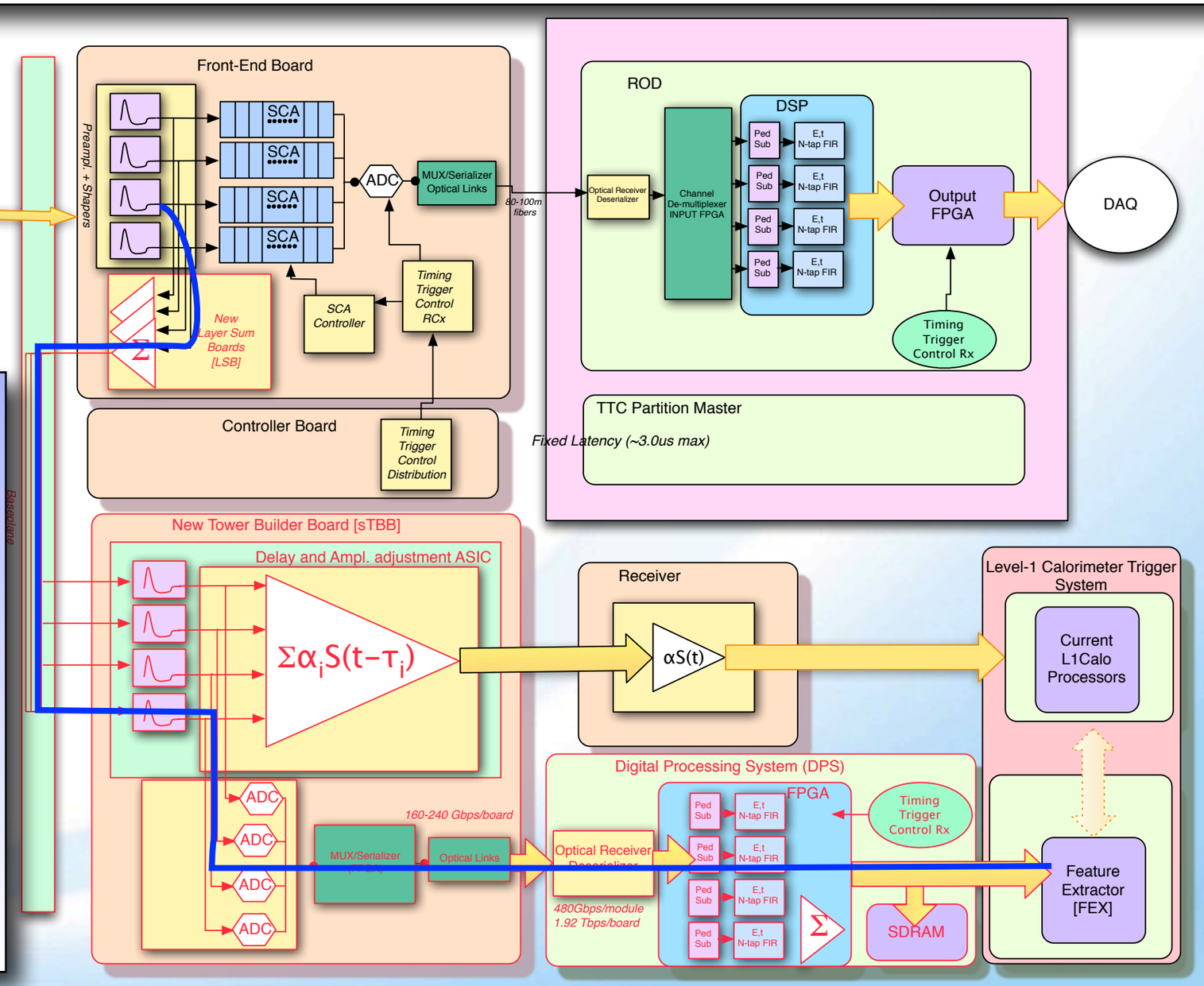

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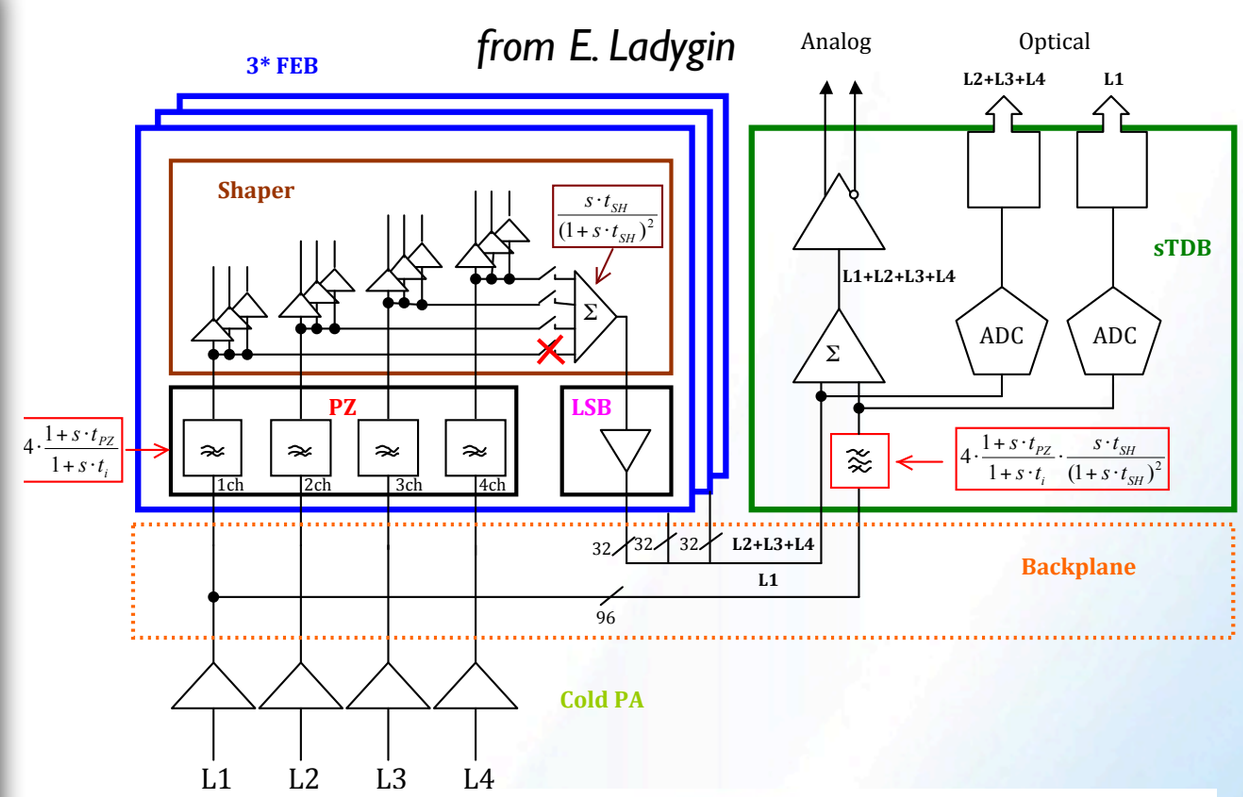
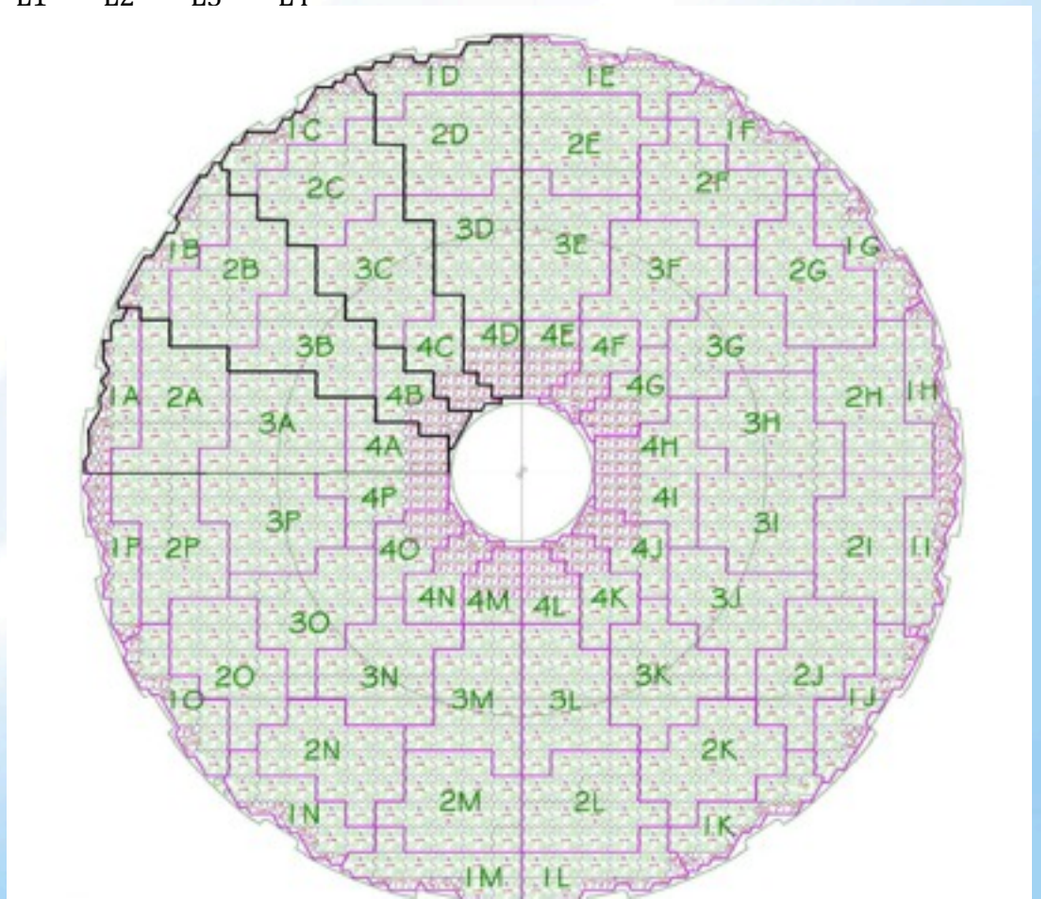
Options for LAr Hadronic End-Cap and Forward Calorimeters

- ***Under study***
- In the Hadronic End-Cap (HEC) calorimeter the tower from the 4 layers is formed by the Layer Sum Boards (LSB) in the Front-End Boards (FEB)
  - The first layer and the sum of the remaining 3 could be sent to the Tower Driver Boards (TDB) separately
  - provided it improves the jet resolution in the Level-1 trigger and sharpens the turn-on curve
- High granularity Forward Calorimeters (FCal) proto-trigger towers could be digitized individually and transmitted optically from the FCal TDBs by upgrading baseplanes and the FEB LSBs and the TDB itself
  - ... Missing Transverse Energy (MET) trigger impacted significantly by pileup in the FCAL due to the size of the trigger towers
- Possible max. granularity:
  - FCAL1: 16 η-bins x 16 φ-wedges
  - FCAL2: 8 η-bins x 16 φ-wedges
  - FCAL3: 4 η-bins x 16 φ-wedges





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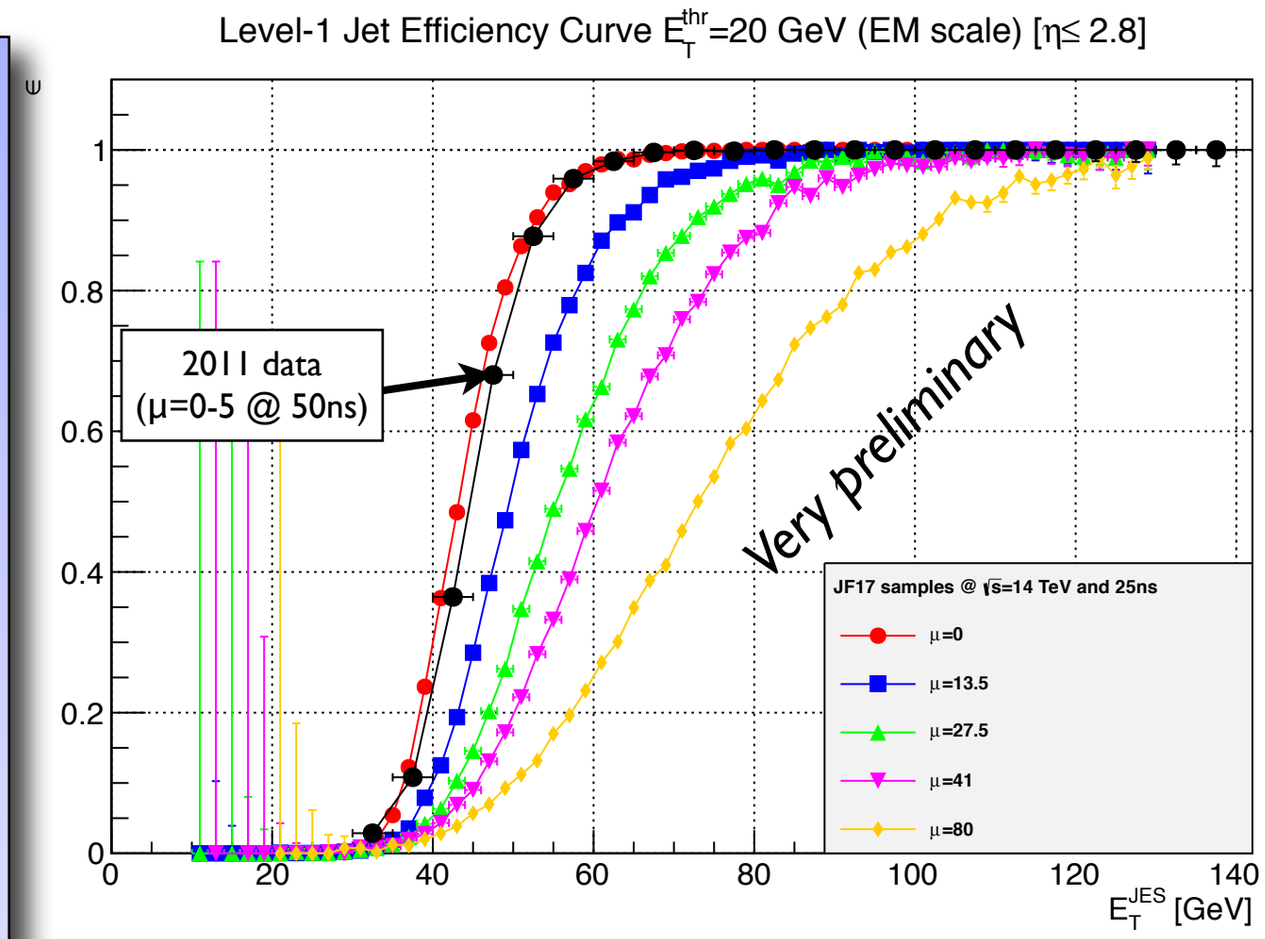
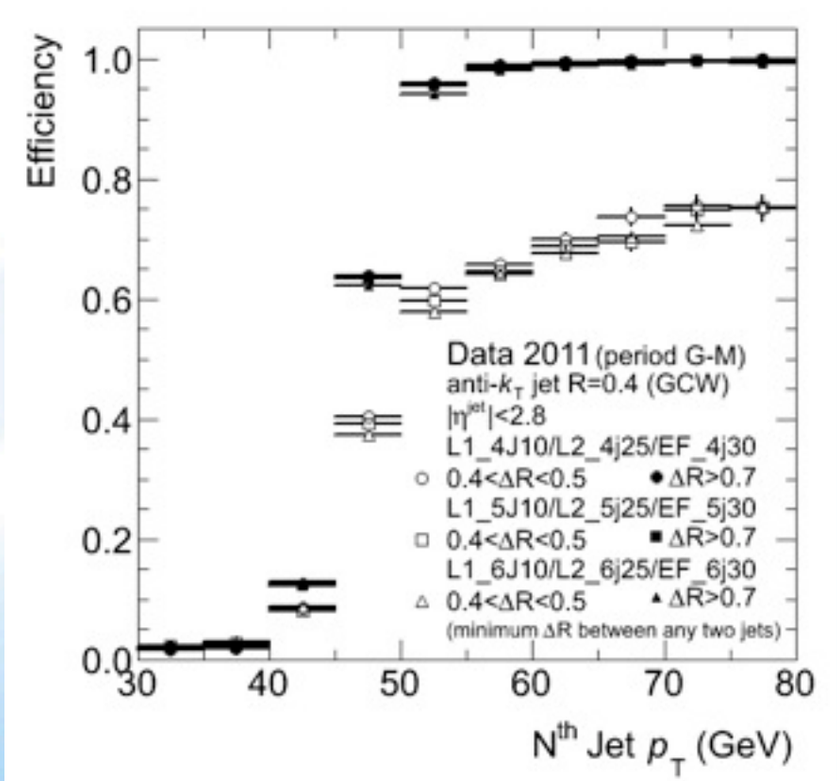




from M. Begel (2011 data)

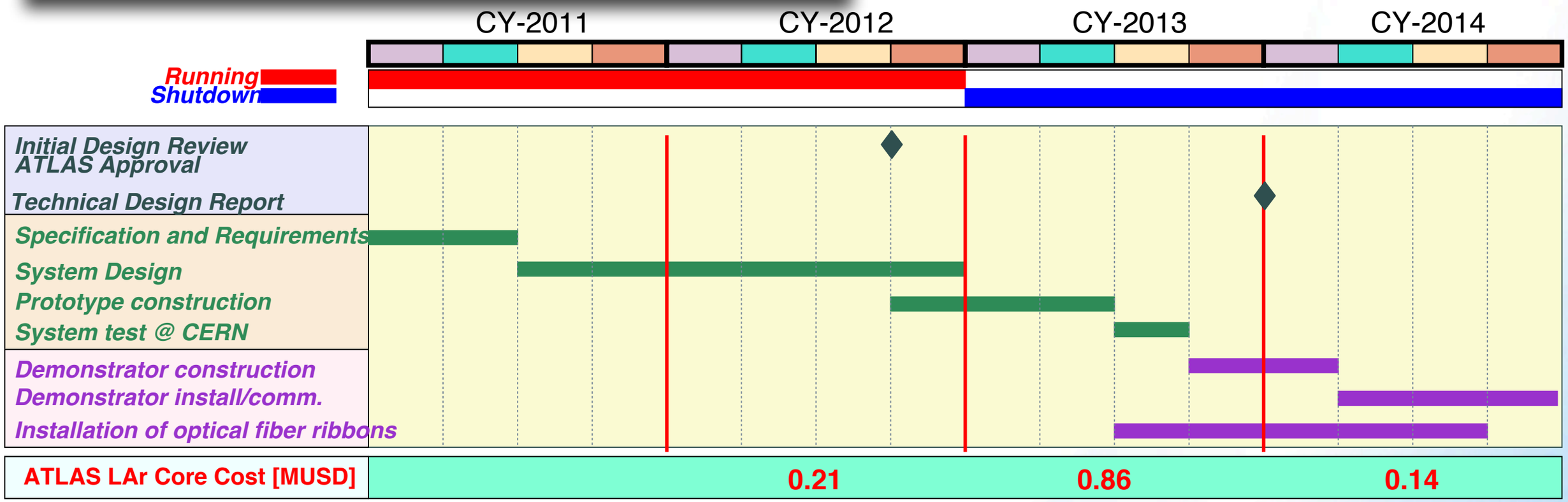
Toward a Phase-I Upgrade Project

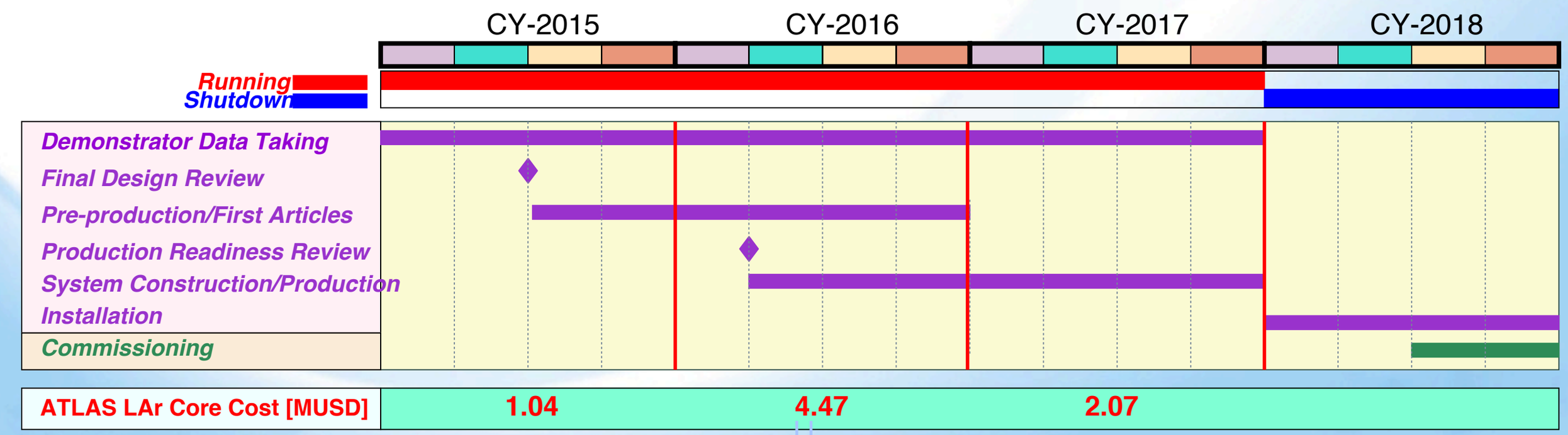
- **ATLAS Approval (Initial Design Review): end of summer 2012**
- Three Steps: design, demonstrator and construction
- Vertical slice/Demonstrator on a $\Delta\eta\times\Delta\varphi=1.4\times0.4$ (LAr), $\Delta\eta\times\Delta\varphi=0.4\times0.4$ (TileCal) partition of the barrel detector during Phase-0 and in the following years
- Purpose of the demonstrator is to validate the architecture of the new calorimeter readout and trigger interface. Not to validate the components (e.g. radiation tolerant)
- **Upgrade Project:** upgrade of all the Tower Builder Boards, baseplanes and large fraction of the Layer Sum Boards in the Front-End Crates, production of the Digital Processing boards and interfaces to the Level-1 trigger processors

	Start	End
System Design	2011	2013
Prototype and Demonstrator	2012	2014
Construction and Installation	2014	2018

Phase-I Upgrade Project

- Milestone and Core costing:
  - Total ATLAS Core Cost: 8.79 MUSD





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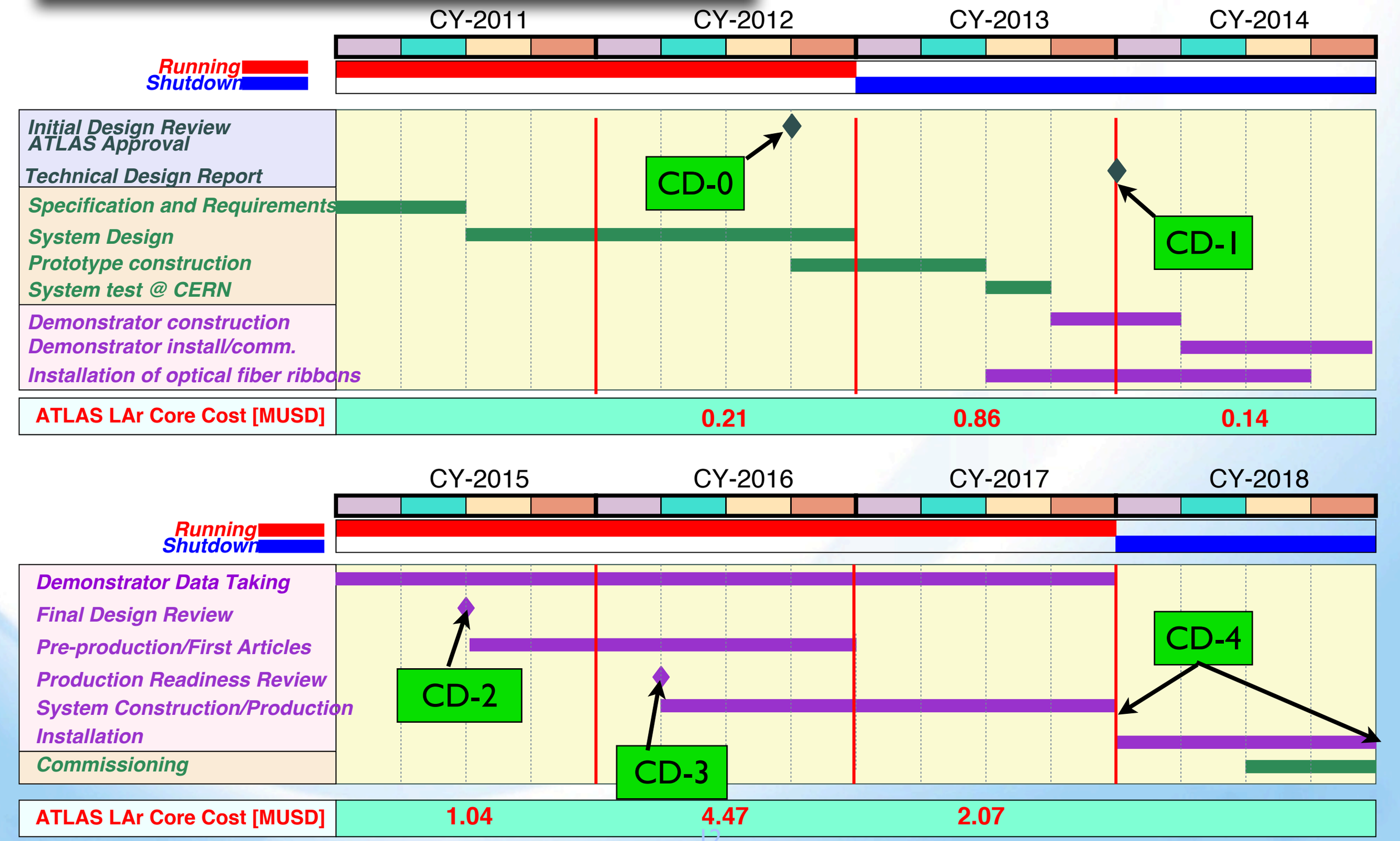

US effort and interests

System Component	Research Group
Front-End Baseplane	Milan
Front-End Crate Connectors/Shielding	Common Funds
Layer Sum Boards	BNL,Milan
New Tower Builder Boards (sTBB) and Integration	BNL,Saclay, LAL
sTBB analog shaping and delay	LAL, Saclay, Penn.
sTBB ADC	Columbia, Grenoble
sTBB ASIC based MUX/Serializer	Nevis,SMU
sTBB FPGA based MUX/Serializer	BNL, SMU, Milan, MPI
sTBB Optical Transm.	SMU
sTBB Mechanics/Cooling	CERN, BNL
Optical Fiber bundles	CERN
Optical Switches	CERN
DPS optical receiver	Arizona, LAPP
DPS processing unit	Arizona, BNL, Dresden, LAPP, SUNYSB
DPS motherboard	LAPP
DPS config. plugin	LAPP
DPS controller plugin	LAPP
DPS rear transition modules	Arizona, Dresden, LAPP
ATCA shelf and infrastr.	Dresden, LAPP
ATCA crate controller	Dresden, LAPP
ATCA switches	Dresden, LAPP
ATCA monitoring and configuration	Dresden, LAPP

- **US participation is approximately:**
  - 35% in deliverables (core costing)
- **Rough estimates with large uncertainties:**
  - Next 8-10 months the migration to an ATLAS Upgrade project should complete. Interests and responsibilities of the different institutions (and technical options) should be better understood

US Effort: Core Costing

		US CORE COST (kUSD)	FY12	FY13	FY14	FY15	FY16	FY17	FY18
Front-End Electronics									
	Layer Sum Boards (LSB) EM (50%)	379	-	8	-	-	372	-	-
	LSB FCAL (50%)	11	-	-	-	-	11	-	-
sTower Builder Boards									
	Pole-zero cancellation ASIC	220	28	28	-	-	165	-	-
	Variable gain ampl.and Delay ASIC (50%)	183	25	25	-	-	133	-	-
	ADC	689	50	50	-	50	539	-	-
	Silicon on Sapphire ASICs: Serializer/Laser Drivers	300	30	30	30	105	105	-	-
	Optical Transmitters	180	-	10	-	85	85	-	-
	Cooling Interface	74	22	-	-	26	26	-	-
	Board Construction and assembly	586	-	71	71	-	222	222	-
Digital Processing System (DPS)									
	sPU Daughter Cards (25%)	498	-	14	-	-	242	242	-
TOTAL US-ATLAS LAr Part.		3,120	154	235	101	266	1,899	463	-
TOTAL ATLAS LAr Core		8,790							
Fraction of total core costing (%)		35.5							

Demonstrator Design and Prototype

Construction and Installation

US Effort: Total Resource Estimate

U.S. ATLAS Phase 1 Upgrade Construction Project
LAr Calorimeter Trigger Readout Cost Profile (AYk$)

LAr Upgrade R&D	FY12	FY13	Total
Core Deliverables $	158.00	228.00	386.00
Non-Core Material $	261.38	282.18	543.56
Travel $	48.46	52.16	100.62
TOTAL M&S	467.84	562.34	1,030.18
Labor	1,922.37	1,988.09	3,910.46
EE	9.15	9.15	
ET	2.00	2.00	
Student	3.72	3.84	
TOTAL	**2,390.21**	**2,550.44**	**4,940.65**

LAr Construction Cost Profile

	FY14	FY15	FY16	FY17	FY18	Total
Labor $	2,015.38	2,281.10	2,498.15	2,231.18	1,244.37	10,270.17
Core Deliverables $	101.00	392.69	1,749.69	221.00	-	2,464.39
Non-Core Materials $	212.70	294.20	184.20	111.70	111.70	914.50
Travel $	49.96	55.26	54.26	54.26	43.46	257.21
TOTAL	**2,379.04**	**3,023.25**	**4,486.30**	**2,618.14**	**1,399.54**	**13,906.26**

LAr Construction FTE Breakout

	FY14	FY15	FY16	FY17	FY18	Total
EE	9.03	9.03	9.28	8.15	5.30	40.79
ME	-	0.30	0.30	0.10	-	0.70
ET	1.70	2.40	2.40	3.20	1.70	11.40
MT	-	-	0.20	0.20	-	0.40
Student/EE PDOC	3.84	4.04	3.84	1.74	1.54	15.00
Total	**14.57**	**15.77**	**16.02**	**13.39**	**8.54**	**68.29**

Conclusions

- **We have proposed to increase the granularity of the calorimeter trigger readout to prepare Level-1 trigger primitives:**
  - Aiming at a very high efficient electron selectivity with algorithms similar to the ones used in the offline reconstruction
  - Effectively reducing the backgrounds from jets mimicking the electrons in the ATLAS calorimeter
  - Improving resolution for Missing Transverse Energy in particular in the forward region
- **We have initiated and we are leading the performance studies and the innovative technical R&D**
  - Building on the several years of experience during construction, commissioning and data analysis.
  - Enabling the whole international collaboration to grow and advance in technology.
- **Our proposal and strategies are today part of the ATLAS baseline upgrade plan for Phase-1 (Letter of Intent being finalized).**
  - **We are seeking in ATLAS formal approval of the LAr Phase-1 upgrade project by end of summer 2012.**
- We are eager to pursue and realize the implementation of our ideas, aiming at a leadership role in construction, installation and commissioning.
  - If supported we need now to plan how to build up critical technical resources in the US for the realization of the upgrade project.

Backup

Core Cost Estimates

New LAr Calorimeter Electronics(LAr)

contacts: F. Lanni

Deliverables		CORE COST (MCHF)	calculated	2012	2013	2014	2015	2016	2017	2018	total	comments
Fill in	*Fill in*	*Fill in*	*calculated*	*Fill in*	*Fill in*	*Fill in*	*Fill in*	*Fill in*	*Fill in*	*Fill in*	*calculated*	
												1 USD = 0.908
												1 EUR = 1.21
Baseplane			1.076									
	Baseplane construction and assembly	0.894		0.000	0.007	0.007	0.440	0.440	0.000	0.000	0.894	
	FEB connectors and shields	0.182		0.000	0.000	0.000	0.091	0.091	0.000	0.000	0.182	
Front-End Electronics			0.743									
	LSB EM	0.689		0.000	0.014	0.000	0.000	0.675	0.000	0.000	0.689	
	LSB FCAL	0.020		0.000	0.000	0.000	0.000	0.020	0.000	0.000	0.020	
	HEC Preshapers	0.034		0.000	0.000	0.000	0.000	0.034	0.000	0.000	0.034	
sTBB/sTDB (total of 140)			2.618									
	Pole-zero cancellation ASIC	0.20		0.025	0.025	0.000	0.000	0.150	0.000	0.000	0.200	
	VGA and Delay ASIC	0.332		0.045	0.045	0.000	0.000	0.242	0.000	0.000	0.332	
	ADC	0.626		0.045	0.045	0.000	0.045	0.490	0.000	0.000	0.626	
	SoS ASICs: MUX/Serializer/Laser Drivers	0.539		0.055	0.055	0.055	0.188	0.188	0.000	0.000	0.539	
	Optical Transmitters	0.324		0.000	0.018	0.000	0.153	0.153	0.000	0.000	0.324	
	Cooling Interface	0.068		0.020	0.000	0.000	0.024	0.024	0.000	0.000	0.068	
	Board Construction and assembly	0.530		0.000	0.065	0.065	0.000	0.201	0.201	0.000	0.530	
Optical Data Transmission			0.591									
	Fiber Bundles	0.365		0.000	0.365	0.000	0.000	0.000	0.000	0.000	0.365	
	Optical Switches	0.226		0.000	0.000	0.000	0.000	0.000	0.226	0.000	0.226	
Digital Processing System (DPS)			2.953									
	DPS Motherboards (total 35)	0.488		0.000	0.027	0.000	0.000	0.231	0.231	0.000	0.488	
	DPS Configurator (total 35)	0.017		0.000	0.001	0.000	0.000	0.008	0.008	0.000	0.017	
	DPS Controller Plugin (total 35)	0.014		0.000	0.001	0.000	0.000	0.007	0.007	0.000	0.014	
	sPU Daughter Cards (4 in a DPS MB, total 140)	1.811		0.000	0.051	0.000	0.000	0.880	0.880	0.000	1.811	
	Rear Transition Modules (1 per DPS MB)	0.402		0.000	0.024	0.000	0.000	0.189	0.189	0.000	0.402	
	Crates (13 DPS MBs in a crate)	0.065		0.000	0.013	0.000	0.000	0.013	0.039	0.000	0.065	
	Crate Controllers	0.072		0.000	0.012	0.000	0.000	0.012	0.048	0.000	0.072	
	Switches	0.025		0.000	0.005	0.000	0.000	0.005	0.015	0.000	0.025	
	Monitoring and config. Server	0.060		0.000	0.012	0.000	0.000	0.012	0.036	0.000	0.060	
Total			**7.981**	0.190	0.783	0.126	0.941	4.063	1.878	0.000	7.981	

Breakdown cost estimate (ATLAS core). In MCHF (1 USD=0.908 CHF)

Demonstrator Construction and Installation